CoolSiC™ MOSFET 1200 V G2 in a TO263-7 (D²PAK) package

About this document

Scope and purpose

This application note introduces the new generation CoolSiC™ MOSFET 1200 V G2 trench in the TO263-7 package for industrial power applications. The purpose of this document is to explain the features of this new family of products. Important application topics are covered to help in designing systems with maximum performance and reliability.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

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1 Introduction

1.1 Target applications

In power electronics, silicon carbide (SiC) MOSFETs perform key role in applications such as:

- Energy storage systems
- EV charging solutions
- High-frequency switch mode power supplies
- Motor drives
- Solar inverters

In any industrial-grade application, the efficiency and performance of SiC MOSFETs helps in meeting high-power demand and ensuring reliability. Their superior characteristics (compared to silicon-based power switches) such as high temperature tolerance, low on-state resistance, and low switching losses makes them ideal for demanding environments.

1.2 Technology features and benefits

The Infineon's CoolSiC™ MOSFET 1200 V G2 employs the vertical trench cell structure with the latest gate oxide process. This design mitigates on-state resistance and optimizes electric field control, resulting in improved switching speed and reduced losses. G2 SiC technology, enhances the device's thermal resistance, which leads to advanced energy efficiency in power circuits.

CoolSiC™ MOSFETs 1200 V G2 deliver a compact design, extended lifetime and reliability in challenging environments. Due to the reduced thermal resistance, cooling efforts can be reduced and therefore more and more high-frequency applications are enabled. Besdies, G2 prodcuts are completely compatible with any system incorporating the predecessor technology (Infineon's CoolSiC™ G1).

Key features of CoolSiC™ MOSFETs 1200 V G2 are:

- Capable of operating at high temperatures
- High blocking voltage
- Fast switching speeds
- Low on-state resistance
- High thermal conductivity
- Avalanche and short circuit withstand capabilities

These features make the CoolSiC™ MOSFET 1200 V G2 a preferred choice for efficient and improved power conversion across diverse applications. Figure 1 shows a comparison between some of the important MOSFET figures of merit of two Infineon CoolSiC™ families. These figure of merit parameters can be translated to application relevant benefits such as faster switching speeds, smaller system deadtime, and lower switching losses.

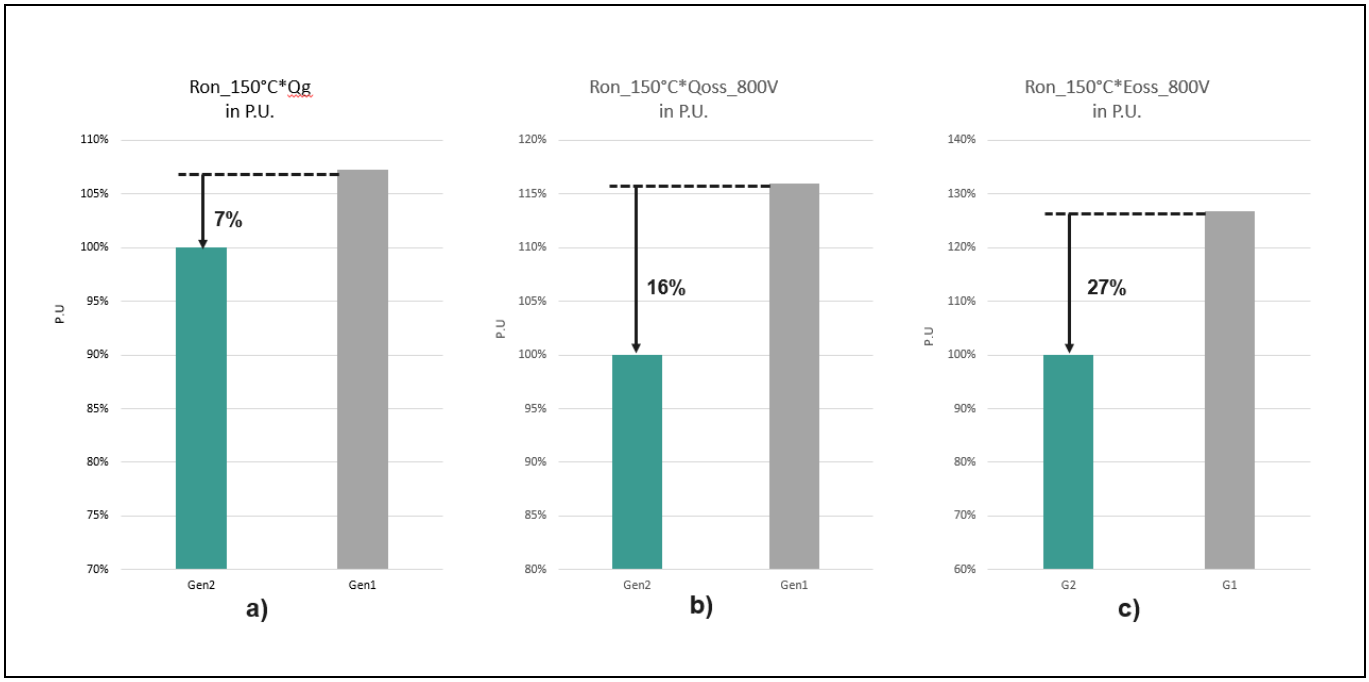


Figure 1 SiC MOSFET figures of merit (a) On-state resistance at 150°C · total gate charge (b) On-state resistance at 150°C · output capacitance charge (c) On-state resistance at 150°C · output capacitance energy.

The technology improvements of G2 allows the D2PAK CoolSiC™ family portfolio to be expanded even further, from the smallest G1 $R_{ds(on)}$ value of 30 mΩ to the 8 mΩ G2 device. Lower SiC MOSFETs RDSon classes offer better power handling, which enables higher power density in electronic systems. The ability to handle elevated power levels leads to reduced component count, a compact system design, and better thermal management. With the potential for higher levels of integration and support for high-voltage applications, these devices are crucial for applications that prioritize power density, efficiency, and space.

1.3 .XT interconnection

Infineon's .XT chip interconnection technology addresses design challenges and enables smaller form factors with stable thermal performance. The new CoolSiC™ MOSFET 1200 V G2 with .XT provides 12% better junction-to-case thermal resistance due to its improved die attachment process. As a result, higher output currents and a prolonged device lifespan can be facilitated. The .XT technology employs diffusion soldering method to minimize solder voids and reduce solder layer thickness. A detailed comparison of different PCB configurations for D²PAK is explained in [1].

2 Extended junction temperature operation

SiC MOSFETs are known for their ability to operate at higher temperatures compared to traditional silicon-based MOSFETs. While the specific temperature ratings can vary between different SiC MOSFET technologies and manufacturers, many SiC MOSFETs are designed to operate reliably at junction temperatures up to 175°C. Infineon's CoolSiC™ MOSFET 1200 V G2 is qualified to operate up to 200°C for a total cumulative time of 100 hours. This device specification has been introduced to allow more reliability under overload conditions and offer engineers more freedom with their system design.

The ability of SiC MOSFETs to withstand short overload conditions is an important consideration in various applications. In industrial motor drives, sudden load changes, additional torque demand, or even power supply fluctuations can lead to overload conditions where the increased junction temperature margin can be useful. Solar inverters are another good example to demonstrate overload conditions. In the grid-tied applications, grid voltage fluctuations can impact the operation of power converters. Voltage sag can influence the output power of the converter and temporarily increase power losses or in severe cases, completely disconnect the system from the grid. In electric vehicle charging applications, the charger's voltage fluctuations are critical: in the case of a drop in the input voltage the current increases temporarily, creating additional stress for the power device.

Figure 2 shows an example of the extended power dissipation capability of an 8 mΩ device due to the higher temperature limit. The grey curve represents a typical semiconductor power limitated by a case temperature of 175°C. In comparison, the green curve of CoolSiC™ G2 shows that 29% more current is enabled at the same operating point.

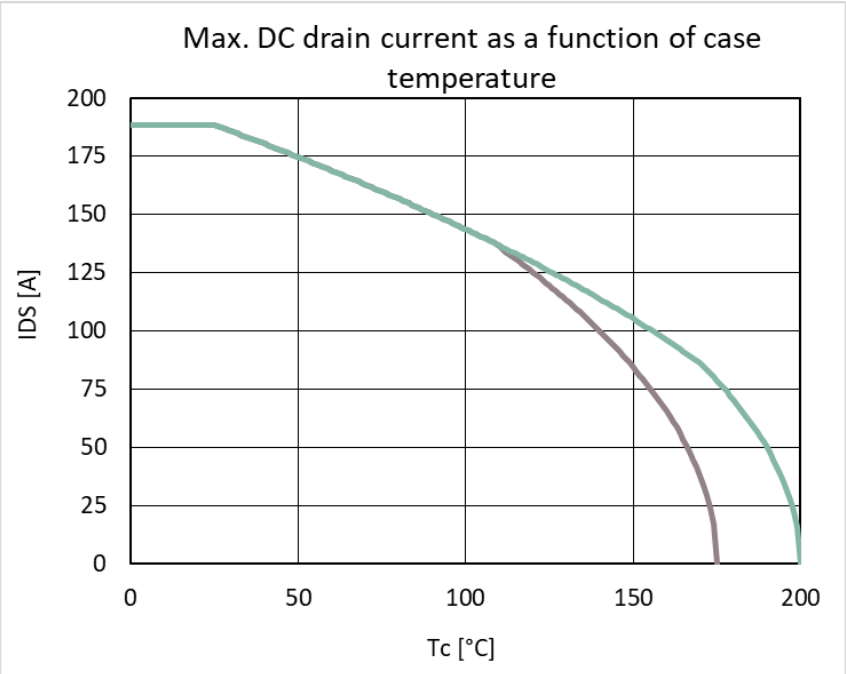


Figure 2 Device (IMBG120R008M2H) max. DC drain current as a function of case temperature.

As stated earlier, the CoolSiC™ MOSFET G2 is qualified to operate at up to 200°C for a total cumulative time of 100 hours.

3 Device selection

Various factors have to be considered when choosing the right MOSFET for any application to ensure optimal performance, reliability, and efficiency. In this chapter, guidelines for selecting an appropriate G2 device for a new power system, and for replacing an existing G1 device are provided.

In the CoolSiC™ MOSFET 1200 V G2 portfolio, the nomenclature of specific part numbers stays the same. Figure 3 shows the nomenclature legend for CoolSiC™ products. A quick way to select a particular type of the device is to check the package code and the product series code that define the technology or generation of the device. After selecting these two parameters, the detailed selection of voltage class, $R_{ds(on)}$ class, or current capability within the portfolio can be looked into.

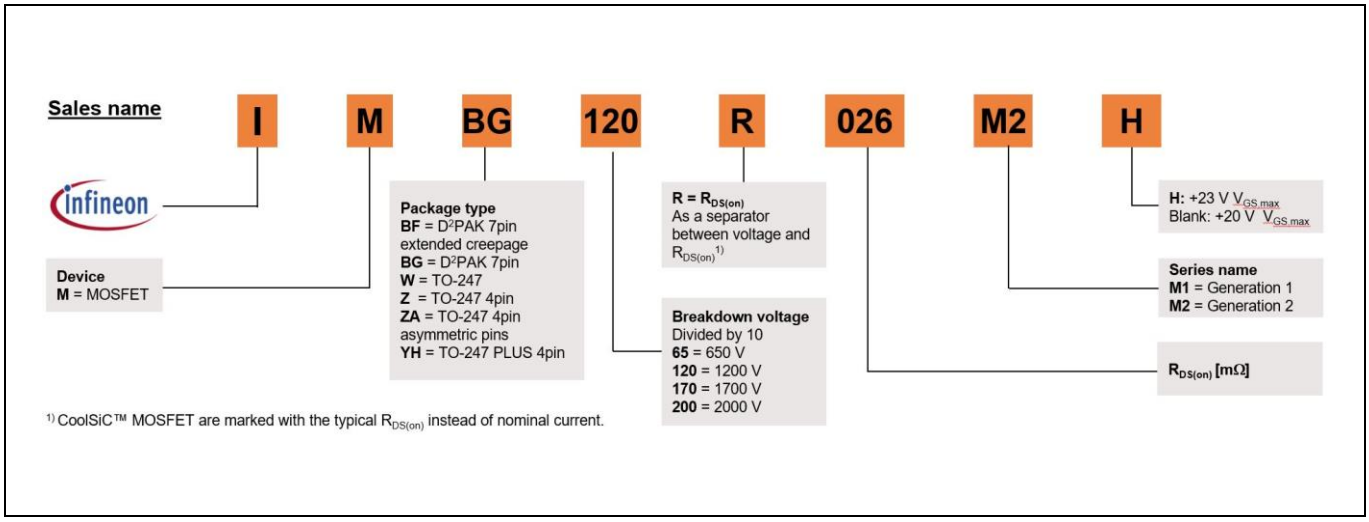


Figure 3 CoolSiC™ nomenclature legend.

Note: Automotive part numbers are not covered in this example. Please check Infineon Power MOSFET, product webpage for more details.

Selecting the MOSFET for a particular application with specific voltage and current ratings, switching frequency conditions, and thermal systems always involves a certain trade-off optimization.

The first defining factor for selecting a MOSFET is the operating voltage of the system. Today, a few voltage classes have become industry standards. Therefore, making the right decision in this regard is pretty straight forward and is guided by the system's maximum voltage. Typical rule of thumb is to allow 30% margin between the device max voltage rating and the operating system bus voltage (e.g. 1200V SiC MOSFETs are typically utilized up to 900V system bus voltage). Selection of the specific $R_{ds(on)}$ class is a more complex process. In fact, Rds(on) value is an important parameter that affects conduction loss. In the case of Infineon's CoolSiC™ family, a comparison with the product names of the previous generation shows that Rds(on) values between G1 and G2 are varying. This is because the product name typically includes the on-state resistance value at 25°C and this value is slightly different for the G2 devices due to technological improvement. Figure 4 shows the on-state resistance of IMBG120R026M2H G2 and IMBG120R030M1H G1 as a function of the junction temperature. The curves show the operating behavior at +15 V (dashed lines) and +18 V (solid lines) gate voltage respectively.

3 Device selection

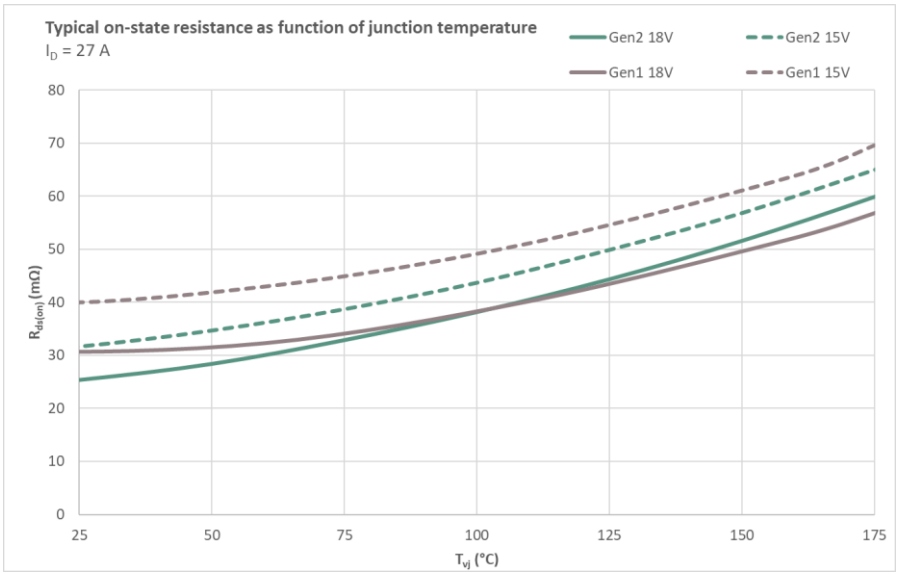


Figure 4 On-state resistance characteristic of G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices as a function of junction temperature at +15 V and +18 V gate voltage.

The G2 MOSFET has an improved channel region within the vertical cell. The contribution of channel resistance in the total resistance is significantly small and the drift layer contribution is more emphasized [2]. Due to this, the on-state curve has a slightly stronger positive temperature coefficient nature. In the CoolSiC™ G2 datasheets the maximum $R_{ds(on)}$ value at 150°C is guaranteed, which is unique in the market. This value can be used as a design parameter while considering worst-case scenarios.

The typical gate-to-source driving voltage for SiC MOSFETs is +18 V. While replacing a G1 device with a new G2 device, it is important to compare the on-state resistance characteristics of both the devices (Figure 4). The device should be chosen according to the thermal conditions for a the worst case operating point, which is typically at higher load operations. By doing so, a more precise matching selection can be done. Additionally, the higher $R_{DS,on}$ temperature dependence of G2 devices results in a tremndous improvement of low-load operations. In one of the following chapter, the overall distribution of device losses in selected applications is discussed to highlight the benefits of the G2 devices.

Guaranteed short circuit capability is another important feature of CoolSiC™ technology, that allows Infineon SiC MOSFETs to be safly used in motor drive applications. Such feature is usually improved by driving the device with +15 V gate-source voltage. The dashed lines in Figure 4 show that G2 devices always have significantly lower conduction losses when driven in such conditions (e.g. at an operating temperature of 100°C, the G2 device has 15% lower $R_{ds(on)}$ compared to the G1 device). As a consequence, the CoolSiC™ technology offers even more attractive performances in motor drive applications and, more generally, in all the applications that requires driving at V_{GS} of +15 V.

3 Device selection

Beside conduction losses, the tendency to operate at always higher switching frequency makes switching losses contribution another important aspect to select a SiC MOSFET. The MOSFET's gate charge and capacitance values can help to choose a device for a desired switching frequency. In G2 MOSFETs, the parasitic capacitance is lower compared to previous generation. This translates into faster switching transients and consequently lower switching losses of G2 vs G1 and allows for operation at higher switching frequencies and lower gate driver losses. The switching behavior of CoolSiC™ MOSFET 1200 V G2 products is discussed in detail in Chapter 4.

Finally, the thermal property needs to be considered when selecting for the best matching SiC MOSFET product. In this sense, a smaller value of a device's thermal resistance allows for higher power dissipation or lower operating temperature, depending on the specific optimization strategy. Due to the improved Chip/Package interface of G2 devices, the resulting R_{th} is 12% better than that of the previous SiC MOSFET generation, thus allowing for 12% higher power to be dissipate for the same device junction temperature increase over the case.

4 Switching behavior of CoolSiC™ MOSFET 1200 V G2

Understanding the switching behavior of SiC MOSFETs is crucial for optimizing power converter designs in various applications. One of the defining characteristics of SiC MOSFETs is the fast switching speed, attributed to the material's high electron mobility. This property enables rapid transitions between the ON and OFF states, reducing switching losses and enhancing overall efficiency.

CoolSiC™ MOSFET 1200 V G2 technology introduces improvements to the device's capacitive nature. As listed in Table 1, a significant reduction in the input and output capacitance, of 13% and 19% respectively, has been achieved. When operating in conditions where the load is relatively small, the improvement in output capacitance is even more pronounced in the G2 device. The input capacitance value determines the required gate driving power. Therefore, by using an Infienon CoolSiC™ MOSFET 1200 V G2 power switch, systems can reduce gate driver losses and optimize the driving circuit.

Table 1 Parasitic capacitances of G2 and G1 devices

		Value	
Parameter	**Symbol**	**IMBG120R026M2H**	**IMBG120R030M1H**
Input capacitance	C_{iss}	1990 pF	2290 pF
Output capacitance	C_{oss}	85 pF	105 pF
Reverse transfer capacitance	C_{rss}	7.4 pF	11 pF

Reducing switching losses is a key objective of high-power electronics design. With the G2 lower switching losses are achievable compared to the previous generation. The switching behavior of a SiC MOSFET depends on several factors such as the operating temperature, the current conducted by the device, and the gate resistance applied to the switch. Figure 5 shows the temperature dependency of IMBG120R026M2H and IMB120R030M1H, exemplarily representing G2 and G1 respectively. Comparison of the turn-on and turn-off energy curves of both devices at 150°C it shows that in the G2 device the switching behavior is better by 7% and 23% respectively.

Design engineers must also consider the current dependency and implement appropriate thermal management strategies to harness the overall switching performance of the G2 MOSFET.

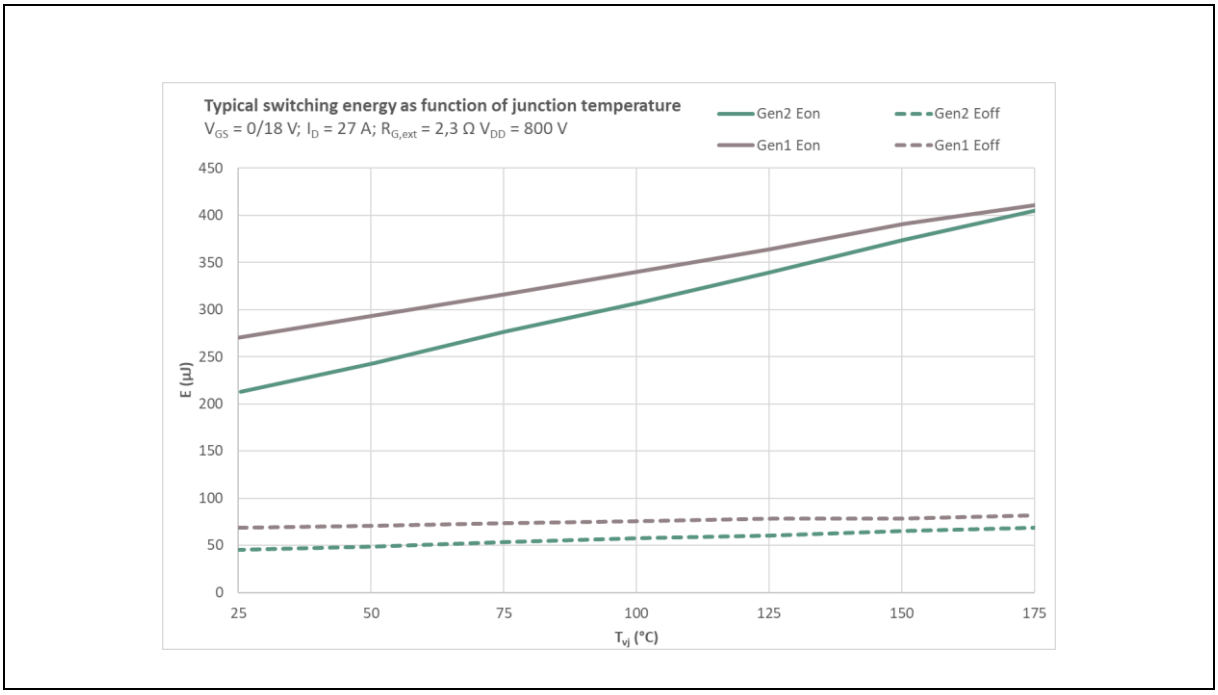


Figure 5 Switching energy of the G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices as a function of junction temperature.

4.1 Choosing a gate resistance for the CoolSiC™ MOSFET 1200 V G2

The applied gate resistance significantly influences the switching behavior of a SiC MOSFET and its overall performance. Gate resistance is a crucial parameter that engineers can manipulate to optimize the transition between the ON and OFF states of the transistor.

A lower gate resistance allows for faster charging and discharging of the gate capacitance, leading to quicker switching transitions. This can reduce switching losses and improve overall efficiency. Low gate resistance contributes to sharper transitions between the ON and OFF states which is crucial for minimizing power dissipation.

On the opposite side, a higher gate resistance slows down the switching process as it increases the time constant of the driving circuit. While this may reduce the risk of voltage overshoots and ringing, excessive gate resistance may compromise switching speed and efficiency. Higher gate resistance can soften the switching transitions, potentially reducing electromagnetic interference (EMI) and mitigating voltage spikes.

Figure 6 shows energy losses of the G2 MOSFET, IMBG120R026M2H and respective G1 IMBG120R030M1H device, across a wide range of gate resistor values. Due to the reasons mentioned before and to utilize the speed of the CoolSiC™ MOSFET fully, designing systems with gate resistance values of up to 25 Ω is recommended. Specific gate resistor value depends on the Rds(on) class of a device. Figure 6 shows that, regardless of the technology of the MOSFET, gate resistor values over 25 Ω results in turn-on energy loss close to 1 mJ per switching cycle, thus resulting in roughly 1W of switching loss per kilohertz of switching frequency.

4 Switching behavior of CoolSiC™ MOSFET 1200 V G2

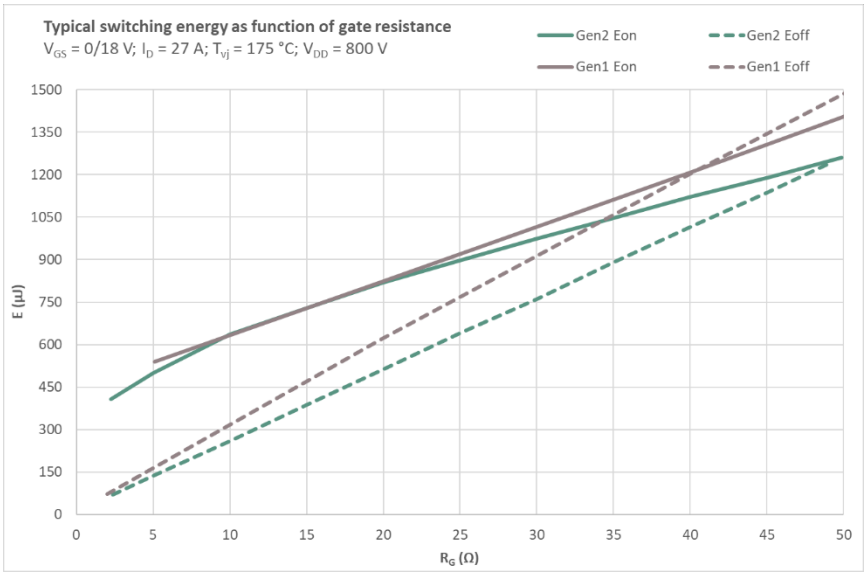


Figure 6 Switching energy loss in G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices as a function of external gate resistance.

When the selection of adequately low R_G is carried out, CoolSiC™ G2 technology demonstrates its advantage compared to the previous generation. As an example, with an external gate resistor of 5 Ω, the switching losses of G2 are approximately 7% lower than corresponding G1 device. In terms of electrical units, if the switching frequency is 60 kHz, at same conditions of Figure 6, switching losses of G2 switch are reduced by 2.5 W as compared to G1 device.

As mentioned, the practical selection of the appropriate gate resistance involves a trade-off between switching speed, losses, and robustness. Engineers must carefully analyze the specific requirements of their application and tailor the gate resistance accordingly to achieve the optimal SiC MOSFET performance. However, a simple plug-and-play replacement of a G1 device with a corresponsding G2 MOSFET[1], without modifying the gate circuit, is possible, thus resulting in improved power dissipation and system efficiency and lifetime.

In conclusion, the benefit of G2 MOSFET lower switching losses is an essential element for next generation power electronics systems.

[1] Selection criteria is based on matching R_{DSon} at 100°C.

5 Body diode reverse recovery

SiC MOSFET-based high frequency converters use device intrinsic freewheeling body diodes to allow current conduction from source to drain terminal when the MOSFET is in the off state. Such a condition usually happens in half-bridge configurations during the dead time phase. A SiC body diode usually has a high forward voltage and associated bipolar reverse recovery charge that results in higher energy conduction and switching loss. This chapter will show experimental results of the switching behavior of the body diode of the CoolSiC™ Gen 2 and discuss the recommended driving strategy to minimize its losses.

The reverse recovery phenomenon in a SiC MOSFET body diode is a well-known aspect in SiC MOSFETs and its effect has been well analyzed in many publications. Right after the MOSFET channel turns off, the body diode briefly conducts in the reverse direction [2], [5]. This reverse recovery effect leads to an undesired increase of power loss. Mitigating these losses involves careful optimization of body diode characteristics from device manufacturers side. Power design engineers, on the other hand, must account for the reverse recovery time and diode characteristics to ensure an efficient and reliable operation of the system, particularly in applications that have very fast switching or strict efficiency requirements.

In Figure 7, the reverse recovery current waveforms of the body diodes in a IMBG120R026M2H G2 device and a IMBG120R030M1H G1 device are shown. The measurement was done at high temperature conditions where the performances of the diode are more critical. It can be observed that the G2 device has comparable diode peak and duration of the current overshoot like the previous generation. The overall shape of the waveform shows that G2 diode softness is comparable to the G1, without high di/dt current spikes. Fast current transients can result in the voltage overshoot which is stressing device and other components in the circuit.

Note: The measurement was performed using a current sensor with 746 MHz bandwidth.

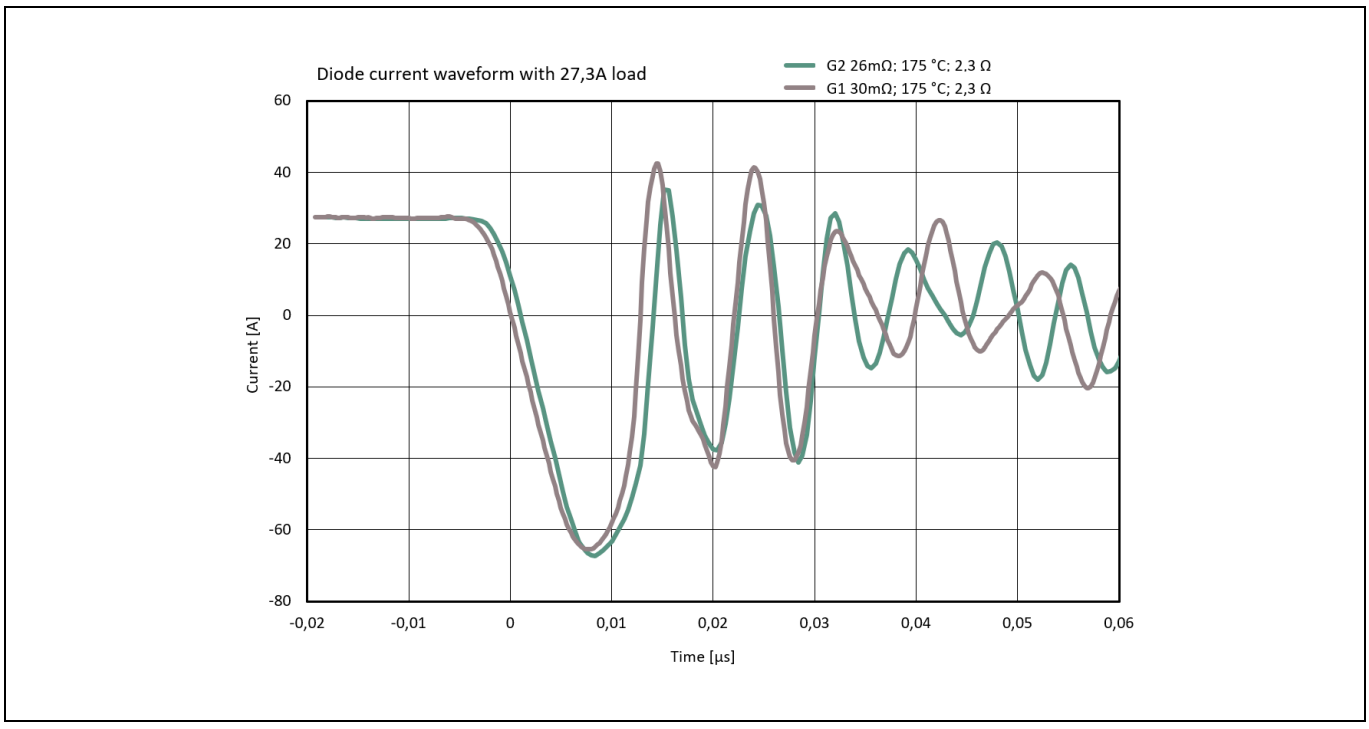


Figure 7 Recovery current waveforms for G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices.

5.1 Enabling shorter deadtimes for additional benefits

The duration of the conduction time of the body diode has a strong influence in the reverse recovery losses as well as in the turn-on losses of the complementary SiC MOSFET. In addition to reducing losses (due to the diode), the deadtime also influences the dynamic response of the power converter. An optimized deadtime allows for better reproduction of the sinusoidal waveform in AC-DC or DC-AC converters.

Today's MOSFETs are capable of switching in the range of a tens of nanoseconds (ns). Figure 8 shows the recommended deadtime operating range for the CoolSiC™ MOSFET 1200 V G2. The switching energy curves show that it is possible to achieve a significant reduction in device recovery losses and turn-on losses. The area marked in green (i.e. from 150 ns to 250 ns) represents the recommended deadtime control range. It is possible to achieve this range with today's driving circuits, especially by using SiC switches. By implementing the recommended values, the turn-on losses can be reduced by 20% and recovery losses by 40% compared to the nominal device values. More details about the influence of deadtime on E_{rec} are provided in [4].

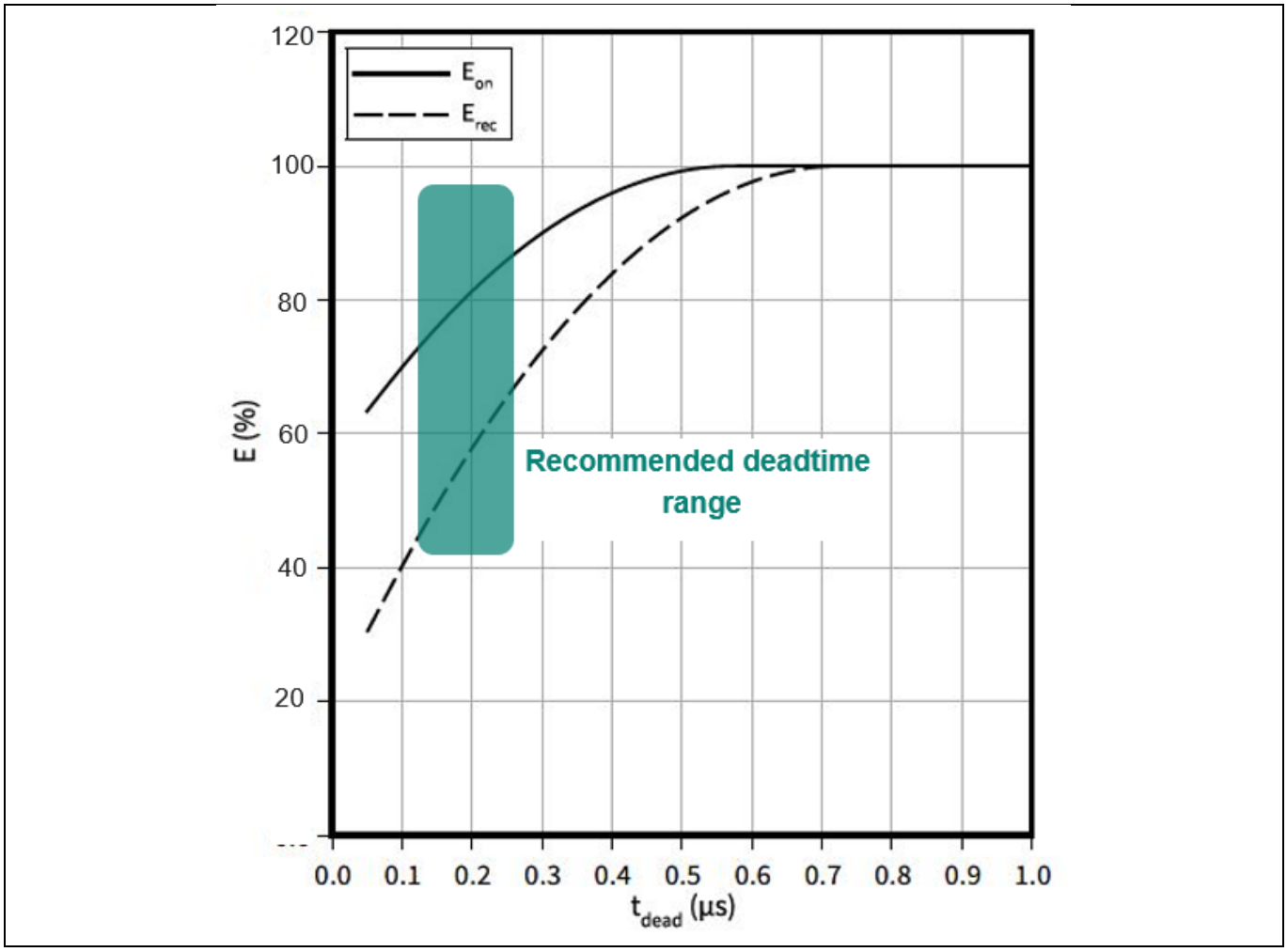


Figure 8 Recommended deadtime range with respective energy loss characteristics.

With SiC MOSFETs, further reduction in deadtime is actually possible. However, it is important to note that the feasibility of applying a very low deadtime is subject to and will include stronger dependencies on various other factors related to the speed of the power switch, the speed of the gate driver, and the parasitic components, such as stray inductance and capacitance, of the circuit.

When selecting the deadtime, a system designer should carefully check and consider the following:

5 Body diode reverse recovery

- The trade-off between shorter deadtimes and a potential shoot-through risk
- The proper match of the selected power switch and gate driver to ensure that the components can support a certain deadtime value

Note: Please check Infineon Gate Driver ICs, product webpage for the proper selection and more details on the available gate driver ICs.

As already mentioned, the deadtime limit depends on multiple factors such as the parasitics in the device and circuit, the speed of the gate driver, and the switched current level. Replacing G1 CoolSiC™ MOSFET with the best matching G2 device allows for a 30% reduction of the required deadtime due to the faster switching speed. This provides a wider design margin even in case of a simple plug-and-play MOSFET replacement.

6 Unipolar gate driving and parasitic turn-on robustness

Parasitic turn-on (PTO) in SiC MOSFETs can occur when the device is unintentionally driven in conduction state by the capacitive current flowing in the C_{GD} and in the gate driving circuit [6]. This is often associated with the presence of parasitic elements in the circuit. The most common reasons that causes PTO are extremely high dV_{DS}/dt, low MOSFET threshold voltage, and large parasitic elements in the circuit that amplify unwanted transients.

SiC MOSFETs switch high currents very fast in power circuits. Due to stray inductance and high speed in one switching cycle, the gate signal of the power switch can easily get distorted. This creates a certain voltage "ringing" on the gate terminal which can exceed device gate threshold level, $V_{gs} > V_{th}$, and can drive the device to the ON state. To counter this unwanted behavior, a dedicated driving Kelvin-source pin is usually provided in the package. In addition to that, the SiC MOSFET technology can be designed with a higher threshold voltage, and the drain-source vs gate-source parasitic capacitance ratio can be minimized to reduce the induced voltage and its influence on the state of the device.

G2 CoolSiC™ products have a threshold voltage ranging from 5.1 V to 3.2 V at 25°C and 175°C respectively. These levels of threshold voltage provide large safety limit for noise on the control signal. In addition, the improved ratio of parasitic C_{DG} and C_{GS} capacitances of CoolSiC G2 technology reduces the disturbance on the gate signal. This results in improved parasitic turn-on robustness. Figure 9 shows the range of the device threshold voltage (light green color) and capacitive-induced gate voltage level (ocean blue). In the G2 device, there is a margin of more than 1 V due to the improved C_{DG}/C_{GS} ratio.

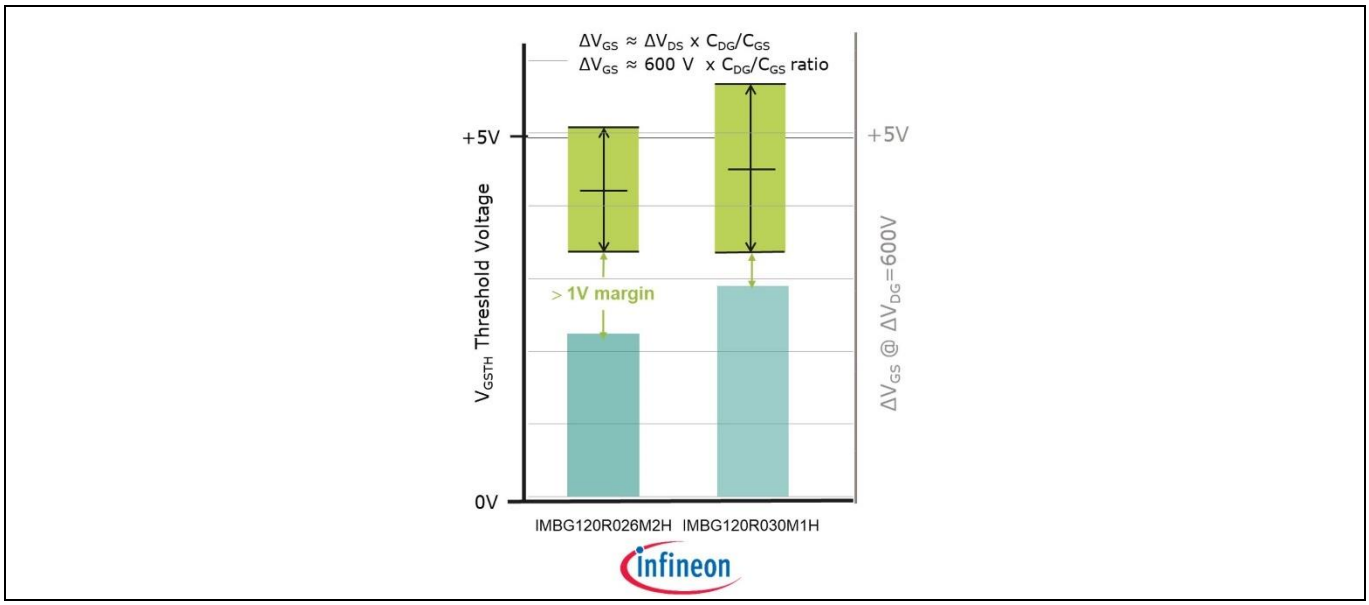


Figure 9 The margin between the threshold voltage and the resulting induced voltage at the gate pin for G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices.

6.1 Recommended MOSFET driving

A general reliability rule associated to the MOSFET power devices it to minimize the OFF-state to ON-state V_{GS} voltage excursion. In previous technologies of SiC MOSFETs, the utilization of unipolar V_{GS} operation was recommended as method to optimize the gate-oxide reliability. Nowadays, with the development of the SiC MOSFET technologies over the years, the reliability of the gate oxide layer and the manufacturing process has significantly improved. As a consequence, today's SiC MOSFETs are designed to tolerate negative gate voltages within specified limits. This allows for higher margin against parasitic turn-on (PTO) especially in presence of high switching transients.

A negative voltage can be used to drive the MOSFET into a more secure and reliable OFF state or to improve the turn-off characteristics. Engineers should follow the voltage levels specified in the datasheet. The G2 MOSFETs in D2PAK offers significantly increased allowed V_{GS} ranges compared to the previous generation, as listed in Table 2. The negative transient and static values can be as low as -10 V and -7 V respectively. The positive values can go up to +23 V and +20 V for transient and static respectively. The transient gate-source voltage value represents the allowable gate overshoot and undershoot levels. The static gate-source voltage refers to the DC level that can be applied at the MOSFET gate.

Table 2 Gate electrical parameters as given in the datasheet

Gate-source voltage, max. transient voltage[2)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$	-10...23	V
Gate-source voltage, max. static voltage	V_{GS}		-5...20	V

Selecting a proper turn-on V_{GS} has a significant impact on the device performances. The $R_{ds(on)}$ characteristic is dependent on the applied gate voltage, and it reduces significantly when V_{GS} increase from 15 V to 18 V. The extended static gate voltage range of the G2 MOSFET is perfect for +18 V driving. Driving the gate of the G2 devices with lower voltage should only be considered in specific cases (e.g. 15 V is generally preferred in applications requiring short circuit capability).

The gate oxide reliability of CoolSiC™ MOSFETs has been proven to be reliable by many years of applications. From a system level point of view, the cost difference between unipolar or a bipolar gate driving schemes is negligible.

Note: To ensure long-term reliable operation of the power switch, the device should not be operated outside of the gate voltage range specified in the datasheet [4].

7 Comparison between losses under different operating conditions

7.1 Hard-switching topology: AC-DC active frontend

Figure 10 shows the loss breakdown of a single switch in a hard-switching topology. The different losses are:

- Conduction loss (purple)
- Turn-on switching loss (green)
- Turn-off switching loss (yellow)
- Recovery loss (light green)

As can be seen, the diode recovery loss represents a negligible percent of the overall device losses. A comparison of IMBG120R026M2H G2 and IMBG120R030M1H G1 devices, under the same operating conditions, shows that the G2 device has 0.7 W (3.5%) less conduction losses and 5.75 W (22.87%) less total switching losses. Its overall operating junction temperature is also 12°C lower, due to the combination of lower losses and better $R_{th,j\text{-}c}$.

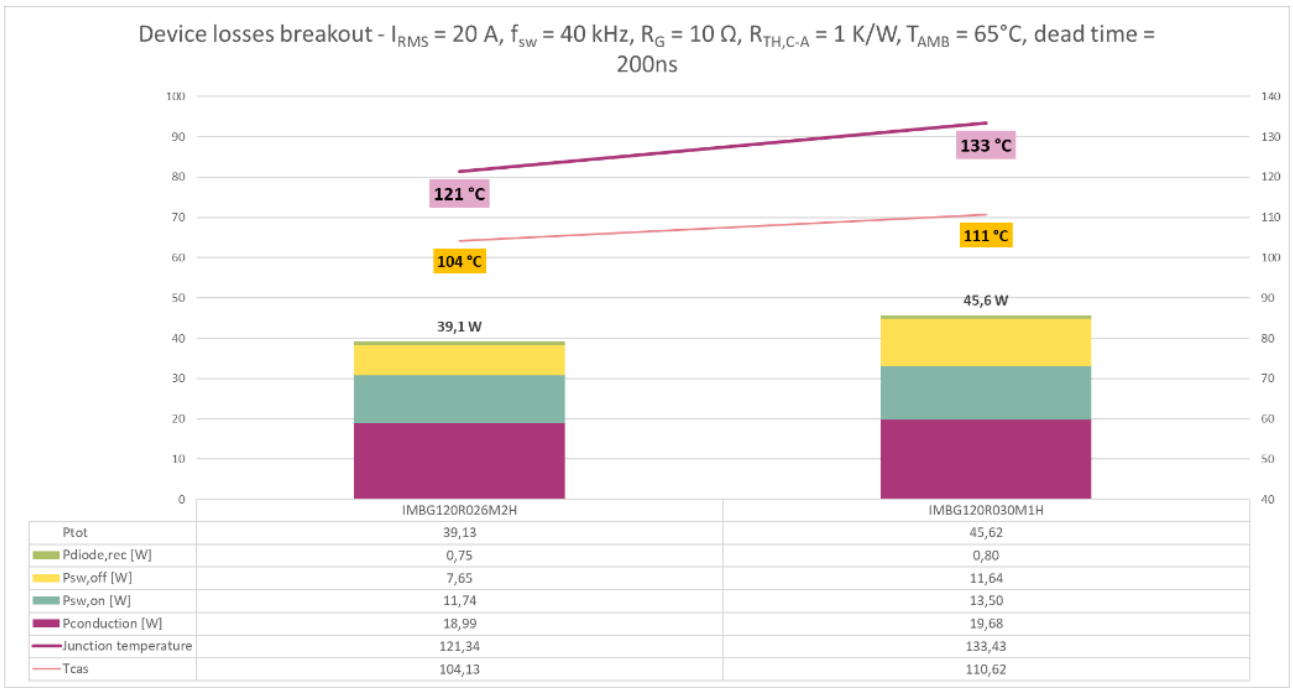
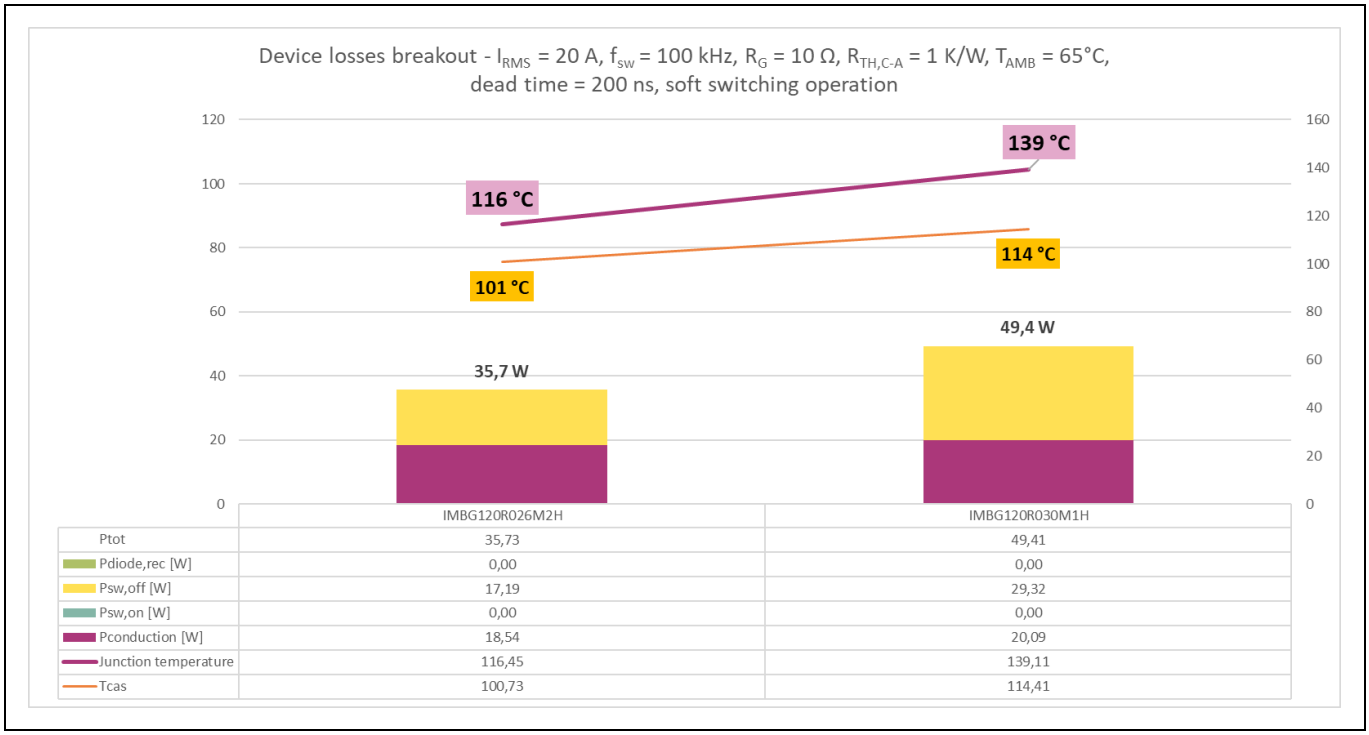


Figure 10 Comparison between the loss breakdown of a single switch in an AC-DC topology for G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices.

7.2 Soft-switching topology: LLC

In a soft-switching topology, the main loss contribution is given by the conduction phase (purple) and turn-off switching phase (yellow). Figure 11 shows the loss breakdown of a single switch. A comparison between IMBG120R026M2H G2 and IMBG120R030M1H G1 devices, under the same operating conditions, shows that the G2 device has a 2.4 W (11.3%) less conduction loss and 12.1 W (41.37%) less total switching loss. Its overall operating junction temperature is also 2°C lower.



	IMBG120R026M2H	IMBG120R030M1H
Ptot	35,73	49,41
Pdiode,rec [W]	0,00	0,00
Psw,off [W]	17,19	29,32
Psw,on [W]	0,00	0,00
Pconduction [W]	18,54	20,09
Junction temperature	116,45	139,11
Tcas	100,73	114,41

Figure 11 Comparison between the loss breakdown of a single switch in a DC-DC topology for G2 (IMBG120R026M2H) and G1 (IMBG120R030M1H) devices.

8 PCB layout of SiC MOSFET circuit

Figure 12 shows a three-phase power board layout of a servo drive as design recommendation for the CoolSiC™ MOSFETs in D²PAK. Board consists of MOSFETs in TO-263-7 package on insulated metal substrate board. Gate source and power source tracks are separated to avoid noise interferance to the driving signal. To reduce loop inductance, power tracks are designed as short as possible. Gate resistors are placed as close as possible to the gate pin of the power MOSFET while the gate driver IC is on the second, standard FR-4, PCB which is interconnecting with IMS board through the signal connectors.

Most important building blocks are emphasized with following designators:

1) HS MOSFET
2) LS MOSFET
3) HV bypass capacitor
4) Gate resistor network
5) Gate signal connector
6) V-phase circuit
7) U-phase circuit

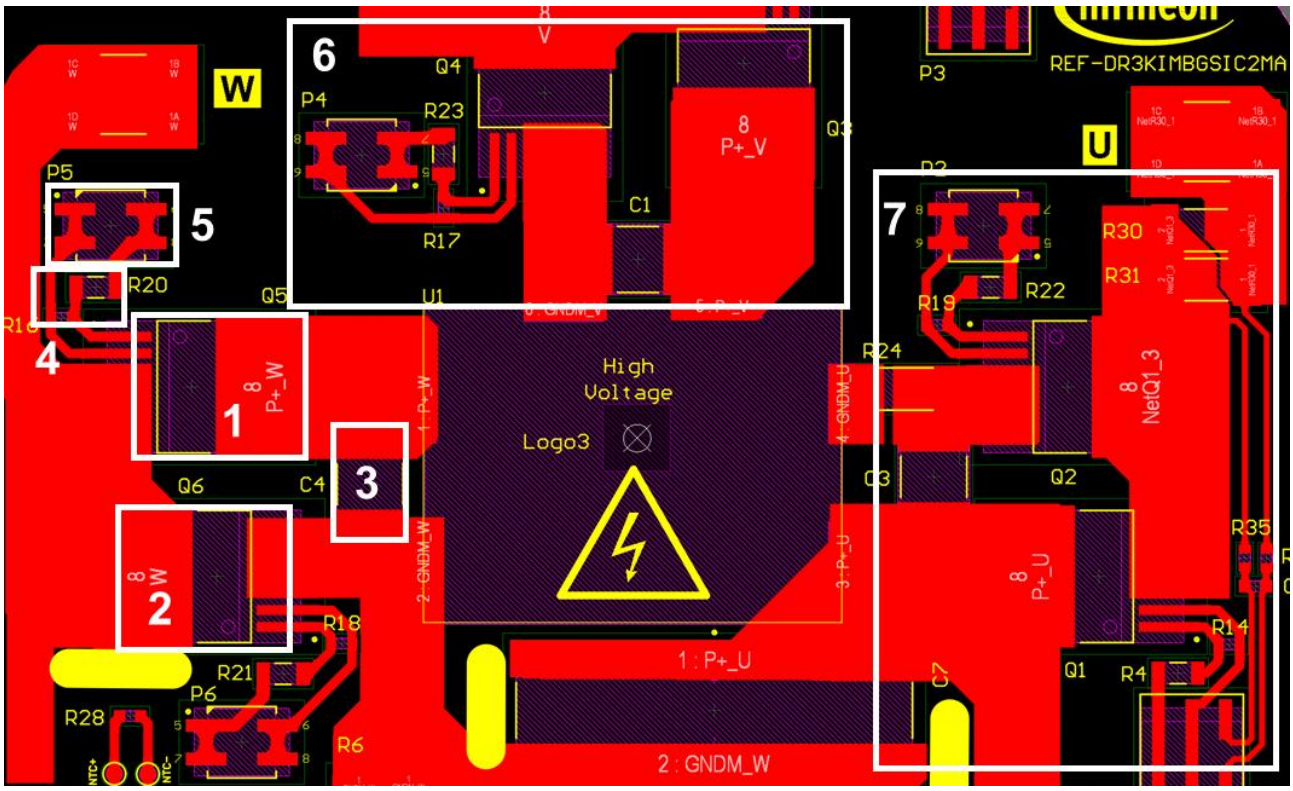


Figure 12 Power circuit PCB layout example of servo drive based on SMD MOSFET on IMS board

References

[1] Infineon: Application Note Z8F80405158
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Rev 1.1		2024-07-03	Minor changes, rework of language

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