CoolSiC™ MOSFET M1H for 1200V and 2000V modules

About this document

Scope and purpose

The benefits of wide-bandgap silicon carbide (SiC) semiconductors arise from their higher breakthrough electric field, larger thermal conductivity, higher electron-saturation velocity, and lower intrinsic carrier concentration compared to silicon (Si). Based on these SiC material advantages, SiC MOSFETs are an attractive switching transistor for high-power applications, such as solar inverters, energy storage systems and offboard and onboard electric vehicles (EV) chargers.

This application note introduces the 1200V and 2000V CoolSiC™ trench MOSFET M1H technology for modules, describing the general features and characteristics of CoolSiC™ MOSFET's M1H generation, which can help in designing power systems effectively using the novel transistor.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Table of contents

1 Infineon SiC Trench CoolSiC™ MOSFET M1H

The CoolSiC™ MOSFET M1H is the successor of the CoolSiC™ MOSFET M1 and brings significant advantages for the applications. Some of its main features and benefits are:

- **On-state resistance $R_{DS(on)}$**
  The CoolSiC™ MOSFET M1H shows compared to the generation M1 a reduced $R_{DS(on)}$ at an application relevant temperature of $T_{vj\,op}$ = 125°C and $V_{GS(on)}$ = 18 V
- **Gate-source voltage**
  The CoolSiC™ MOSFET M1H offers new gate-source voltage values (specified in the datasheet) for the highest flexibility:
  - New recommended gate-source voltage window from 15 V to 18 V and from 0 V to - 5 V
  - The maximum rated gate-source voltages (V_{GS}) are extended to 23 V and -10 V to cover overshoots and undershoots
- **Maximum virtual junction temperature**
  The CoolSiC™ MOSFET M1H allows for operation at a temperature of $T_{vj\,op}$ = 175°C under overload conditions.
- **Enhanced stability**
  The CoolSiC™ MOSFET M1H offers a new level of threshold voltage stability under real application conditions.

The current modules with 1200V and/or 2000V CoolSiC™ MOSFET M1H product range are shown in Figure 1. The Easy family products are available in industry and automotive grade (AQG324 compliant).

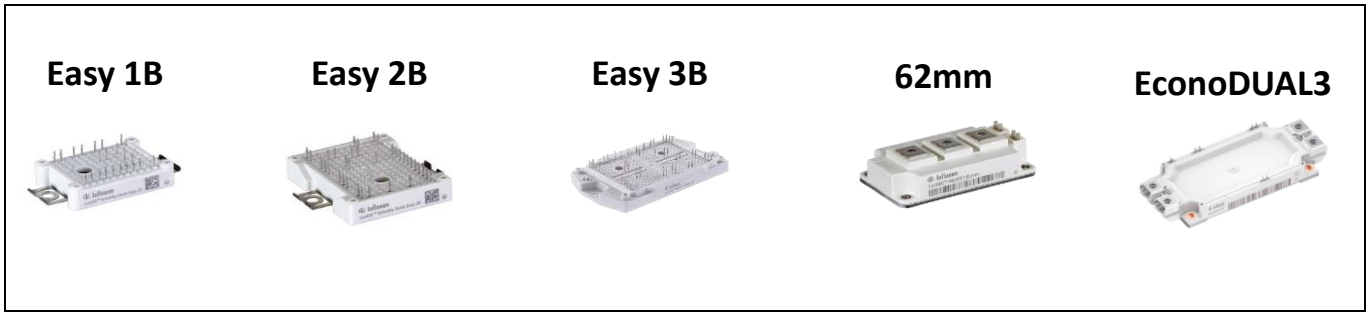

Figure 1 **Module solutions using the CoolSiC™ MOSFET**

2 Gate-source voltage – the right choice

The CoolSiC™ MOSFET technology is used in a wide range of applications, which of may have different requirements. The newly introduced CoolSiC™ MOSFET M1H technology offers a flexible gate-source voltage range to simplify the design-in process and to reach the highest utilization levels of the technology in the respective applications.

There are many trade-offs to be considered for choosing the right gate-source voltage. The criteria below show an overview about some of the most important parameters that are affected by the choice of gate-source voltage:

- Performance:
  - On-state resistance $R_{DS(on)}$
  - Body diode I-V characteristics
  - Dynamic switching behavior
- Driver stage:
  - Gate charge: driver-output power rating
  - Complexity of the driver stage: unipolar vs. bipolar power supply
- Parasitic turn-on
- $V_{GS(th)}$ drift
- FIT rates
- Short-circuit capability

This chapter explains the impact of the gate-source voltage on the individual parameters listed above.
The data in this chapter was acquired using specific part numbers but the general behavior can be transferred to other packages or chips using the CoolSiC™ MOSFET M1H technology.

2.1 Data sheet definitions of gate-source voltage

One of the advantages of the CoolSiC™ MOSFET M1H technology is that the devices can be operated within a flexible gate-source voltage range. The wide gate-drive voltage window for the positive and negative voltage provides flexibility for the application so that depending on the individual use case the best operating point can be chosen.

Gate-source voltage – the right choice

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}		T_{vj} = 25 °C	1200	V
Implemented drain current	I_{DN}			15	A
Continuous DC drain current	I_{DDC}	T_{vj} = 175 °C, V_{GS} = 18 V	T_H = 105 °C	15	A
Repetitive peak drain current	I_{DRM}	verified by design, t_p limited by T_{vjmax}		30	A
Gate-source voltage, max. transient voltage	V_{GS}	D<0.01		-10/23	V
Gate-source voltage, max. static voltage	V_{GS}			-7/20	V

Table 4 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
On-state gate voltage	$V_{GS(on)}$		15 ... 18	V
Off-state gate voltage	$V_{GS(off)}$		0 ... -5	V

Figure 2 Data sheet values for gate-source voltages

With regard to the gate-source voltage, we must distinguish between the maximum static gate-source voltages, the maximum dynamic gate-source voltages, and the recommended on-state and off-state gate voltages.

The maximum static gate-source voltages describe the steady-state condition. Gate-source voltages up to +20 V and -7 V set the upper and lower limit. Since this rating is specified as a maximum rated value, it must not be exceeded except for the dynamic condition as described below.

The maximum dynamic gate-source voltages describe the transient voltage peak during the turn-on and turn-off event. It can reach maximum peak voltages of +23 V and -10 V for a duty cycle of less than 1%. This is the maximum rated value and must not be exceeded.
A duty cycle is defined as the entire time period as well as the time when the gate-source voltage exceeds the maximum static gate-source voltages. Figure 3 depicts an exemplary gate-source voltage waveform. For simplicity, the envelope (green dotted line in Figure 3) can be used to extract the timeframe t1 and t2. Equation [1] shows how to calculate the duty cycle.

$$D = \frac{t1}{T} = < 1\%\,; \qquad D = \frac{t2}{T} = < 1\% \qquad [1]$$

In addition to the maximum rated values, Infineon recommends users to drive the devices in a certain voltage range. The on-state voltage range is between + 15 V…+ 18 V and an off-state gate voltage range is between 0 and -5 V. The range may be limited in 2 kV CoolSiC™ MOSFET M1H products, due to a higher risk of parasitic turn-on (PTO). Depending on the individual requirements in the respective application, the $V_{GS(on)}$ and $V_{GS(off)}$ levels must to be defined carefully.

The characteristic values in the datasheet of the CoolSiC™ MOSFET M1H are specified at $V_{GS(on)}$ = + 18 V and $V_{GS(off)}$ = - 3 V, which show a good trade-off between the performance and lifetime for many applications.

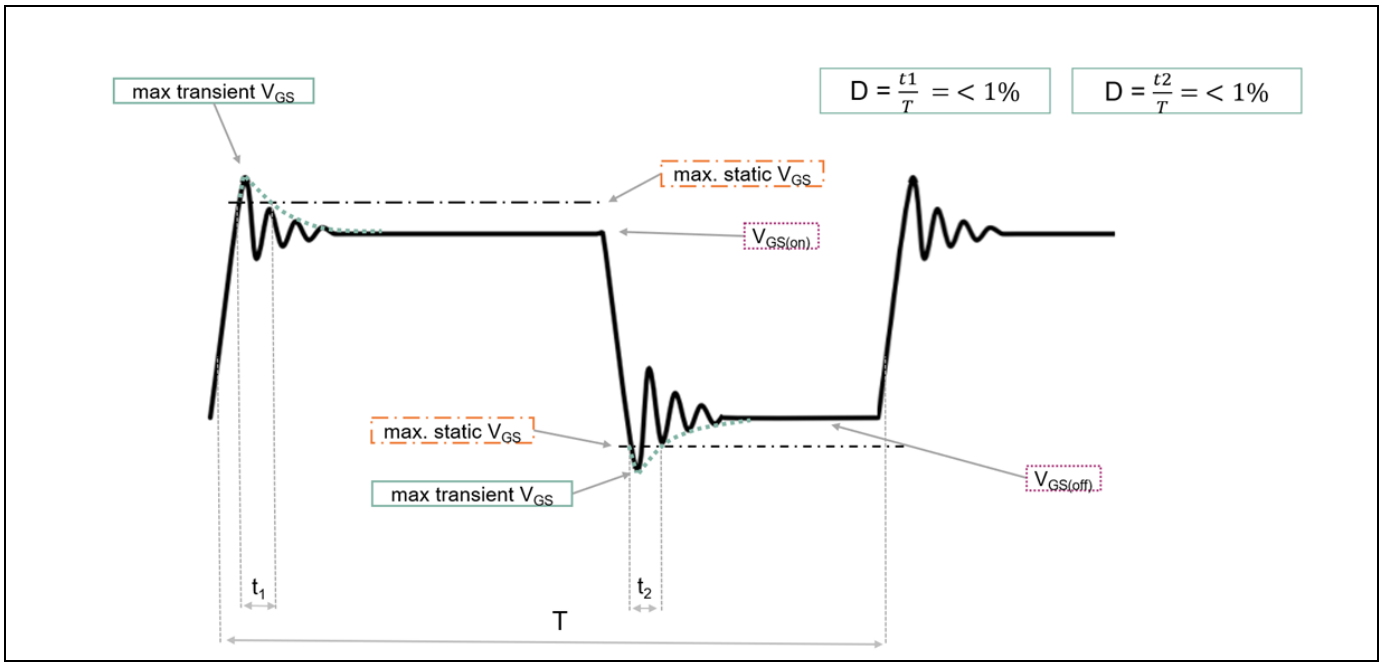

Figure 3 Schematic gate-source voltage waveform

2.2 Device characteristics of CoolSiC™ MOSFET M1H to be considered for the right choice of gate voltage

This chapter describes the impact of the gate-source voltage on several key parameters of the CoolSiC™ MOSFET M1H.

2.2.1 On-state resistance $R_{DS(on)}$

As described in the previous chapter, it is recommended to drive the devices with on-state between +15 V and +18 V and off-state between 0 V and -5 V, with possible exceptions on the 2kV CoolSiC™ MOSFET M1H portfolio. Transient peak voltages during the switching event can reach up to +23 V and -10 V with a duty cycle of 1%. Thus the typical on-resistance of the device is determined at $V_{GS(on)}$=+18 V and +15 V in the respective data sheets.

The choice of the on-state gate voltage has an impact on the static performance of the device. The $R_{DS(on)}$ at room temperature as well as the temperature dependency differs among different on-state gate voltages.

The I-V curves or output characteristics of a MOSFET are measured in pulse mode for different junction temperatures - 25°C, 125°C and 175°C. Figure 4 (left and right) shows the drain current as a function of drain-source voltage V_{DS} with different on-state gate-source voltages $V_{GS(on)}$. The solid black curves are typical results at 25°C, and the dashed curves are those at higher junction temperature of 125°C and 175°C.

The total $R_{DS(on)}$ resistance is determined by the sum of the single resistances. These are namely the channel resistance (R_{ch}), the resistance of the junction field-effect transistor (R_{JFET}), the epitaxial layer resistance of the drift region (R_{epi}) and the resistance of the highly doped SiC substrate (R_{Sub}). The MOSFET's channel resistance has a negative temperature characteristic due to the behavior of the interface states, while the drift region and intrinsic JFET have positive temperature characteristics. Because of the advantageous channel orientation along the preferred crystal plane with a low density of interface defects, the total $R_{DS(on)}$ of CoolSiC™ MOSFET is not dominated by the MOSFET's channel resistance, so that the total $R_{DS(on)}$ exhibits a positive temperature coefficient in the complete temperature range. This behavior is beneficial for balancing the current distribution of parallel devices. [1]

Gate-source voltage – the right choice

Especially the MOSFET channel resistance depends on the applied positive on-state gate voltage. The higher the on-state gate voltage the lower the $R_{DS(on)}$.

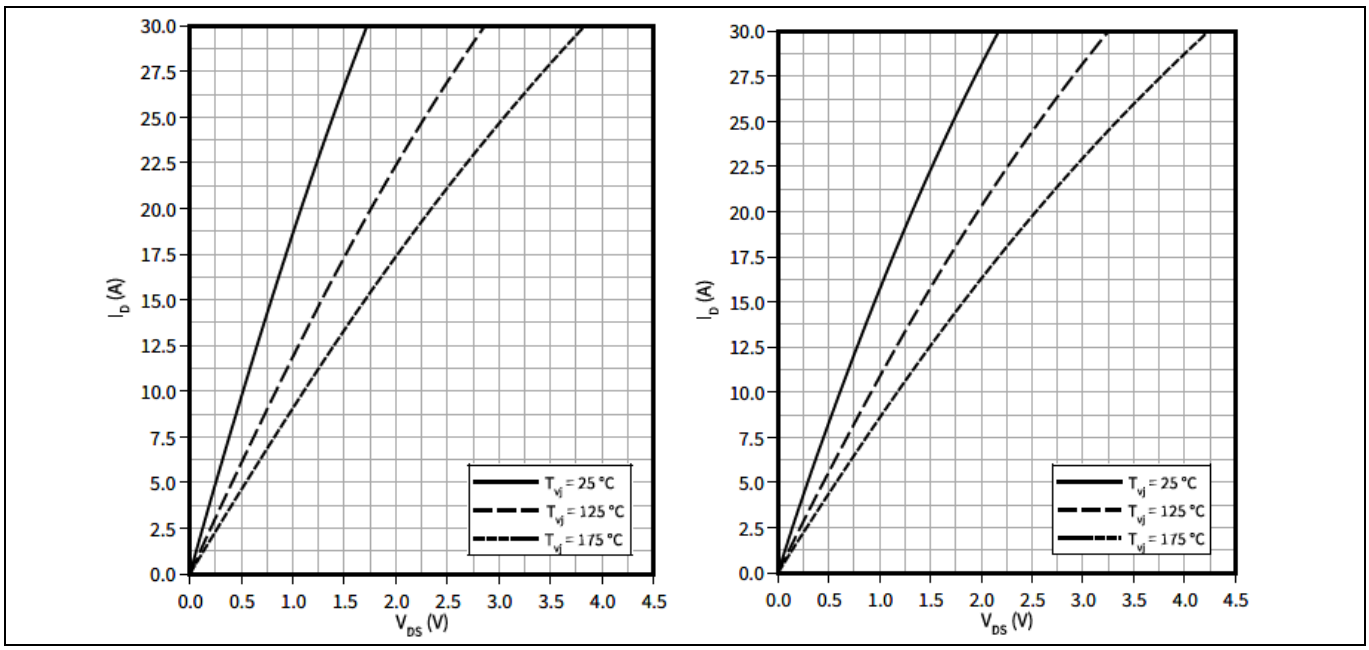

Figure 4 **(Left) Typical output characteristics, V_{GS} = 18 V parameter, with T_j=25°C, 125°C and 175°C; (Right) Typical output characteristics, V_{GS} = 15 V parameter, with T_j=25°C, 125°C and 175°C**

The on-state resistance $R_{DS(on)}$ as a function of junction temperature T_{vj} is shown in Figure 5 (left). At a rated current of I_{DS} = 15 A, the $R_{DS(on)}$ = 53 mΩ at T_j=25°C and $V_{GS(on)}$ = +18 V; at T_j = 25°C and $V_{GS(on)}$ = +15 V, $R_{DS(on)}$ = 63.5 mΩ.
It can be observed that the temperature dependacy for $V_{GS(on)}$ = +18 V is more pronounced than for $V_{GS(on)}$ =+15 V. This is because at different on-state gate voltages the contribution of the MOSFET's channel resistance is lesser and the resistance of the epitaxial layer is more dominant. [1]

As the SiC MOSFET is a voltage-controlled device, it turns on gradually with increasing gate-source voltage. The right curves of Figure 5 are almost linear up to drain currents of about 30 A, if the gate source voltage is above 13 V. For higher drain currents or lower gate-source voltages, there is a significant reduction of the current slope with increasing V_{DS}. This behavior is a consequence of the built-in junction field effect transistor (JFET), which is formed by the deep p+ wells. As the p+ wells are linked to source, the junction channel of the JFET is controlled by a drain-source voltage drop. Hence, the JFET channel is narrowed down with increasing V_{DS}. [1]

Exceeding 13 V of gate voltage, the drain current decreases with temperature, resulting in better paralleling performance of multiple devices. Below 13 V gate voltage, the drain current increases with temperature. It is not recommended to have $V_{GS(on)}$ below +13 V for on-state.

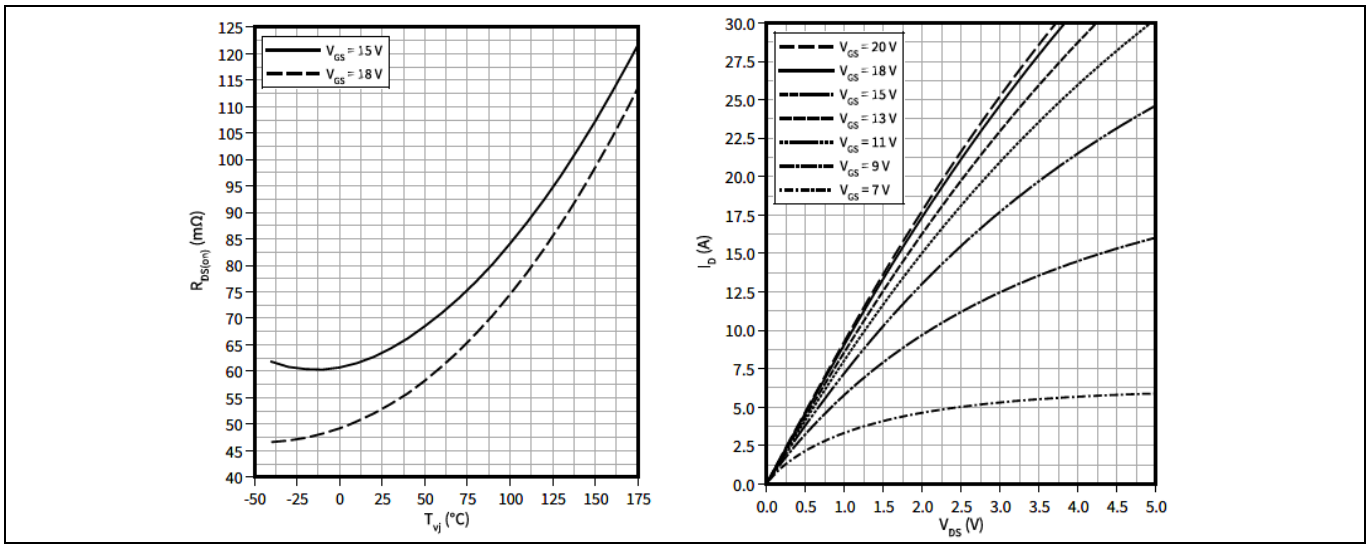

Figure 5 (Left) Typical on-resistance vs. junction temperature. I_{DS} = 15 A, V_{GS} = 18 V and 15 V; (Right) Typical output characteristics, V_{GS} = +7 – +20 V parameter, with T_j = 175°C

2.2.2 Forward characteristics of the body diode

The choice of the off-state gate voltage also has an impact on the performance of the body diode.
The CoolSiC™ MOSFET M1H integrates an intrinsic body diode with p-n junction behavior. As shown in Figure 6 (left), the intrinsic bipolar body diode has a relatively high forward voltage V_{SD} (about 4.2 V at 15 A, V_{GS}=-3 V) compared to silicon parts. The forward voltage drop changes with the negative gate voltage. At 0 V the forward voltage is lower than at -5 V.

The forward voltage V_{SD} has a negative temperature coefficient, and the temperature dependency is almost similar for gate voltages between 0 V and -5 V (see Figure 6 on right).

Since the voltage drop is quite high, it is not effective to use the body diode to conduct current for long periods of time. The continuous current rating provided on the datasheet is a theoretical value calculated based on T_c, T_{vjmax} and conduction losses. When high currents are continuously applied through the body diode path, this can result in asymmetrical current distribution when chips are paralleled, potentially leading to thermal runaway due to the negative temperature coefficient. However, operating at these current levels during typical deadtimes cause no issues.

Fortunately, the CoolSiC™ MOSFET M1H can conduct reverse current from the source to the drain through the channel if a positive bias is applied to the gate. This mode of operation is called synchronous rectification (or third quadrant operation) and achieved by a positive on-state gate voltage of typically +15 V to+18 V on the gate. As shown in Figure 6 (left), synchronous rectification mode is highly recommended to limit conduction losses. Similar to the forward direction of the MOSFET, +18 V shows lower V_{SD} than +15 V.

Gate-source voltage – the right choice

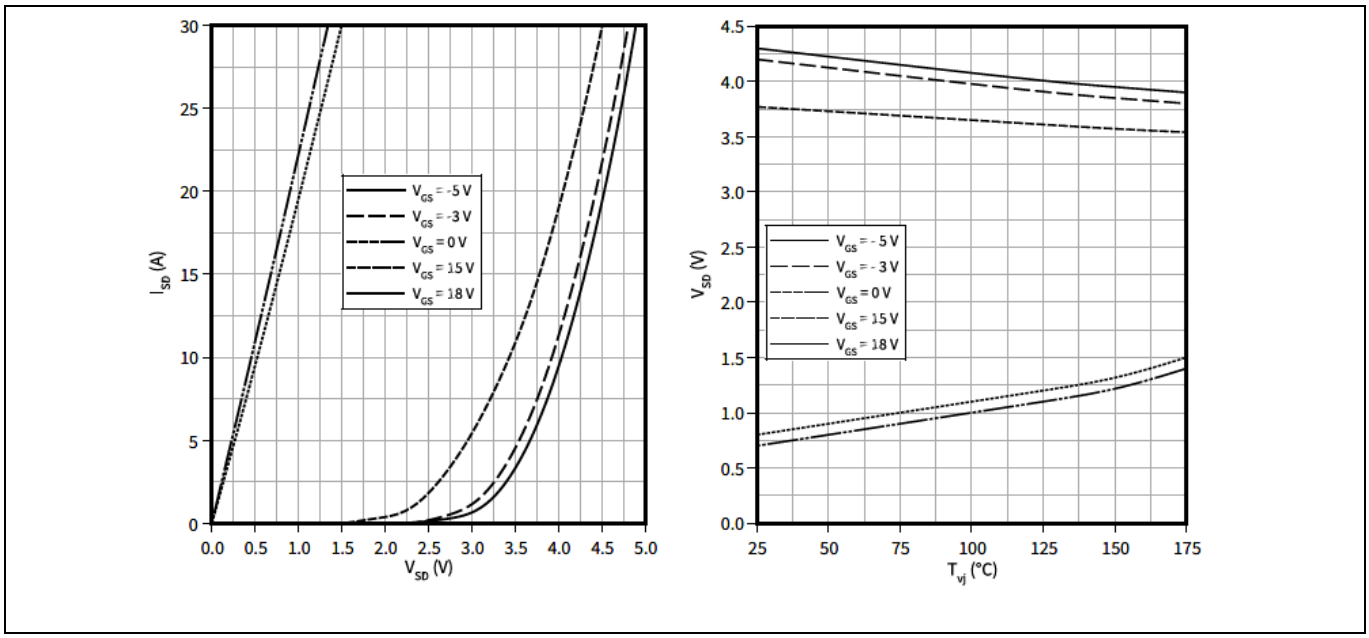

Figure 6 **(Left) Reverse current I_{SD} as function of voltage at different gate voltages and T_{vj} =25°C (Right) V_{SD} temperature dependency at different gate voltages**

Applying synchronous rectification has the additional benefit that the positive temperature coefficient of the MOSFET in reverse direction will support current sharing in case of paralleling. Figure 7 shows exemplary waveforms for four modules in parallel. The first pulse uses synchronous rectification after the dead time, while for the second pulse, the body diode is conducting the current. The results confirm that synchronous rectification leads to better current sharing between the current waveforms.

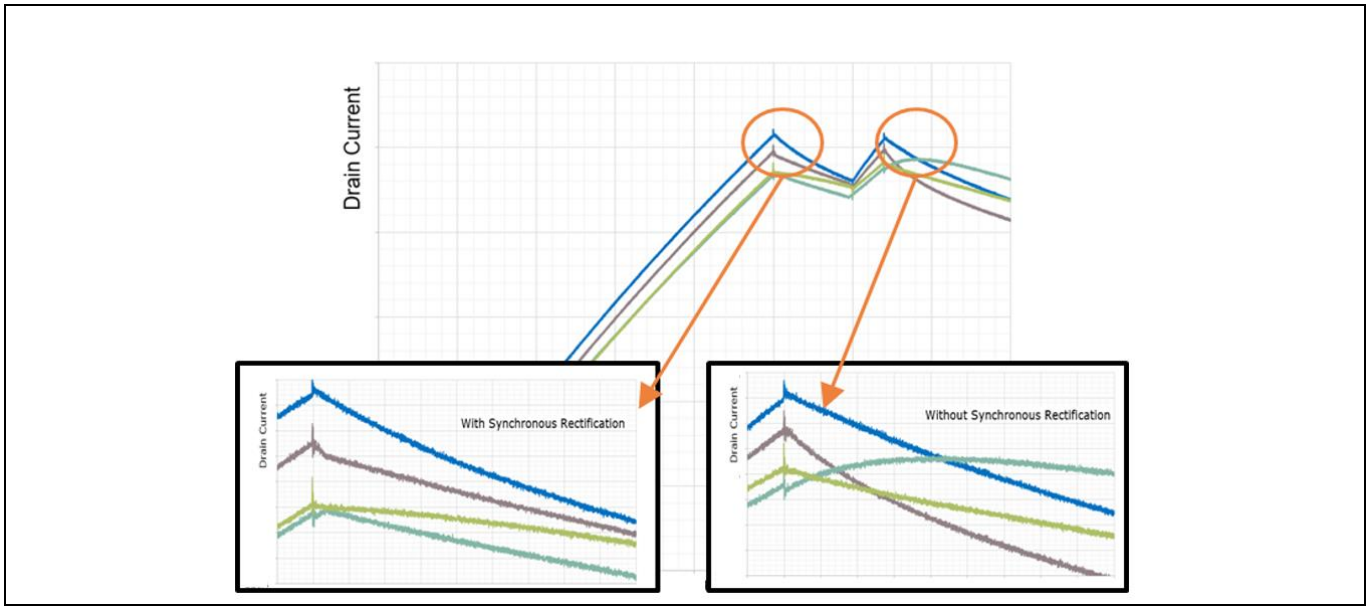

Figure 7 **Paralleling of four modules: drain current waveform with and without synchronious rectification**

2.2.3 Dynamic behavior

During every switching event, the effect of the $V_{GS(th)}$ hysteresis can be observed. This effect is best visible by measuring the gate charge, the transconductance, or by comparing the switching waveforms for turn-on and turn-off. The lower the level of $V_{GS(off)}$, the better the hysteresis effect can be observed.
A turn-on at $V_{GS(off)}$ = -5 V leads to a dynamically reduced threshold voltage compared to a turn-on at $V_{GS(off)}$ = -0 V. At -5 V, an earlier start of the Miller phase can be observed, and the voltage during the Miller phase is lower which results in a higher transconductance [3]

Where a constant delta between $V_{GS(off)}$ and $V_{GS(on)}$ was applied, e.g -5 V/+15 V and -2 V/+18 V, investigations showed that the Miller phase was reached earliest at the lowest $V_{GS(off)}$ level, resulting in the highest transconductance [3].

If $V_{GS(on)}$ is kept constant, e.g., at 18 V, the lowest $V_{GS(off)}$ level shows the highest dv/dt during turn-on. Figure 8 (left) shows the maximum dv/dt during turn-on for different $V_{GS(off)}$ levels and a constant $V_{GS(on)}$ of 18 V. However, for turn-off, the Miller ramp is independent of the $V_{GS(off)}$ level at the same position. Nevertheless, a slight acceleration can be observed, but mainly due to higher driving voltage, e.g 0 V/+18 V versus -5 V/+18 V (see Figure 8 (right)) [4].

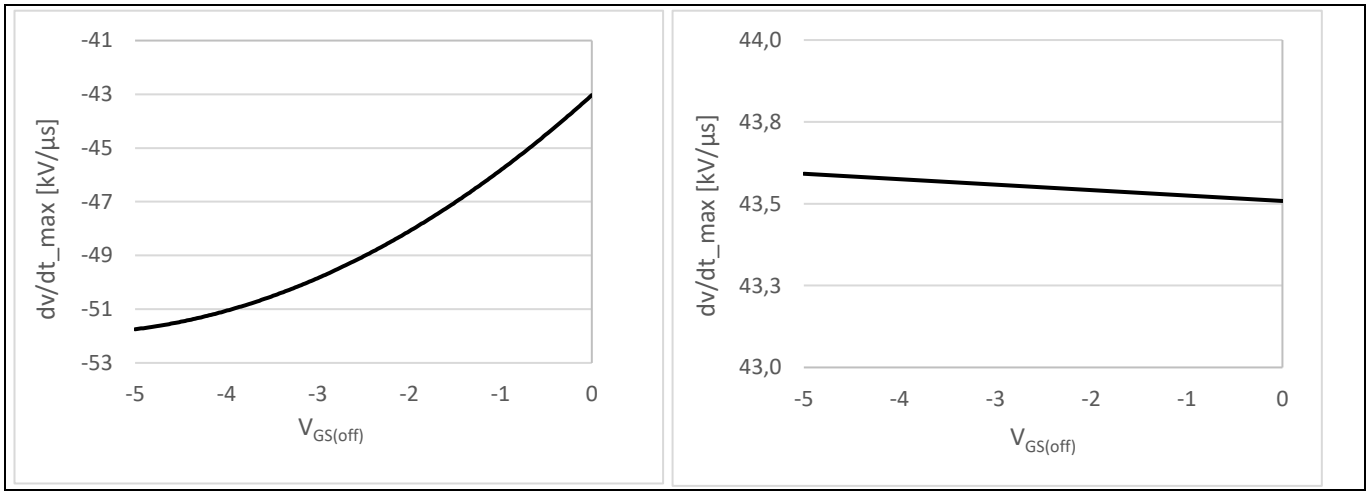

Figure 8 **(Left) Turn-on with FS55MR12W1M1H_B11: dv/dt vs. $V_{GS(off)}$ at DC-link=600 V, T_{vjop} = 25°C, R_{gon} = 4 Ω, R_{goff} = 3 Ω, I_{DS} = 15 A, V_{GS} = 18 V.**
(Right) Turn-off with FS55MR12W1M1H_B11: dv/dt vs. $V_{GS(off)}$ at DC-link=600 V, T_{vjop} = 25°C, R_{gon}= 4 Ω, R_{goff} = 3 Ω, I_{DS} = 15 A, V_{GS} = 18 V.

2.2.4 Parasitic turn-on

Many applications that make use of the CoolSiC™ MOSFET modules try to minimize switching loss by accepting steep transients in the voltage and current. Therefore, the immunity of the device against parasitic turn-on is paramount. With the CoolSiC™ MOSFET M1H, this topic has been addressed in the chip design.

Unwanted parasitic turn-on of a semiconductor switch can occur when its antiparallel diode is turned off. A schematic scenario is shown in the drawing in Figure 9. The current I_L is freewheeling via the body diode of the low-side device S2 until switch S1 turns on. When the load current has fully commutated to S1, S2 starts blocking the voltage between the drain and the source. Via the Miller capacitance C_{GD}, the rising drain potential on S2 pulls up the gate voltage. In case the threshold level is exceeded a shoot-through occurs [2].

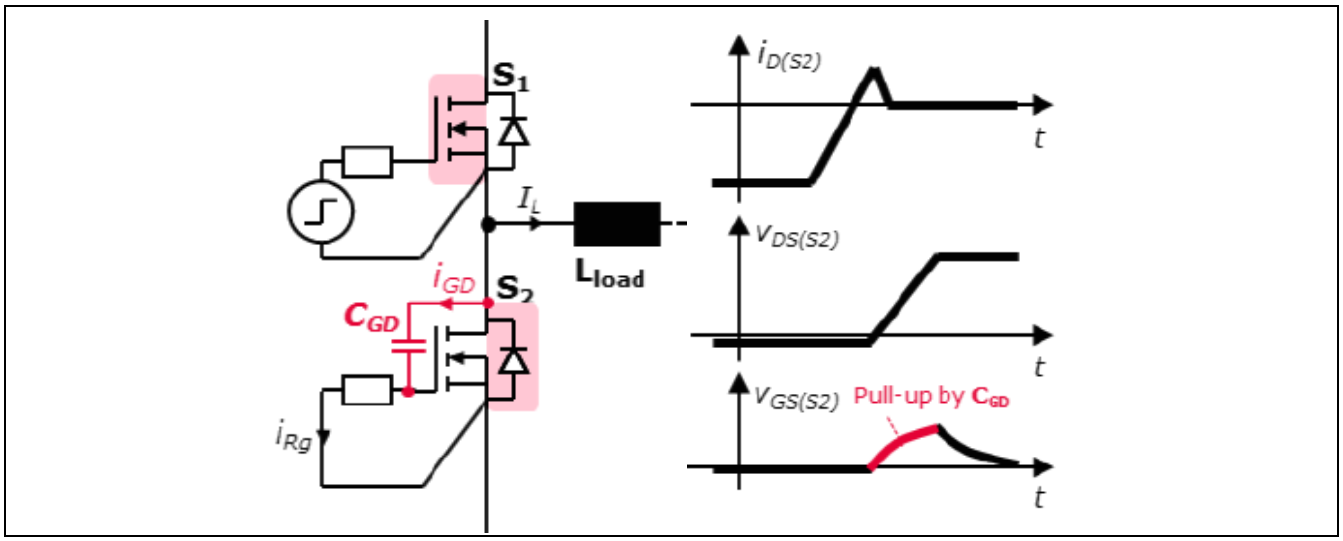

Figure 9 Schematic explaination of a parasitic turn-on event [2]

The gate-charge characteristic of a certain device gives an indication of the principal resilience against parasitic turn-on. The lower the ratio $Q_{GD}/Q_{GS,th}$ of a device the higher the resilience. Devices with a charge ratio smaller than one are considered insusceptible to parasitic turn-on as far as inductive voltage drops can be neglected. That holds true for CoolSiC™ MOSFET M1H technology. While a brief look at the data sheet of a switch is enough to get an impression of the charge ratio and its susceptibility to parasitic turn-on, the indication is often rather qualitative. First, the influence of the blocking voltage is typically not shown, and second, due to the DIBL effect (drain-induced barrier lowering), a clear separation of $Q_{GS,th}$ and Q_{GD} is difficult [2].

Another indication about immunity against parasitic turn-on is given by the threshold voltage $V_{GS(th)}$. The threshold voltage is the gate-source voltage required for the current to start flowing through the channel of the device at a specific drain-to-source current. Figure 10 (left) shows the threshold voltage versus temperature at I_{DS} = 6 mA for the 55 mΩ device. The threshold voltage $V_{GS(th)}$ is measured by first applying one 1 millisecond pulse-gate voltage at a V_{GS} = +20 V as a precondition [1, 6], then the threshold-voltage value of $V_{GS(th)}$ is read at V_{GS}= V_{DS} by forcing current I_{DS} = 6 mA . Results show that, the typical threshold voltage $V_{GS(th)}$ equals 4.3 V at 25°C and I_{DS}= 6 mA. This provides good noise immunity against parasitic turn-on, meaning ease of use for the device.

Typically, SiC MOSFETs have a short-channel effect resulting in a reduction of threshold voltage at higher drain voltages. The effect is called DIBL already known from low-voltage Si power MOSFETs. [1]. For the CoolSiC™ MOSFET M1H, the $V_{GS(th)}$ is reduced when blocking V_{DS} voltage increases as shown in Figure 10 on the right. With DC voltage at normal maximum operating voltage of 800 V, the $V_{GS(th)}$ of CoolSiC™ MOSFET M1H is typically 2.6 V at a junction temperature of 150°C.

Gate-source voltage – the right choice

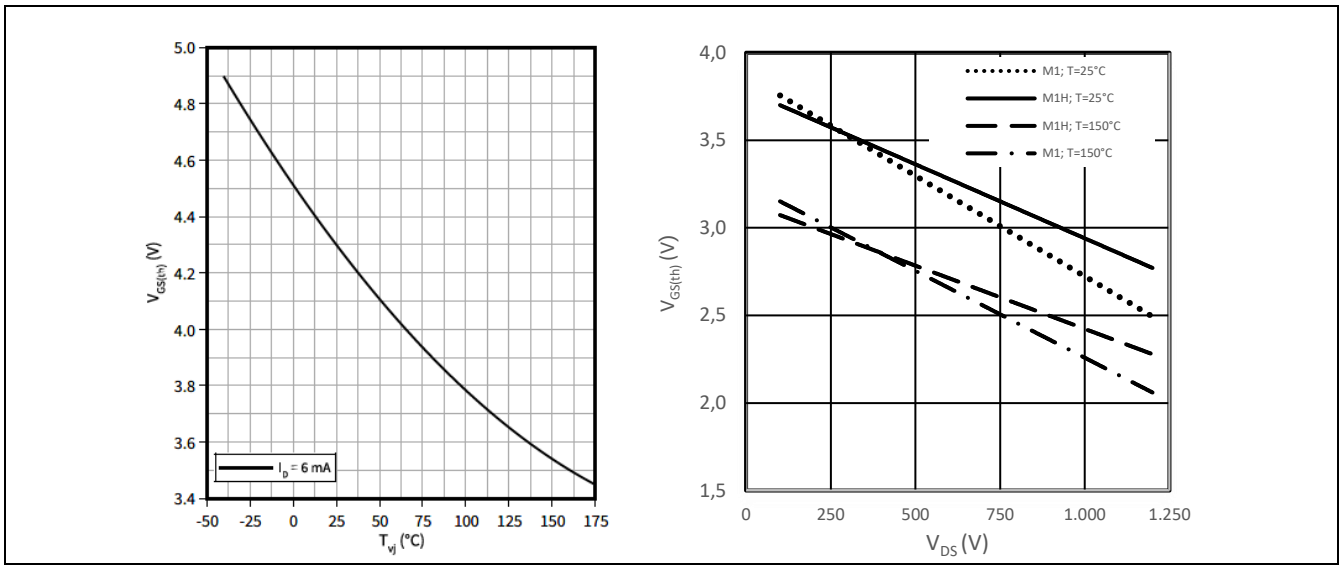

Figure 10 **(Left) Typical gate-source threshold voltage as a function of junction temperature (I_{DS}=6 mA, V_{GS}=V_{DS}); (Right) Typical gate-source threshold voltage as a function of drain-source voltage ($T_{vj,op}$ = 150°C)**

If a parasitic turn-on occurs, additional losses can be observed. Figure 11 shows the turn-on losses of the FS55MR12W1M1H_B11 for different $V_{GS(off)}$ levels. For the measurements a double-pulse test setup was used. In the setup, the active switch is turned off with -3 V, while the negative gate-sourve voltage of the passive switched was varied between 0… -5 V. The turn-on losses of the active switch start slightly to rise from -2 V for the passive switch, which indicates that a parasitic turn-on occured.

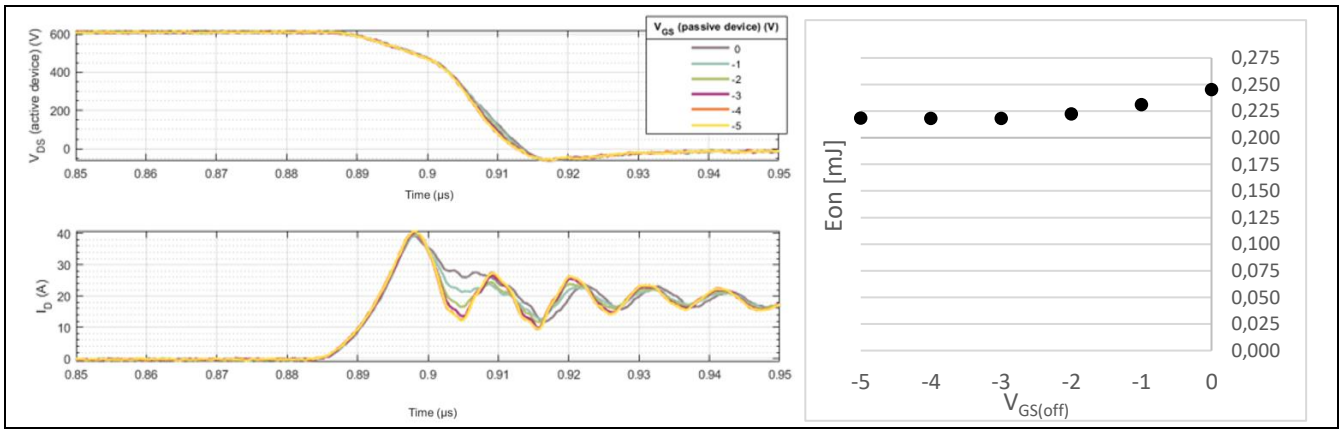

Figure 11 **(Left) FS55MR12W1M1H_B11: Turn-on at DC-link=600 V, T_{vjop} = 25°C, R_{gon} = 4 Ω, R_{goff}= 3 Ω, I_D=15 A. Passive switch $V_{GS(off)}$ = 0…-5 V; Active switch at $V_{GS(off)}$ = -3 V**
(Right) FS55MR12W1M1H_B11: Eon (active switch) vs. $V_{GS(off)}$ (passive switch) at DC-link = 600 V, T_{vjop} = 25°C, R_{gon} = 4 Ω, R_{goff} = 3 Ω, I_D=15 A; Active switch at $V_{GS(off)}$ = -3 V

The following parameters have an impact:

- Temperature – $T_{vj\,op}$
- DC-link voltage - V_{DS}
- R_{gon} of the active device and R_{goff} of the passive device
- Gate-source voltage - $V_{GS(on)}$ and $V_{GS(off)}$
- Current - I_D

Gate-source voltage – the right choice

Depending on the individual requirements in the respective application, the $V_{GS(off)}$ level needs to be defined carefully to prevent parasitic turn-on or to keep the additional losses at an acceptable level.

2.2.5 Dynamic characteristics of the passive switch

The SiC-MOSFET die operated in the freewheeling path (S2 in Figure 9) contains two internal structures – the MOSFET with a gate and channel, and a bipolar diode structure usually referred to as a body diode. Both structures contribute to the dynamic behavior as follows:

- Capacitive contribution from both parts, leading to a capacitive charge Q_C and a stored energy E_{oss}
- Contribution from the plasma in the bipolar diode, negligible at moderate currents and temperatures but becoming relevant at more demanding conditions
- Contribution from the SiC-MOSFET due to parasitic turn-on

Measuring E_{fr} according to IEC 60747-8 is comparable to measuring the reverse recovery of a diode. This measurement value only shows the summed up effect of all the three contributions. However, the dependencies and the thermal effects are different.

- For the capacitive contribution, there is no other significant parameter besides the DC-link voltage. The energy E_{oss} is dissipated at the next turn-on event of this device in case of hard switching or is recovered in case of soft switching
- The contribution from plasma, besides the parameters already mentioned, is a function of di/dt and stray inductance. As the off-state voltage also governs the current sharing between the channel and the diode structure, it has to be considered as a further parameter. This energy has to be considered as a switching loss
- The contribution from parasitic turn-on varies with the gate condition on the passive switch and the duration the diode as been in conduction mode. Figure 11 describes the impact of the gate driving condition on the passive switch. Details on the impact of conduction time are provided in [7]. Also, this energy contributes to switching loss.

The datasheet only documents the overall value of the charge and energy to keep the data simple and transparent.

2.2.6 Gate charge and gate driver output power rating

The total gate charge, Q_G, is defined as the charge from the origin (e.g., $V_{GS(off)}$ = - 3 V) to the point on the curve at which the driving voltage equals the actual gate-to-source voltage of the device (e.g., $V_{GS(on)}$ = 18 V). Thus, the choice of the on-state and off-state gate voltage has an impact on the share of the gate charge required when using a lower voltage range for driving. Figure 12 provides the gate-charge characteristic at I_{DS}=15 A for the FS55MR12W1M1H_B11. Here the typical value of Q_G=0.045 µC can be read off. This means that depending on the applied gate-source voltage, the required output power (P_{GD}) for the gate driver can be derived accordingly.

- $P_{GD} = f_{sw} \times Q'_G \times \Delta V_{GS}$
- f_{sw} = SiC MOSFET switching frequency
- Q'_G = Gate charge, reading taken from diagram for the voltage range actually used
- $\Delta V_{GS} = |V_{GS(on)}| + |V_{GS(off)}|$ (Steady state values)

As explained in Section Figure 7, the start of the Miller ramp depends on the applied negative gate-source voltage.

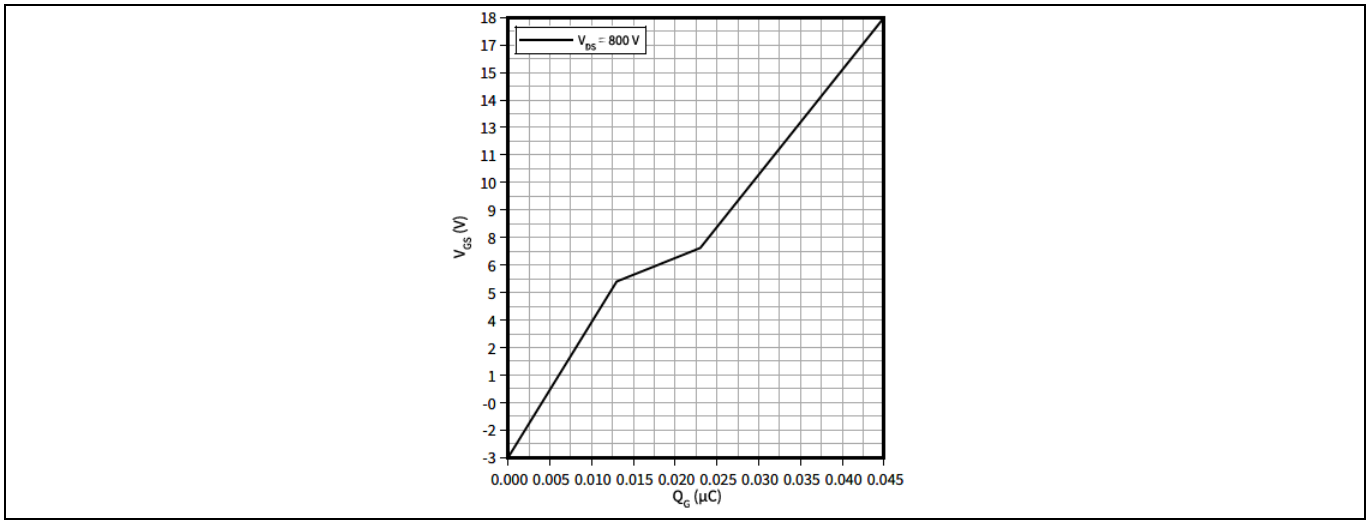

Figure 12 Typical gate charge, $V_{GS} = f(Q_G)$, $I_{DS} = 15$ A, $V_{DS} = 800$ V, turn-on pulse

2.2.7 Short-circuit capability

Figure 13 depicts the typical short-circuit waveforms of a 1200 V device for different $V_{GS(off)}$ voltages. Initially, the drain current increases rapidly and reaches the peak current level. After the peak current is reached, the drain current decreases significantly. This is due to the reduction in carrier mobility and JFET effect with temperature increase as a consequence of self-heating. The waveforms show clean and robust behavior, which proves a typical 2 µs SC capability. Typically, the modules can withstand ten short-circuit events over their lifetime.

The peak current level at the beginning strongly depends on the DC-link voltage, the temperature, the internal layout concept of the module and the applied $V_{GS(on)}$ and $V_{GS(off)}$ level.
Due to the DIBL effect with increasing DC-link voltage or temperature, the saturation current rises more strongly [4].
The same holds true for the applied $V_{GS(off)}$ level. The lower the applied $V_{GS(off)}$ voltage, the higher is the peak current when the short circuit starts to occur. Figure 13 shows clearly that the peak current is higher for $V_{GS(off)} = -5$ V than for $V_{GS(off)} = 0$ V. This effect should be considered for the short-circuit protection design.
Depending on the module's internal layout concept, current rises slower when a negative feedback is induced via the di/dt against the applied V_{GS}. In such cases, the peak current is reduced but the dynamic losses are higher.

Note: Not all modules are specified with short-circuit capability in the respective data sheet. In case a short circuit is specified, it is mandatory to apply +15 V for $V_{GS(on)}$ and 0…-5 V for $V_{GS(off)}$ for the above-mentioned reasons. 2kV CoolSiC™ MOSFET M1H products generally show no short-circuit specification.

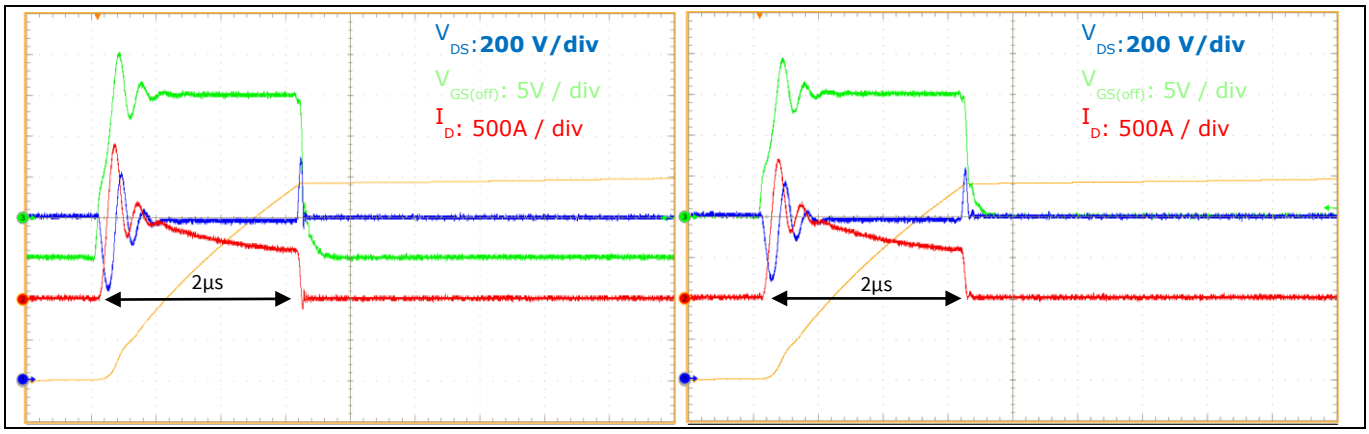

Figure 13 (Left) Typical short-circuit waveforms at V_{DS} = 800 V and V_{GS} = -5 V (right) Typical short-circuit waveforms at V_{DS} = 800 V and V_{GS} = 0 V

2.2.8 $V_{GS(th)}$-drift

The CoolSiC™ MOSFET M1H shows significant improvements with regard to threshold voltage stability. This allows designers to extend the allowed gate operation window significantly when compared to M1. Extensive tests under various operating conditions were carried out by Infineon to develop a predictive model that describes the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}). This provides the opportunity to predict the worst-case $R_{DS(on)}$ change for arbitrary mission profiles accurately.

The impact of the $V_{GS(th)}$ increase on the $R_{DS(on)}$ differs among the voltage classes of the devices. The higher the voltage class, the more pronounced is the contribution of the epitaxial layer resistance (R_{epi}). Consequently, the R_{epi} is more dominant, and contributes more to the total $R_{DS(on)}$ compared to smaller voltage classes. As a consequence, we can conclude that the impact of the drift in $V_{GS(th)}$ on $R_{DS(on)}$ is less severe for higher voltage classes

To assess the $R_{DS(on)}$ drift for the worst-case, end-of-mission profile (EoMP) of individual applications, the total number of switching events until EoMP should be considered. This number can be easily calculated from the target lifetime, the total operating time, and the switching frequency of the application.

For more information please see: AN2018-09 Guidelines for CoolSiC MOSFET gate drive voltage window [3]

2.2.9 FIT rates and lifetime

The bathtub curve is widely used to describe the FIT rates. The bathtub curve can be divided into three parts:

- A first part with a decreasing failure rate, also known as early failure. Screening processes in the production lines sort out the weak devices and exclude them from the field
- The second part shows a constant flat failure rate. For SiC MOSFETs, this area is mainly defined by gate oxide fails and cosmic ray effects
- In the third and last part, an increasing failure rate can be observed. This section is also known as the wear out (intrinsic material failures)

For on-state operation, Infineon recommends V_{GS} = +15 to +18 V for the CoolSiC™ products. For off-state operation a V_{GS} of 0 V to -5 V is recommended for CoolSiC™ MOSFET M1H. The trade-off between a longer lifetime and performance is well balanced at this operating voltage.

In general, our device could be driven with higher gate-source voltages than 18 V, which further improves the on-state behavior. However, the lifetime of the gate oxide will be reduced, since gate-oxide stress is higher, thus accelerating the aging of the device. Furthermore, the failure rate is increased by using a higher gate-source voltage than 18 V.

For operating conditions that deviate from Infineon recommendations, please consult with your Infineon contact for impact on lifetimes and FIT rates.

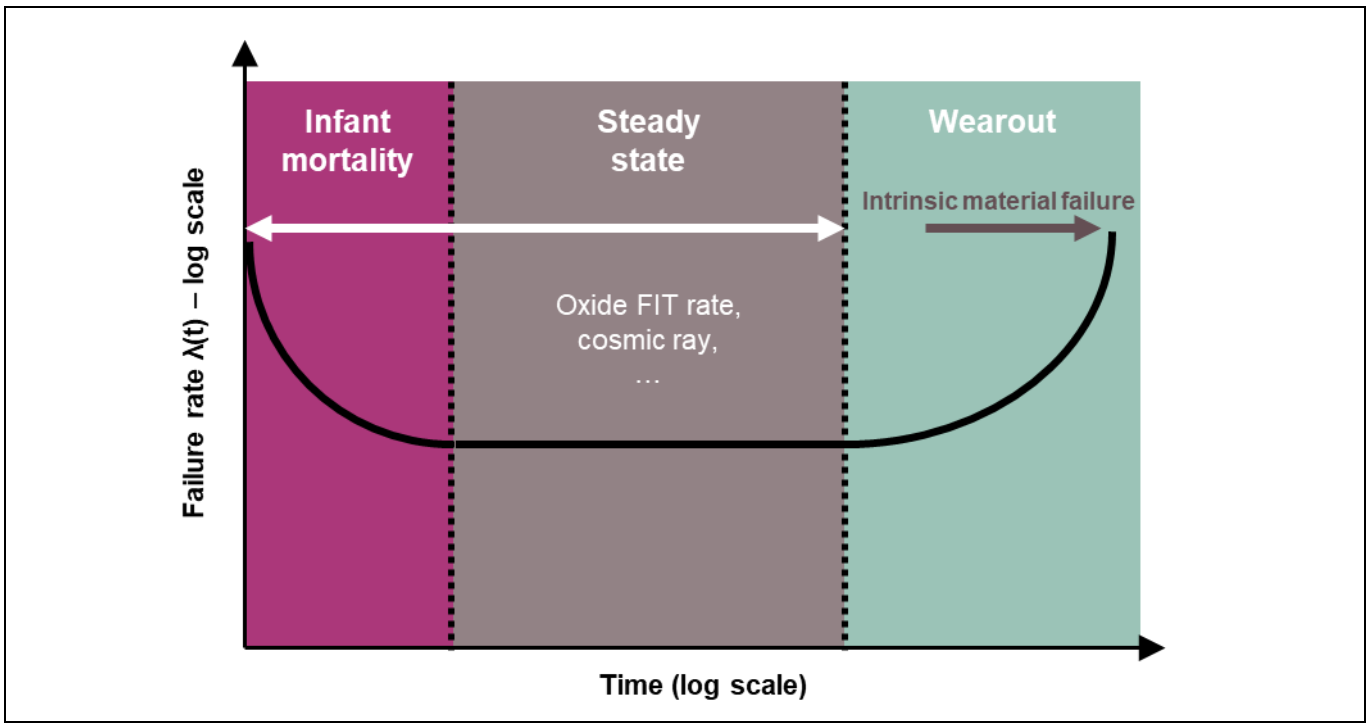

Figure 14 A typical bathtub curve

3 Optimizing switching performance: Design and driving

An external gate resistance critically impacts the switching speed and must be carefully chosen. Constraints on V_{DS} and V_{GS} under different operating conditions should be kept in mind for both active and passive switches. Exceeding these limits can cause irreversible drift in electrical parameters or accelerate degradation, leading to reduced lifetime. Conversely, higher external gate resistance means slower switching speed and higher switching losses. This necessitates the identification of the sweet spot that balances both switching speed and reliability.

With a low-inductive design, the drain-source voltage overshoot (passive switch during turn-on and active switch during turn-off) can be reduced significantly. Both E_{on} and E_{off} can be reduced by reducing the DC-link inductance or selecting a smaller gate resistance, R_G.

Figure 15 shows E_{on}, E_{off}, and the sum of both at different DC-link inductances. All in all, the total switching loss can be reduced significantly through a low-inductive design. This is essential for maximizing the performance and efficiency of the inverter in operations with high switching frequency. Reducing E_{off} is highly important, especially in DC-DC resonant converters with ZVS, where turn-off losses are the highest contributors to switching losses.

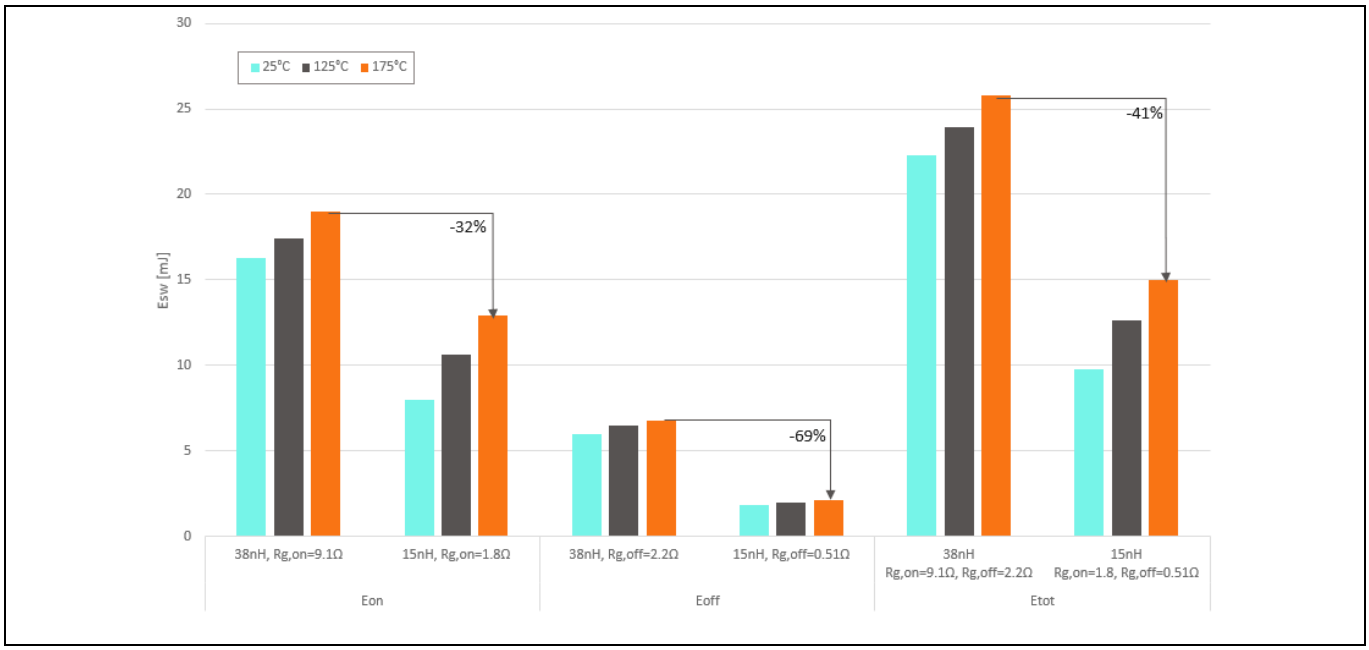

Figure 15 Influence of Ls on the total Esw at Vdc=1200V, Ic=160A and V_{GS} = -3/18V in the 2kV CoolSiC™ MOSFET M1H device

A gate driver designed following the recommendations in [8] and [9] and with minimal gate-loop inductance, provides significant benefits for fast switching applications.

Optimizing the dead time is equally important. Dead time refers to the brief period (typically in the range of 100 – 1000 nanoseconds) when both the high-side and low-side switches are turned off simultaneously. This interval is necessary to prevent shoot-through currents and ensure a reliable, damage-free design.

Infineon defines dead time as the time between the on and off PWM signals, as explained in Figure 16. To set an appropriate dead time, any additional gate driver and delays in switch reaction should be considered.

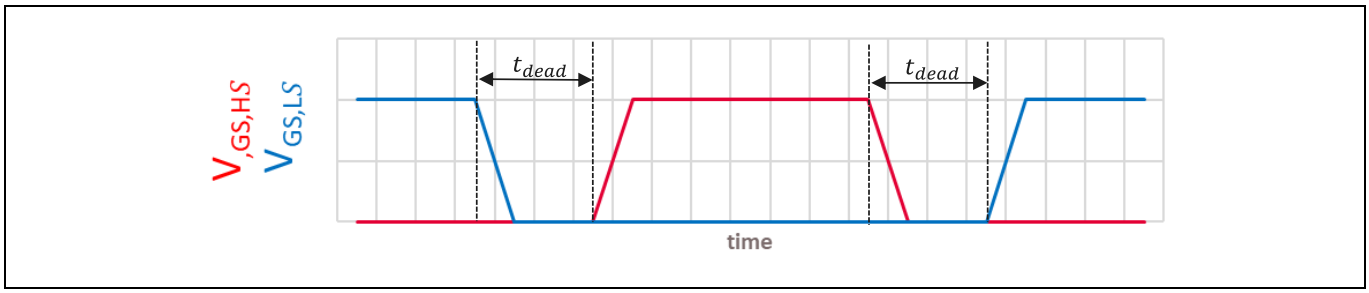

Figure 16 Deadtime definition

The dead time should be long enough to mitigate the risk of short circuits but short enough to minimize the voltage peak, Vrmax, which is caused by the body diode's reverse recovery during turn-on.

During the deadtime, the body diode conducts the load current and stored charge accumulates in the body diode. When the voltage direction changes, a high dv/dt is applied to the body diode, causing a high di/dt and consequently, a voltage overshoot (Figure 17). When testing with reduced deadtime of 100 nanoseconds, the overvoltage is reduced more than 400V for a 2kV CoolSiC™ MOSFET M1H device at T_{vj} = 175 °C, V_{DD} = 1200 V, I_D = 160 A, V_{GS} = -3 V / 18 V.

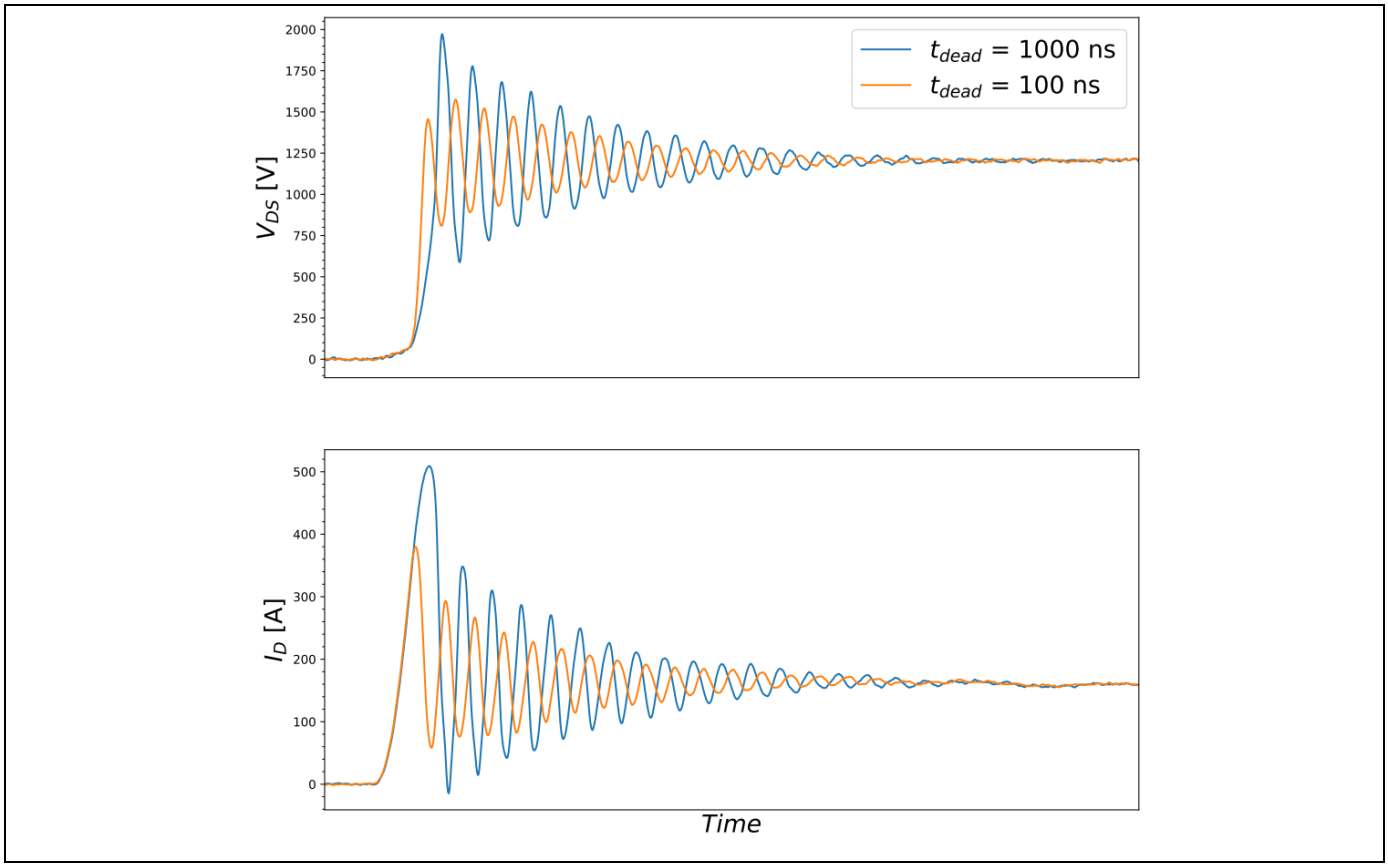

Figure 17 Exemplary diode recovery waveform showing the influence of the dead time (1000 nanoseconds s and 100 nanoseconds) in a 2kV CoolSiC™ MOSFET M1H device at 15nH DC-link inductance
(Top) Drain Source Voltage
(Bottom) Drain Current

Optimizing switching performance: Design and driving

When possible, lower the tdead value so that the device does not reach its equilibrium stage, thus minimizing Qrr. This in turn decreases the turn-on energy loss, Eon, and the recovery loss, Erec, [7], [10].

This impact is visible in some product datasheets. Additional diagrams (see Figure 18) are provided for the cases where normalized switching losses are shown as a function of dead time at nominal current and nominal gate resistance but were originally defined with a large dead time. The lowest dead time may vary for each product and refers to the best case. If no further information is provided in the datasheet, the losses are measured with no deadtime control and thus, refer to measurements with large deadtime in the saturated area. The saturation happens due to the saturation on the plasma concentration and happens earlier the smaller the voltage class.

With the FF6MR20W2M1H 2 kV CoolSiC MOSFET product [11], turn-on losses can be reduced by up to 35% and recovery losses by up to 65%. The performance gain is even more significant in cases where R_g has been optimized due to a low dead time and thus, faster switching. This can be seen in Figure 19 where switching losses are given as a function of current at two different dead times and respectively adjusted R_g values. This information is also available in the product datasheets where values with low dead time are referred to as “optimized” or marked with an additional “o”.

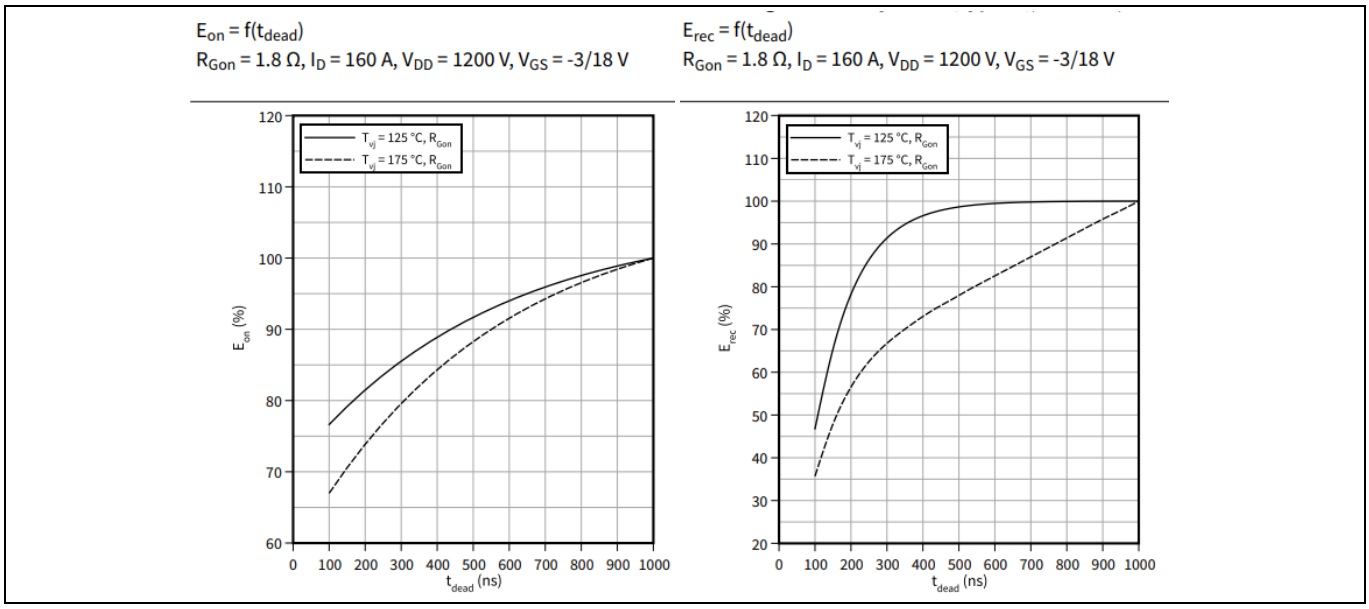

Figure 18 Normalized turn-on and recovery energies as a function of deadtime with FF6MR20W2M1H_B70

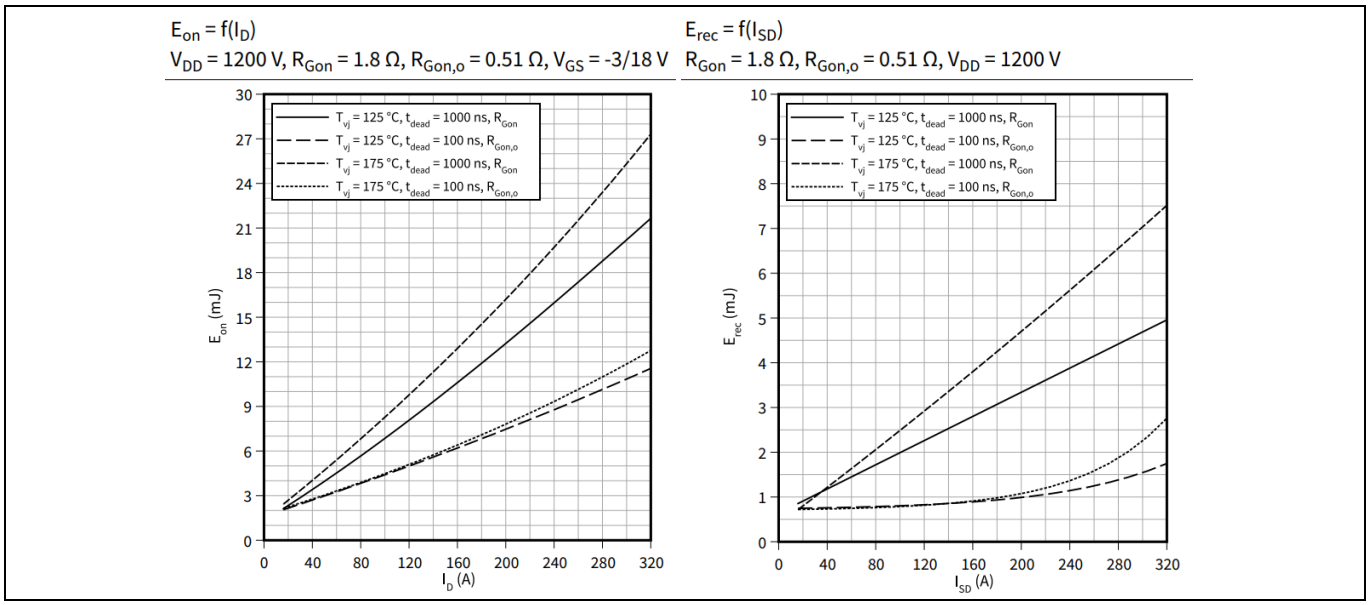

Figure 19 Turn-on and recovery energies as a function of current and deadtime with FF6MR20W2M1H_B70

When the measures above, low DC-link inductance and low deadtime, are implemented, the gate source voltage can still be a limiting factor that restricts the possibility of faster switching if reached the maximum limits of 23V and -10V. The easiest way to evaluate it is measuring at the gate-source terminals. However, this does not have a direct relation to the undershoots and overshoots seen by the die. The overshoots and undershoots are influenced by the internal inductances of the gate loop, the internal resistance of the SiC MOSFET, and the resistance inherent in the layout design itself (Figure 20). To assess the actual voltage seen by the die, an approach for post-processing of signals is discussed in [10]. Reach out to your Infineon contact for additional guidance on the evaluation.

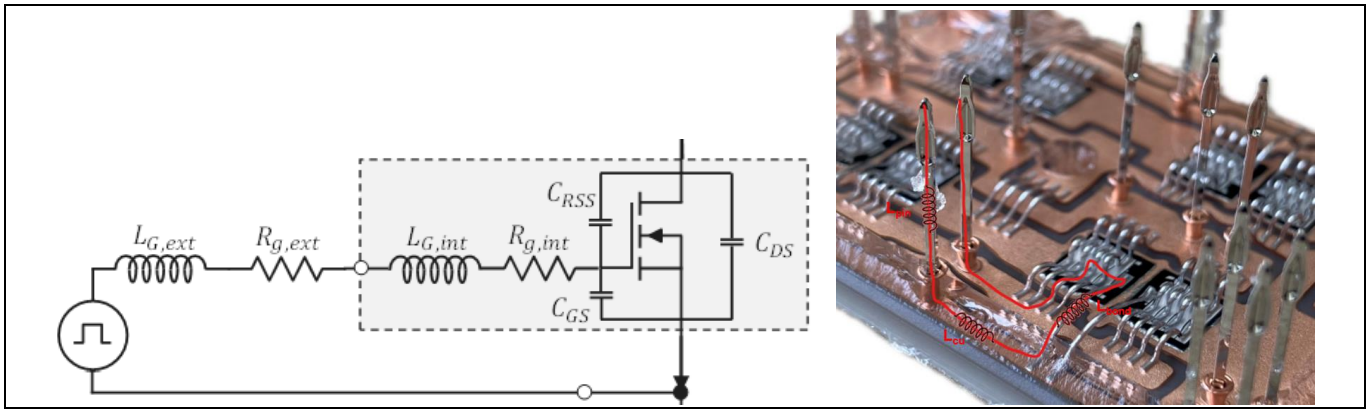

Figure 20 Internal gate-loop inductance

4 Maximum virtual junction temperature $T_{vj\ op}$

4.1 Definition of 175°C operation junction temperature

CoolSiC™ MOSFET M1H allows for operation at a temperature of $T_{vj\ op}$ = 175°C under overload conditions. This matches the typical requirement in several applications where high current and thus, temperature is only required in the short term.

Figure 21 shows the definition of the allowed operation junction temperature under switching conditions for CoolSiC™ MOSFET M1H. For normal operation, the maximum junction temperature is 150°C. During overload conditions, a maximum junction temperature above T_{vjop}= 150°C and up to T_{vjop} = 175°C is allowed for a maximum duration of t_1= 60 seconds. The overload duration where the T_{vjop} is above 150°C must be within 20% of the load cycle time (T), e.g. t_1=60 seconds every T=300 seconds. This ability to withstand a higher junction temperature (over 150°C) can enable higher power density. However, it can also result in higher heatsink temperatures.

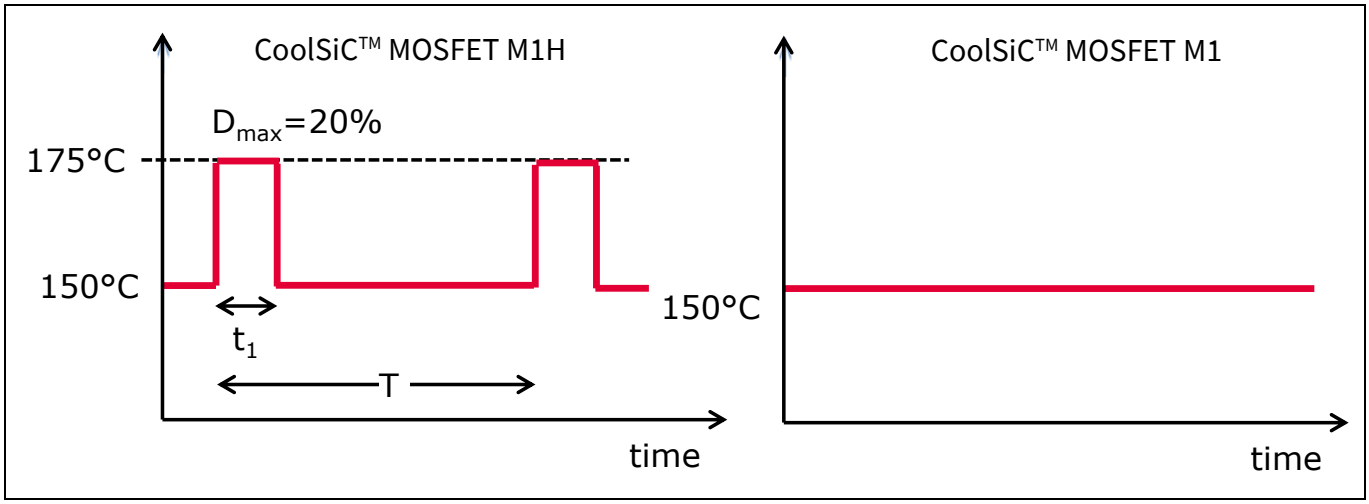

Figure 21 Maximum operation junction temperature definition for CoolSiC™ MOSFET M1H and M1

The maximum temperature definition shown in Figure 21 should be considered as the maximum Tvjop limit including the temperature ripple caused by the fundamental output frequency. Figure 22 provides two examples of junction temperature profiles. In Figure 2216 (left), Tvjop exceeds 150°C for t1 = 50 seconds. It is below 150°C for the rest of the T = 300 seconds cycle. Therefore, the duty cycle is 16.7%. This condition is acceptable from the point of view of a maximum operating junction temperature. Another example is shown in Figure 22 (right). In this case, the temperature exceeds the maximum curve of the junction temperature for the entire duration of the load profile. This operation would not be allowed.

The number of hours the temperature can be allowed to exceed 150°C in an application depends on the time constant of the heatsink. In addition, operating with this load profile at boundary conditions for more than several hundred hours can lead to traces of silicone oil on the module housing. If this type of load profile is to be used for a high number of hours, please contact your Infineon support channel to perform a detailed analysis for your application.

In the case of an automotive grade product, please refer to the respective datasheets for the maximum allowed junction temperature to ensure the proper functioning and reliability of the product.

Maximum virtual junction temperature Tvj op

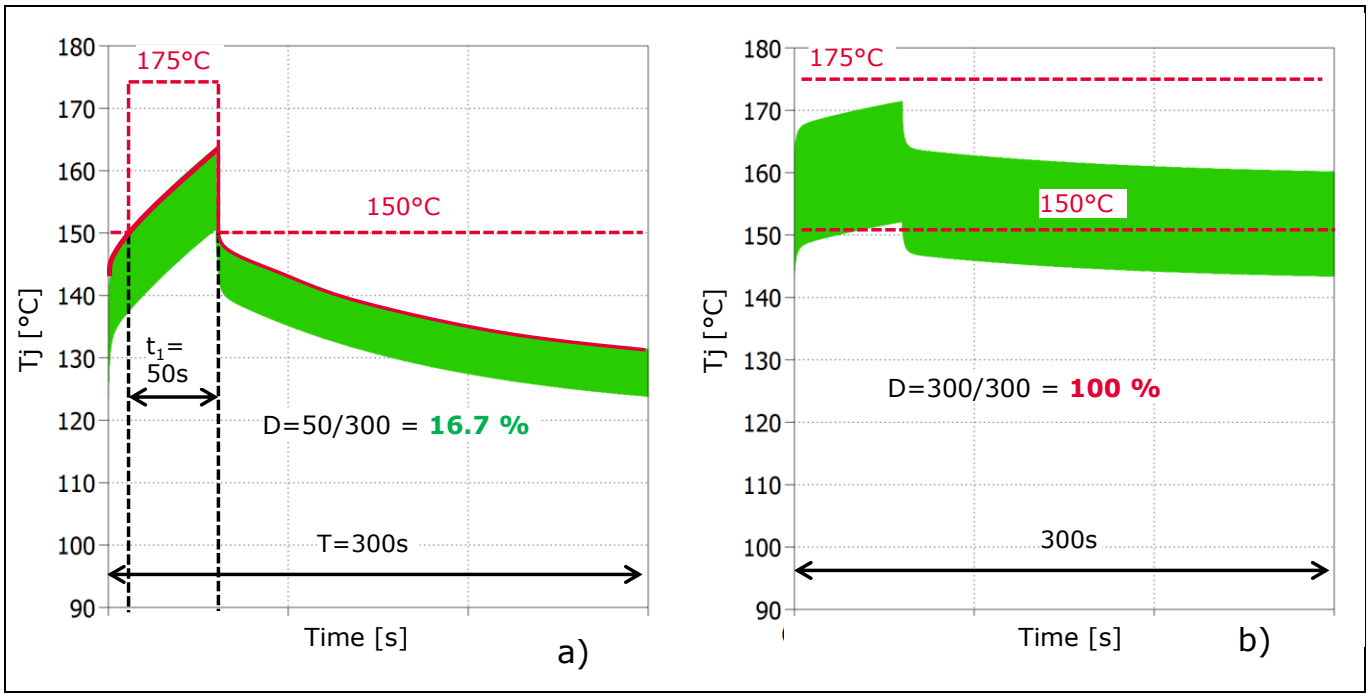

Figure 22 Examples illustrating when the 175°C junction temperature operation is allowed (left) and not allowed (right)

4.1.1 System-temperature limitation for even higher operation temperature

The CoolSiC™ MOSFET M1H allows a 25 K higher operating junction temperature than the M1. With this feature, the system using M1H has even higher power density and component temperatures, e.g., PCB, heatsink, and module frame. Several restrictions should be considered as described in the following sections.

4.1.1.1 Frame-temperature limitation

The relative temperature index (RTI) value is specified in the datasheet. The value is the characteristic parameter related to thermal degradation of the plastic material. During the operation, the module-frame temperature should not exceed this value. Otherwise, the UL standard ratings will be violated.

4.1.1.2 PCB-temperature limitation

With a higher junction temperature, the power density of the system can also be higher. This means that, in case of easy modules, the current that goes through each pin can increase, as some pinouts for M1 and M1H modules are the same. With this increase in current, the PCB temperature rise should be carefully considered. The maximum allowed PCB temperature depends on the PCB material itself. Thicker copper layers, wider tracks, increased number of layers, and system cooling can help reduce the PCB temperature.

4.1.1.3 Heatsink-temperature limitation

If the module is pre-applied with Infineon's thermal interface material (TIM), the heatsink temperature should not exceed the operating temperature allowed for the thermal interface material.

5 Glossary

$R_{DS(on)}$	Resistance at the actual junction temperature, given at the datasheet current I_{DS}
$V_{GS(th)}$	Voltage between gate and source at which current starts to flow
I_{DSS}	Drain-source leakage current at shorted gate-source voltage = 0 V and V_{DSS}= 1200 V
V_{GS}	Bias between gateand source, corresponds to V_{ge} in an IGBT
I_{DS}	Load current flowing between drain and source
V_{DS}	Bias between drain and source, corresponds to V_{ce} in an IGBT
C_{rss}	This value is defined as defined as the capacitance effective between gate and drain. It is measured at 800 V, which is the typical DC-link voltage in the application. It equals the gate-drain capacitance.
C_{gs}	Effective capacitance between source and gate
C_{iss}	This value is defined as the capacitance effective between gate and source. It is measured at 800 V, which is the typical DC-link voltage in the application. It equals the sum of gate-source capacitance and gate-drain capacitance.
C_{gd}	Effective capacitance between drain and gate
C_{oss}	This value is defined as the capacitance effective between source and drain. It is measured at 800 V, which is the typical DC-link voltage in the application. It equals the sum of gate-drain capacitance and gate-source capacitance.
C_{ds}	Effective capacitance between source and drain
R_{G_int}	Effective internal gate resistance, comprising the sum of the resistance of the distributed gate network and additional resistors added to the gate pad
E_{on}	Turn-on loss energy, measured with integration limits according to IEC 60747-8, but with inductive load
E_{off}	Turn-off loss energy, measured with integration limits according to IEC 60747-8, but with inductive load
E_{tot}	Total loss energy, sum of E_{on} and E_{off}
Q_{GD}	Typically the gate charge needed to pass the Miller plateau
Q_G	Total gate charge
$Q_{GS,pl}$	Gate charge needed to reach the Miller from the off-state V_{GS}
R_G	Externally applied gate resistance, adds to R_{G_int}
$R_{G(on)}$	Externally applied gate resistance for turn-on
$R_{G(off)}$	Externally applied gate resistance for turn-off
$T_{vj\,op}$	Virtual junction temperature during operation. The term “virtual” refers to a temperature measured by temperature sensitive electrical parameters as described in the standards of the IEC 60747 series

6 Reference

[1] AN2017-46: CoolSiC™ 1200 V SiC MOSFET Application Note

[2] K. Sobe, T. Basler, and B. Klobucar, “Characterization of the parasitic turn-on behavior of discrete CoolSiC™ MOSFETs”, PCIM 2019

[3] AN2018-09: Guidelines for CoolSiC MOSFET gate drive voltage window

[4] T. Basler, D. Heer, D. Peters, T. Aichinger, and R. Schörner, “ Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET”, PCIM 2018

[5] AN2018-14: TRENCHSTOP™ 1200 V IGBT7 T7 Application Note

[6] FS55MR12W1M1H_B11 data sheet: Revision 1.20, 2022-06-09

[7] P. Sochor, A. Huerner, M. Hell, and R. Elpelt “Understanding the Turn-off Behavior of SiC MOSFET Body Diodes in Fast Switching Applications” PCIM 2021

[8] AN2017-04: Advanced gate drive options for silicon carbide (SiC) MOSFETs using EiceDRIVER™

[9] AN2013-10: External Booster for Driver IC

[10] R. Hensch, H. Ali, and D. Domes, “Understanding Gate-Source Oscillations and Application of Low Dead Times in SiC Power Modules”, ECCE Europe 2024

[11] FF6MR20W2M1H_B70 data sheet: Revision 1.00, 2024-08-23

Revision history

Document version	Date of release	Description of changes
Revision 1.0	2022-06-09	First release
Revision 2.0	2024-11-20	Included 2kV M1H, considerations of Vgs in chip, DC-link inductance and deadtime.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2018-01-0520

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN2017-4613

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

Please note that this product is not qualified according to the AEC Q100 or AEC Q101 documents of the Automotive Electronics Council.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.