Dual Gate MOSFET 80 V and evaluation board

Linear operation and low RDS(on) combined in a single MOSFET

About this document

Scope and purpose

This document should gives guidance on how to use the Dual Gate MOSFET for short circuit clamping and capacitor charging in disconnect switch applications. This will also be explained based on available evaluation boards and measurements.

Intended audience

This document is intended for design engineers of automotive power distribution and disconnect switch applications such as 48 V battery disconnect switches, which require high short circuit robustness and capacitor charging capability.

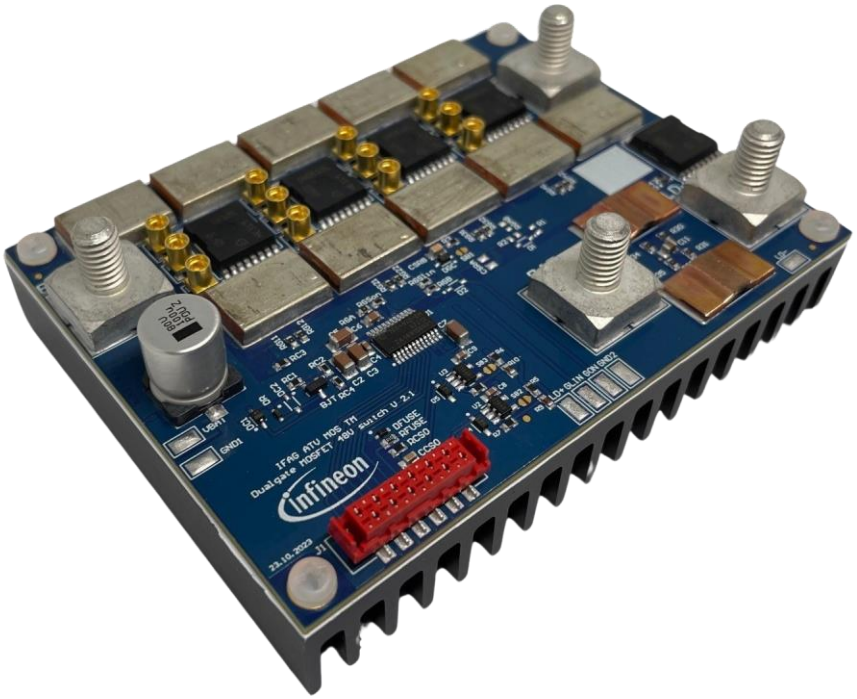

Table of contents

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Table 1 Safety precautions

	**Caution:** *The heatsink and the device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only qualified personnel familiar with the challenges of handling high current circuits should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing, or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

1 Challenges of today's disconnect switches

The structure of modern vehicle's board nets is becoming increasingly complex. This is due to the growing number of loads, the shift from Pb to Li-ion or other battery types, and the need for functional safety measures such as fail operation. As a result of these factors, the use of battery and load disconnect switches has also increased, with MOSFETs being the preferred high load switch of choice. To achieve the desired on-resistance of the main switch for steady-state operation, multiple MOSFETs are often switched in parallel. In many cases, the main switch is bi-directional to halt current in both the charging and discharging directions of the battery.

In Figure 1, a simplified schematic of a battery disconnect switch is shown. The need to stop current in both directions is due to protection measures that are put in place in case of failure events such as overvoltage or overcurrent due to short circuits. This is particularly important for off-board connections, such as the cable harness connecting other control units to the disconnect switch. These cables can have large inductances, which are shown in Figure 1, and must be considered after over-current turn-off. Cable inductances can store considerable amounts of energy, which must either be dissipated by the disconnect switch MOSFETs or other protection circuitry, such as freewheeling circuits.

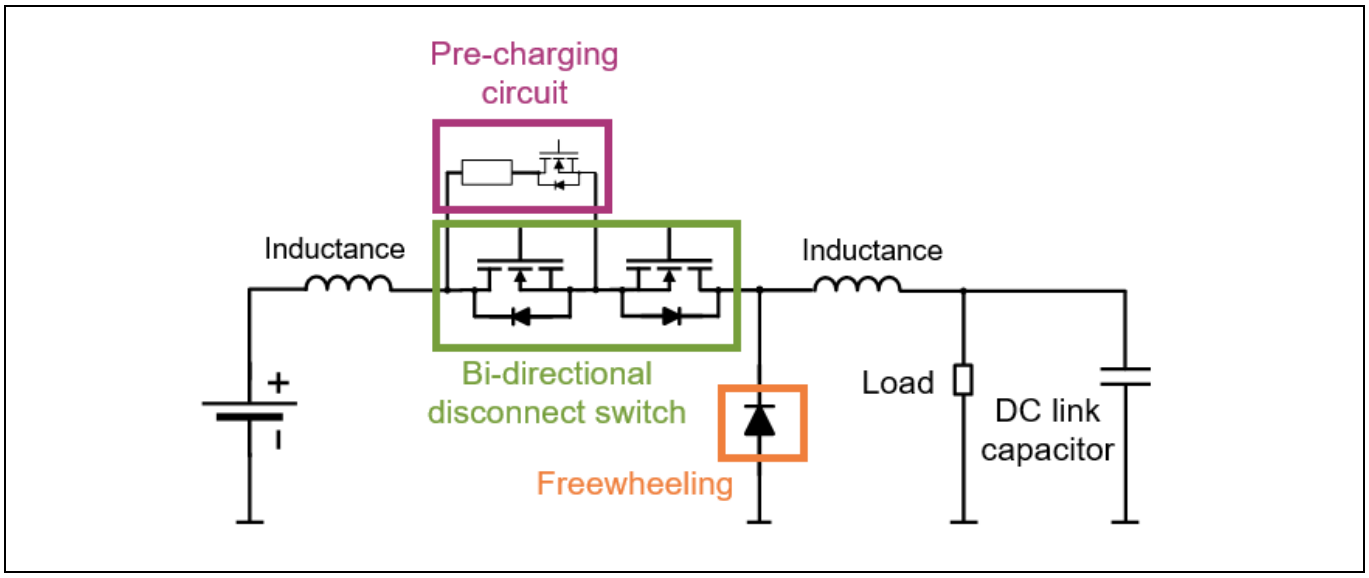


Figure 1 Typical bi-directional battery disconnect switch with freewheeling diode and pre-charging circuit

1.1 Capacitor charging and in-rush current limitation

In disconnect switch applications, it is often necessary to charge high-capacity capacitors that are located near the loads. However, regular MOSFETs are not suitable for limiting the in-rush current into large capacitors due to limitations on their safe operating area (SOA) and transfer characteristics, such as the transconductance.

Controlling in-rush currents in MOSFETs can be quite challenging due to the steep dependency of drain current on gate voltage, which is also known as transconductance. Additionally, the temperature coefficient often imposes restrictions on the safe operating area (SOA). Unfortunately, limiting the current is often not possible due to these factors. There are two areas of operation for MOSFETs, the thermally stable and unstable regions on the transfer characteristic, as shown in Figure 2. Operating in the thermally unstable area can cause severe degradation due to inhomogeneous temperature distribution or even thermal runaway, caused by the high positive temperature coefficient. On the other hand, operating in the thermally stable area with standard RDS(on) optimized MOSFETs poses a significant challenge due to very high currents, leading to high self-heating, even if the temperature distribution on the chip is homogeneous.

Due to the high zero temperature coefficient of RDS(on) optimized MOSFETs, it is nearly impossible to operate them reliably in linear mode, making them unsuitable for many applications.

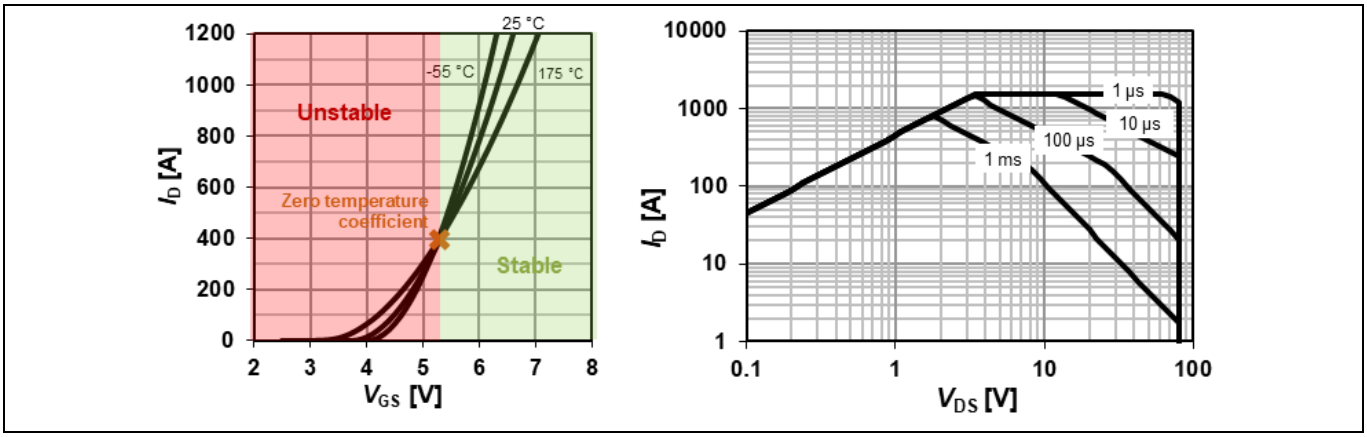


Figure 2 Transfercharacteristics and SOA of a standard OptiMOS™ 5 trench MOSFET

As a consequence, the charging concept is typically implemented using a separate pre-charging path comprising a costly large power resistance to limit the current, together with a small low power MOSFET as illustrated in Figure 1. Alternatively, a DCDC converter with soft-start functionality could be used to charge the DC link capacitance, which may be even more costly.

In Figure 3 below, an exemplary charging waveform with power resistor pre-charging path is shown. In this example, a 33 mF capacitor is charged with a 1 Ω resistor. The curve shape is asymptotically approaching the target capacitor voltage of 48 V. The charging process slows down over time, which is a well-known RC time constant charging behavior. The resistor power reduces quadratically with the current. Thus, individual control of power and self-heating of the resistor is not possible to exploit the maximum charging speed for the capacitor.

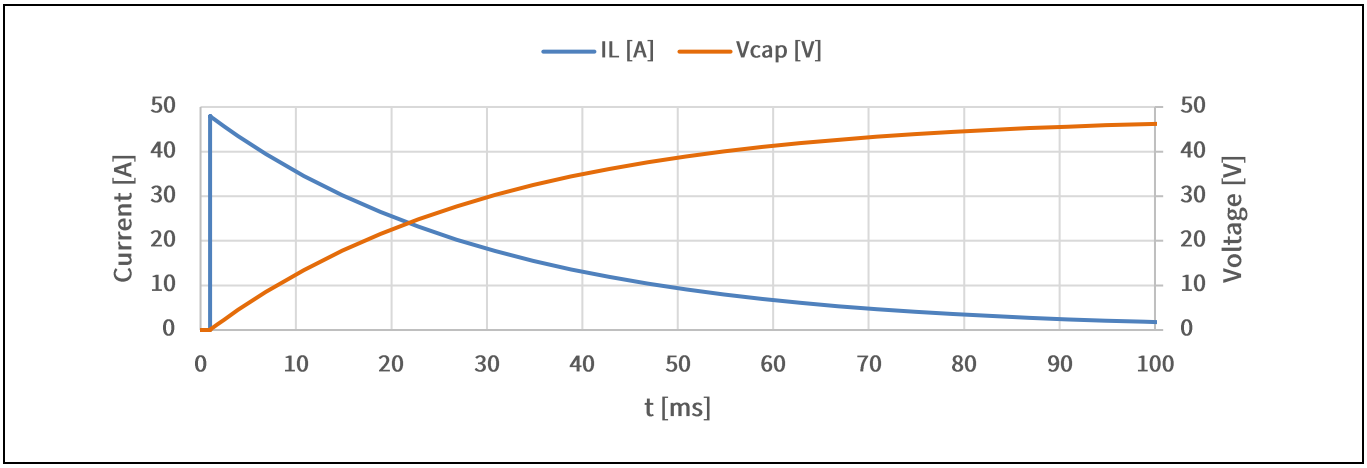


Figure 3 Capacitor charging 0 V → 48 V with pre-charging path (1 Ω, 33 mF)

1.2 Short circuit robustness (avalanche and active voltage clamping)

One of the significant challenges in disconnect switches is ensuring their short circuit robustness. When a short circuit or an overcurrent event is detected, the MOSFETs are turned off to protect the system and the MOSFETs from damage. However, the energy stored in the cable harness inductance still needs to be dissipated. Without

additional countermeasures, this energy dissipation would happen within an avalanche event of the disconnect switch MOSFETs.

In the simplified schematic shown in Figure 4 and the simulation diagram in Figure 5, an avalanche event with short circuit turn-off at 700 A is simulated. To avoid latch-up destruction and over-heating, MOSFETs require a high avalanche current and energy rating. If the current or energy rating of the MOSFETs are exceeded, additional protection measures may be necessary. Thus, it is essential to consider these factors when designing and implementing disconnect switches.

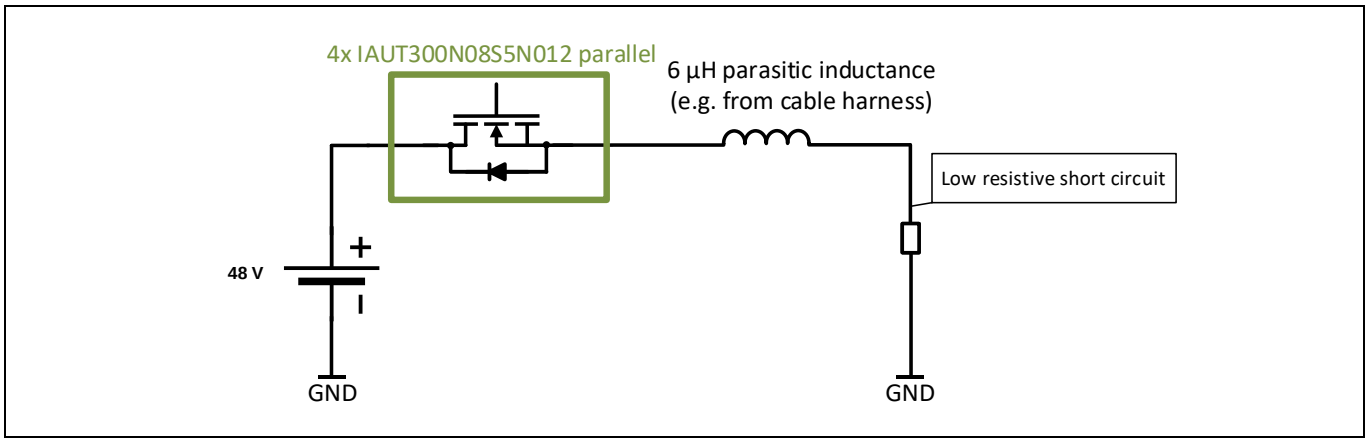


Figure 4 Simplified 48 V disconnect switch short circuit scenario with parasitic inductance

One of the common issues faced in avalanche events is the limited time of exposure due to hot carrier injection over life-time, which causes accelerated degradation of the device. During avalanche, strong electrical fields are generated in the device that accelerate free carriers leading to impact ionization. However some hot carriers might be injected into the field or gate oxide, which leads to parameter drifts and limits the lifetime of the device and in turn limits the time of avalanche exposure and the number of events that can occur.

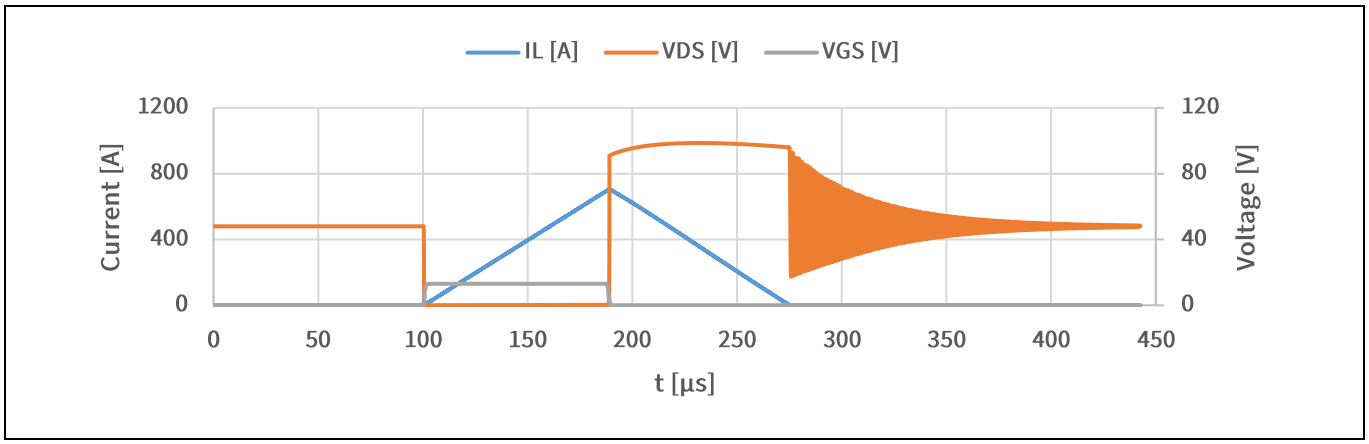


Figure 5 Exemplary avalanche event simulation after short circuit turn-off

To dissipate energy in a different way, active clamping is employed. This involves operating the device in linear mode instead of avalanche mode. This is done by limiting the drain-source voltage below the break-down voltage but higher than the battery voltage. During clamping, a small gate voltage is maintained to keep the gate channel open as necessary to conduct the current and limit the drain-source voltage.

An exemplary simulation of active clamping is shown in Figure 6. However, operating MOSFETs in the thermally unstable region may result in limitations of the SOA and place them in the critical area of thermal instability, as discussed in the previous chapter. Also, paralleling devices with steep transfer characteristics in linear mode is almost impossible due to process variations such as gate threshold tolerances, as one of the parallel devices is likely to take most of the current.

Therefore, it is important to carefully consider the trade-offs between avalanche and active clamping modes of operation, as well as the impact on device lifetime and SOA limitations, when designing disconnect switches.

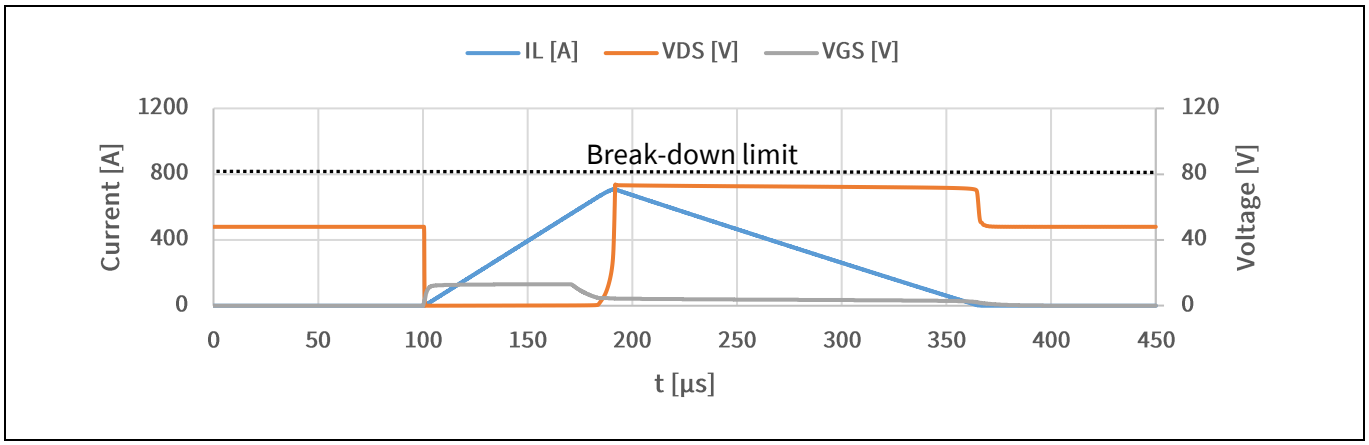


Figure 6 Exemplary active clamping event simulation after short circuit turn-off

2 Introduction of the Dual Gate MOSFET

The IAUTN08S5N012L Dual Gate MOSFET is designed to offer an optimized capacitor charging and short-circuit concept. This innovative approach leads to cost savings by eliminating the need for a separate pre-charging path. Moreover, this design enhances the short-circuit robustness of the system, making it an ideal choice for demanding applications where reliable and efficient performance is critical. To get a quick overview of the product features, please refer to Table 2.

Table 2

Product	Technology	V_{DS} [V]	Max. $R_{DS(on)}$ [mΩ]	Package	Gate channel
IAUTN08S5N012L	OptiMOS™ 5	80 V	1.15	TOLL (PG-HSOF-8-2)	Normal level

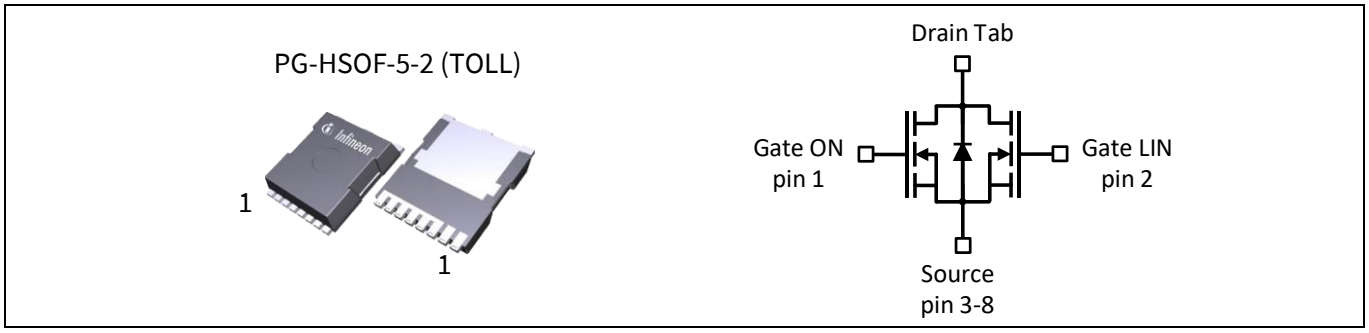


Figure 7 Dual Gate MOSFET TOLL package and equivalent circuit symbol

2.1 Two MOSFETs in one package – the Dual Gate approach

The Dual Gate MOSFET comprises two interleaved transistors on the same silicon chip, with a common drain and source, but separate gates that are individually accessible through dedicated pins. One gate represents the ONFET, which delivers a low $R_{DS(on)}$ for steady-state operation, while the other gate represents the LINFET, which offers excellent SOA and linear operation performance, making it suitable for charging capacitors controlling in-rush current and active clamping after short-circuit turn-off.

Sharing a chip means that both MOSFETs benefit by utilizing the silicon cooling area or thermal capacitance of each other. When both MOSFETs are turned on, the increase of $R_{DS(on)}$ is negligibly small compared to a standard single-gate MOSFET of the same technology. In the following chapters, we will explain the advantages of the Dual Gate MOSFET in more detail and how it can offer improved performance in various applications.

2.2 LINFET enhanced SOA and transconductance

The LINFET transistor has been specially engineered to achieve a significantly enhanced SOA, which is comparable to that of a planar MOSFET, and far superior to that of a standard trench MOSFET. This has been made possible by implementing two key design features. Firstly, the zero-temperature coefficient of the transfer characteristics has been reduced, which effectively reduces the area of thermal instability and minimizes the positive temperature coefficient. Secondly, the LINFET and ONFET share a single chip, which allows the LINFET to take advantage of the larger chip area of the ONFET. This design optimization ensures that the LINFET operates more reliable. In fact, the LINFET transistor exhibits superior performance compared to a standard trench MOSFET regarding the capability to operate in linear mode. A graphical representation of the improvement in the SOA of the LINFET transistor can be observed in Figure 8. For instance, when subjected to high drain-source voltages and 1 ms pulse timing, the SOA current is increased by a factor of 8 when compared to the ONFET (representative for a standard MOSFET of the same technology and chip size).

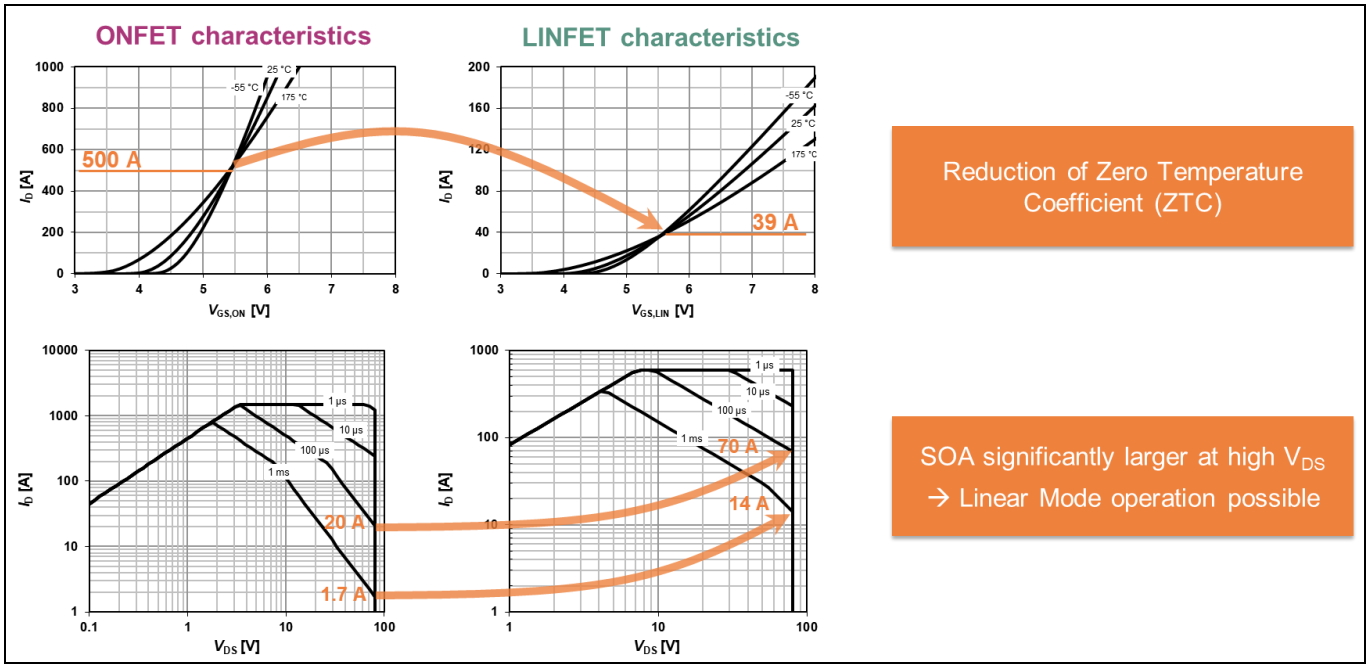


Figure 8 Comparison of LINFET and ONFET performance - zero temperature coefficient and SOA

The low transconductance (g_m), which characterizes the change in drain current with respect to gate voltage ($dI_D/dV_{GS,LIN}$), is the second key advantage of the LINFET transistor. This results in two benefits: Firstly, it allows for more precise control of current based on the tolerances of an externally applied gate voltage. Secondly, it minimizes the impact of gate threshold voltage $V_{GS(th)}$ variation on the current. In addition, when multiple MOSFETs in parallel are controlled at the same gate voltage, the LINFET transistor improves current sharing in linear mode. In Figure 9 below, a comparison between the ONFET (representative of a standard MOSFET) and LINFET (with reduced transconductance) is shown. To simplify, the transconductance process variation is neglected and only the minimum and maximum gate threshold variation is considered to analyze the variation in drain current. When we take 60 A as a reference typical current to compare the minimum and maximum currents, we see a large current range of 5 A to 190 A for the ONFET and a small range of 40 A to 80 A for the LINFET. This clearly demonstrates the advantage of low transconductance.

The improved SOA of the LINFET transistor opens up new target applications such as short circuit clamping or capacitor charging. The low transconductance helps to accurately control the in-rush current and enables current sharing of multiple parallel MOSFETs in linear mode.

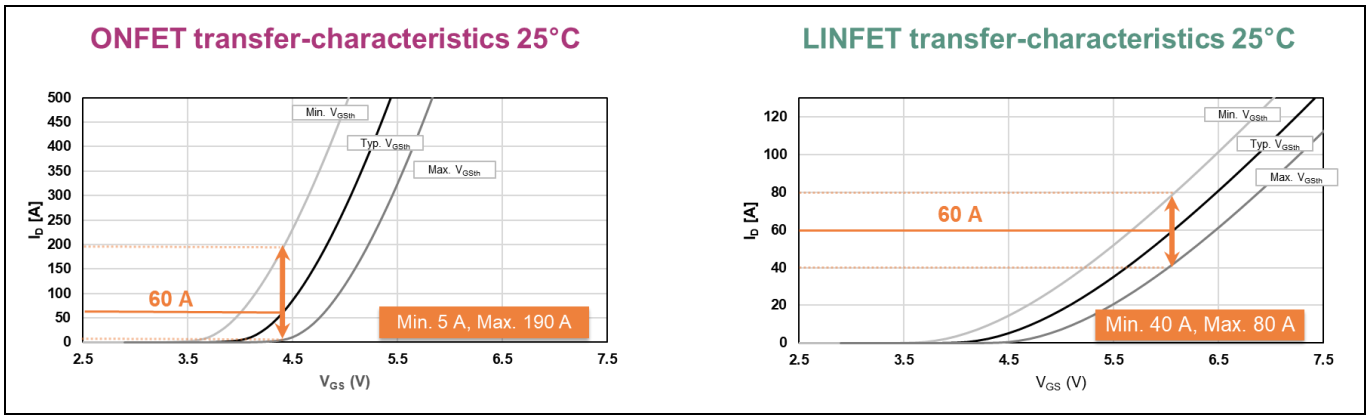


Figure 9 Comparison of ONFET and LINFET performance – transconductance and current tolerance

3 How to solve challenges in disconnect switch applications using a Dual Gate MOSFET

The following chapters will highlight the advantages and usage of the Dual Gate MOSFET in disconnect switch applications. These benefits and applications will be demonstrated using a reference design that supports pulsed capacitor charging and short circuit clamping.

3.1 Capacitor charging

The LINFET of the Dual Gate MOSFET, with its improved SOA and low transconductance, is an excellent candidate for in-rush current limitation for capacitor charging. The following chapters will delve into greater detail about how to use the LINFET for in-rush current limitation.

3.1.1 Fixed gate voltage to limit the current

One simple way to limit in-rush current for the LINFET is to adjust the gate voltage. The targeted current limit can be determined based on the transfer- and output characteristics of the device. However, this approach still leaves room for variation due to process variations and other product characteristics. Therefore, it is important to evaluate and consider these factors to find a good compromise between charging speed and self-heating.

To minimize these efforts, the minimum and maximum current limit precision is specified in the datasheet at various conditions of gate voltage (5.6 V, 6.2 V) and drain-source voltage (6 V, 48 V) conditions.

It is recommended to operate at a gate voltage of 5.6 V for two reasons. Firstly, 5.6 V is very close to the zero-temperature coefficient of the device, which means the current is almost independent of temperature. Secondly, Zener diodes can be used to limit the gate voltage. 5.6 V Zener diodes have a very small temperature coefficient, making them well-suited for this purpose. A simplified circuit with a Zener diode D_{GC} is shown in Figure 10. Note that a series resistance is needed to limit the power dissipation of the Zener diode.

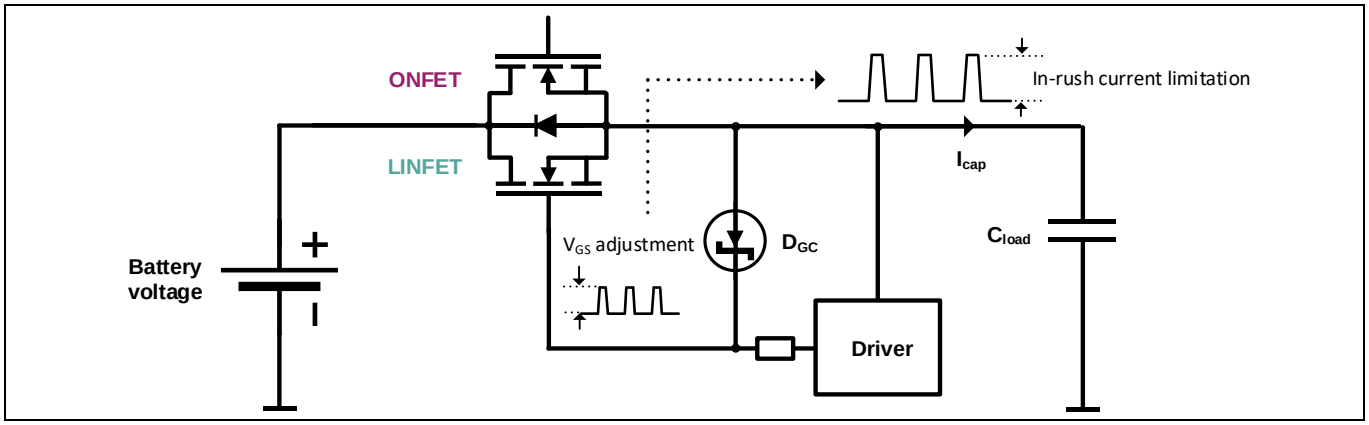


Figure 10 Gate voltage limitation with zener diode to limit in-rush current

To control current with simplicity and accuracy while minimizing the effect of temperature, 5.6 V Zener diodes can be used to limit the gate voltage. However, a high-side driver with higher output voltage than 5.6 V is needed to ensure that the Zener diode can really limit the voltage.

Variations in current resulting from the Zener diode voltage tolerance can be determined based on the LINFET transconductance listed in the datasheet. The transconductance, dI_D / $dV_{GS,LIN}$, is around 50 S (or A/V) at gate voltage 5.6 V. A Zener diode voltage variation of ± 110 mV (2% accuracy, as for example BZT52-B5V6S-AU at I_Z = 5

mA) would result in an additional current variation of around ± 5.5 A, in addition to the current limit precision tolerances listed in the datasheet.

3.1.2 Feedback loop to limit the current

There is another method for accurately limiting current that involves using a feedback loop with operational amplifiers. This approach is more complex and requires additional components, but it offers more precise current control. The process involves current sensing with a shunt and using appropriate reference voltages to adjust the target current. Figure 11 shows a simplified circuit diagram of this approach.
To implement this method, a current sense amplifier (CSA) is required to process and amplify the shunt resistor voltage as accurately as possible. Operational amplifier (OPA) then compares the amplified shunt current sense signal to a voltage reference V_{REF} that represents the targeted current limit. As long as the current is lower than the targeted current, OPA will amplify the voltage difference of amplified current sense signal and voltage reference to drive the LINFET gate. As the current increases close to the target value, the input voltage difference of OPA decreases close to 0 V. Therefore OPA should be able to process really low input voltage differences accurately to avoid unwanted ringing or disturbance of the pulsed output current.

It's important to note that when paralleling Dual Gate MOSFETs to achieve higher current and using the same gate voltage for multiple devices in parallel, current sharing is not equal due to process variations. This could be avoided using only one device for capacitor charging or using a feedback loop and current sense for each device in parallel. This approach requires significantly more effort and adds cost to implement.

However, many systems require at least one shunt resistor for current sensing and a high-side driver with integrated current sense amplifier to get an amplified current signal. In this case, just one operational amplifier might be needed in addition. As this method is more complex and not necessarily beneficial when paralleling, an alternative simple and low cost approach is to use zener diodes to limit the gate voltage and the current as described in chapter 3.1.1.

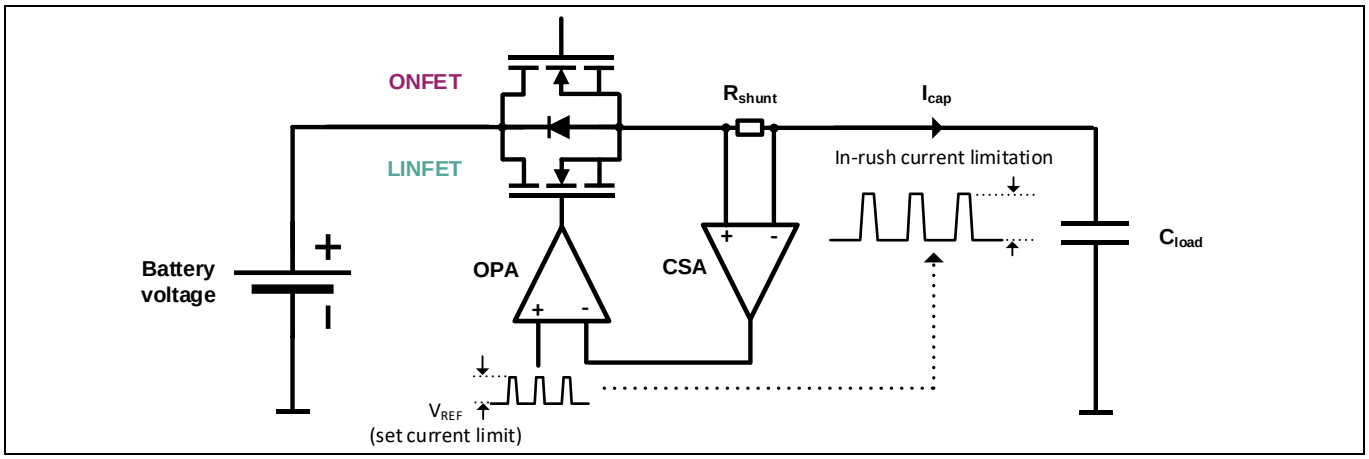


Figure 11 LINFET driven with operational amplifiers to limit the current based on V_{REF}

3.1.3 Advantages of capacitor charging with Dual Gate MOSFET

Using a Dual Gate MOSFET for capacitor charging reduces cost and saves board space as there is no requirement for a separate pre-charging circuit, which can often require high power SMD resistors that consume a lot of PCB area. However, using a MOSFET operating in linear mode can increase the charging speed significantly compared to usage of a power resistor. One key difference when using a MOSFET instead of a power resistor to limit current is the pulsed nominal charging current that can be maintained throughout the charging waveform.

Meanwhile, using a power resistor results in an asymptotic waveform, where the waveform is determined by the RC time constant of the power resistor and the charged capacitance. As a result, the charging speed using a power resistance is very slow towards the end, as the current reduces over time. The power of the resistor decreases quadratically with the current, means in the end of the charging process the power is very low. In contrast, with a MOSFET, the pulse current stays constant and only the drain-source voltage reduces as the charging progresses. The power reduces, but not quadratically with current as for the power resistor solution. However, the reduced amount of power could be easily compensated by increasing the pulse length towards the end of the charging pattern to exploit the allowed self-heating per pulse. In other words, a pulse width modulation scheme with MOSFETs offers more flexibility and can accelerate the charging even further.

The waveforms of both methods are compared in Figure 12, where V_R represents the voltage across the power resistance and V_{DS} represents the voltage across the Dual Gate MOSFET. V_{CAP} shows the voltage of the DC link capacitor, which is representative of the charging state.

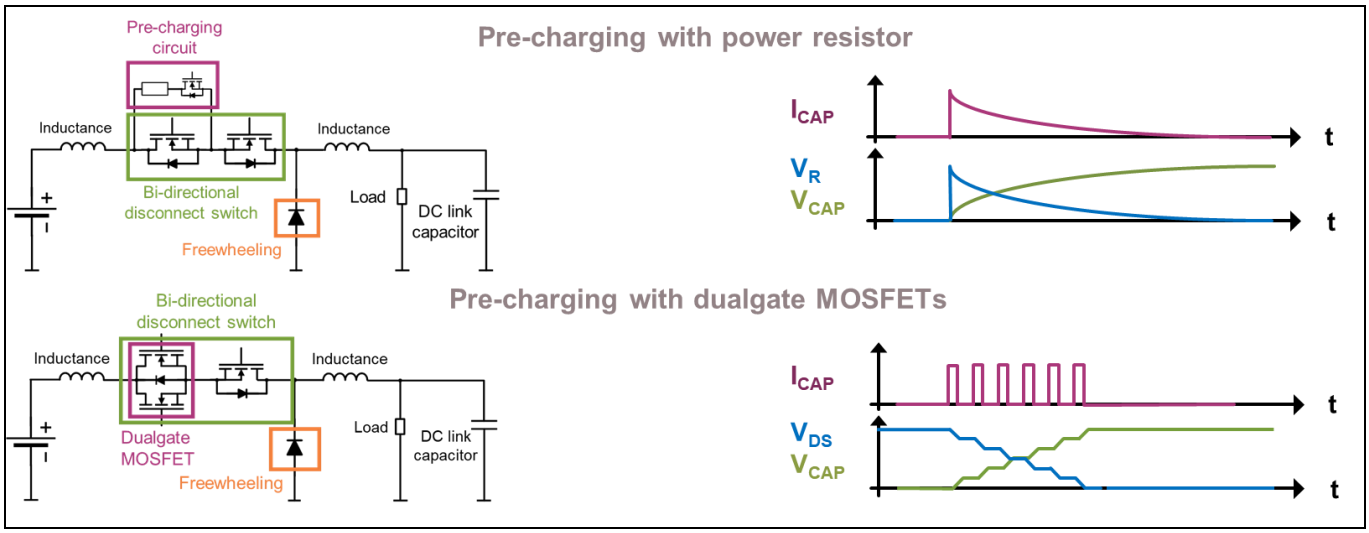


Figure 12 Simplified comparison of pre-charging with power resistance and Dual Gate MOSFETs

3.1.4 Pulsing to control self-heating

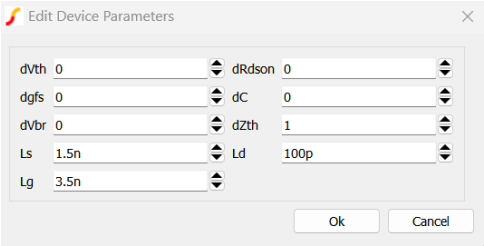
Another crucial aspect to be considered is self-heating. In most cases, the capacitors are too large, and merely switching on the LINFET with limited gate voltage isn't enough to control self-heating in an appropriate manner. Furthermore, since the device will experience a capacitor charging event during every car start-up, lifetime degradation is also an important factor to explore. The self-heating is dependent on following three factors: Z_{thja}, device current I_D and drain-source voltage V_{DS}. To limit self-heating and degradation over the device's lifetime, we recommend considering the following guidelines:

- Operation close or higher than the zero temperature coefficient ($V_{GS,LIN}$ > 5 V) to avoid operation in the unstable temperature region.
- Junction temperature rise ΔT_j < 60 °C per charging pulse

- Junction temperature T_j < 175°C

To estimate self-heating during pulsed capacitor charging, spice simulation can be used. In below Figure 13 and Figure 14 an exemplary simplified simulation with one Dual Gate MOSFET is shown. In the following example simulations a zener diode with 5.6 V break-down voltage and 4.7 kΩ series resistance is used to limit the gate voltage and the current.

Spice model parameter setting (valid for all subsequent simulations):



Simulation conditions:

- Ta = 85°C, VBAT = 48 V
- C1 = 5 mF (load capacitor)
- Pulse width (fixed): 100 µs
- Period: 1 ms
- Cycle number: 70

Typical charging time is around 60 ms with a temperature rise per pulse below 60°C and staying below 175°C junction temperature (Tj).

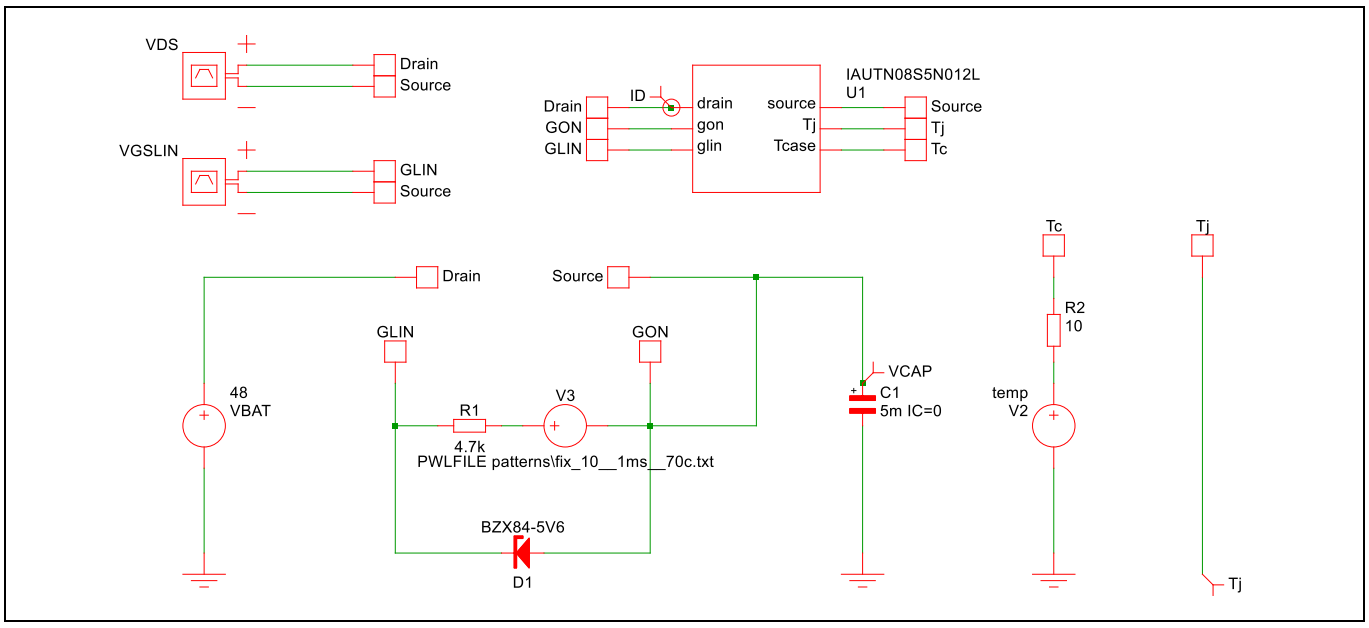


Figure 13 Simulation schematic charging 5 mF with Dual Gate MOSFET to 48 V (fixed pulse width)

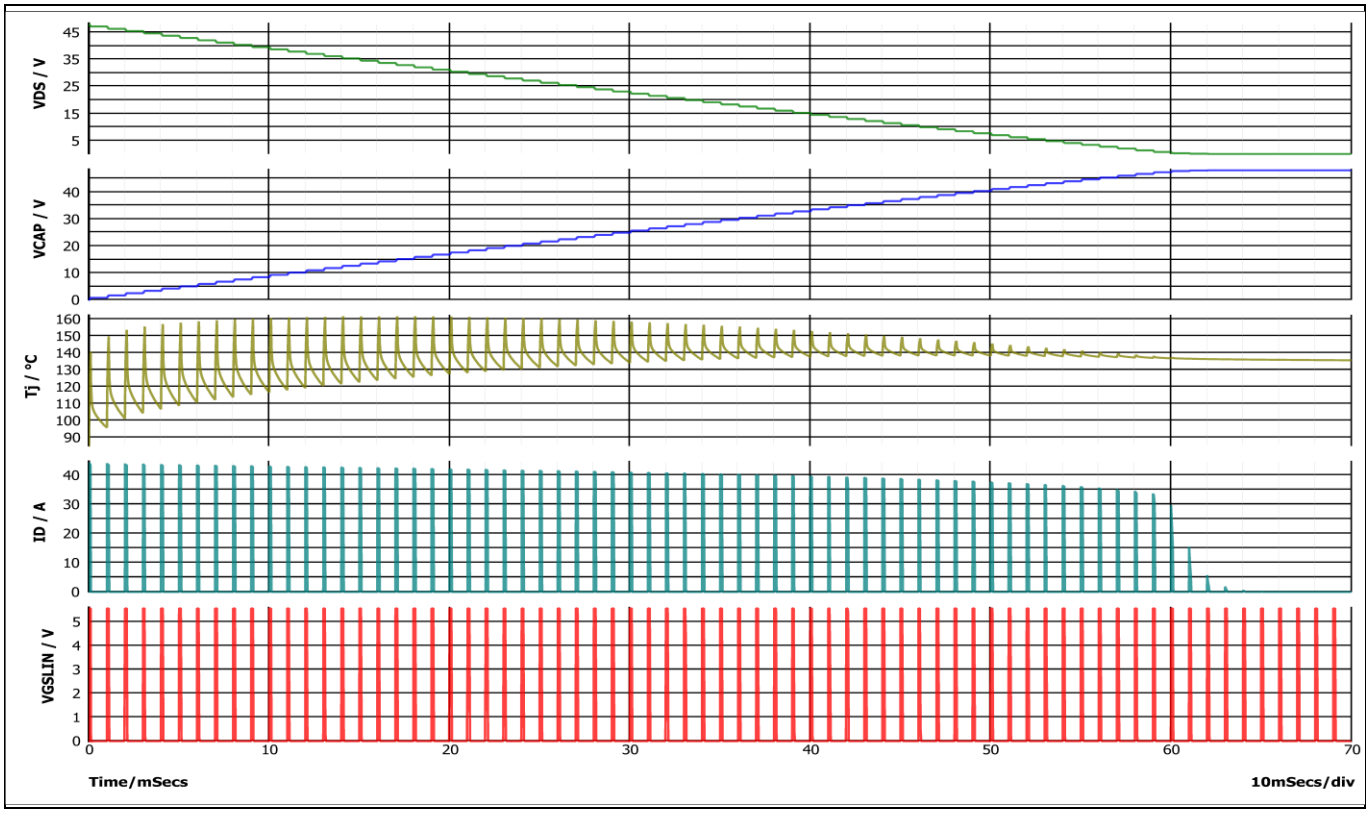


Figure 14 Simulation graph charging 5 mF with Dual Gate MOSFET to 48 V (fixed pulse width)

3.1.5 Capacitor charging with pulse width modulation

As we have discussed in the previous chapter, the drain-source voltage, and consequently, the power dissipation during capacitor charging, decreases as the capacitor voltage increases. This phenomenon provides an opportunity to increase the pulse width during the charging process, enabling us to maximize the allowed temperature increase per cycle and minimize the overall charging time. To achieve this increased pulse width, various modulation schemes such as linear, parabolic, or other functions that are dependent on charging time, power, or drain-source voltage can be employed. A charging pattern dependent on time is pre-defined and applied to achieve this modulation over time. Below, you will find two examples with time dependent functions for the duty cycle that illustrate modulation over time with fixed charging patterns.

Example conditions:

n = 25 (number of pulses)
T = 2 ms (period)
D_{start} = 10% (start duty cycle)
D_{end} = 80% (end duty cycle)

Example 1 - Linear increase of pulse width based on duty cycle function D(t):

$$D(t) = \frac{D_{end} - D_{start}}{T \cdot n} t + D_{start}$$

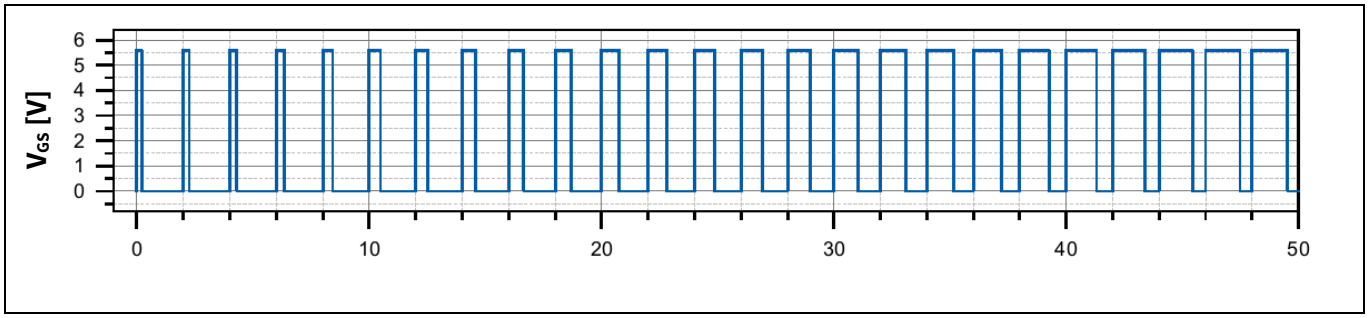


Figure 15 Linear increase of pulse width

Example 2 - Parabolic increase of pulse width based on duty cycle function D(t):

$$D(t) = \frac{D_{end} - D_{start}}{(T \cdot n)^2} t^2 + D_{start}$$

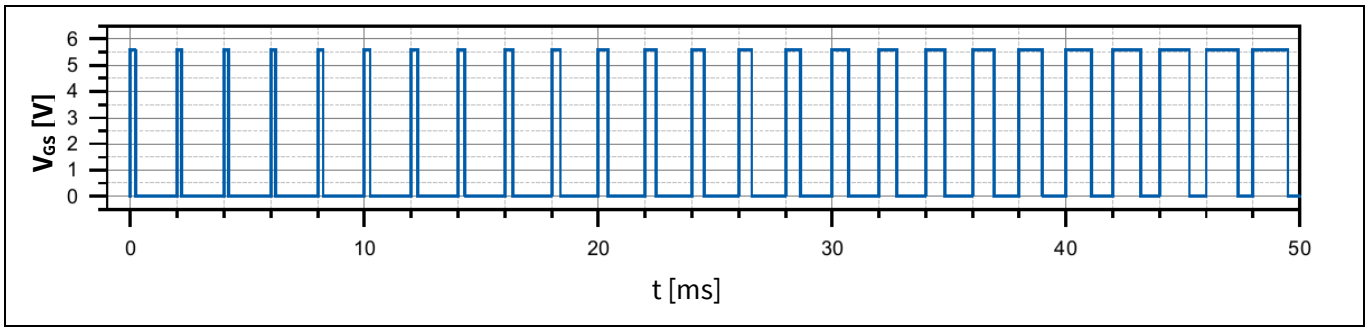


Figure 16 Parabolic increase of pulse width

In theory, the best way to limit self-heating is by controlling the duty cycle based on the thermal impedance of the device (Z_{thjc}) or system (Z_{thja}). However, this approach requires the microcontroller to handle a lot of processing steps in a short time and accurate sensing of the MOSFET's power, which depends on drain current and drain-source voltage.

Considering now the recommendations for self-heating mentioned in chapter 3.1.4 and applying a suitable pulse width modulation pattern to accelerate charging as much as possible, find below a simulation example (refer to Figure 17 and Figure 18).

Simulation conditions:

- Ta = 85°C, VBAT = 48 V
- C1 = 5 mF (load capacitor)
- Parabolic modulation of pulse width
- Pulse width (start): 100 µs
- Pulse width (stop): 600 µs
- Period: 1 ms
- Cycle number: 70

Typical charging time is around 40 ms with a temperature rise per pulse below 60°C and staying below 175°C junction temperature (Tj). This accelerates the charging by 20 ms compared to a fixed duty cycle.

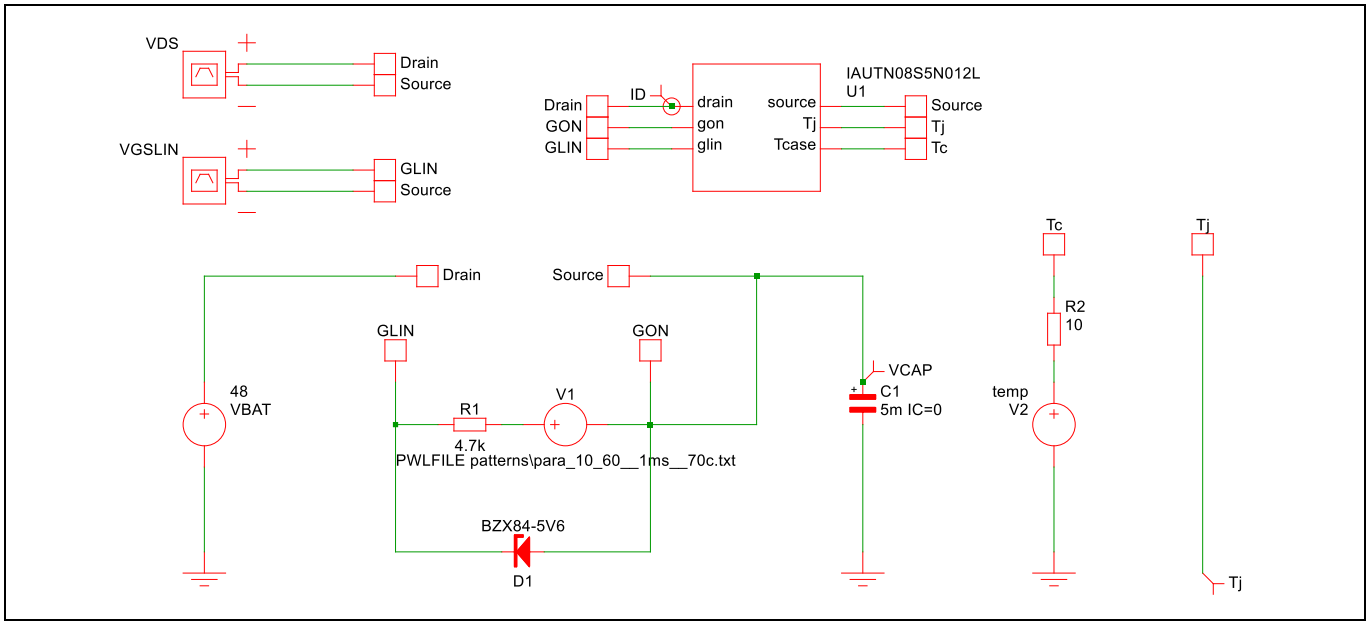


Figure 17 **Simulation schematic charging 5 mF with Dual Gate MOSFET to 48 V (parabolic modulation of pulse width)**

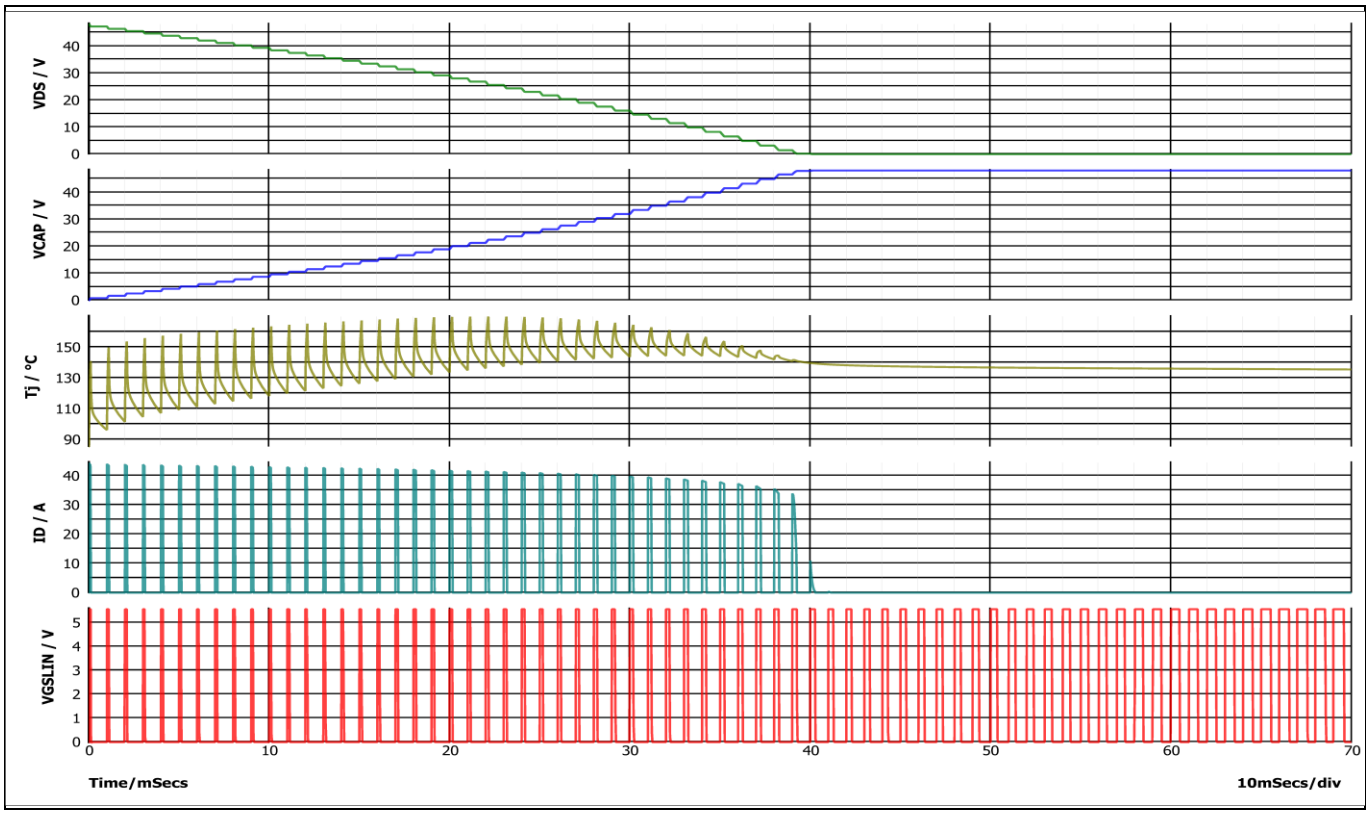


Figure 18 **Simulation graph charging 5 mF with Dual Gate MOSFET to 48 V (parabolic modulation of pulse width)**

3.1.6 Slow-switching to minimize board-net inductance coupling

In most disconnect switch applications, it's typical to have board-net inductances that result from the cable harness. As discussed earlier, these inductances can be particularly significant during short circuits, but they also affect capacitor charging.

During each current pulse of capacitor charging, there's a high current rise and fall dI_D/dt that induces a voltage at the inductances. The acceptable range of dI_D/dt and voltage coupling depends on the system requirements. Undervoltage could cause shut down of IC components connected to the affected node. Similarly, overvoltage could lead to electrical overstress of components.

Therefore, it's highly recommended to limit the dI_D/dt to an acceptable range. To effectively achieve this goal, one can leverage RC components to slow down both the gate voltage and drain current. This approach is proven to be the simplest and most effective. An exemplary simulation is shown in Figure 19, Figure 20 and Figure 21.

Simulation conditions:

- Ta = 85°C, VBAT = 48 V
- C1 = 5 mF (load capacitor)
- Parabolic modulation of pulse width
- Pulse width (start): 100 µs, Pulse width (stop): 600 µs
- Period: 1 ms
- Cycle number: 70
- Parasitic inductance L1 of 1 µH (representing e.g. cable harness inductance)
- Slow switching capacitor C2 of 22 nF to slow down the slope of gate voltage

It was once simulated without slow switching capacitor (dashed line) and once with slow switching capacitor (straight line) in the graph shown in Figure 20 and Figure 21.

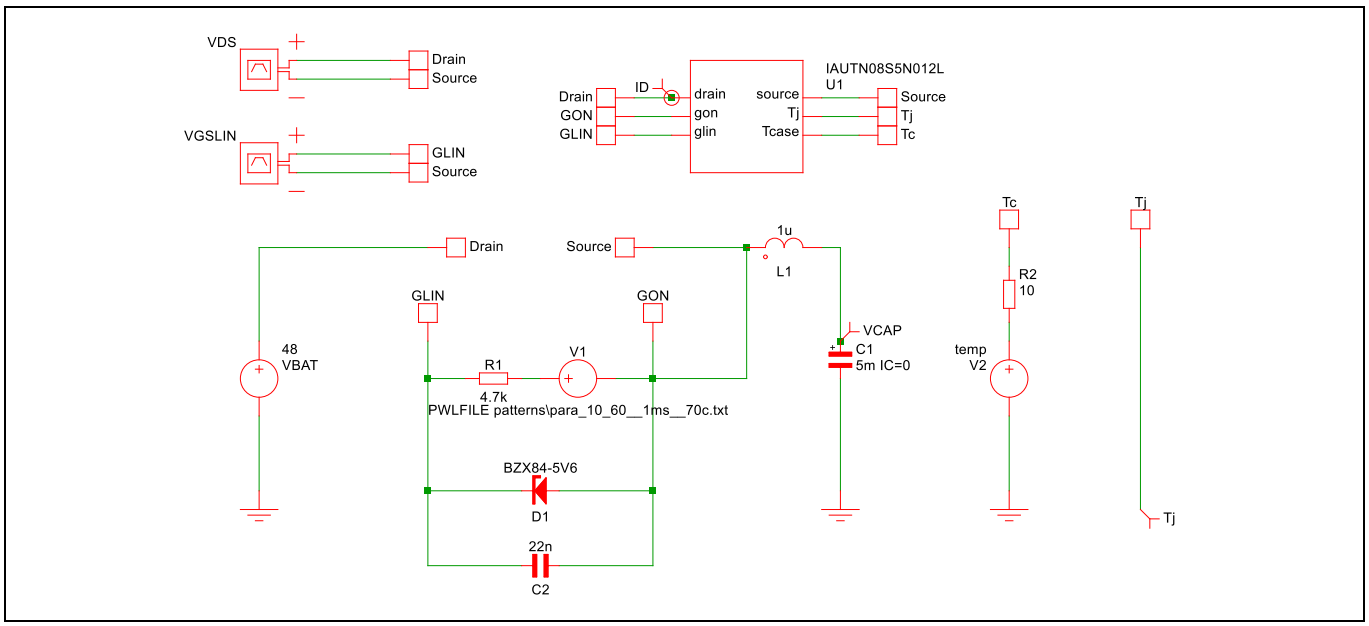


Figure 19 Simulation schematic charging 5 mF with Dual Gate MOSFET to 48 V (parabolic modulation of pulse width) including inductive coupling effects

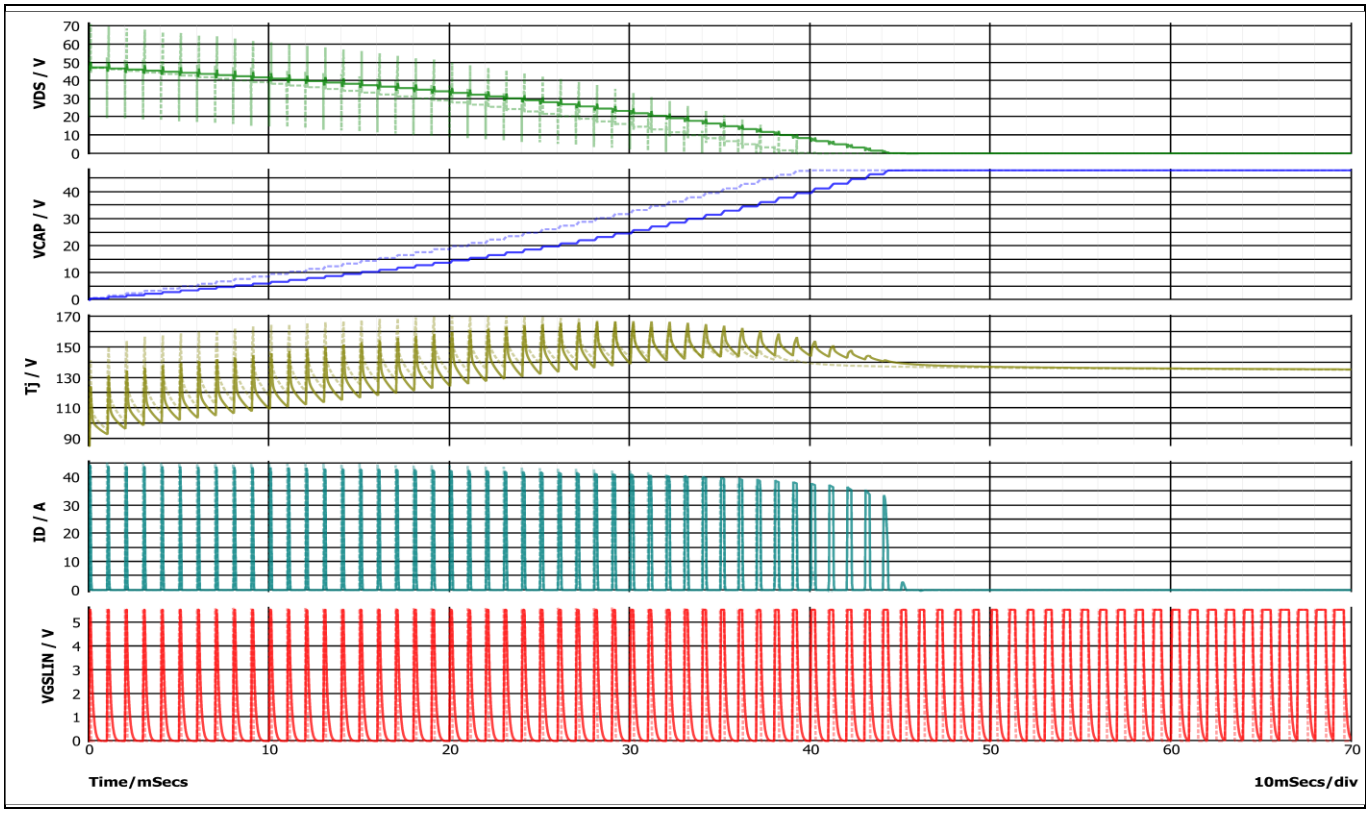


Figure 20 **Simulation graph charging 5 mF with Dual Gate MOSFET to 48 V (parabolic modulation of pulse width) with inductance 1 µH. Dashed line without capacitor C2.**

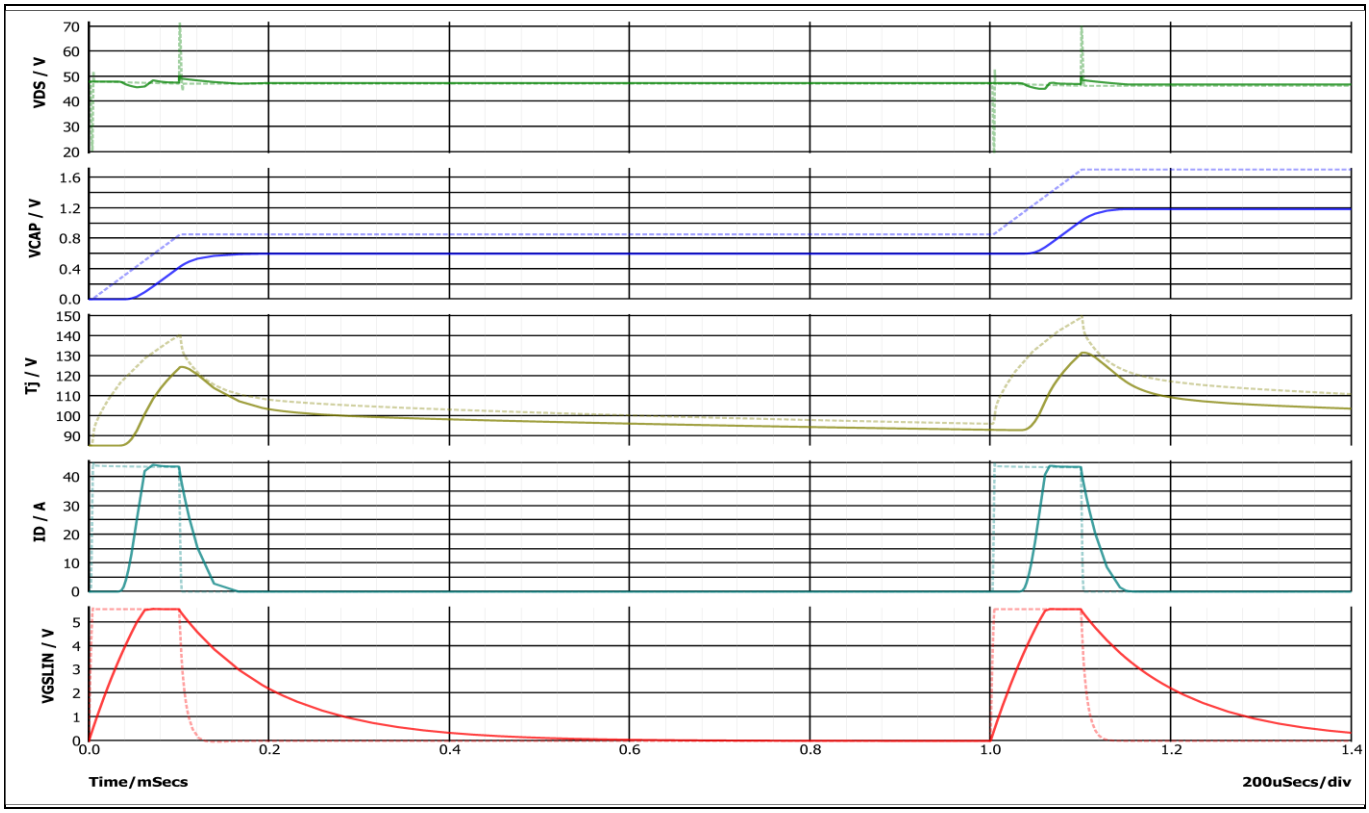


Figure 21 **Simulation graph (zoomed) charging 5 mF with Dual Gate MOSFET to 48 V (parabolic modulation of pulse width) with inductance 1 µH. Dashed line without capacitor C2.**

3.1.7 Short circuit detection using the LINFET

The current pulses of capacitor charging can also serve as a short-circuit detection test during the system's startup. If the sensed capacitor voltage fails to rise as expected, it typically indicates a short-circuit or overload condition at the disconnect switch output. To carry out this test, the voltage output, which is expected to be the capacitance voltage, must be sensed and measured on the disconnect switch board (e.g. with an ADC). Upon observing an insufficient rise in the sensed voltage, the charging procedure can be halted. The advantage of this approach is that the LINFET can limit the pulsed current to a reasonably low level, thereby facilitating the control of self-heating during short circuits.

3.2 Short circuit clamping (avoidance of avalanche operation)

Another advantage of the product is its capability to be robust with short circuit clamping. In this way, avalanche can be avoided minimizing the impact of hot carrier injection degradation and being able to limit the drain-source voltage. Within the framework of this application two structures will be shown. We will begin by presenting a straightforward setup consisting of a zener diode connected directly to the gate. Following that, we will delve into a more intricate solution featuring a bipolar transistor circuit combined with a zener diode configuration. For the purpose of the upcoming descriptions, we will assume that the ONFET is in the off state.

3.2.1 Simple structure with zener diode directly to gate

Figure 22 shows a simple solution for a short circuit clamping circuit with a LINFET. During short circuit turn-off, the parasitic inductance leads to a drain-source overvoltage, which can lead to MOSFET avalanche and can damage the system. To prevent this, a specific level of overvoltage is set. When the overvoltage reaches this level, the LINFET is turned on with a suitable amount of gate voltage to conduct the inductor current. The current, and therefore the drain-source clamp or overvoltage level, is variable as it also depends on the gate voltage $V_{GS,LIN}$.

$$V_{DS,clamp} = V_{R2} + V_{DC} + V_{DR} + V_{GS,LIN} \approx V_{DC} + V_{GS,LIN}$$

When selecting the Zener diode voltage level, it's important to choose a value that keeps the $V_{DS,clamp}$ below the breakdown voltage of the Dual Gate MOSFET. This way, the MOSFET's integrity will be maintained and the circuit will function correctly.

Resistor R_2 serves to limit the current through the zener diode. However, it should be chosen to be small enough so as not to limit the clamp speed.

On the other hand, R1 serves as a pull-down resistor, playing a crucial role in defining the bias current of the zener diode during clamping operations. Additionally, it is responsible for discharging the gate when the drain current decreases, which subsequently leads to a decrease in the gate voltage. To ensure proper operation, it is recommended to select the pull-down resistance such that it achieves a bias current exceeding 1 mA.

Diode D_R functions as a reverse polarity protection diode. Its purpose is to prevent current from flowing from the gate to the battery during a reverse polarity condition.

In summary, this method is relatively simple and requires fewer components. However, it's less accurate in terms of V_{DS} limitation due to the impact of the MOSFET gate-source voltage, which can be significant especially when high short circuit current need to be clamped.

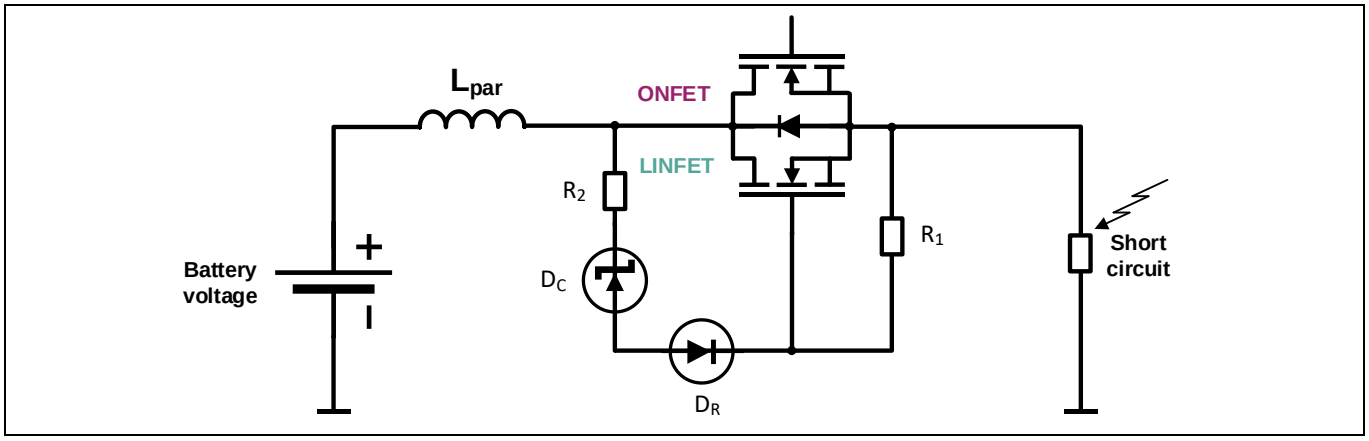


Figure 22 Simple short circuit clamping structure with Zenering directly to the gate

3.2.2 Enhanced structure with BJT and zener diode

The enhanced short circuit clamping structure is slightly more complex and requires more components. However, it offers a much higher degree of accuracy when it comes to limiting the drain-source voltage. One of the key advantages of this structure is that the Zener diode is connected directly to source of the Dual Gate MOSFET, rather than the gate of the LINFET. This is achieved by additionally using a bipolar transistor (BJT) to pull up the gate voltage during clamping. The value of the drain-source voltage clamp can be calculated:

$$V_{DS,clamp} = V_{R2} + V_{R3} + V_{DC} \approx V_{BE,BJT} + V_{DC} + \frac{V_{BE,BJT}}{R_2} \cdot R_3$$

Also with this circuit $V_{DS,clamp}$ should stay below the breakdown voltage of the Dual Gate MOSFET. This way, the MOSFET's integrity will be maintained and the circuit will function correctly.

Also in this circuit diode D_R functions as a reverse polarity protection diode. Its purpose is to prevent current from flowing from the gate to the battery during a reverse polarity condition.

The current flowing through R_3 and the zener diode is determined by R_2 and the base-emitter voltage V_{BE} of the bipolar junction transistor (BJT). To prevent avalanche noise and ensure stable operation, it is essential to match this current to the specific zener diode type. A recommended current of 1 mA is suitable in this case, although this value also results in a voltage drop that contributes to the drain-source clamp voltage.

The capacitor C_C plays a crucial role in limiting the drain-source voltage ramp-up rate (dV_{DS}/dt). This allows the zener diode sufficient time to respond and constraining the drain-source voltage overshoot to remain below the breakdown voltage. However, C_C should not be excessively large, as this could lead to a slow reaction time, increased energy during clamping, and compromised circuit stability. The voltage slope is determined by the capacitor value C_C and the current through R_3.

The optional resistor R_4 defines the node potential between the base-collector diode of the Bipolar Junction Transistor (BJT) and diode D_R. Since these diodes are configured in opposing directions, noise can potentially disrupt the operation of the BJT circuit.

To achieve a rapid reaction speed, the BJT used in the short-circuit clamping circuit should possess a high bandwidth. Furthermore, the resistors, zener diode, and capacitor can be fine-tuned to optimize transient performance. Nevertheless, it is vital to strike a balance between stability and reaction speed when making these adjustments to ensure optimal circuit operation.

The use of low-noise avalanche zener diodes facilitates the selection of lower bias currents, which in turn minimizes the effect of the R3 voltage drop on the drain-source clamp voltage and consequently reduces the response time of the circuit.

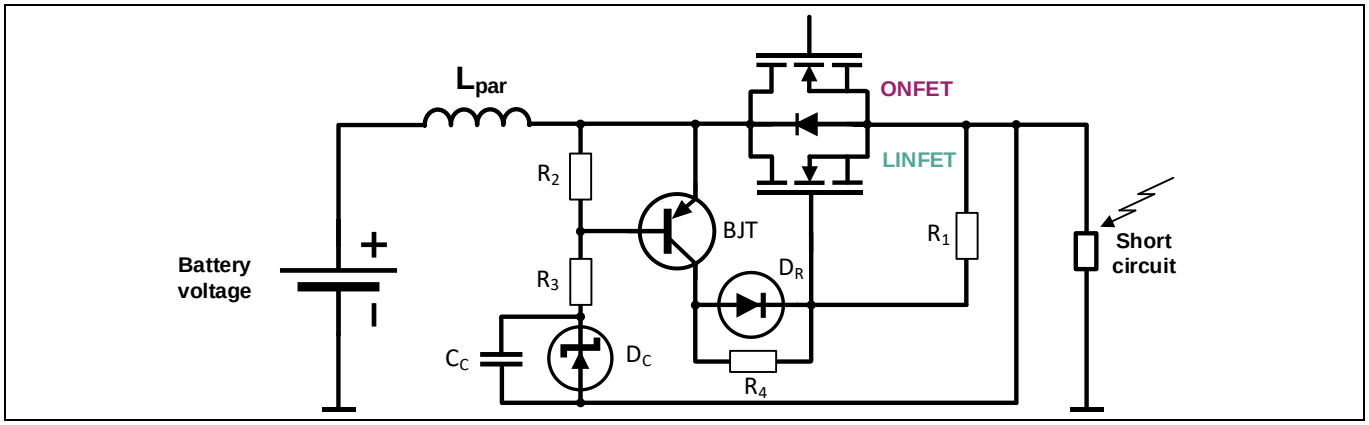


Figure 23 Enhanced clamping structure with BJT and Zener diode referring to MOSFET Source

3.2.3 Appropriate choice of zener diodes for voltage limitation (clamping)

Ensuring a high and reliable reaction speed of voltage limitation by zener diodes requires careful consideration of the appropriate types. These diodes exhibit two different kinds of break-down voltage behaviors: zener break-down and avalanche break-down. Generally, zener break-down dominates in low voltage zener diodes, usually below 6 V, while avalanche break-down is more common in zener diodes above 6 V.

To initiate an avalanche breakdown, two conditions must be met. The first is the presence of an adequate reverse voltage that generates the electric field strength required, while the second is the availability of free electrons that result from leakage current. The probability of an avalanche after an overvoltage event depends on how quickly impact ionization and breakdown occur. This probability can be significantly increased by selecting diodes with high leakage current and applying a high enough bias current during voltage limitation.

Using diodes with low leakage and low avalanche probability can cause voltage clamping malfunction that leads to toggling between overvoltage higher than the zener diode break-down voltage and break-down, usually resulting in an avalanche. This phenomenon is often referred to as avalanche noise and can cause delayed or even missing responses of the clamping circuit if the avalanche is not triggered.

To prevent such scenarios, it is highly recommended to modify clamping circuits, including resistors and BJTs or other components, to match the type of Zener diode used. Thus, you can ensure a high and dependable reaction speed of voltage limitation by zener diodes.

3.2.4 Replacement of TVS diodes for overvoltage clamping

Inductive energy dissipation using TVS protection diodes can be a challenge due to their dependency on breakdown voltage, which is influenced by process variation, temperature, and current. Consequently, there is a wide range of clamped voltage that can be produced to protect other circuitry from overvoltage. However, by utilizing the LINFET component of the Dual Gate MOSFET for voltage clamping, the TVS diode can be replaced, resulting in a significant improvement in voltage limitation accuracy. In this case, the ONFET Gate is not required and is thus shorted to Source. In the past, planar technology MOSFETs were frequently used to create MOSFET-based clamping circuits. Nonetheless, the advantage of the LINFET in this scenario is its substantially lower gate charge, which significantly increases the clamp's response time.

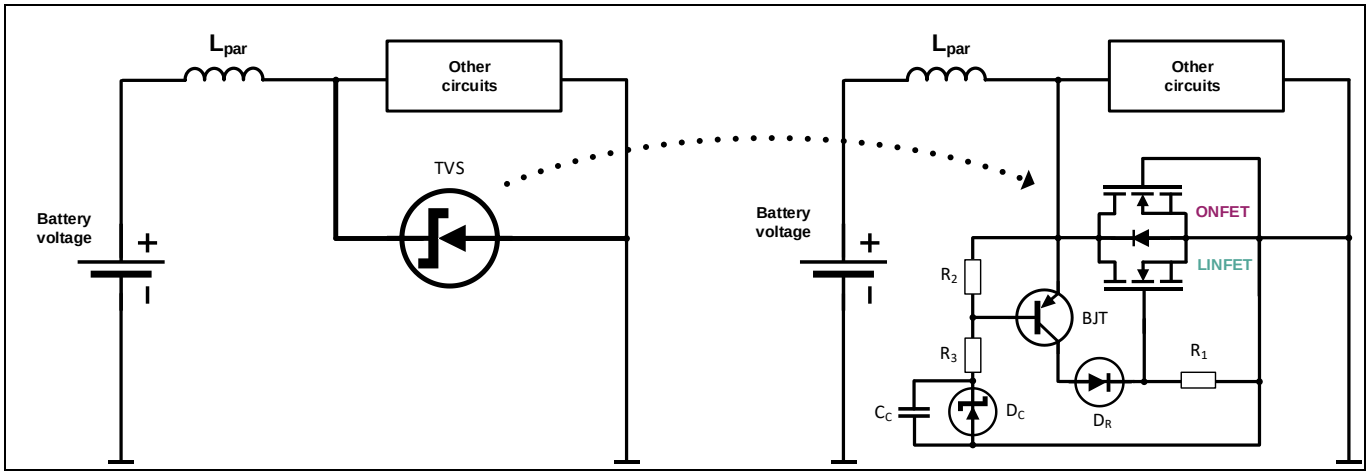


Figure 24 Replacing TVS protection diodes with Dual Gate MOSFET to improve clamping accuracy

4 Evaluation board

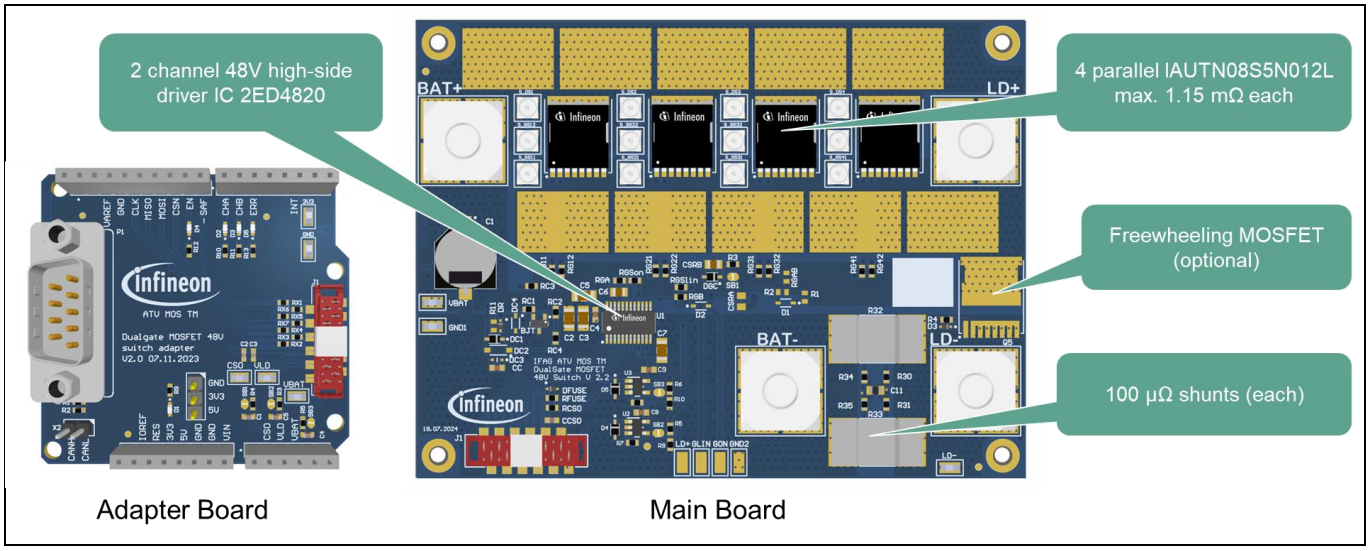


Figure 25 Dual Gate 48V switch main board and adapter board

4.1 Features

- Uni-directional 48 V switch for continuous current up to 250 A (12 kW)
- 4 layer board with optimized passive cooling concept for best thermal performance
- Capable of capacitor pre-charging and high short circuit robustness using IAUTN08S5N012L
- Shunt based current measurement and monitoring in low-side path
- Overcurrent protection with adjustable thresholds
- Adaptor board to flexibly connect various kinds of µC (Aurix™, Traveo™, XMC™, Arduino)
- One Eye GUI to control driver and to adjust capacitor charging patterns (supported by KIT_XMC_PLT2GO_XMC4200 or KIT_XMC47_RELAX_V1)

4.2 Technical data and recommended operation conditions

Table 3

Parameter	Symbol	Comment	Value	Unit
Main board size	W x L x H	With heatsink	75 x 100 x 31	mm^3
Adaptor board size	W x L x H		53 x 64 x 19	mm^3
Recommended supply voltage	VBAT+	DC	48	V
Digital supply voltage	VDD	IO voltage µC/driver	3.3	V
Continuous current	IDC	DC current, T_a = 25°C	250	A
Combined MOSFET resistance	$R_{DS(on)}$	T_a = 25°C, 1 mΩ each MOSFET	250	µΩ
Combined shunt resistance	R_{shunt}	T_a = 25°C, 100 µΩ each shunt	50	µΩ

4.3 Simplified circuit

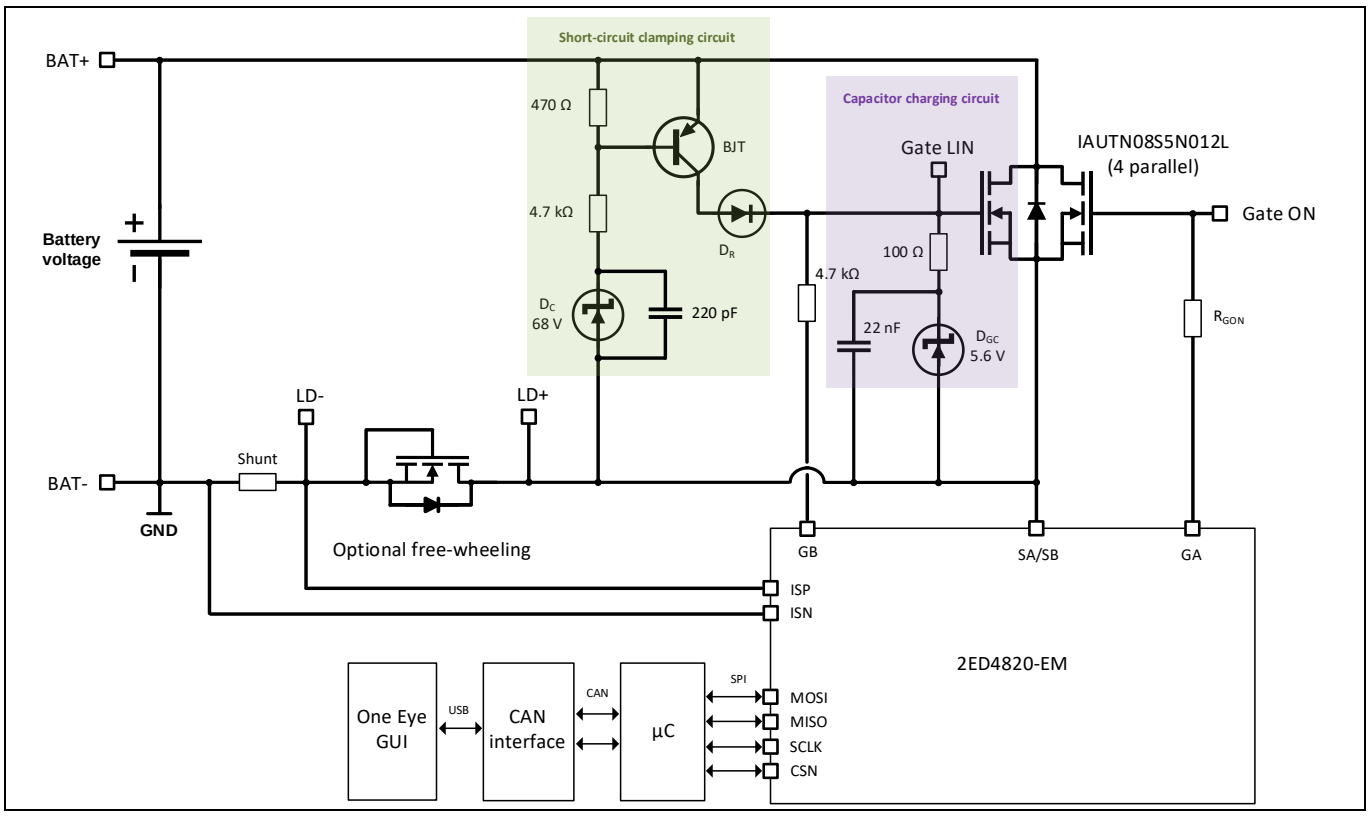


Figure 26 Simplified Dual Gate 48V switch board circuit

Selected components are in line with what was already explained in chapter 3.1 and chapter 3.2.

The capacitor charging circuit is designed to limit in-rush currents during capacitor charging. The inclusion of a zener diode limits the gate voltage, while the 22 nF capacitor slows down the switching speed, minimizing under- and overshoots of drain-source voltage during capacitor charging.

To prevent entry into avalanche, the short-circuit clamping circuit limits the drain-source voltage below the break-down voltage of the Dual Gate MOSFET at a voltage of typically 71 V. The drain source voltage slope is limited to typically 5 V/µs to ensure smooth transition into the clamp voltage and give zener diodes as well as clamp circuit enough reaction time.

Decoupling the capacitor charging circuit from the short-circuit clamping circuit is achieved with the 100 Ω resistor, with gate voltage control being predominantly managed by the latter.

For current sensing with the driver 2ED4820-EM, the shunt 50 µΩ (2x 100 µΩ) is employed. Communication between the driver and the Microcontroller (µC) is facilitated via SPI, while the Microcontroller is controlled via a CAN interface connected to the PC via USB. The One Eye GUI is used to control the driver.

Loads can be connected at terminals LD+ and LD-.

4.4 Quick start-up guide

4.4.1 Additionally required components before start-up

- CAN interface Vector Informatik GmbH or PEAK-System Technik GmbH
- MMCX cable adapters (MMCX male to SMA female) and SMA connectors for probing
- Power supply (48 V), oscilloscope, current probe and at least 2 differential voltage probes and a standard voltage probe
- Capacitor bank to buffer the power supply (required for capacitor charging). The capacitor bank should be several times higher in capacitance compared to the load capacitor.
- 4 cables (>25 mm^2 copper diameter) with M6 or M8 lugs for screw connection on board. Please pay attention with M8 lugs to not create a short circuit to the MMCX sockets at VBAT+.
- Test loads (resistors, active loads, capacitors, inductors)
- D-sub cable female-female connector to connect CAN interface to the adapter board. If the D-sub cable has an integrated 120 Ohm termination, resistor R2 on the adapter board can be removed.
- Jumper wire cable (CAN-High, CAN-Low) to connect XMC KIT CAN signal to the adapter board.
- Micro-USB cable and power supply for the XMC4700 Relax KIT

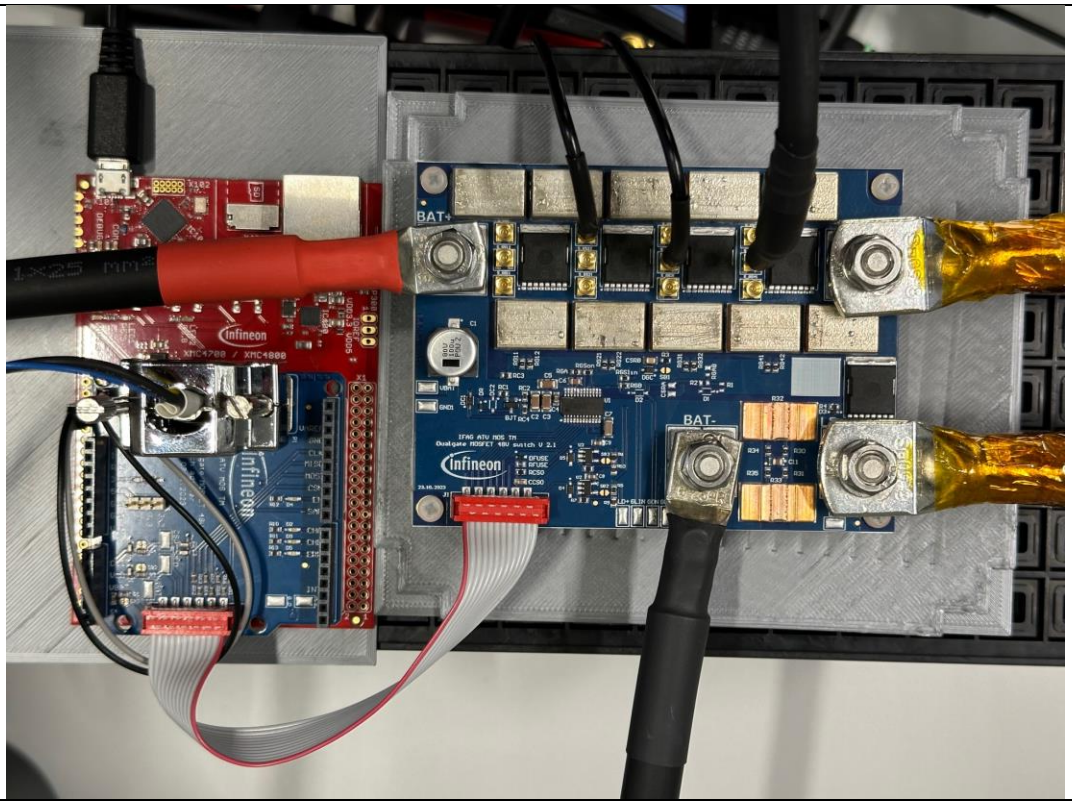


Figure 27 Board connections (example with KIT_XMC47_RELAX_V1) top view

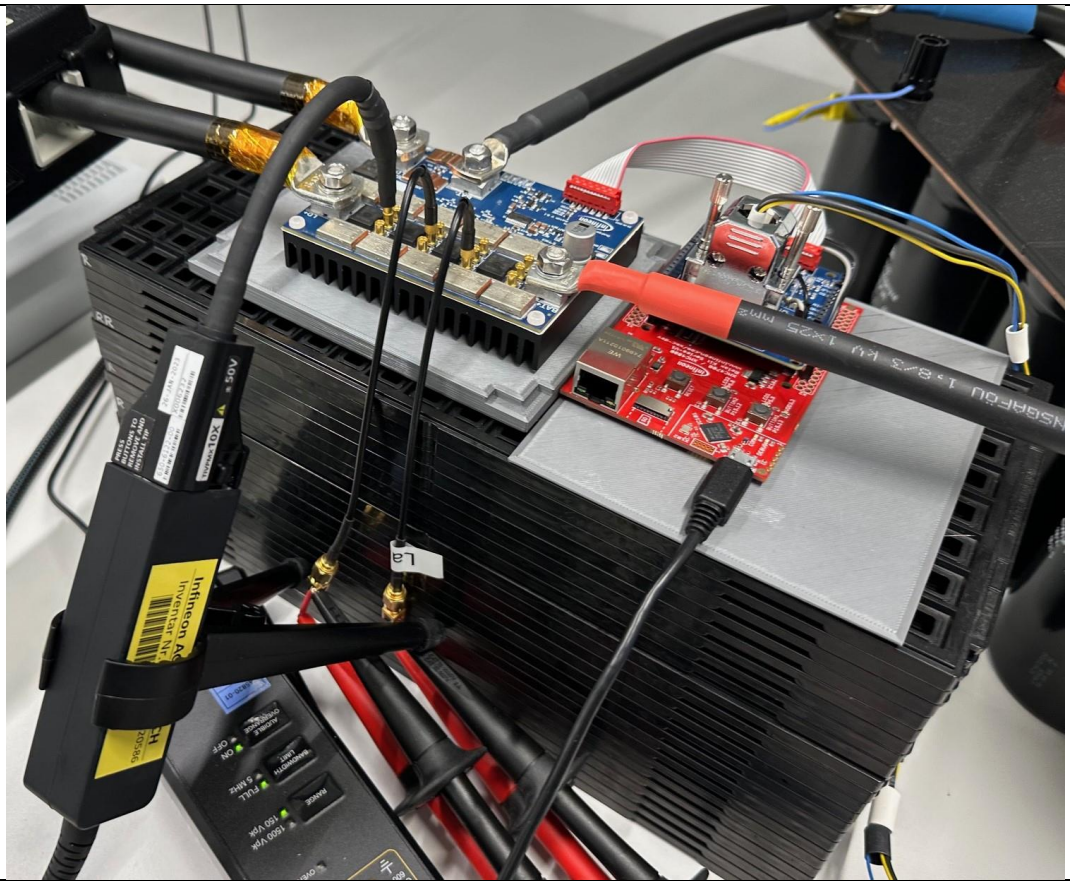


Figure 28 Board connections (example with KIT_XMC47_RELAX_V1) side view

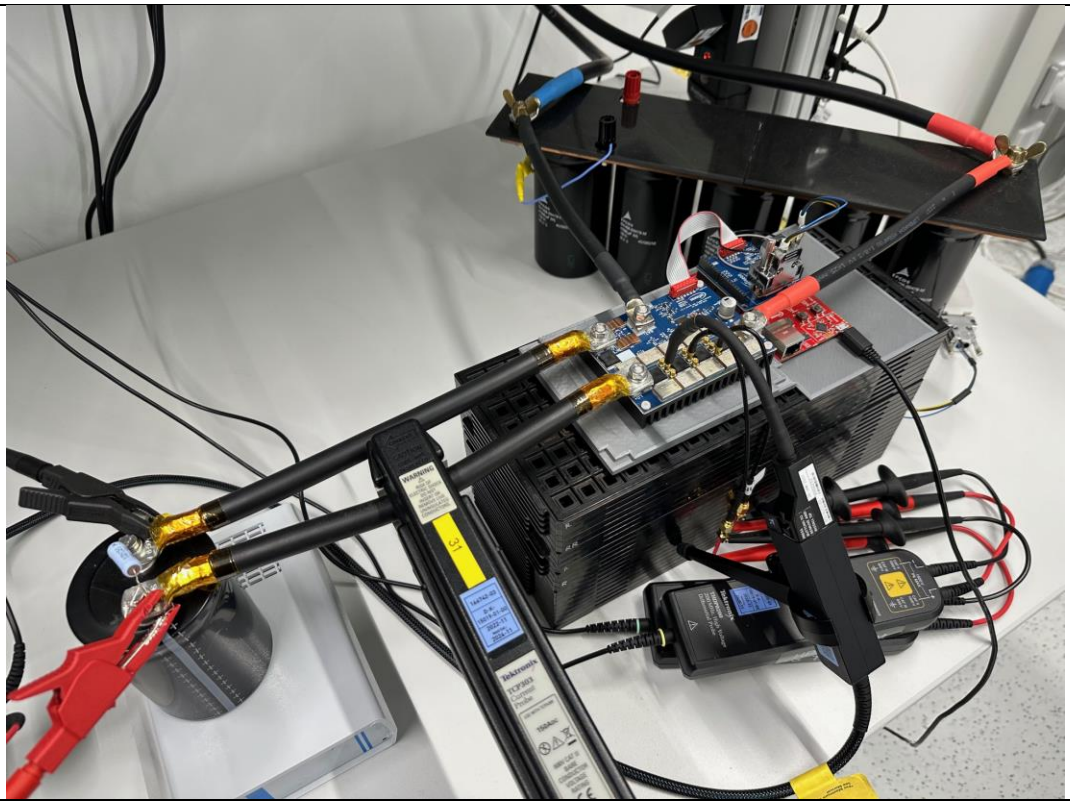


Figure 29 Exemplary setup with load capacitor (33 mF) and capacitor bank

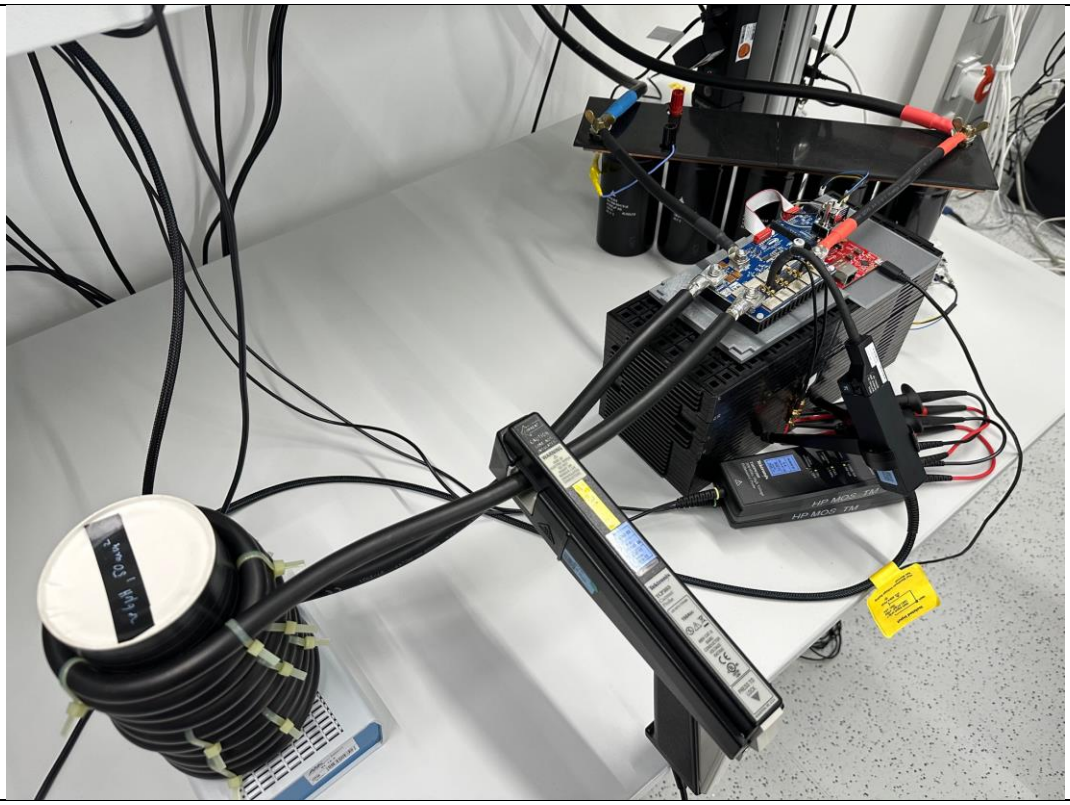


Figure 30 Exemplary setup with load inductance (6.5 µH) and capacitor bank

4.4.2 Download and prepare One Eye and XMC KIT

1. Please install the latest version of One Eye: Link
2. Download latest Dual Gate MOSFET One Eye configuration file and XMC code here: Link
3. Flash your XMC Microcontroller with the .hex or .elf file (e.g. using SEGGER J-Flash Lite)
4. Open One Eye and load the Dual Gate MOSFET configuration file
5. Setup the CAN interface (refer to chapter 4.5)

4.4.3 Interfaces SPI, CAN and USB

The MOSFET Gates can be turned on and off by gate driver 2ED4820-EM, which is connected to the Microcontroller via SPI. The Microcontroller is controlled via CAN bus interface, which is connected to the PC via USB. Interfaces from Vector Informatik GmbH and PEAK-System Technik GmbH are most suitable and were verified. To control the CAN Interface, the One Eye control suite can be used. Therefore, download the Dual Gate MOSFET One Eye configuration file into One Eye.

4.5 How to use One Eye GUI

One Eye provides seamless control over the Dual Gate MOSFET switch board through an intuitive graphical user interface (GUI) that is easy to use (refer to Figure 31). The GUI is split into two tabs. The primary tab is used to manipulate the driver channels A and B, along with the generation of custom pulse patterns (e.g. for capacitor charging with channel B). The Driver Settings tab, on the other hand, enables you to modify individual driver settings

to suit your needs. Before connecting the driver, it is essential to first configure the CAN interface. To do this, simply click on the “Setup CAN Interface” button and set up the CAN interface (refer to Figure 32).

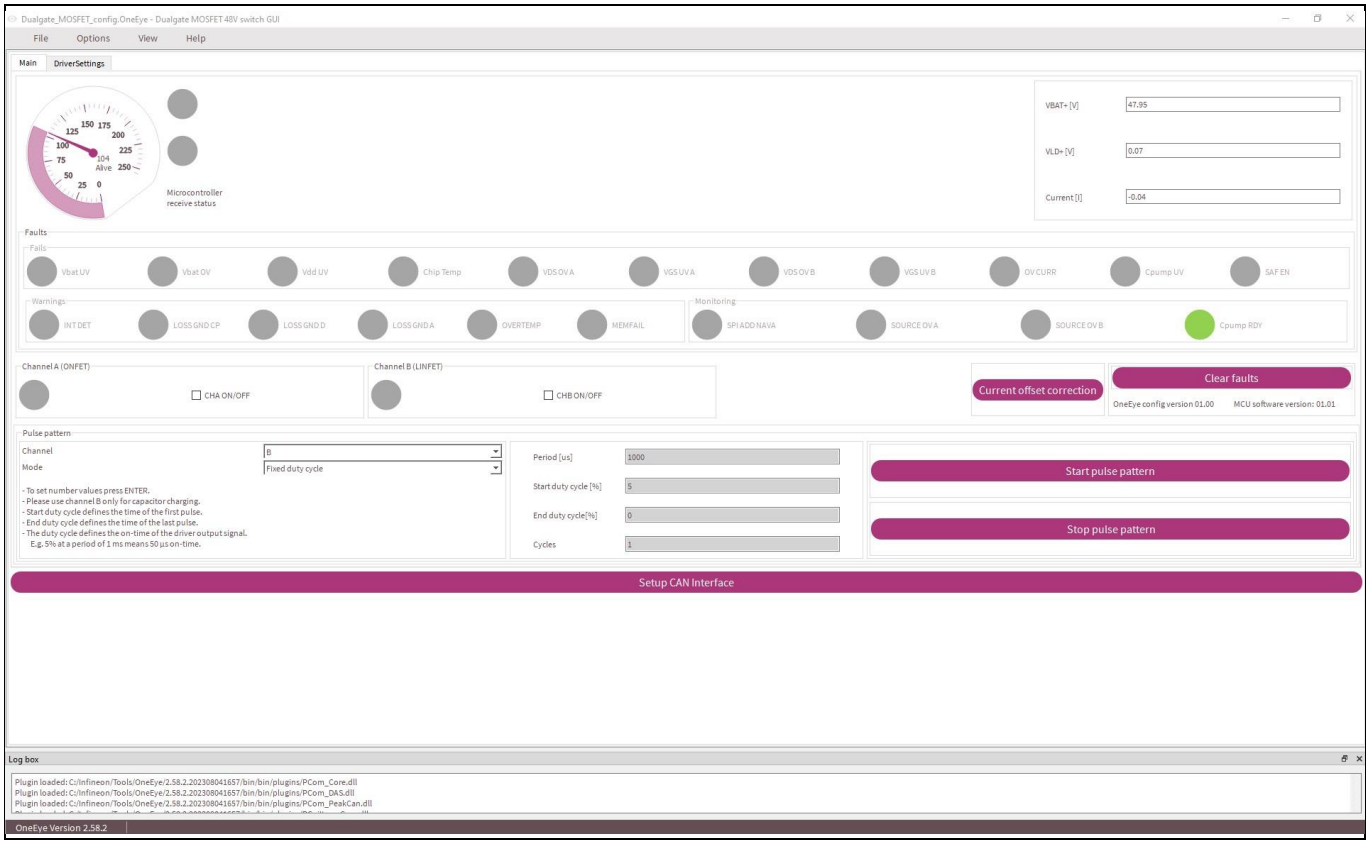


Figure 31 One Eye GUI Dual Gate MOSFET – main tap

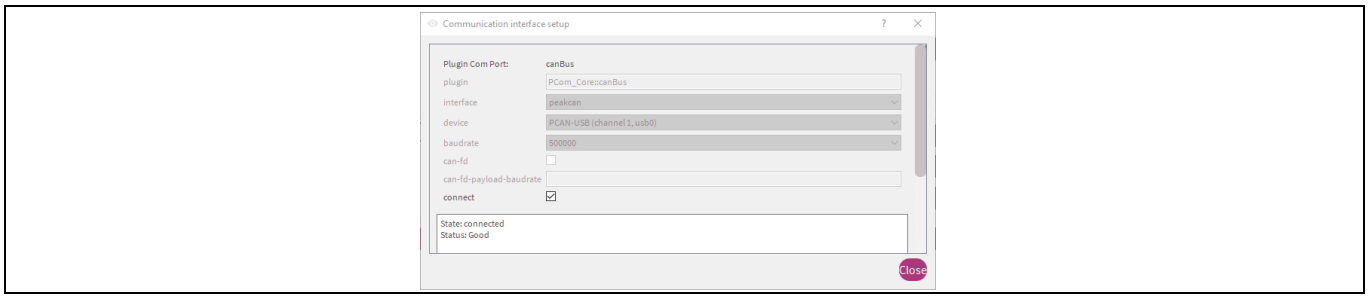


Figure 32 One Eye GUI Dual Gate MOSFET – CAN interface configuration

The main tab is divided into four subsections for easy navigation. The first subsection, located on the top left side, comprises the alive counter and the receive status of the microcontroller. The alive counter allows you to ensure that the microcontroller and the CAN interface is functioning correctly, while the receive status indicates, that the microcontroller received the previously sent command.

The section at the top right, you can find the measured voltage applied to VBAT+ (power supply supply) and VLD+ (load), along with the current measured by shunts and gate driver.

The middle section shows the status of various functions of the driver as for example appearing faults and monitoring. Faults can be cleared by pressing the button “Clear Faults”.

The fields “Channel A (ON-FET)” and “Channel B (LIN-FET)” are used for channel control and on/off status monitoring.

In section “Pulse pattern” the gate channels can be operated in a pulsed way (e.g. to perform capacitor charging). There are three modes to perform the pulsing:

- Fixed duty cycle (same pulse width overall charging pattern)
- Linear increasing duty cycle (linear function to increase the pulse width)
- Parabolic increasing duty cycle (parabolic function to increase the pulse width)

Regarding the functions and meaning of Period, D_{start}, D_{end} and cycle numbers, please also refer to chapter 3.1.5. When operating with fixed duty cycle, D_{start} will be used as fixed duty cycle overall cycles. **Please press “Enter” for every value typed in** for Period, D_{start}, D_{end} and cycle number. Elsewise, the value will not be set correctly.

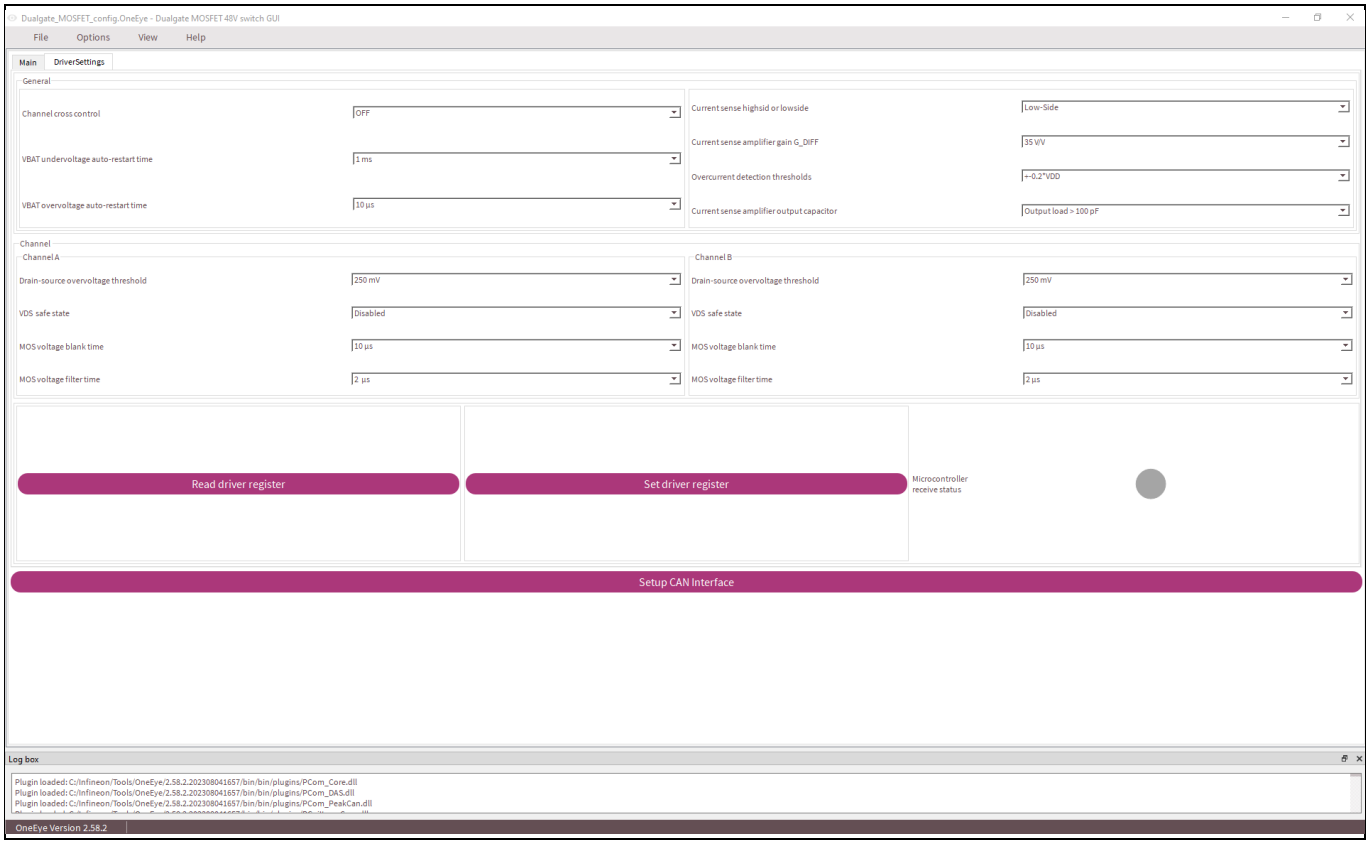


Figure 33 One Eye GUI Dual Gate MOSFET – driver settings

However, it is crucial to exercise caution when dealing with capacitive loads to prevent damage and overloading of the board. For every capacitor charging or loading scenario a detailed assessment must be done. Please just use channel B (LINFET) for capacitor charging as the ONFET is not suited to limit in-rush currents. To initiate the pulse pattern, press “Send pulse pattern” button. The pattern can be stopped by pressing “Stop pulse pattern”. The microcontroller captures the parameters and sets them automatically to the minimum or maximum allowed values if exceeded. Note that if the start duty cycle is larger than the end duty cycle, the process will not start.

The Driver settings tab presents two distinct sections (refer to Figure 33). The first section encompasses general driver settings, while the second section is dedicated to channel specific settings, divided between the left A-ONFET and the right B-LINFET. To ensure the correct input of standard values, we recommend reading out the parameter beforehand.

4.6 Driver 2ED4820-EM configuration

Table 4 lists the possible configuration settings for the gate driver 2ED4820-EM.

Table 4 Driver configuration settings

Register name	Description	Setting	Value
VBATOVARST	**VBAT overvoltage auto-restart time**		
		0	10 µs
		1	50 µs
		2	200 µs
		3	1 ms
VBATUVARST	**VBAT undervoltage auto-restart time**		
		0	1 ms
		1	5 ms
		2	20 ms
		3	50 ms
MOSBLK_A **MOSBLK_B**	**MOSFET voltage blank time ch. A** **MOSFET voltage blank time ch. B**		
		0	10 µs
		1	20 µs
		2	50 µs
		3	100 µs
MOSFLT_A **MOSFLT_B**	**MOSFET voltage filter time ch. A** **MOSFET voltage filter time ch. B**		
		0	0.5 µs
		1	1 µs
		2	2 µs
		3	5 µs
VDSTH_A **VDSTH_B**	**Drain-source overvoltage threshold ch. A** **Drain-source overvoltage threshold ch. B**		
		0	100 mV
		1	150 mV
		2	200 mV
		3	250 mV
		4	300 mV
		5	400 mV
		6	500 mV
		7	600 mV
VDSA_SS **VDSB_SS**	**Safe state in case of VDS overvoltage ch. A** **Safe state in case of VDS overvoltage ch. B**		
		0	channel is deactivated

Register name	Description	Setting	Value
		1	channel stays active
CHCRCTRL	**Channel cross-control**		
		0	cross control deactivated
		1	cross control activated
CSAG	**Current sense amplifier gain**		
		0	10 V/V
		1	15 V/V
		2	20 V/V
		3	25 V/V
		4	31.5 V/V
		5	35 V/V
		6	40 V/V
		7	47.7 V/V
CSA_COUTSEL	**Current sense output load**		
		0	< 100 pF
		1	> 100 pF
OCTH	**Overcurrent detection threshold**		
		0	$V_{DD}/2 \pm 0.1\ V_{DD}$
		1	$V_{DD}/2 \pm 0.2\ V_{DD}$
		2	$V_{DD}/2 \pm 0.25\ V_{DD}$
		3	$V_{DD}/2 \pm 0.3\ V_{DD}$

For channel B (LINFET) a blank time of 10 µs is recommended to avoid charge pump errors.

The actual overcurrent threshold value in Ampere is depending on the setting of the current sense amplifier gain (csag) and the overcurrent detection threshold setting (octh). Table 5 shows the resulting values for a 50 µΩ shunt resistor. The default factory setting is csag 5 and octh 1 which amounts in an overcurrent threshold of 377 A.

Table 5 Overcurrent threshold values dependent on gain and threshold (default value 377 A)

$V_{DD}/2$	10 V/V	15 V/V	20 V/V	25 V/V	31.5 V/V	35 V/V	40 V/V	47.7 V/V
± 0.1 V_{DD}	660 A	440 A	330 A	264 A	210 A	189 A	165 A	138 A
± 0.2 V_{DD}	1320 A	880 A	660 A	528 A	419 A	**377 A**	330 A	277 A
± 0.25 V_{DD}	1650 A	1100 A	825 A	660 A	524 A	471 A	413 A	346 A
± 0.3 V_{DD}	1980 A	1320 A	990 A	792 A	629 A	566 A	495 A	415 A

Table 6 Default configuration 2ED4820-EM

Command	Description	Setting	Value
VBATOVARST	**VBAT overvoltage auto-restart time**	0	10 µs
VBATUVARST	**VBAT undervoltage auto-restart time**	0	1 ms
MOSBLK_A	**MOSFET voltage blank time ch. A**	0	10 µs
MOSBLK_B	**MOSFET voltage blank time ch. B**	0	10 µs

Command	Description	Setting	Value
MOSFLT_A	**MOSFET voltage filter time ch. A**	1	1 µs
MOSFLT_B	**MOSFET voltage filter time ch. B**	1	1 µs
VDSTH_A	**Drain-source overvoltage threshold ch. A**	2	200 mV
VDSTH_B	**Drain-source overvoltage threshold ch. B**	2	200 mV
VDSA_SS	**Safe state in case of VDS overvoltage ch. A**	0	channel is deactivated
VDSB_SS	**Safe state in case of VDS overvoltage ch. B**	0	channel is deactivated
CHCRCTRL	**Channel cross-control**	0	cross-control deactivated
CSAG	**Current sense amplifier gain**	5	35 V/V
CSA_COUTSEL	**Current sense output load**	1	> 100 pF
OCTH	**Overcurrent detection threshold**	1	VDD/2 ± 0.2 VDD

4.7 Capacitor charging 33 mF simulation vs. measurement results

- Ta = 25°C, VBAT = 48 V
- C1 = 33 mF (load capacitor), ~400 nH cable inductance
- Parabolic modulation of pulse width, cycle number: 90
- Pulse width (start): 80 µs, Pulse width (stop): 240 µs, Period: 1 ms

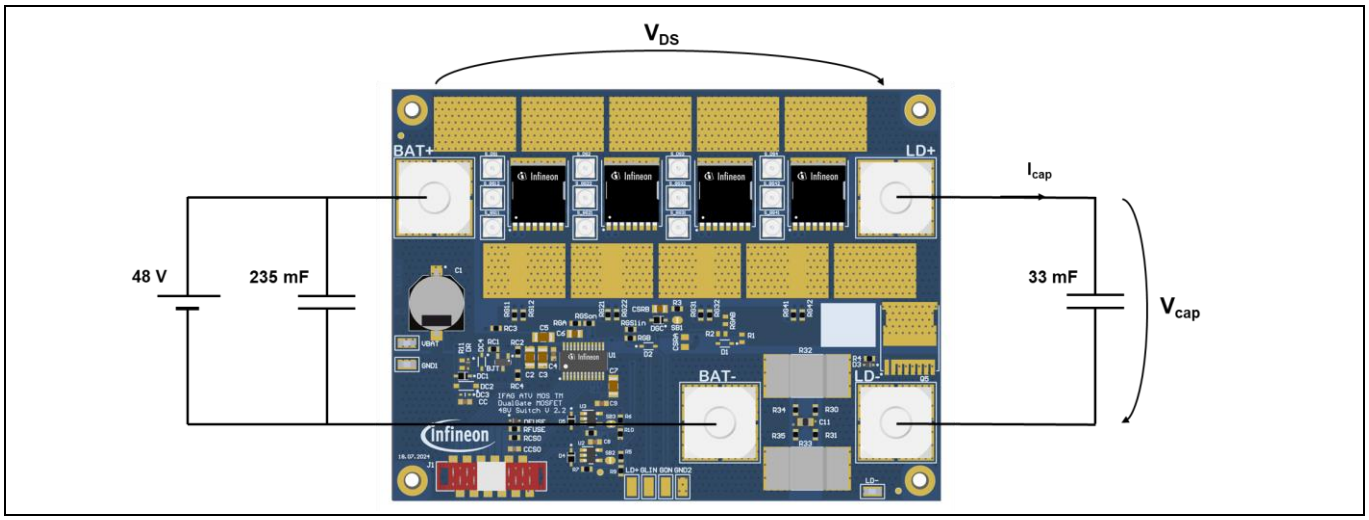


Figure 34 Capacitor charging simplified measurement/simulation setup

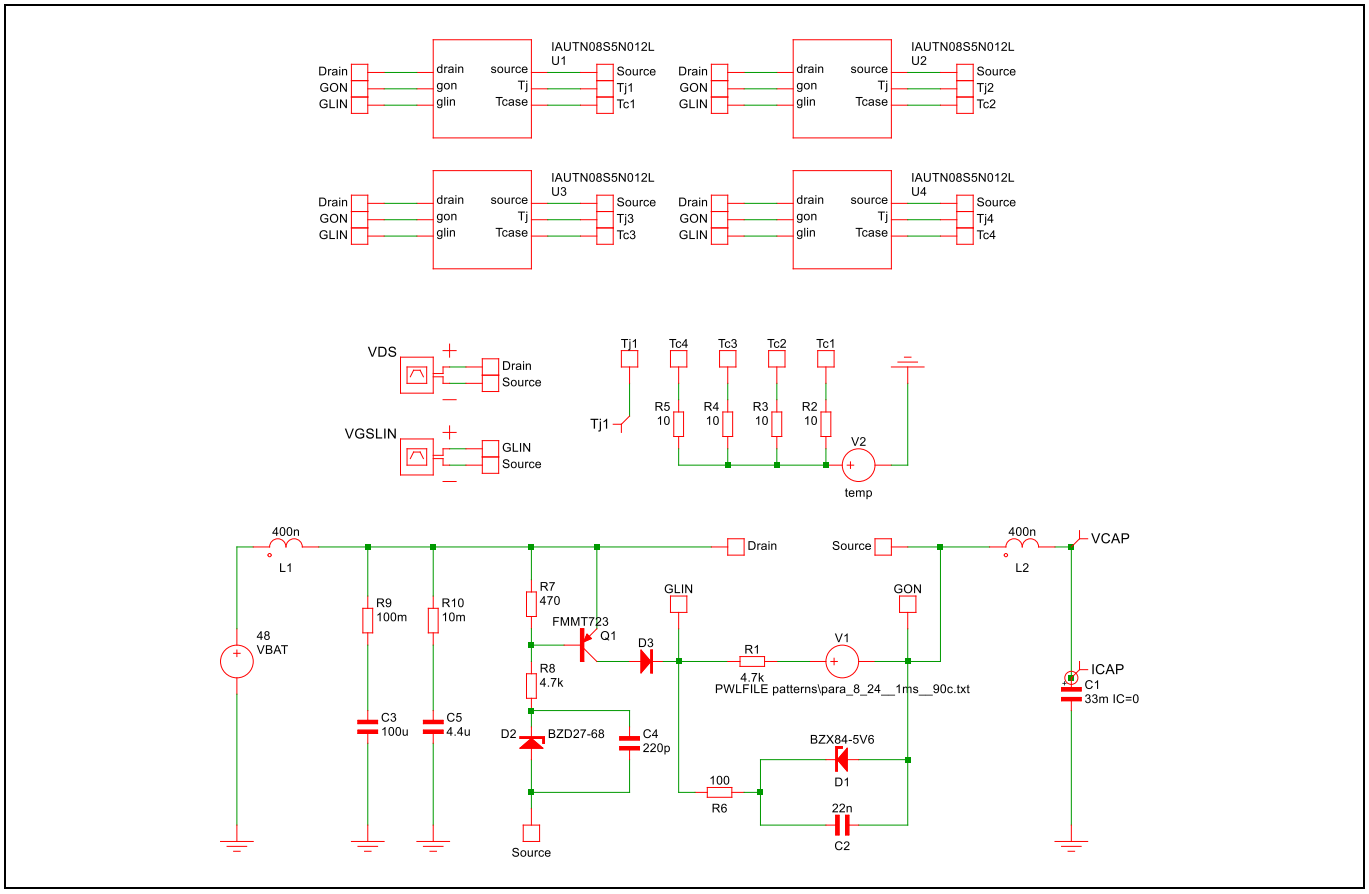


Figure 35 Board simulation schematic – 33 mF capacitor charging

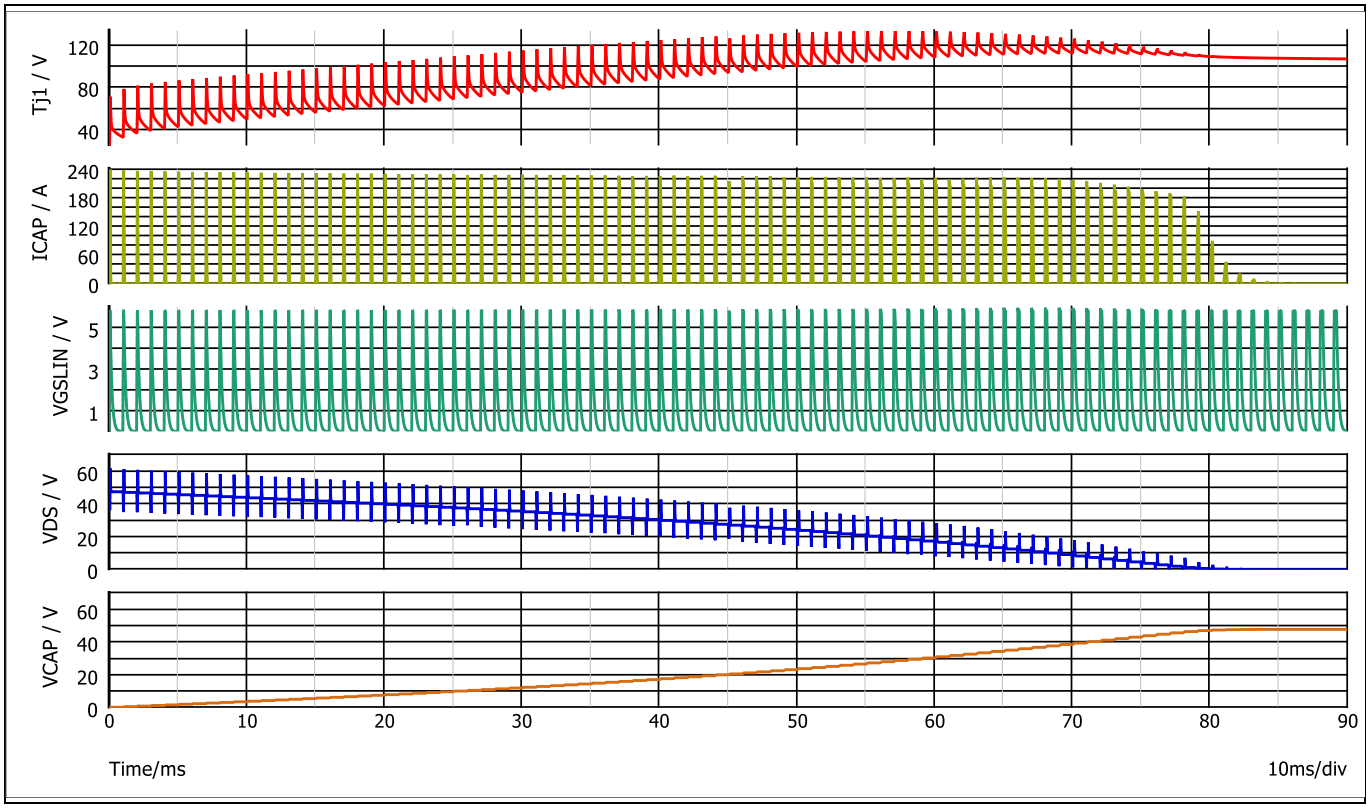


Figure 36 Board simulation graph – 33 mF capacitor charging

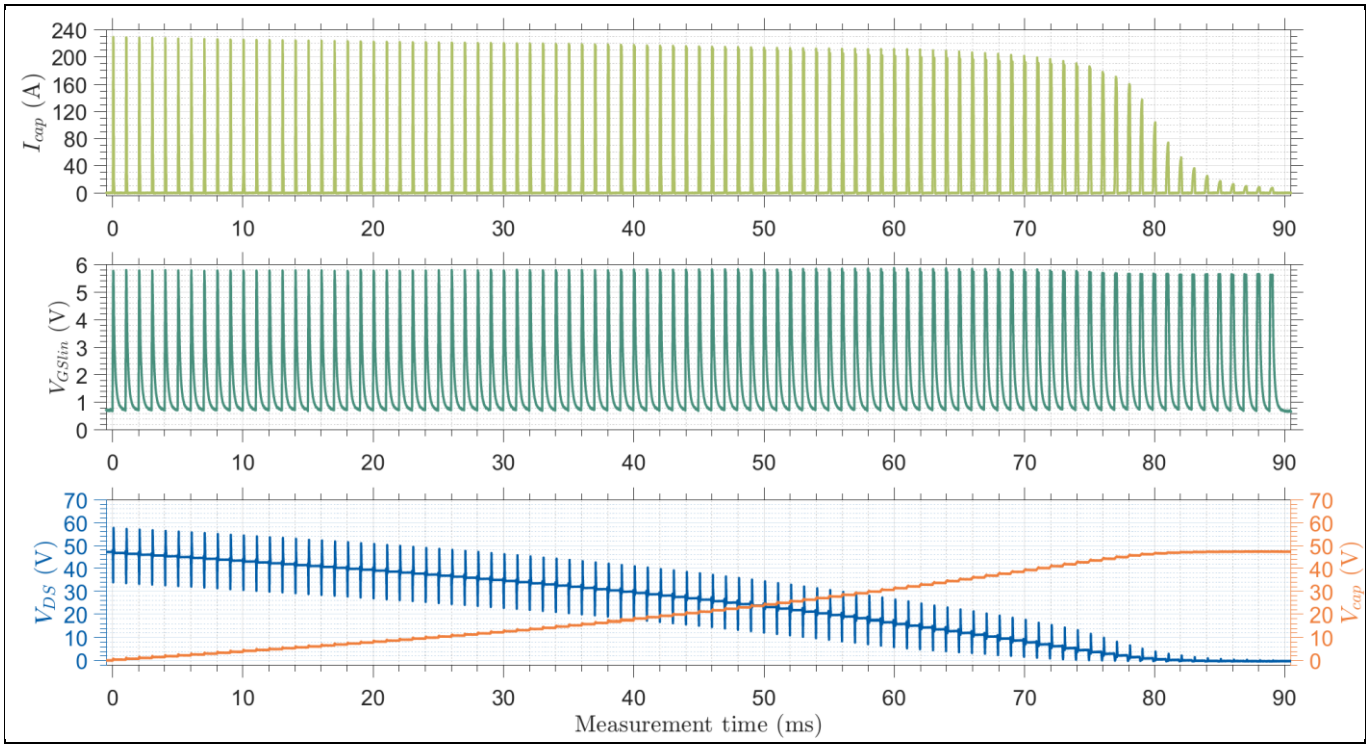


Figure 37 Board measurement graph – 33 mF capacitor charging

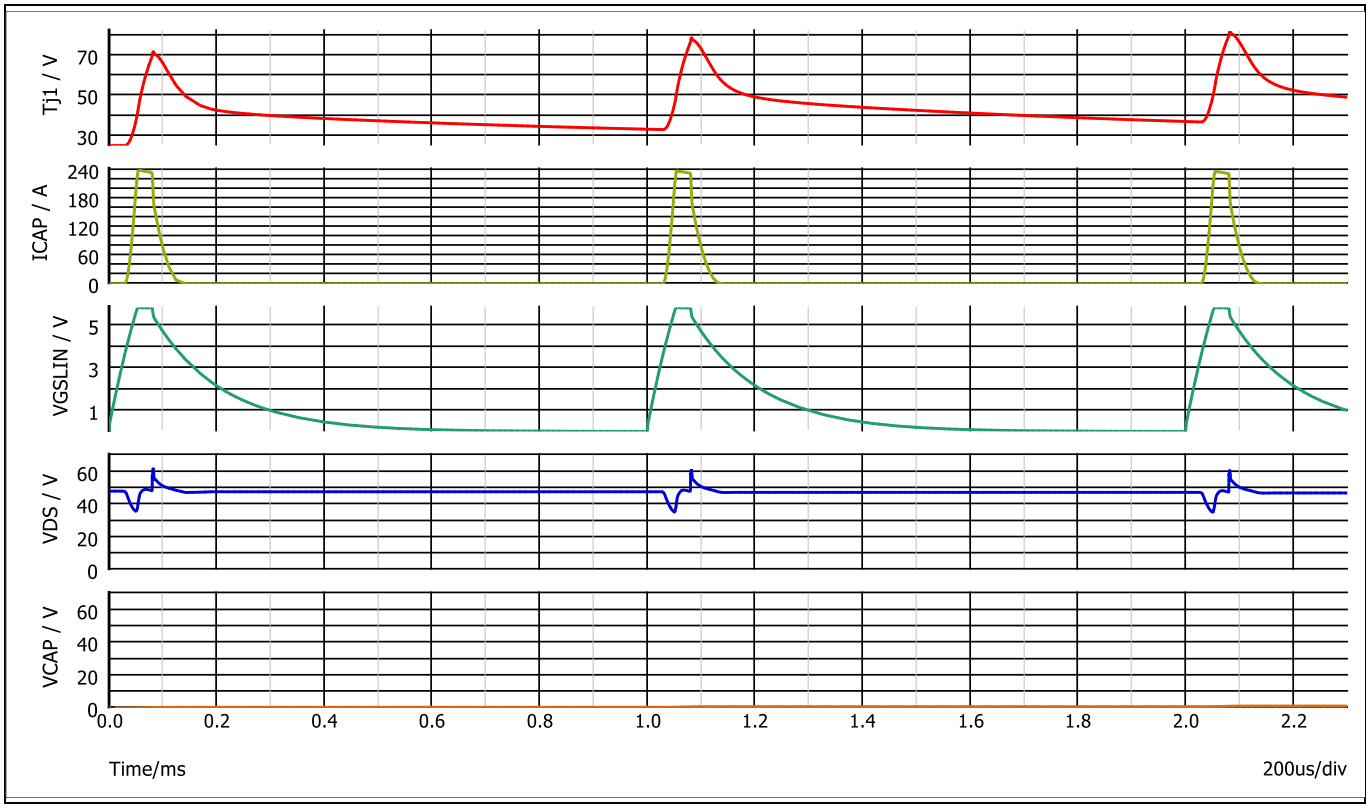


Figure 38 Board simulation graph – 33 mF capacitor charging (zoomed)

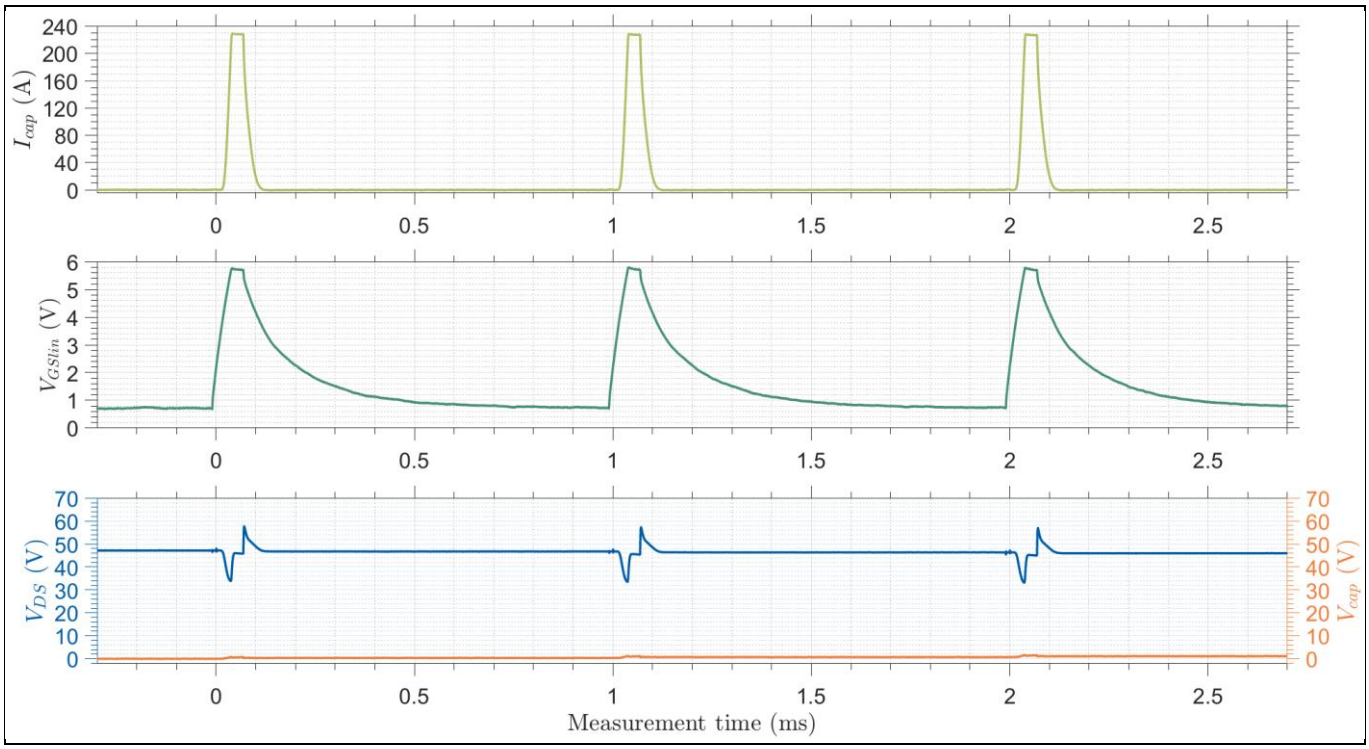


Figure 39 Board measurement graph – 33 mF capacitor charging (zoomed)

4.8 Clamping with 6.5 µH load inductance simulation vs. measurement

- Ta = 25°C, VBAT = 48 V
- 400 nH setup cable inductance (L1), 6.5 µH load and cable inductance (L2)
- Gate voltage pulse (ONFET) to charge up inductance L2 to ~480 A representing over-current turn-off. Discrepance of 480 A to target 377 A due to driver and clamp circuit delay time.
- LINFET to clamp the drain-source voltage at around 71 V after turn-off of ONFET

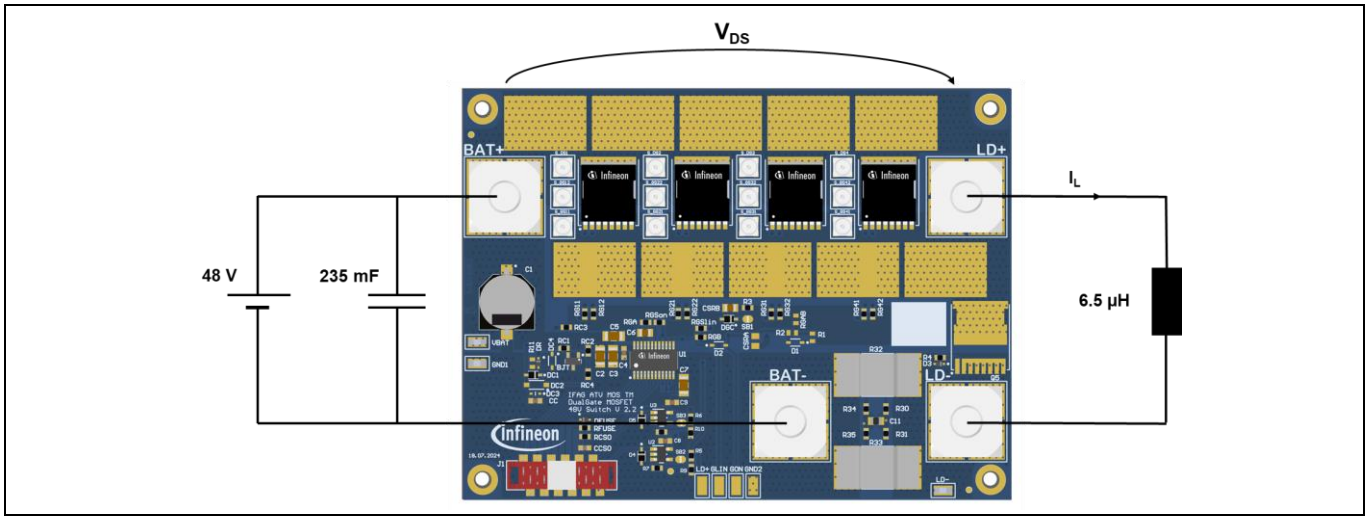


Figure 40 Active clamping simplified simulation/measurement setup

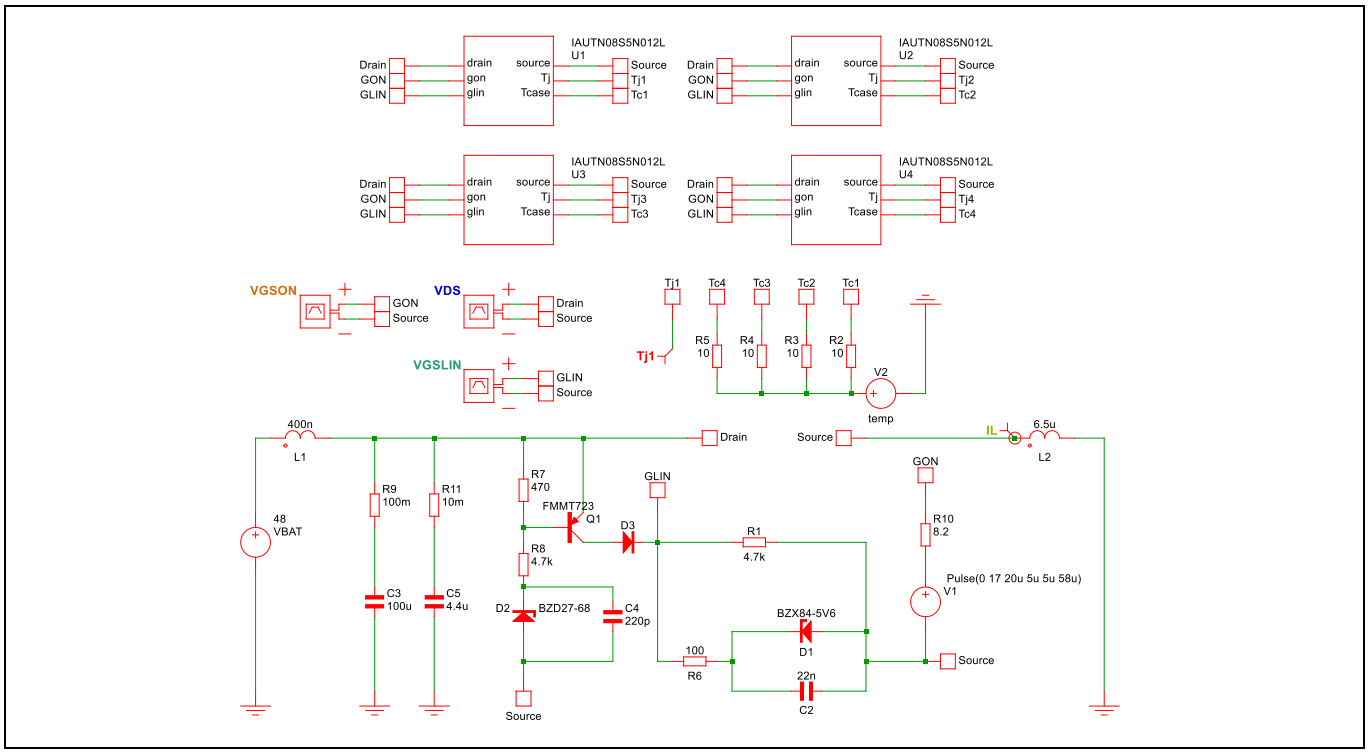


Figure 41 Active clamping simulation schematic with 6.5 µH inductance

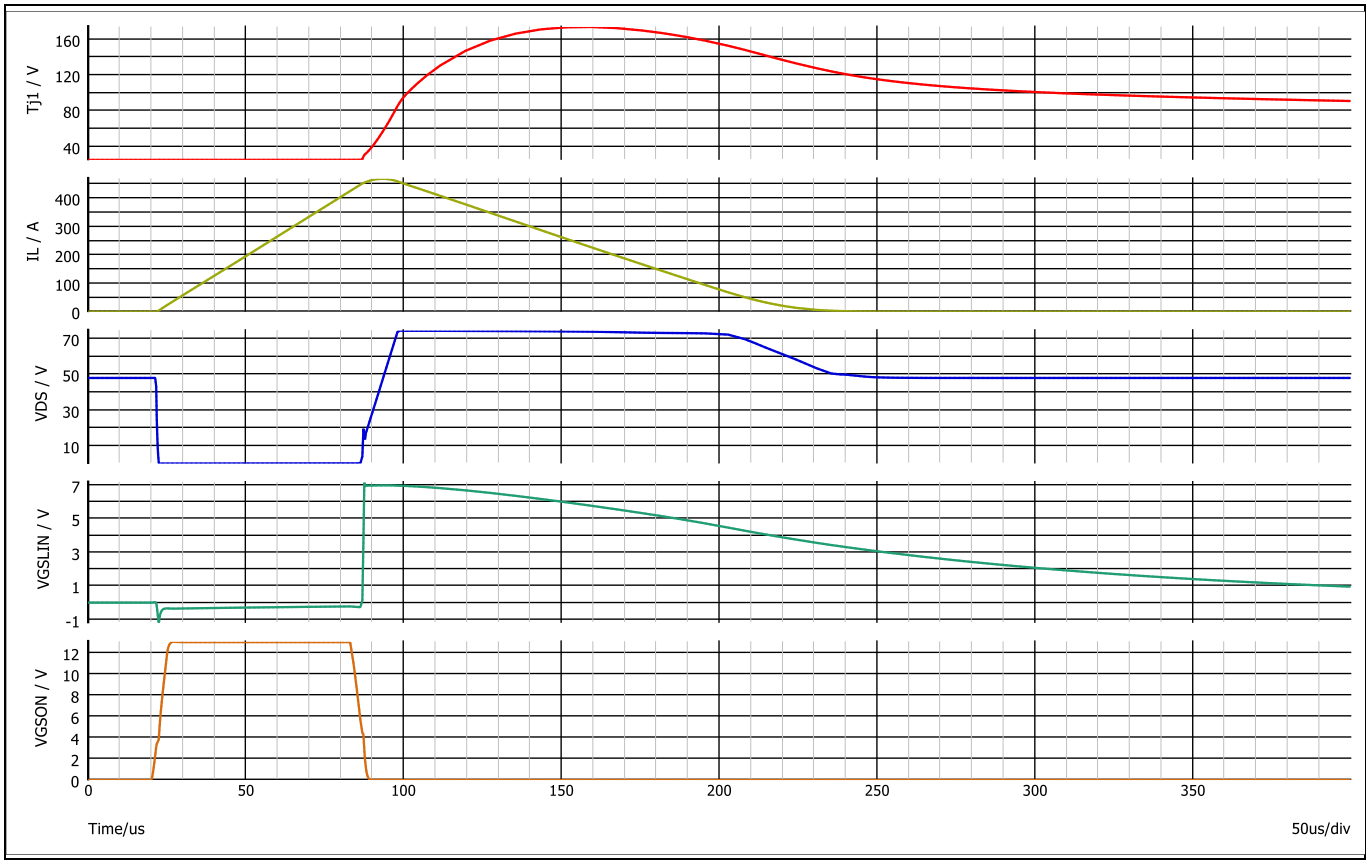


Figure 42 Active clamping simulation graph with 6.5 µH load inductance

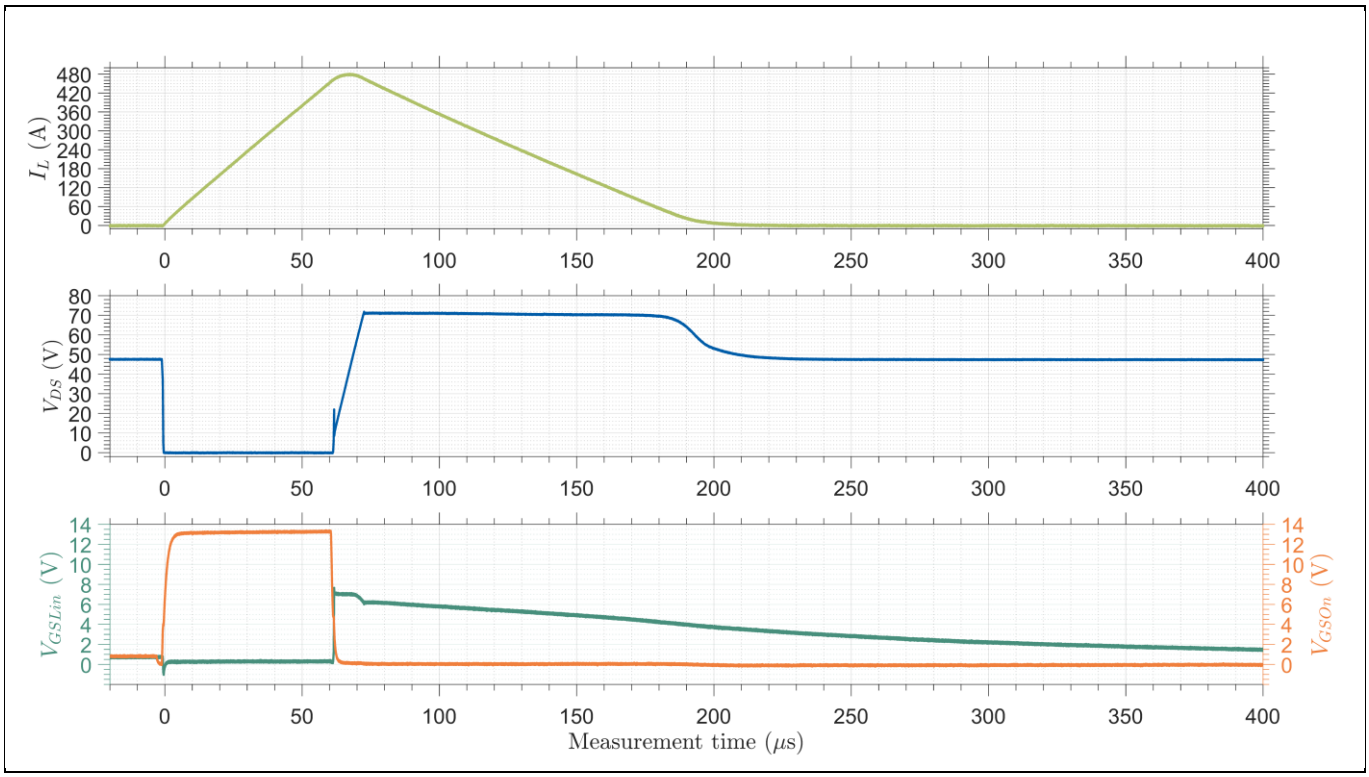


Figure 43 Active clamping measurement with 6.5 µH load inductance

4.9 Bill of material main board

Table 7 BOM main board

Designator	Qty	Type	Voltage	Value	Package	Manufacturer	Man. number
CCSO	1	Capacitor	50V	100 nF	0603	TDK	CGA3E2X7R1H104K
C11	1	Capacitor	16V	2.2 uF	0805	TDK	CGA4J3X7R1C225K
C2, C3, C5	3	Capacitor	100V	2.2 uF	1206	TDK	CGA5L3X7S2A225K
C4, C8, C9	3	Capacitor	100V	100 nF	0603	TDK	CGA3E3X7S2A104K
C6	1	Capacitor	100V	220 nF	0805	TDK	CGA4F3X7S2A224K
C7	1	Capacitor	100V	1 uF	1206	TDK	CGA5L2X7R2A105K
CSRB	1	Capacitor	100V	22 nF	0805	TDK	CGA4J2X7R2A223K
C1	1	Capacitor	80V	100 uF	10x10 mm²	Vishay	MAL215099702E3
CC	1	Capacitor	100V	220 pF	0603	TDK	CGA3E2NP02A221JT
R30, R31, R34, R35, G11, RG12, RG21, RG22, G31, RG32, RG41, RG42, RGA	13	Resistor	100V	8.2 Ω	0603	Vishay	CRCW0603- HP
RFUSE	1	Resistor	100V	0.1 Ω	0603	Vishay	CRCW0603- HP
RGSlin, RGSon	2	Resistor	100V	150 kΩ	0603	Vishay	CRCW0603- HP
RC1, RC3	2	Resistor	100V	0 Ω	0603	Vishay	CRCW0603- HP
RC2	1	Resistor	100V	470 Ω	0603	Vishay	CRCW0603- HP
RC4, RGB	3	Resistor	100V	4.7 kΩ	0603	Vishay	CRCW0603- HP
R7, R8	3	Resistor	100V	5 kΩ	0603	Vishay	CRCW0603- HP
R3	1	Resistor	100V	100 Ω	0603	Vishay	CRCW0603- HP
R4, RCSO	2	Resistor	100V	10 kΩ	0603	Vishay	CRCW0603- HP
R5, R6	2	Resistor	100V	2.7 MΩ	0603	Vishay	CRCW0603- HP
R9, R10	2	Resistor	100V	100 kΩ	0603	Vishay	CRCW0603- HP
R11	1	Resistor	100V	47 kΩ	0603	Vishay	CRCW0603- HP
R32, R33	2	Shunt Resistor		100 µΩ	15x7.75mm²	Vishay	WSLP5931L1000FEA
Q1, Q2, Q3, Q4	4	MOSFET	80 V	1.15 mΩ	TOLL	Infineon	IAUTN08S5N012L
2ED4820-EM	1	Gatedriver	70 V	-	DSO	Infineon	2ED4820-EM
DFUSE	1	Zener diode	3.6 V	-	SOD-523	Onsemi	SZMM5Z3V6T1G
DGC	2	Zener diode	5.6 V	-	SOD-323	Panjit	BZT52-B5V6S-AU
DC1	1	Zener diode	68 V	-	SOD-323	Vishay	BZX384C68
D3	1	Zener diode	18 V	-	SOD-523	Panjit	SZMM5Z18VT1G
D4,D5	2	Zener diode	3.3 V	-	SOD-323	Panjit	BZT52-B3V3S-AU
DR	1	Diode	100 V	-	SOD-523	Onsemi	SBAS16XV2T1G
U2, U3	2	OPV	-	-	SOT-23-5	TI	OPA316QDBVTQ1
BJT	1	Bipolartransistor	100 V	-	SOT-23-3	Diodes	FMMT723QTA
X1, X2, X3, X4	4	Power connector	-	-	-	Würth	K97878
J1	1	Connector	-	-	-	Würth	690367291276
SDS1, SDS2, SDS3, SDS4, SGS11, SGS21, SGS31, SG41, SGS12, SGS22, GS32, SG42,	12	MMCX connector	-	-	-	Molex	734152061

4.10 Bill of material adapter board

Table 8 BOM adapter board

Designator	Qty	Type	Voltage	Value	Package	Manufacturer	Man. number
C1, C4, C5	3	Capacitor	50 V	1 nF	0603	TDK	CGA3E2X7R1H102K
C2, C3	2	Capacitor	50 V	100 nF	0603	TDK	CGA3E2X7R1H104K
R3, R4, R5	3	Resistor	100V	1 k Ω	0603	Vishay	CRCW0603- HP
R9, R10, R11, R12, R13	5	Resistor	100V	220 Ω	0603	Vishay	CRCW0603- HP
RX1, RX2, RX3, RX4, RX5, RX6, RX7	7	Resistor	100V	1 kΩ	0603	Vishay	CRCW0603- HP
R2	1	Resistor	100V	120 Ω	0603	Vishay	CRCW0603- HP
J1	1	Connector				Würth	690367291276
X1	1	Header				Samtec	SAM8814-ND
X2	1	Header				Samtec	SAM8736-ND
X5	1	Socket				Samtec	SSW-110-03-T-S
X6, X8	2	Socket				Samtec	SSW-108-03-T-S
X7	1	Socket				Samtec	SSW-106-03-T-S
P1	1	D-Sub connector				Würth	61800929221
D1, D2, D3, D4	4	LED - G			0603	Rohm	SML-D12P8WT86
D5	1	LED - R			0603	Rohm	SML-D12U8WT86

4.11 Main board layout and schematic

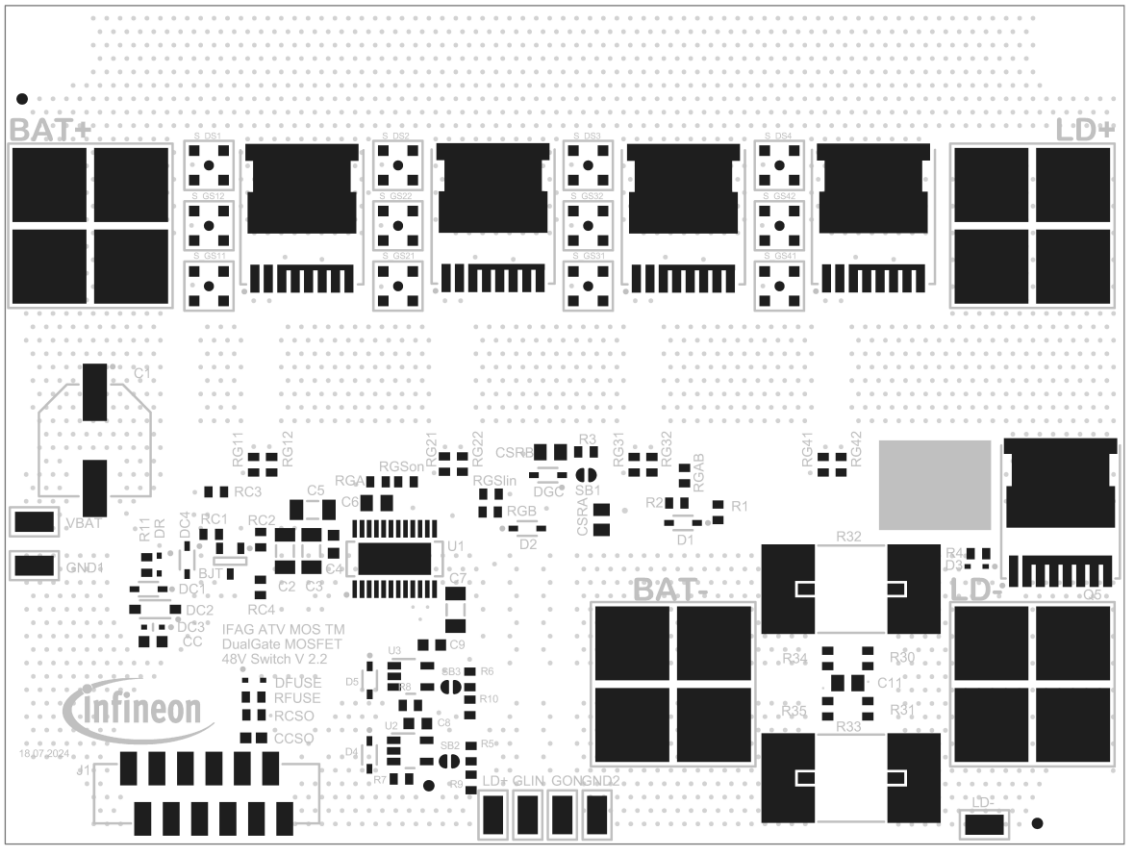


Figure 44 Main board component placement (top layer)

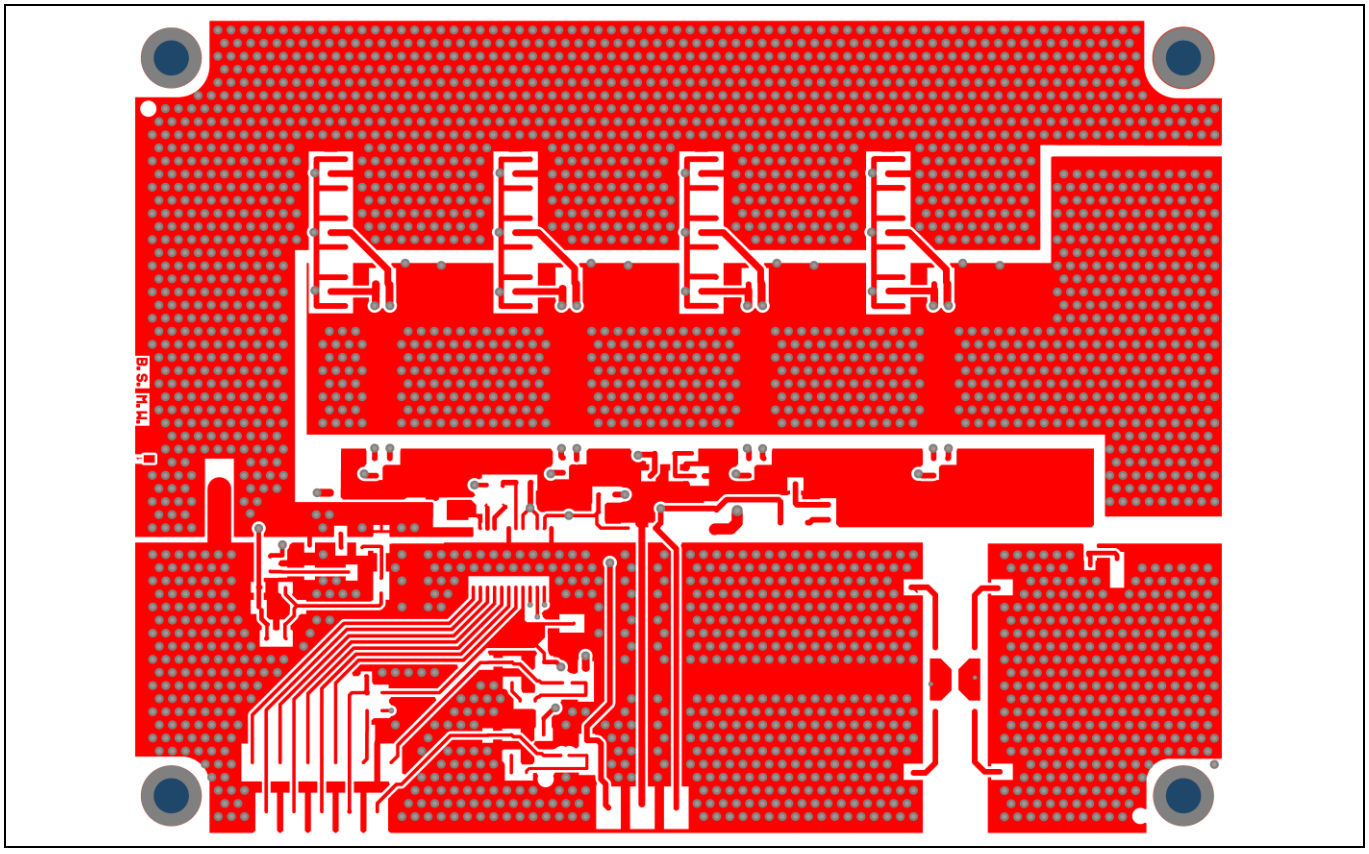


Figure 45 Main board top layer

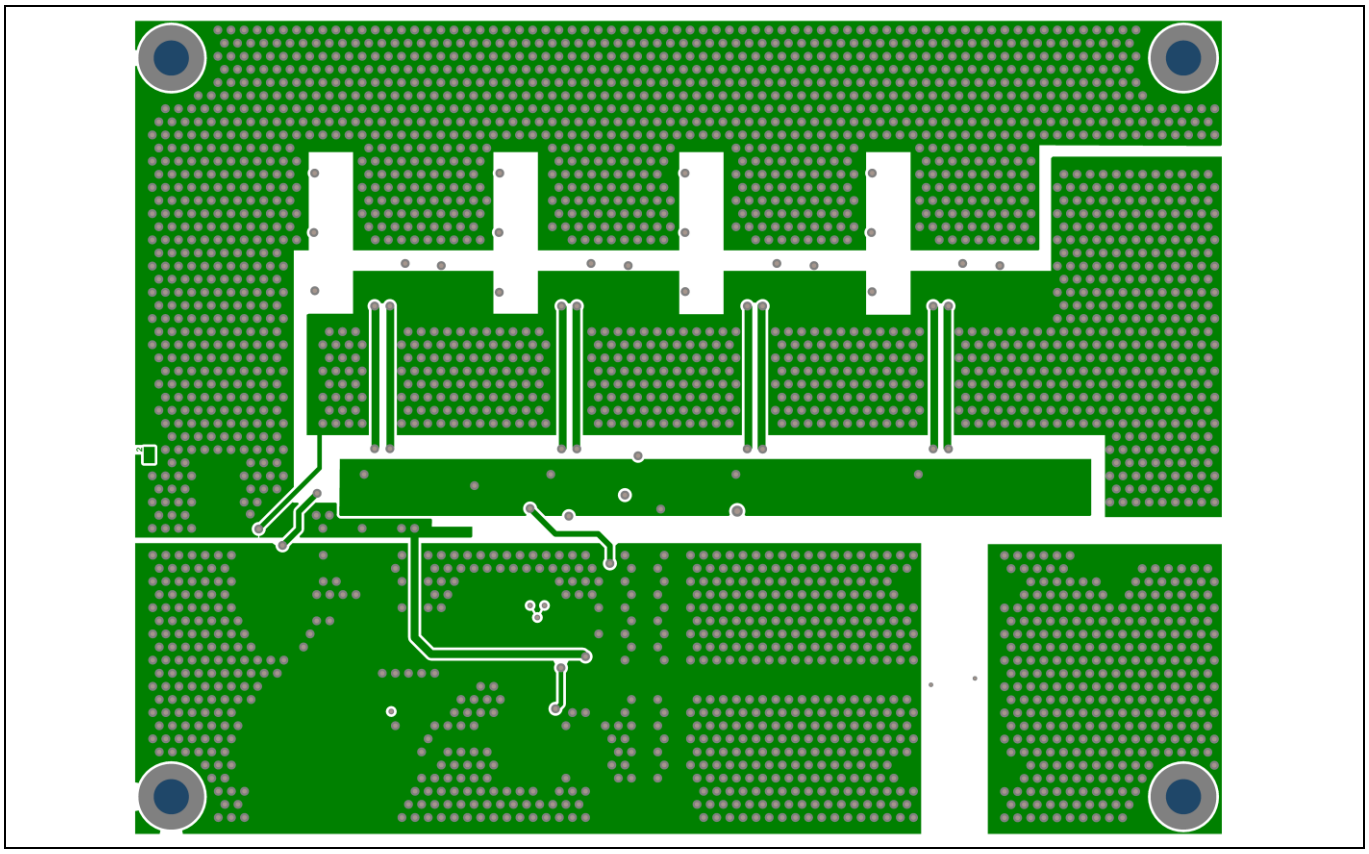


Figure 46 Main board middle layer 1

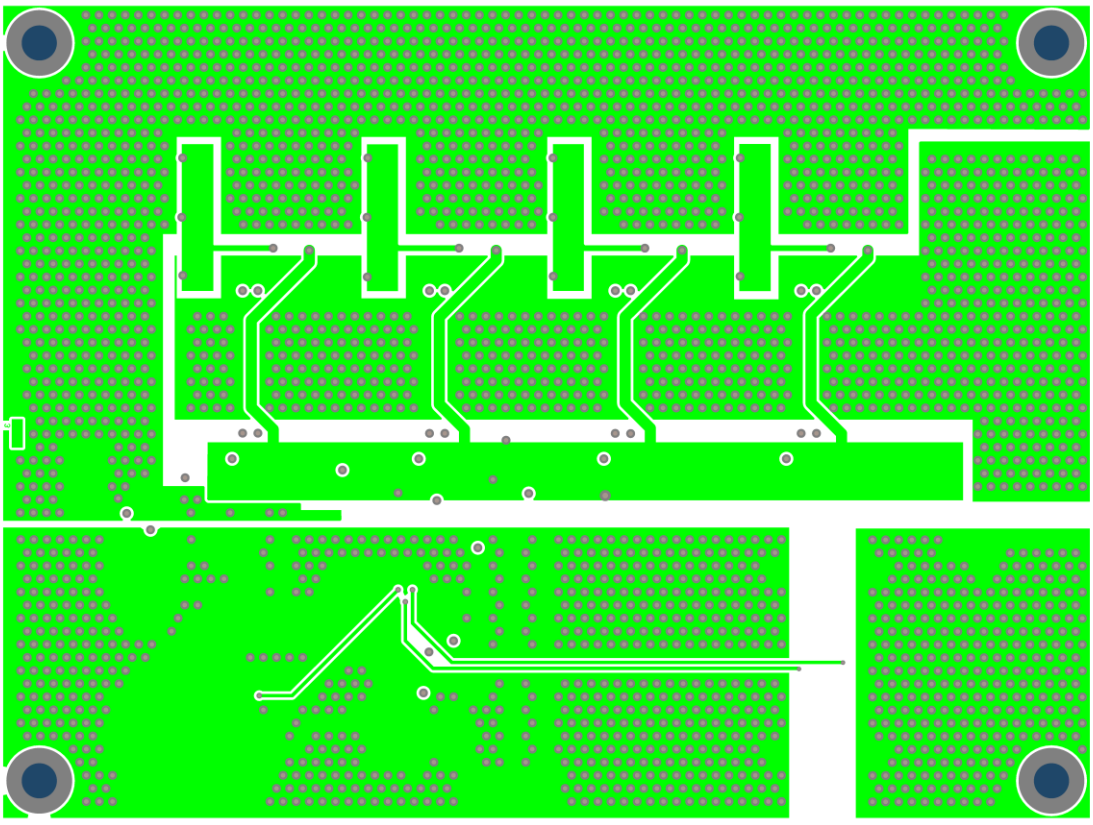


Figure 47 Main board middle layer 2

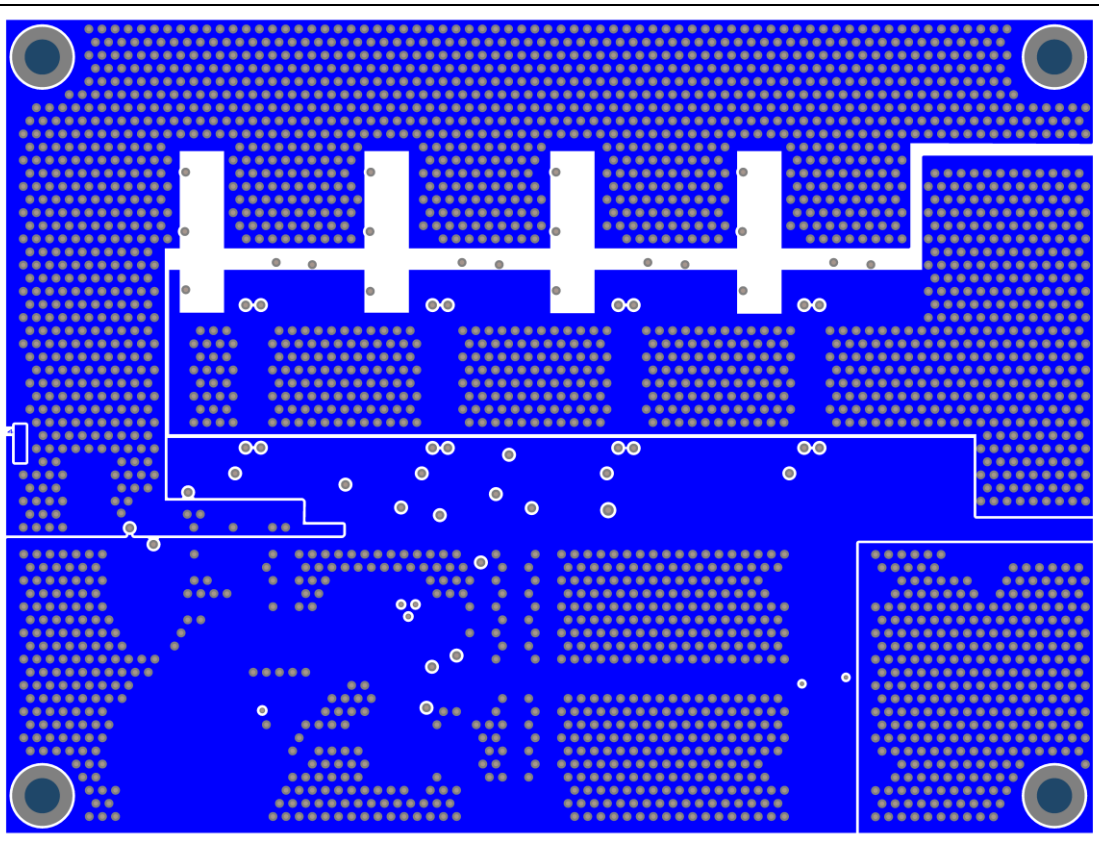


Figure 48 Main board bottom layer

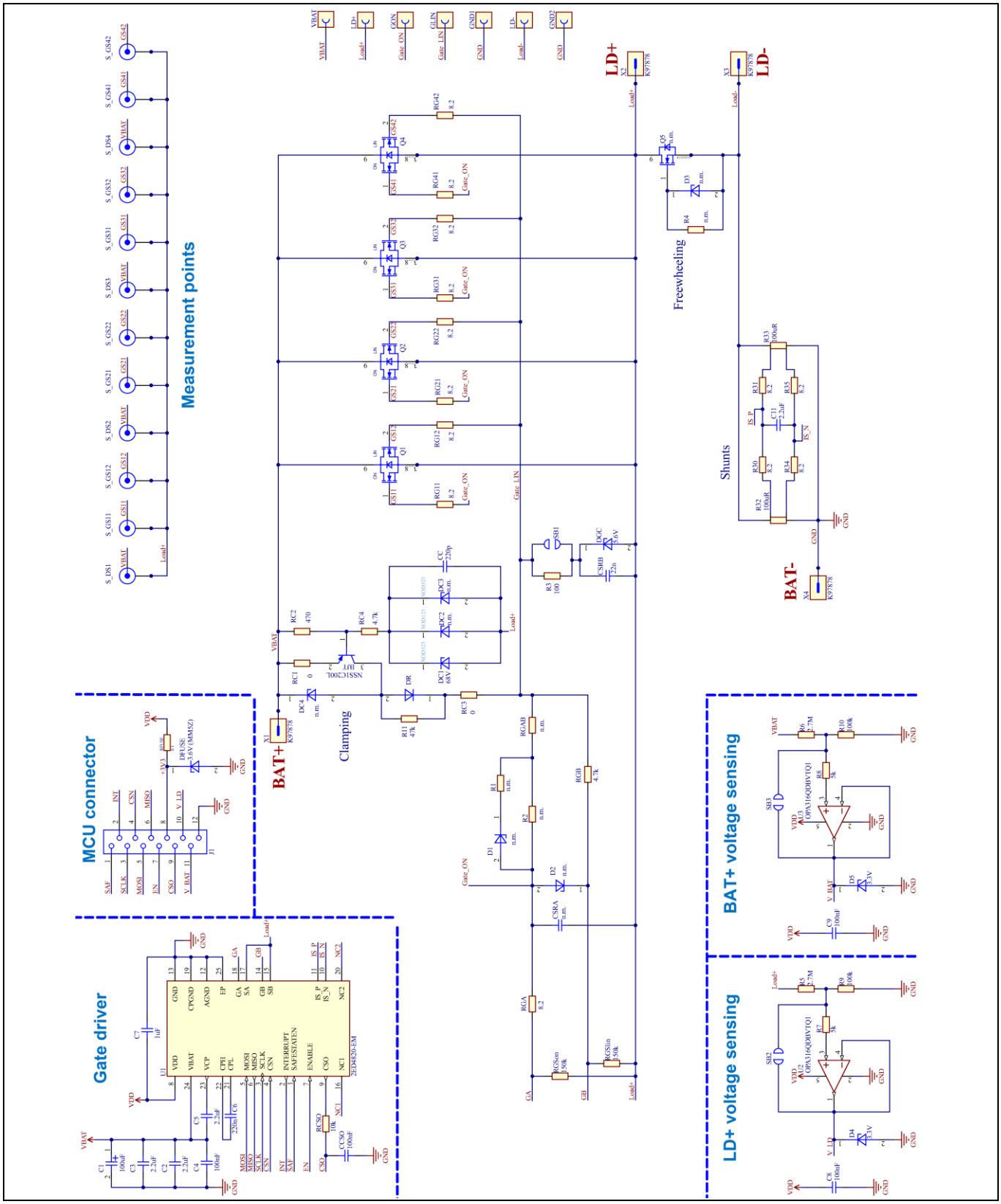


Figure 49 Main board schematic

4.12 Board stack and thermal design

- Board with thickness 1.55 mm (FR4) and four copper layers, each with 70 µm thickness.
- FR4 filled vias (0.4 mm hole diameter) with cap at top and bottom connected to each copper layer.
- Copper pieces (15 mm x 10 mm x 3 mm) coated with tin for better solderability.
- Passive coolant SK 81/75/SA (100 mm x 75 mm x 15 mm) connected via thermal foil BOYD BCTIM-210-1076 / BGDX8 (alternative: BGDX20).

The use of copper bar pieces offers a cost-effective alternative to PCB copper or aluminum cores, while still providing enhanced current carrying capacity and thermal cooling capabilities. Additionally, the copper bar pieces facilitate improved heat dissipation and reduce self-heating generated by the board itself. By utilizing individual pieces rather than a single long copper bar, the risk of board bending during the soldering process is significantly minimized.

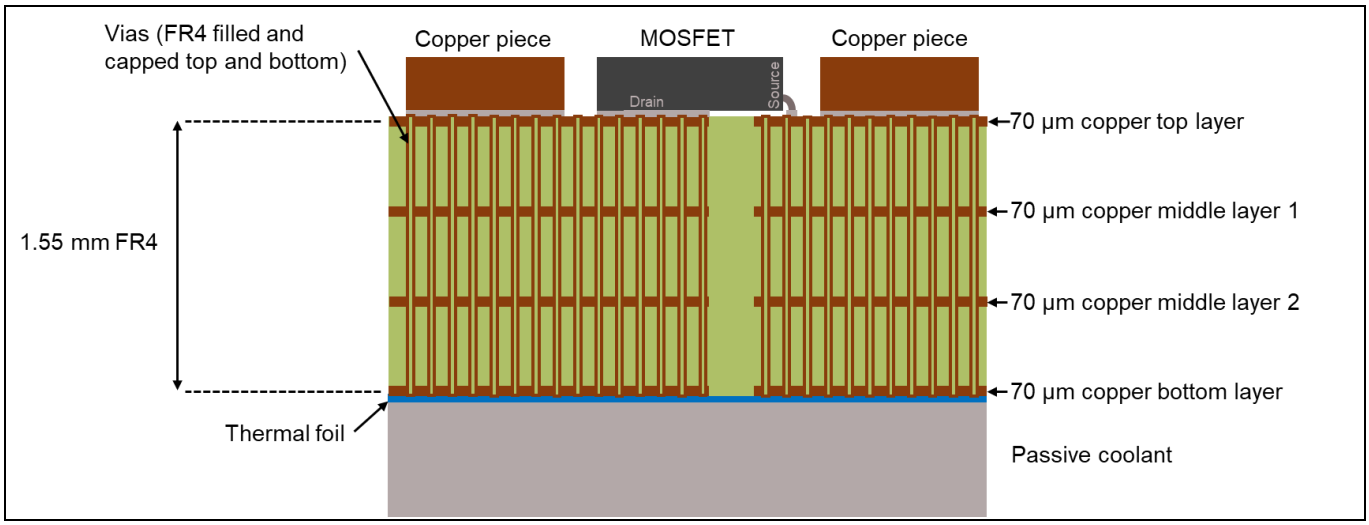


Figure 50 Dual Gate MOSFET main board material stack

4.13 Thermal performance

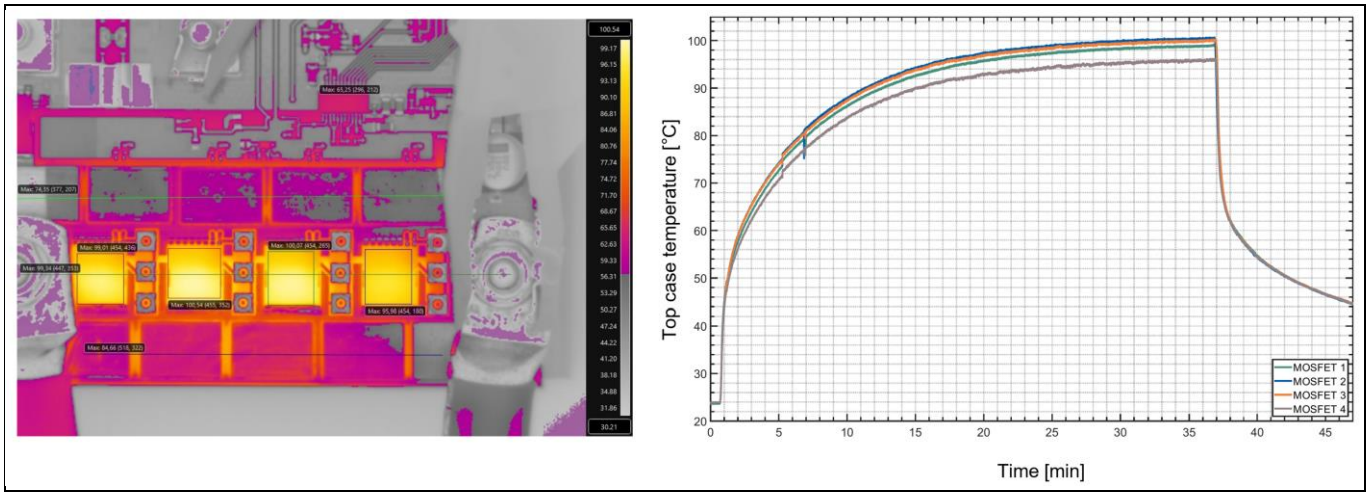


Figure 51 Thermal camera measurement for 35 minutes with 250 A load at T_a = 25°C

4.14 Adapter board layout and schematic

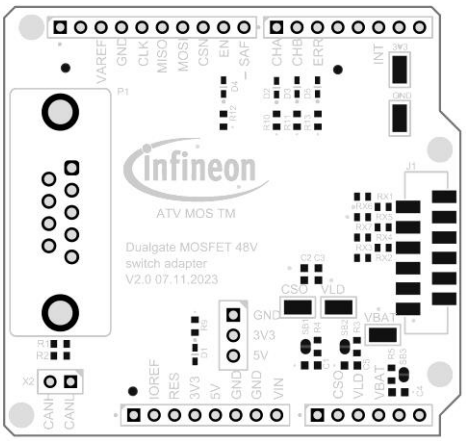


Figure 52 Adapter board component placement (top layer)

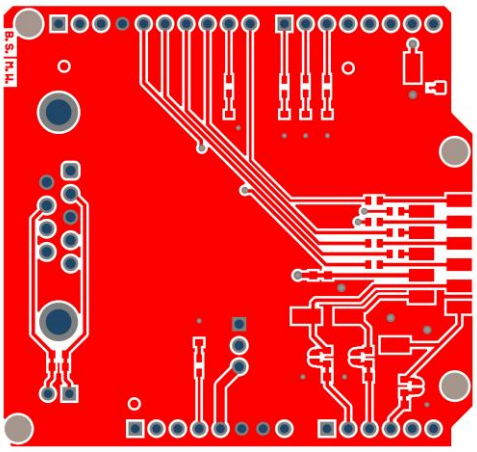


Figure 53 Adapter board top layer

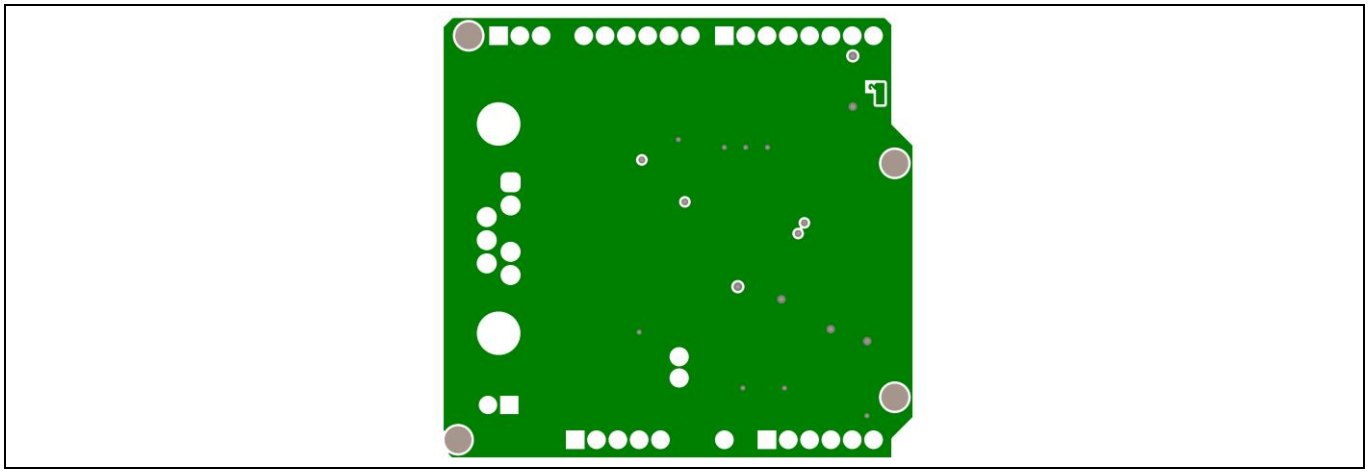


Figure 54 Adapter board middle layer 1

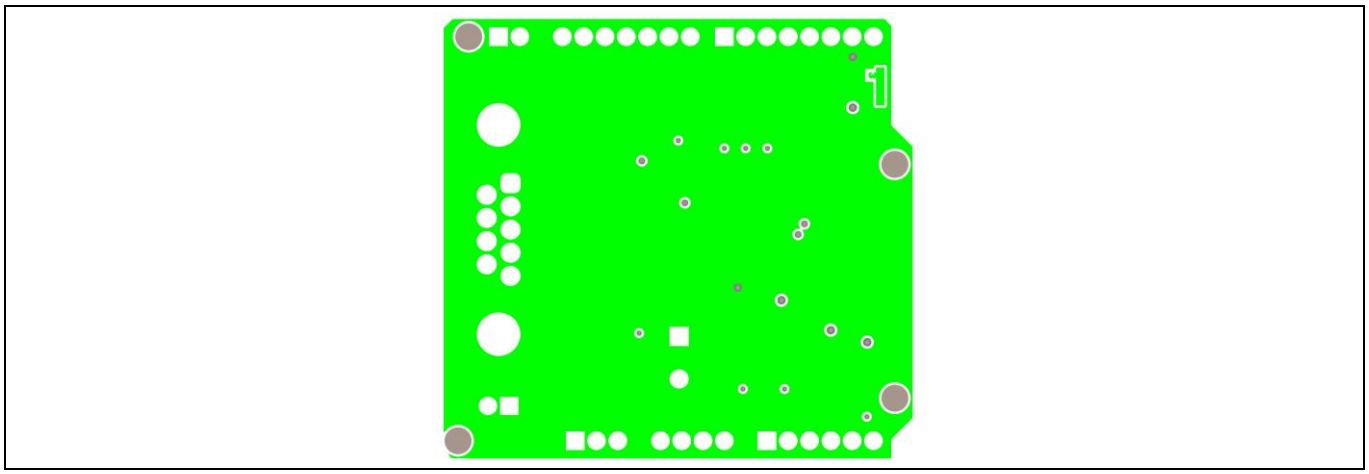


Figure 55 Adapter board middle layer 2

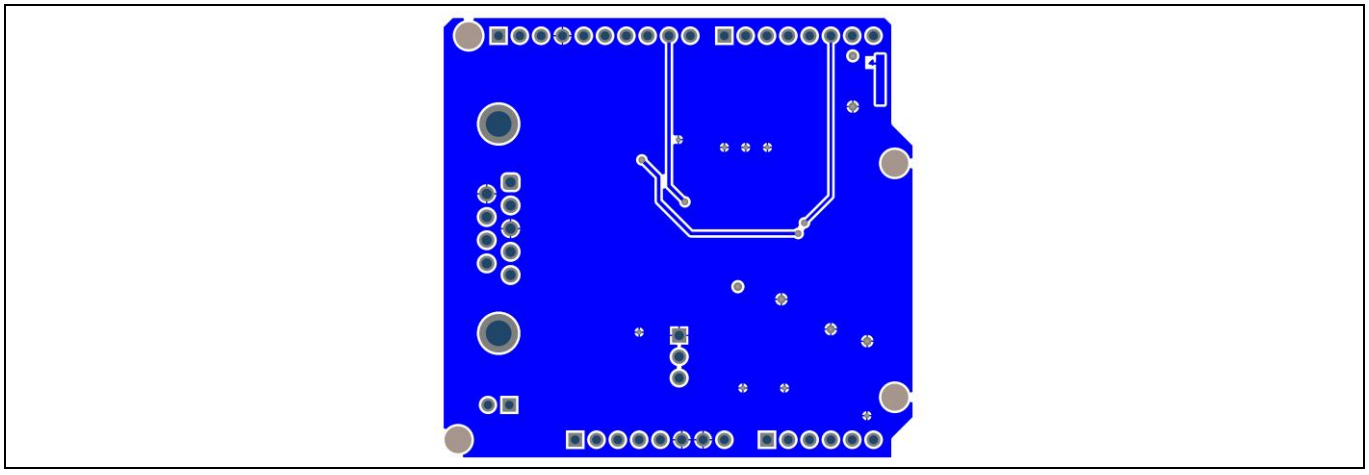


Figure 56 Adapter board bottom layer

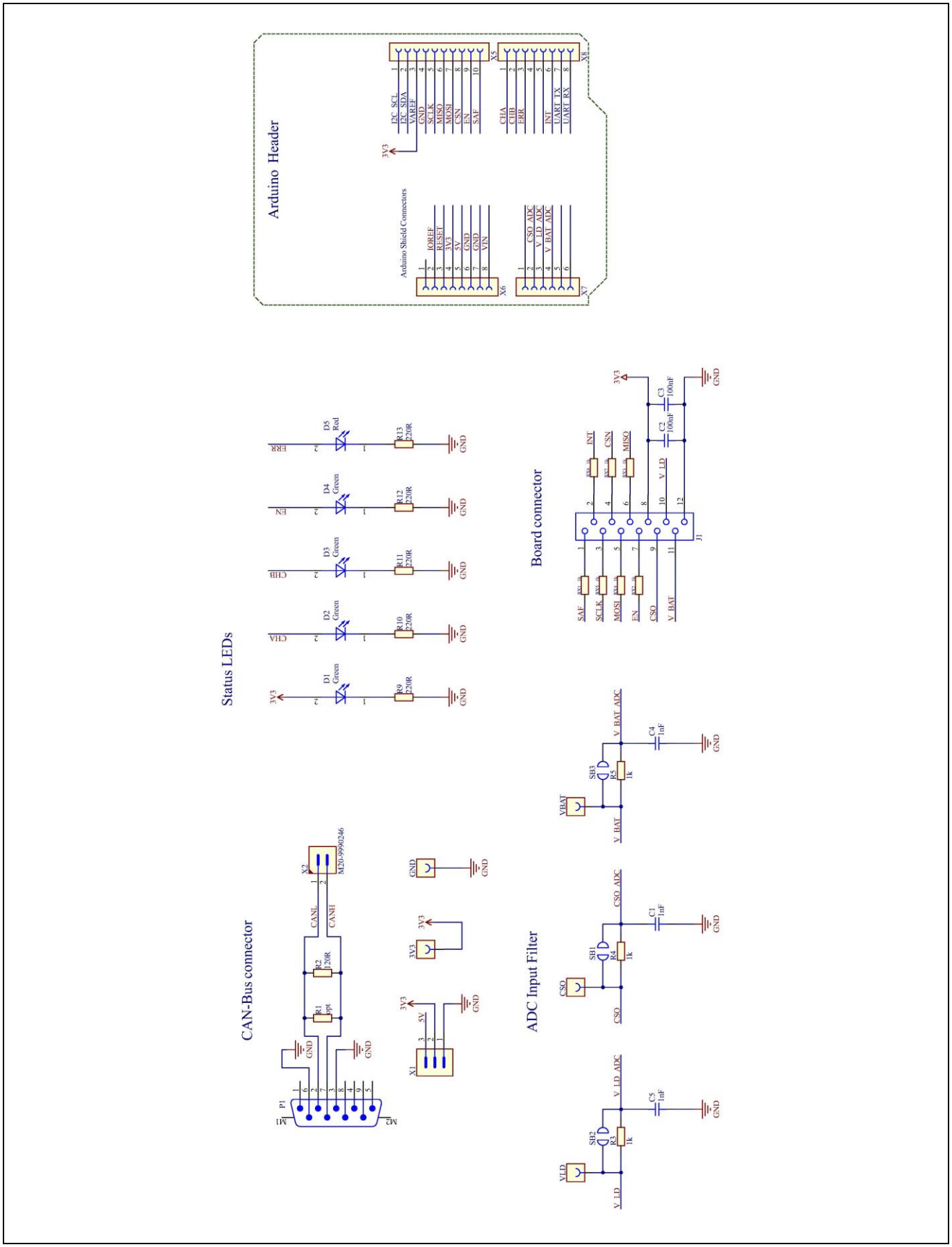


Figure 57 Adapter board schematic

Revision history

Document version	Date of release	Description of changes
V 1.00	08.02.2024	Initial application note
V 1.10	21.02.2024	Added chapter, which provides recommendations for appropriate zener diodes in clamping circuits and update of board bill of materials.
V 2.0	24.09.2024	New board version 2.2 with updated BJT active clamp circuit for improved zener diode compatibility. Added chapters for Dual Gate main board stack and thermal performance.

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Edition 2024-09-24

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
Z8F80559829

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