

ESD145-B1-W01005

Bi-directional ESD protection device, 18 V, 0.2 pF, 01005



Product description

This Infineon ESD (electrostatic discharge) protection device has a bi-directional and symmetric I/V characteristic and excellent clamping performance.

Feature list

- ESD / transient protection according to:
 - IEC61000-4-2 (ESD): ± 18 kV (air) / ± 18 kV (contact)
 - IEC61000-4-4 (EFT): ± 2.5 kV / ± 50 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 3.5 A (8/20 μ s)
- Bi-directional maximum working voltage: $V_{WM} = \pm 18$ V
- Line capacitance: $C_L = 0.2$ pF at $f = 1$ MHz
- Clamping voltage: $V_{cl} = 12.5$ V at $I_{TLP} = 16$ A with $R_{dyn} = 0.58 \Omega$
- Very low reverse current: $I_R < 1$ nA
- Small form factor SMD size 01005, low profile (0.43 x 0.23 x 0.15 mm³)



Potential applications

- NFC, RF Antenna

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

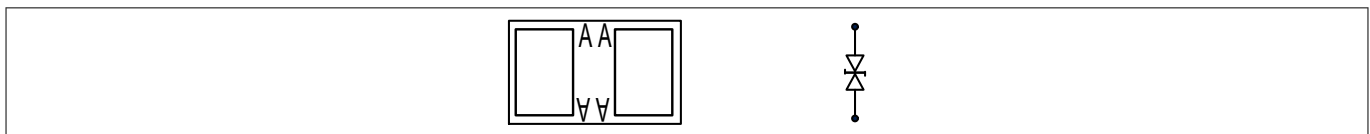


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

| Product name / Ordering code | Package | Pin configuration | Marking | Pieces / Reel |
|---|---------|------------------------|---------|---------------|
| ESD145-B1-W01005/ ESD145B1W01005E6327XTSA1 | WLL-2-2 | 1 line, bi-directional | AA | 15 k |

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1 Absolute maximum ratings

1 Absolute maximum ratings

Table 2 Absolute maximum ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | Unit | Note or test condition |
|-------------------------------|---------------------|--------|------|------|---|
| | | Min. | Max. | | |
| Working voltage ¹⁾ | V_{WM} | -18 | +18 | V | |
| ESD discharge voltage | V_{ESD} (contact) | -18 | +18 | kV | Discharge network: $R = 330 \Omega$, $C = 150 \text{ pF}$ ²⁾ |
| | V_{ESD} (air) | -18 | +18 | | |
| Peak pulse power | P_{PK} | - | 21 | W | Stress pulse: 8/20 μs current waveform ³⁾ |
| Peak pulse current | I_{PP} | -3.5 | +3.5 | A | |
| Operating temperature | T_{op} | -55 | +125 | °C | |
| Storage temperature | T_{stg} | -65 | +150 | | |

Attention: *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.*

¹⁾ Device snaps back to a low holding voltage, refer to application note [AN525](#) for latch-up prevention.

²⁾ Based on IEC61000-4-2.

³⁾ Based on IEC61000-4-5.

2 Electrical characteristics

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Note: $T_A = 25^\circ\text{C}$, unless otherwise specified. Device is electrically symmetrical.

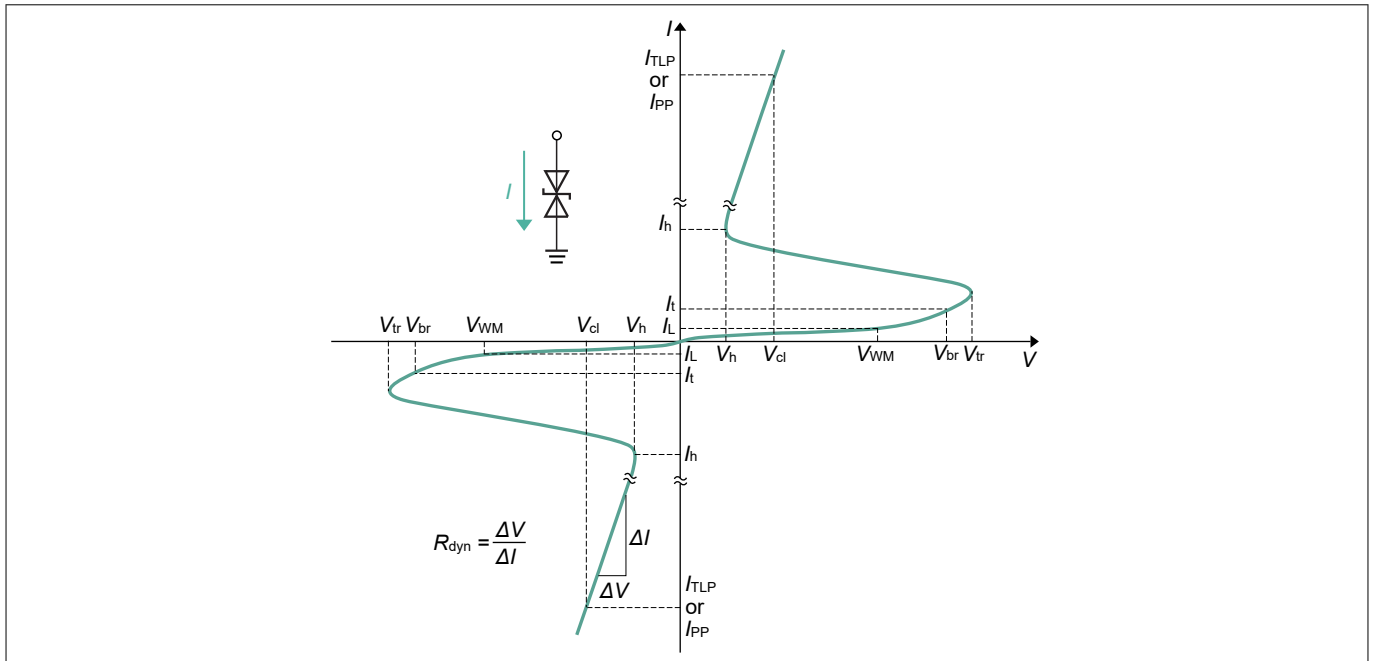


Figure 2 I/V characteristic curve

Table 3 I/V characteristic parameters

| Symbol | Parameter |
|-----------|---|
| I_h | Holding current |
| I_L | Leakage current |
| I_{PP} | Peak pulse current, based on IEC61000-4-5 |
| I_t | Test current |
| I_{TLP} | TLP current |
| R_{dyn} | Dynamic resistance |
| V_{br} | Breakdown voltage |
| V_{cl} | Clamping voltage |
| V_h | Holding voltage |
| V_t | Test voltage |
| V_{tr} | Trigger voltage |
| V_{WM} | Maximum working voltage |

Note: For more detailed explanation of electrical parameters, refer to [1].

2 Electrical characteristics

Table 4 DC characteristics

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|-------------------|----------|--------|------|------|------|-------------------------|
| | | Min. | Typ. | Max. | | |
| Breakdown voltage | V_{br} | 18.5 | 22 | 28.5 | V | $I_t = 1 \text{ mA}$ |
| Holding voltage | V_h | – | 1.9 | – | | $I = I_h$ |
| Holding current | I_h | – | 25 | – | mA | $V = V_h$ |
| Leakage current | I_L | – | – | 50 | nA | $V_{WM} = 18 \text{ V}$ |

Table 5 AC characteristics

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|-------------------|--------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Line capacitance | C_L | – | 0.2 | 0.35 | pF | $V = 0 \text{ V}, f = 1 \text{ MHz}$ |
| | | – | 0.18 | – | | $V = 0 \text{ V}, f = 2.5 \text{ GHz}$ |
| Series inductance | L_S | – | <1 | – | nH | Extracted from S-parameters |

Table 6 Protection characteristics

| Parameter | Symbol | Values | | | Unit | Note or test condition |
|--|-----------|--------|------|------|----------|--------------------------|
| | | Min. | Typ. | Max. | | |
| Clamping voltage (TLP) ^{4) 5)} | V_{cl} | – | 8 | – | V | $I_{TLP} = 8 \text{ A}$ |
| | | – | 12.5 | – | | $I_{TLP} = 16 \text{ A}$ |
| Clamping voltage (8/20 μs) ⁶⁾ | | – | 3 | – | | $I_{PP} = 1 \text{ A}$ |
| | | – | 5 | – | | $I_{PP} = 3 \text{ A}$ |
| Dynamic resistance ⁴⁾ | R_{dyn} | – | 0.58 | – | Ω | |

⁴⁾ TLP parameters: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$, averaging window 30-60 ns.

⁵⁾ Refer to application note AN210 [2]

⁶⁾ $t_p = 8/20 \mu\text{s}$. Stress pulse based on IEC61000-4-5.

3 Typical characteristic diagrams

3 Typical characteristic diagrams

Note: $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

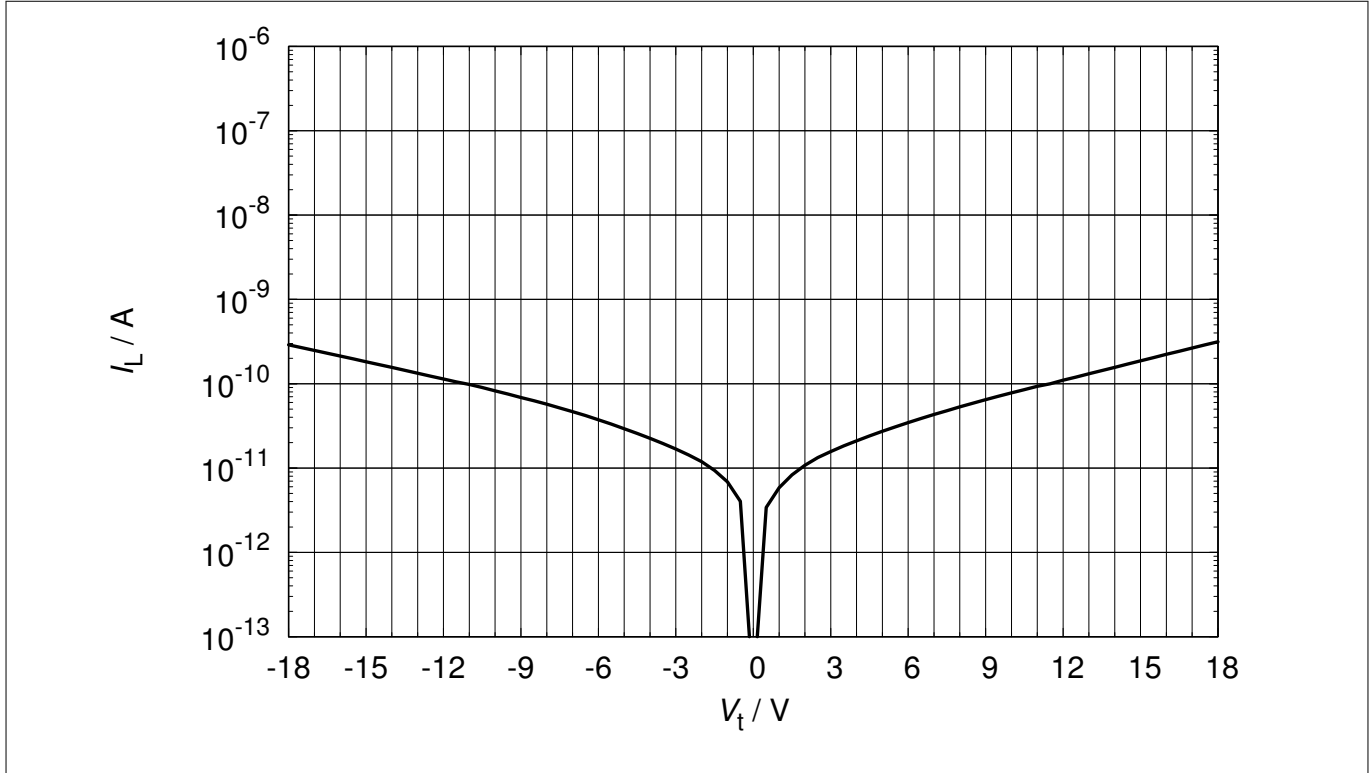


Figure 3 Leakage current: $I_L = f(V_t)$

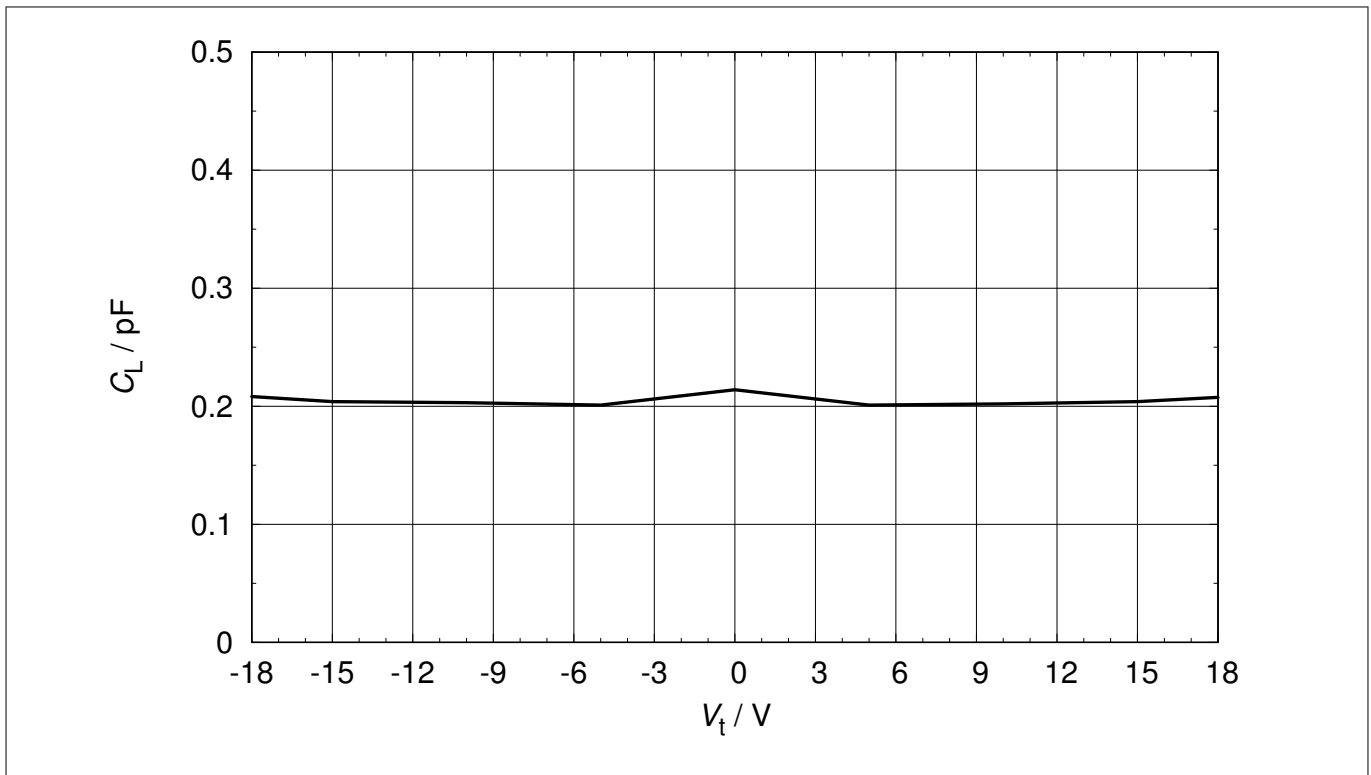


Figure 4 Line capacitance: $C_L = f(V_t)$, $f = 1\text{ MHz}$

3 Typical characteristic diagrams

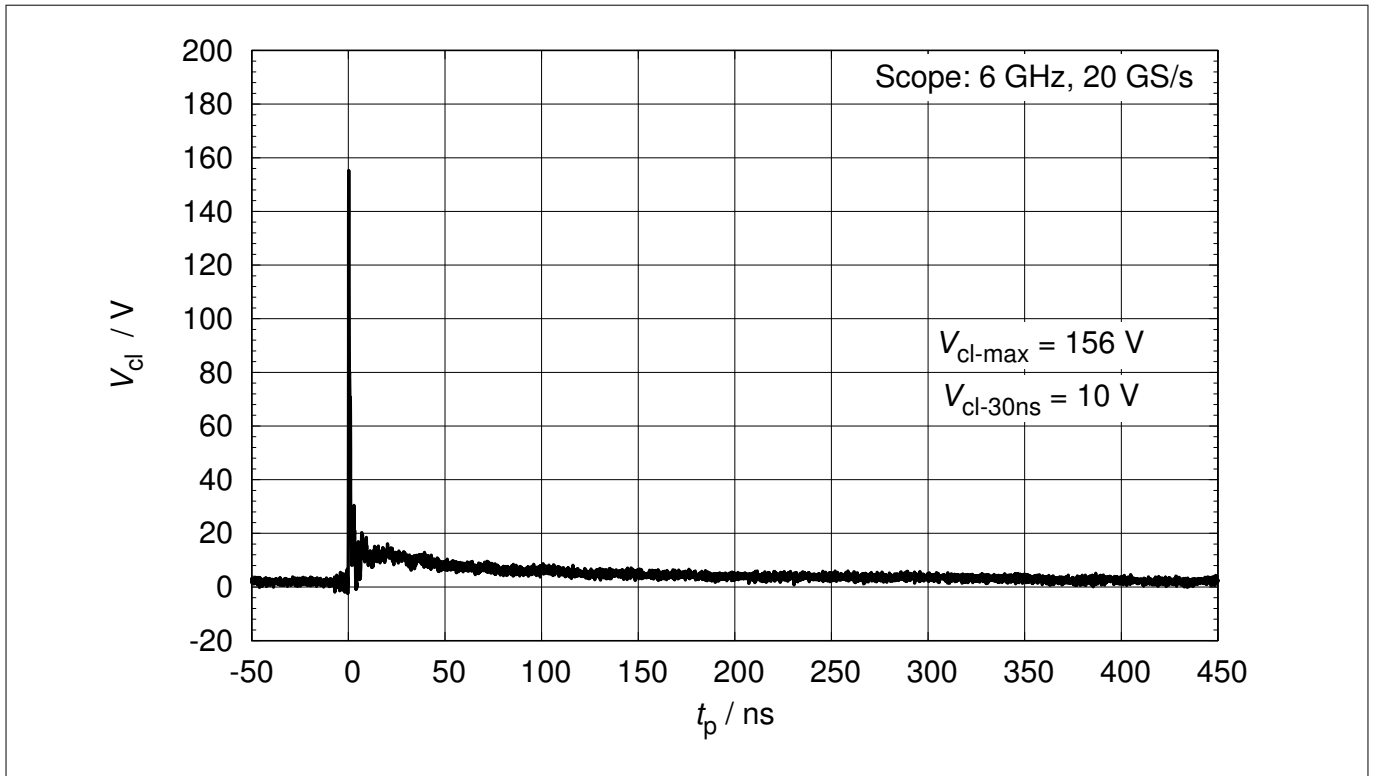


Figure 5 Clamping voltage (ESD): $V_{cl} = f(t_p)$, 8 kV positive pulse according to IEC61000-4-2

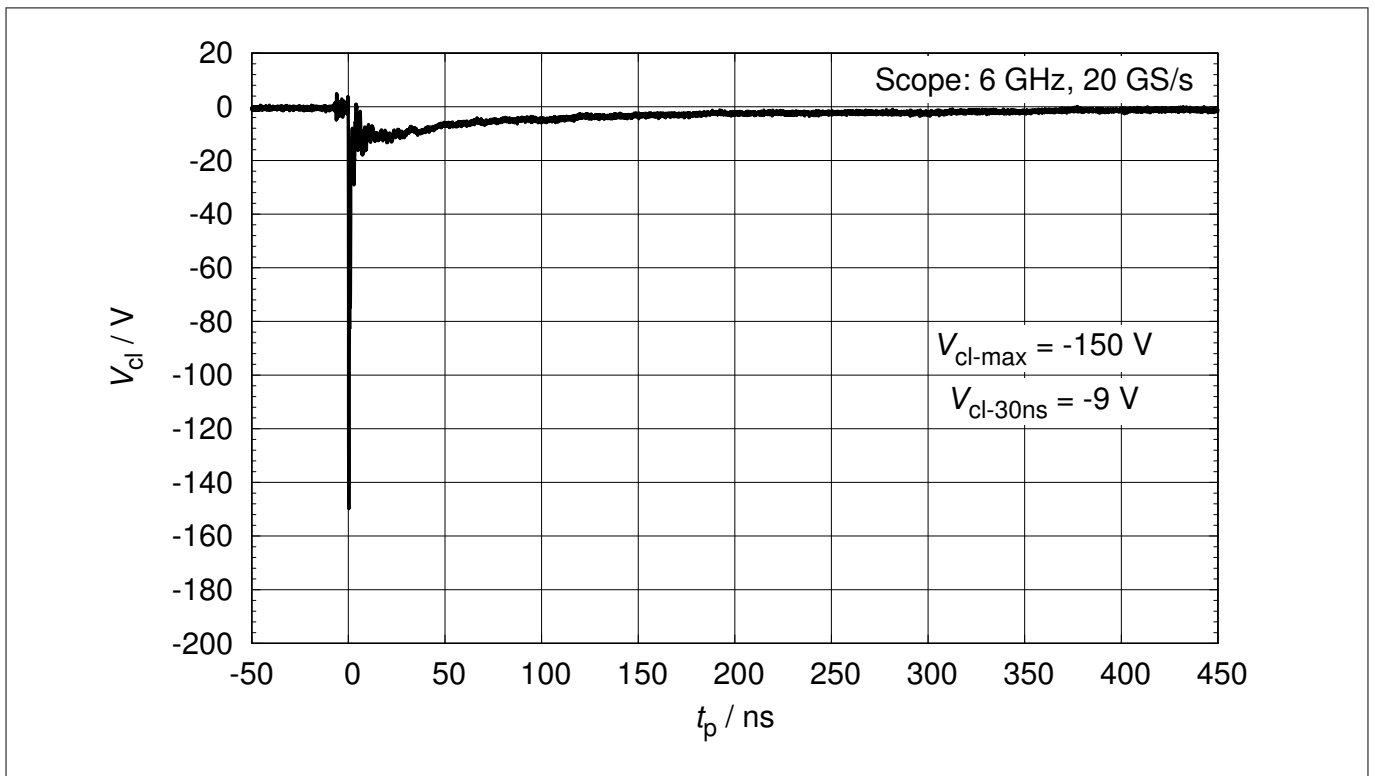


Figure 6 Clamping voltage (ESD): $V_{cl} = f(t)$, 8 kV negative pulse according to IEC61000-4-2

3 Typical characteristic diagrams

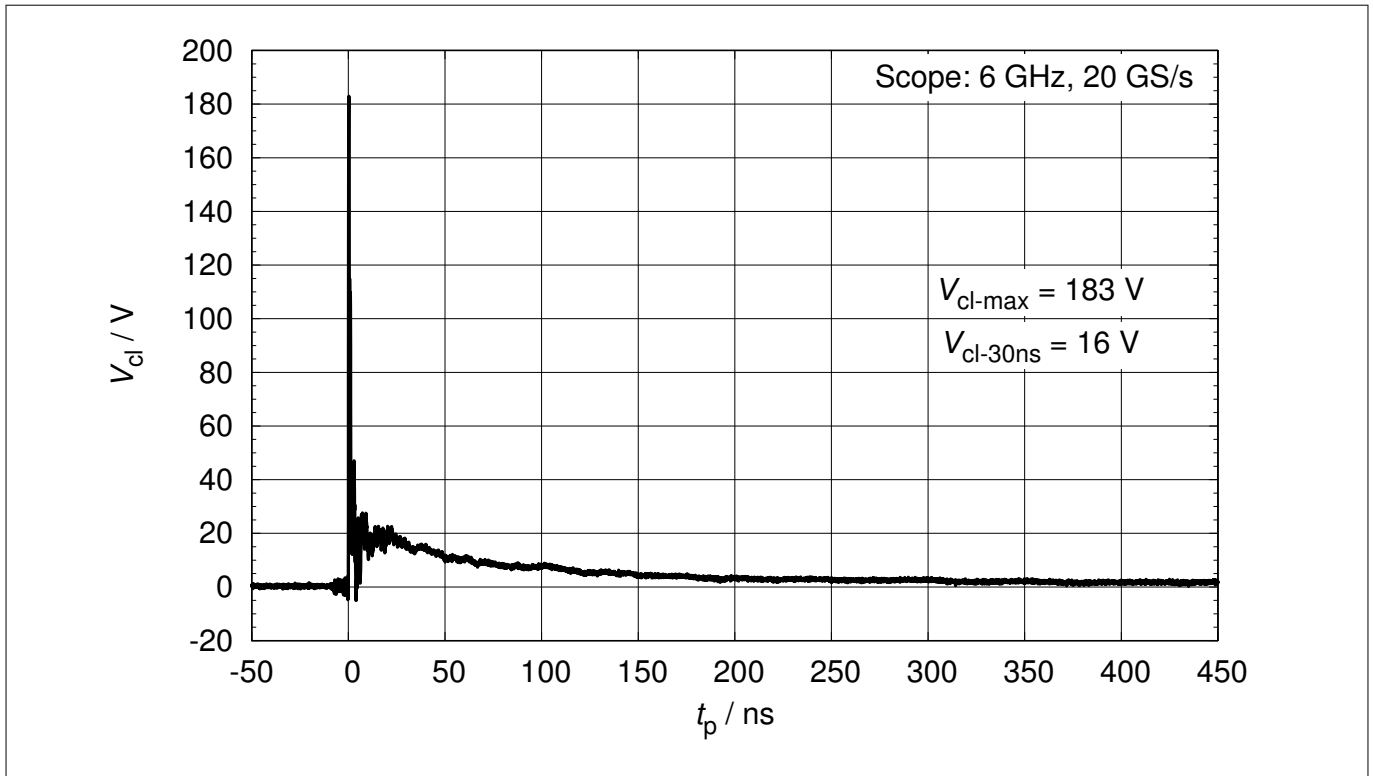


Figure 7 Clamping voltage (ESD): $V_{cl} = f(t)$, 15 kV positive pulse according to IEC61000-4-2

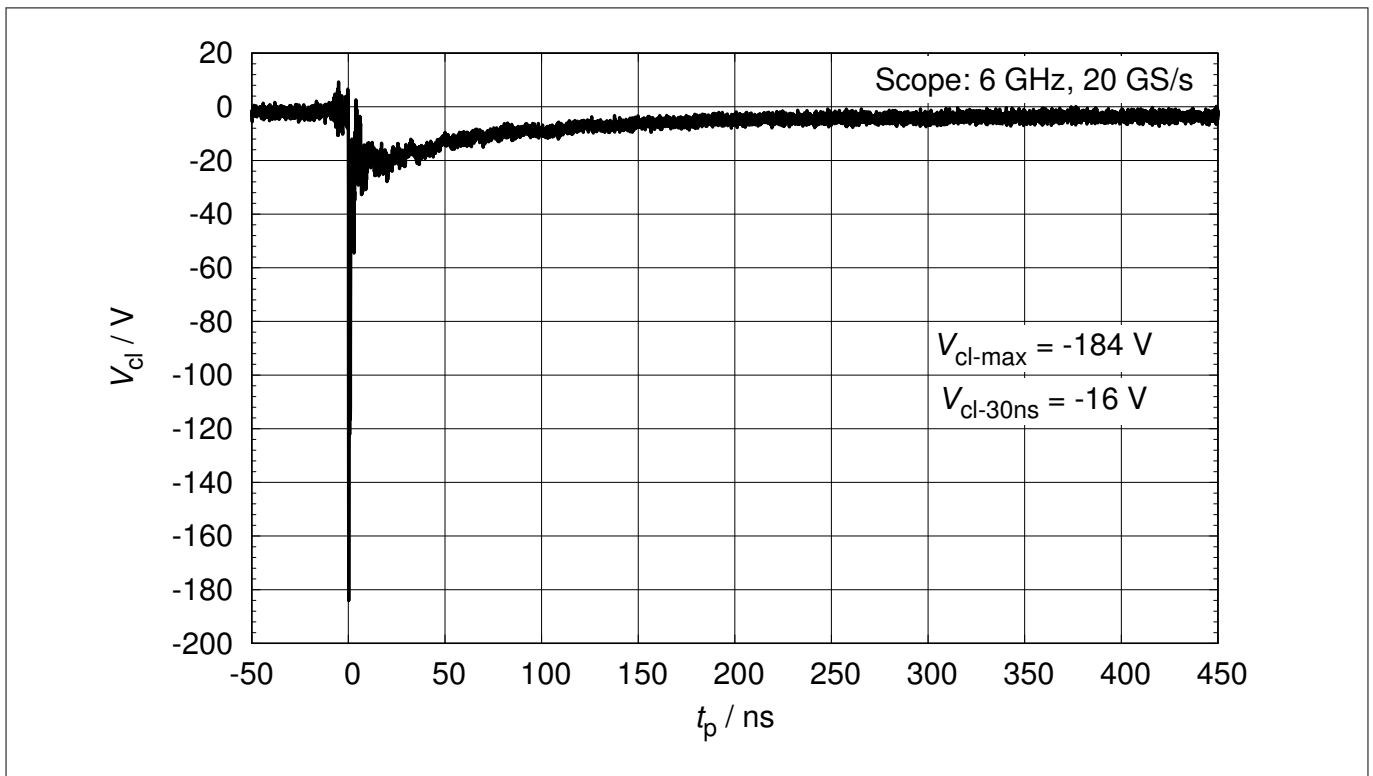


Figure 8 Clamping voltage (ESD): $V_{cl} = f(t)$, 15 kV negative pulse according to IEC61000-4-2

3 Typical characteristic diagrams

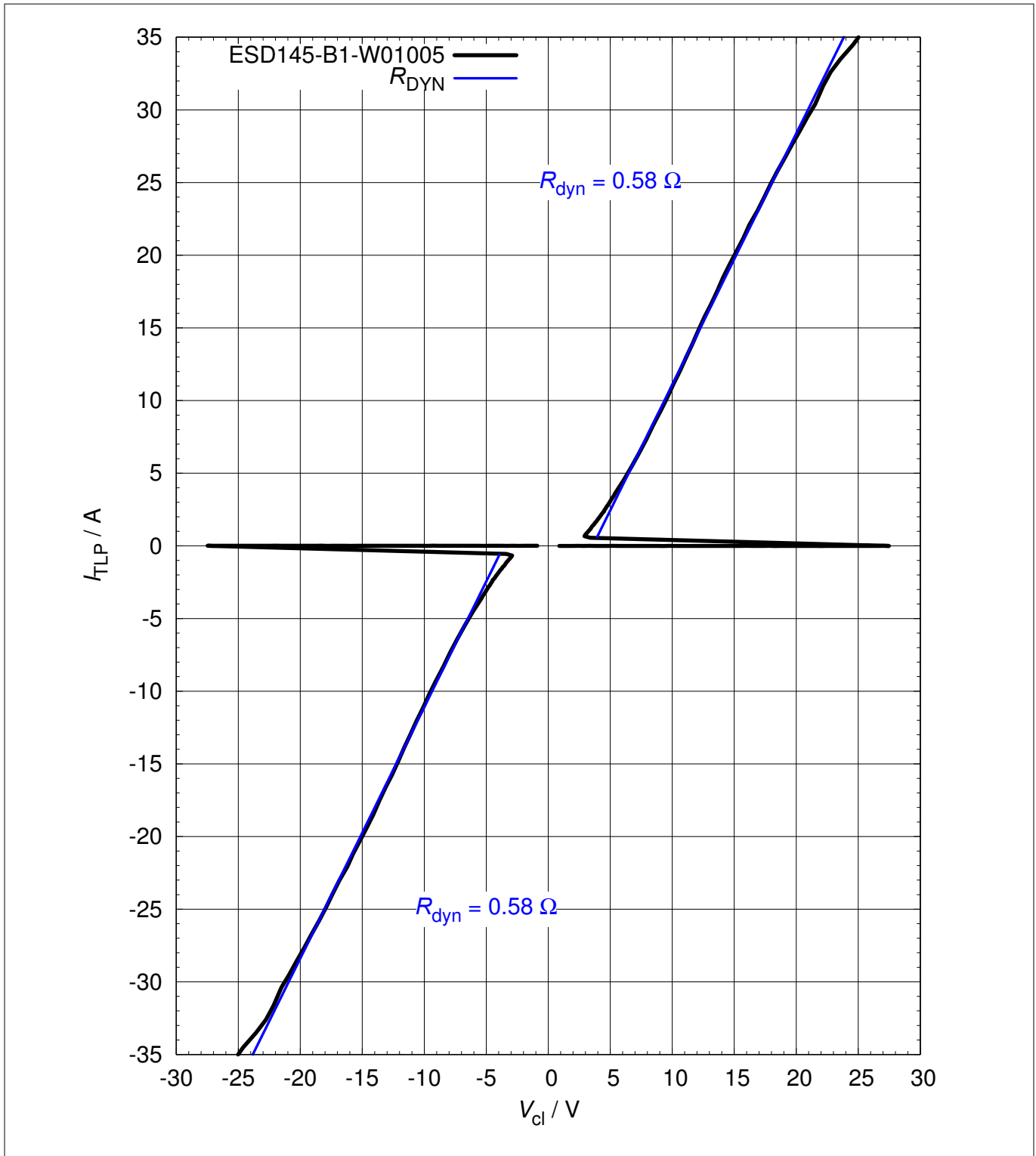


Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$

3 Typical characteristic diagrams

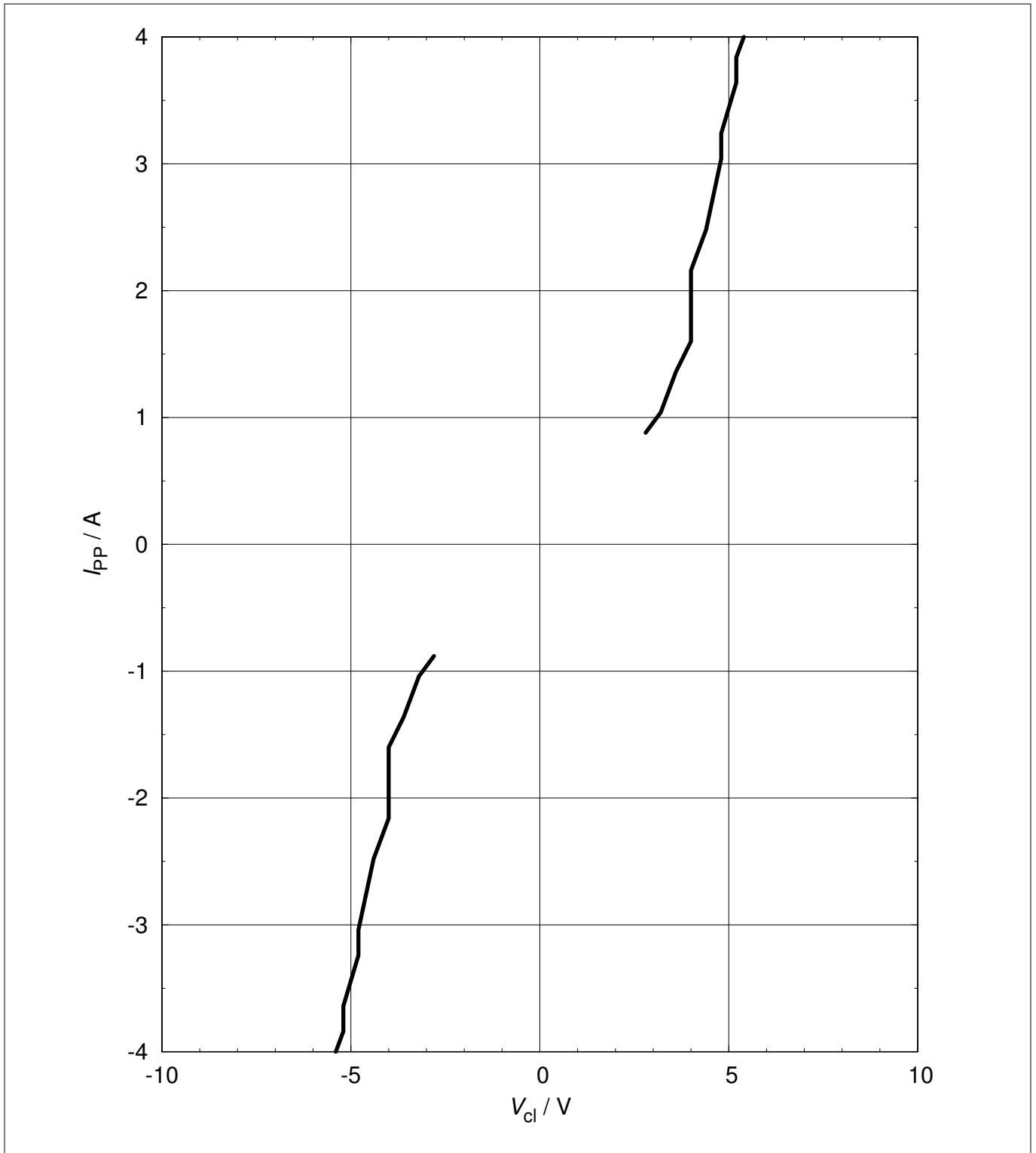


Figure 10 Clamping voltage (Surge): $I_{PP} = f(V_{Cl})$ according to IEC61000-4-5

3 Typical characteristic diagrams

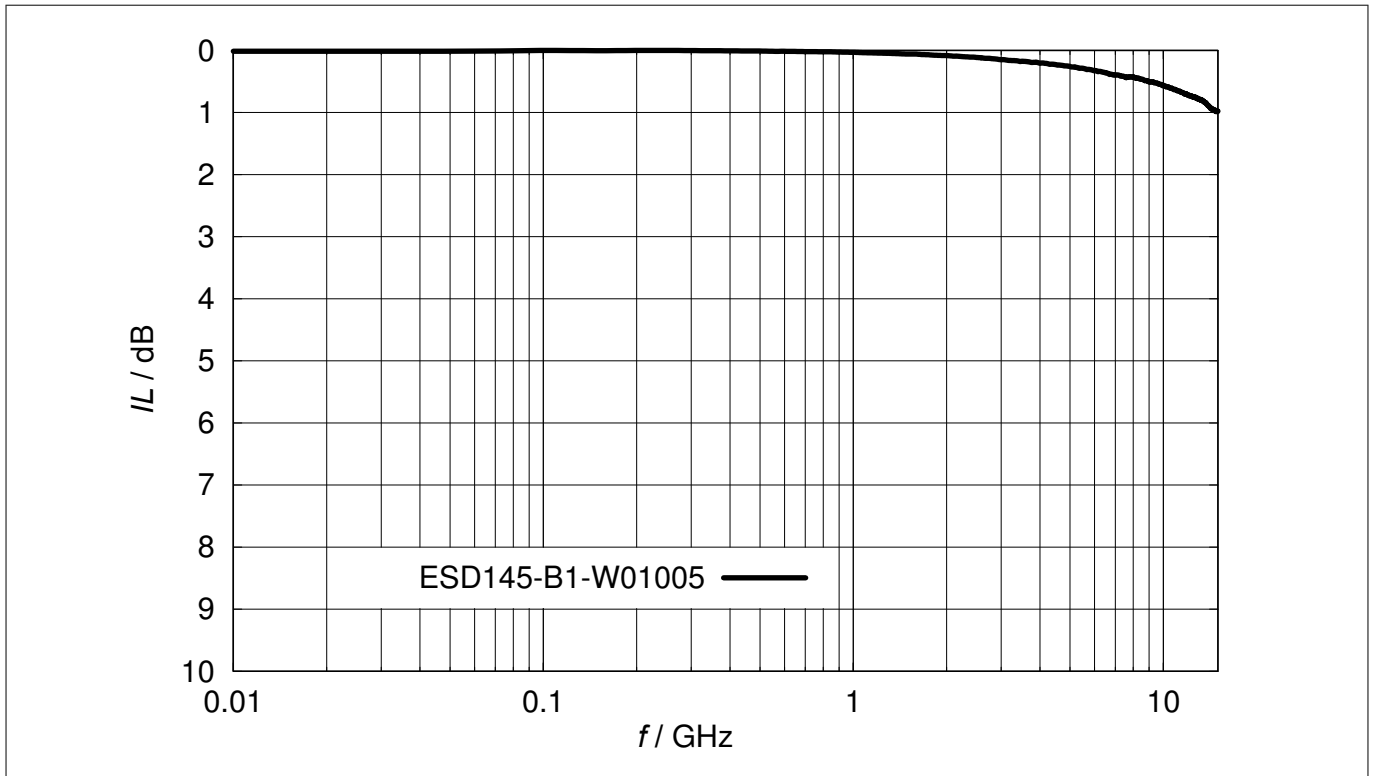


Figure 11 Insertion loss vs. frequency in 50 Ohm system

4 Package information WLL-2-2

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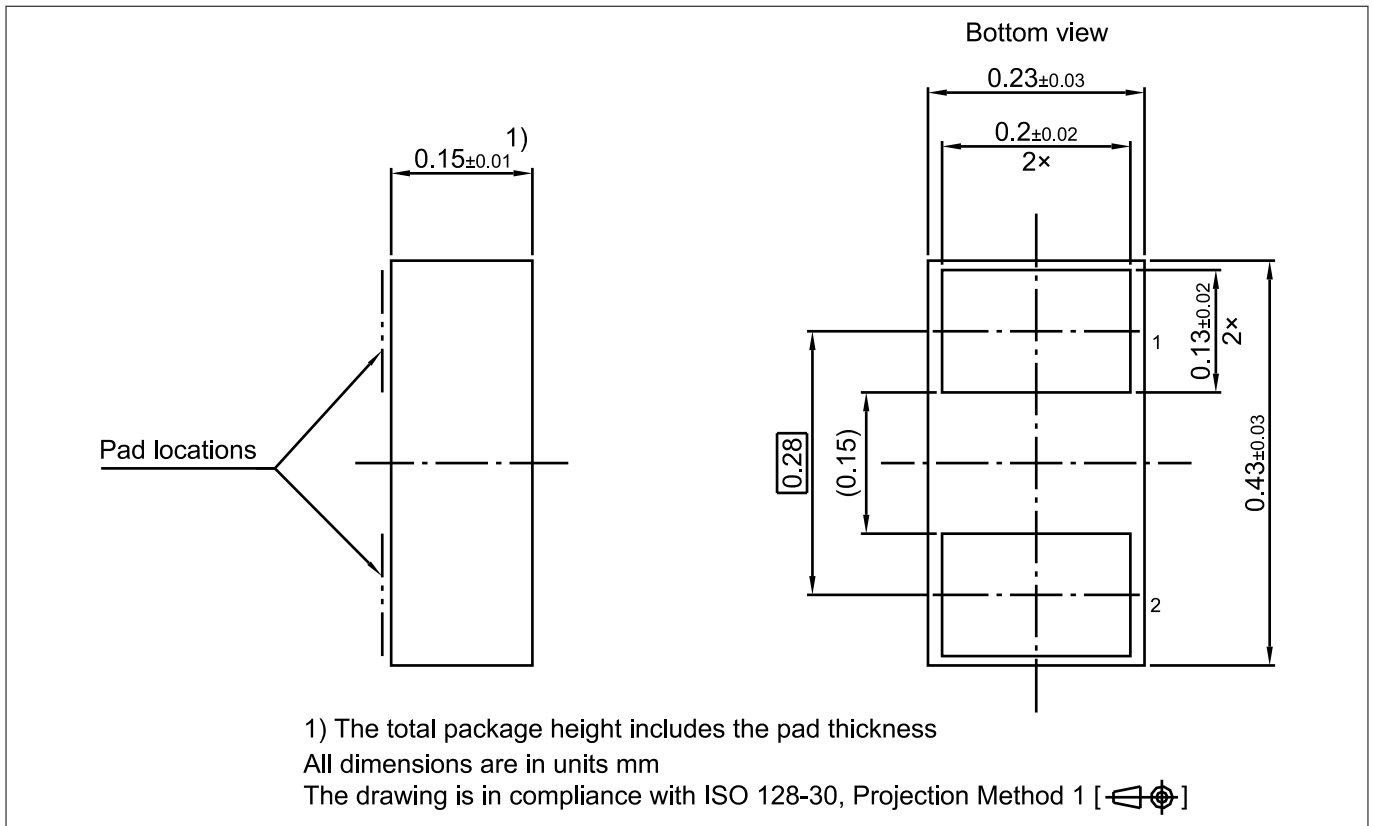


Figure 12 WLL-2-2 package

Note: For package information including footprint, packing and assembly recommendation refer to:

<https://www.infineon.com/cms/en/product/packages/SG-WLL/SG-WLL-2-2/>

5 References

5 References

| | |
|-----|---|
| [1] | Infineon AG - Understanding ESD protection device characteristics |
| [2] | Infineon AG - Application note AN210 : Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology |

6 Revision history

| Document version | Date of release | Description of changes |
|-------------------------|------------------------|--|
| 1.0 | 2017-08-14 | <ul style="list-style-type: none">• First final datasheet release |
| 2.0 | 2020-11-30 | <ul style="list-style-type: none">• New datasheet layout• Editorial changes |
| 2.1 | 2024-01-05 | <ul style="list-style-type: none">• Added link to application note in Table 2 |

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