# EZ-USB™ FX5
USB 5Gbps peripheral controller

Infineon

USB 5Gbps to high-bandwidth LVDS/LVCMOS data interface with dual-core ARM® Cortex® CPU and direct USB-C support

Infineon's EZ-USB™ FX5 extends the legacy of EZ-USB™ FX3, the industry's gold standard for USB peripheral controller, with faster GPIF and LVDS interfaces increasing the total bandwidth to max out USB 5 Gbps.

The EZ-USB™ FX5 is a family of USB 5Gbps peripheral controllers targeting the next-generation USB applications in camera, video, imaging, and data acquisition markets. EZ-USB™ FX5 consists of dual ARM® Cortex®-M4 and M0+ core CPUs, a 512 KB flash, an 128 KB SRAM, an 128 KB ROM, seven serial communication blocks (SCBs), a cryptography accelerator, and a high bandwidth data subsystem providing DMA data transfers between LVDS/LVCMOS and USB ports at speeds up to 5 Gbps. An additional 1 MB SRAM is included in the high bandwidth data subsystem to provide buffering for USB data. EZ-USB™ FX5 also supports USB Type-C plug orientation detection and flip-mux function without the need for external logic.
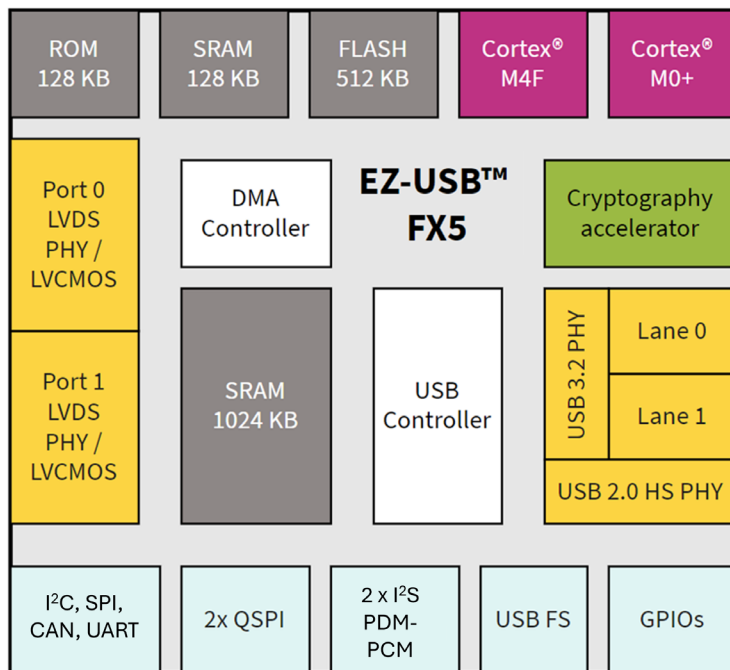
Key features

USB 3.2 Gen1 device port
- Integrated PHY: 5 Gbps, 480 Mbps
- USB-C plug orientation detection and correction

Dual-core CPU
- 150 MHz ARM® Cortex®-M4F
- 100 MHz ARM® Cortex®-M0+

Memory subsystem
- 512 KB flash
- 1024 KB + 128 KB SRAM

Dual-mode high bandwidth data interface
- LVDS / SubLVDS: up to 16 RX data lanes @1.25 Gbps
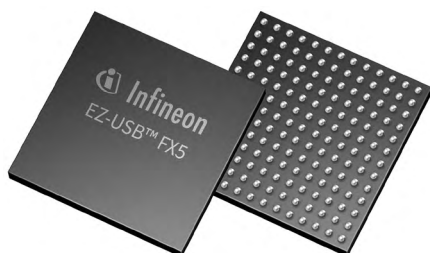- LVCMOS: up to 32-bit data bus @ 160 MHz DDR RX

Peripheral I/O ports
- 2x Quad-SPI (QSPI)
- 7 serial communication blocks (I²C, SPI, CAN, UART)
- USB full-speed (12 Mbps) device
- 2x I²S/PDM-PCM and GPIOs

Cryptography accelerator
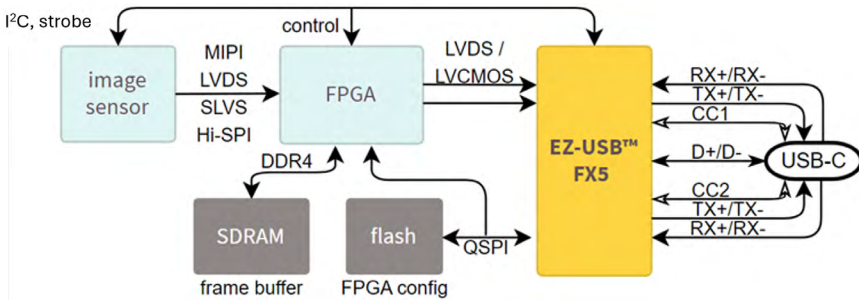**Package**
- 10 mm x 10 mm, 169-ball, 0.75 mm ball pitch

Application example: machine vision camera

The 5 Gbps performance allows uncompressed 4K videos to be transmitted at 30 frame-per-second. Both USB 5Gbps lanes of EZ-USB™ FX5 can be connected directly to a USB-C receptacle without a mux.

The controller can automatically detect the plug orientation, transfer data to the active lane, and correct the polarity of each USB 5Gbps differential pair.

An FPGA is connected between a high-speed image sensor and EZ-USB™ FX5 to perform image acquisition and processing, and transfers images to the controller via LVDS or LVCMOS connection. For LVDS mode, each lane can support up to 1.25 Gbps. For LVCMOS mode, the 32-bit data bus can deliver 10 Gbps throughput with DDR clocking. EZ-USB™ FX5 DMA fabric allows maximum USB 5Gbps bandwidth to be used with auto header and trailer insertion.

Key benefits

- Smaller PCB footprint and optimized BOM cost 10x10 BGA package
- USB-C direct connection without a high-speed signal mux
- Integrated FLASH
- Quick start development
- Firmware jumpstart with configuration utility
- USB Video Class, UVC, firmware ready
- USB3 Vision firmware ready
- DVK with standard FMC for quick connection to FPGA boards
- All-in-one programming and debugging accessory board
- Application notes for hardware and software

EZ-USB™ FX5 part detail

Part number	USB-C	LVDS	LVCMOS	QSPI	Crypto	FLASH [KB]	SRAM [KB]
CYUSB3081			✓			n/a	512 KB
CYUSB3082			✓			256 KB	512 KB
CYUSB3083	✓	✓	✓	✓		512 KB	1024 KB
CYUSB3084	✓	✓	✓	✓	✓	512 KB	1024 KB