EZ-USB™ HX3 Automotive USB 3.2 Gen 1 (5 Gbps) Hub

General description

EZ-USB™ HX3 Automotive is a family of USB 3.2 Gen 1 (5 Gbps) hub controllers compliant with the USB 3.1, Gen 1 specification. EZ-USB™ HX3 supports SuperSpeed (SS) (5 Gbps), High-speed (HS), Full-speed (FS), and Low-speed (LS) on all the ports. It has integrated termination, pull-up, and pull-down resistors, and supports configuration options through pin-straps to reduce the overall BOM of the system.

EZ-USB™ HX3 Automotive includes the following Infineon-proprietary features:

- **SEZ-USB™ HX3 with shared link feature:** Enables extra downstream (DS) ports for onboard connections in embedded applications.
- **EZ-USB™ HX3 with ghost charging:** Enables charging of devices connected to the DS ports when no host is connected on the upstream (US) port.

Features

- Automotive Electronics Council (AEC) Q100 qualified
- USB 3.1, Gen 1-Certified Hub, TID# 330000060
- Supports up to four USB 3.1, Gen1-compliant DS ports
  - All ports support SS (5 Gbps) and are backward-compatible with HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps)
  - SS and USB 2.0 link power management (LPM)
  - Dedicated Hi-Speed transaction Translators (Multi-TT)
  - LED status indicators – suspend, SS, and USB 2.0 operation
- Shared Link for embedded applications
  - Each DS port can simultaneously connect to an embedded SS device and a removable USB 2.0 device
  - Enables up to six device connections
- Enhanced battery charging
  - Each DS port complies with the USB Battery Charging v1.2 (BC v1.2) specification
  - Ghost Charge: Each DS port can emulate a Dedicated Charging Port (DCP) when the host is not connected to the US port
  - Accessory Charger Adapter Dock (ACA-Dock): Enables charging and simultaneous data transfer for a smart phone or a tablet acting as a host compliant to BC v1.2
  - Apple charging supported on all DS ports
- Integrated Arm® Cortex® -M0 CPU
  - 16-KB RAM, 32-KB ROM
  - Configure GPIOs for overcurrent protection, power enable, and LEDs
  - Upgrade firmware using I^2C EEPROM or an external I^2C master
- Vendor-command support to implement a USB-to-I^2C bridge
  - Firmware upgrade of an external ASSP connected to HX3 through USB
  - In-system Programming (ISP) of the EEPROM connected to HX3 through USB

Features

- Extensive configuration support
  - Pin-strap configuration for the following functions:
    - Vendor ID (VID)
    - Charging support for each DS port
    - Number of active ports
    - Number of non-removable devices
    - Ganged or individual power switch enables for DS ports
    - Power switch polarity selection
  - Custom configuration modes supported with eFuse, I^2C EEPROM, or I^2C slave
    - SS and USB 2.0 PHY parameters
    - Product ID (PID)/VID, manufacturer, and product string descriptors
    - Swap DP/DM signals for flexible PCB routing
- Software features
  - Microsoft logo certified
  - Compatible with Mac OS and Linux
  - Customize configuration parameters with the easy-to-use Infineon's "Blaster Plus" software tool
  - Automotive qualification
  - AEC-Q100 auto qualified
- Flexible packaging options
  - 68-pin QFN (8 × 8 × 1.0 mm)
  - 88-pin QFN (10 × 10 × 1.0 mm)
  - 100-ball BGA (6 × 6 × 1.0 mm)
- Temperature range
  - For BGA package: –40°C to +85°C
  - For QFN package: –40°C to +105°C

Block diagram

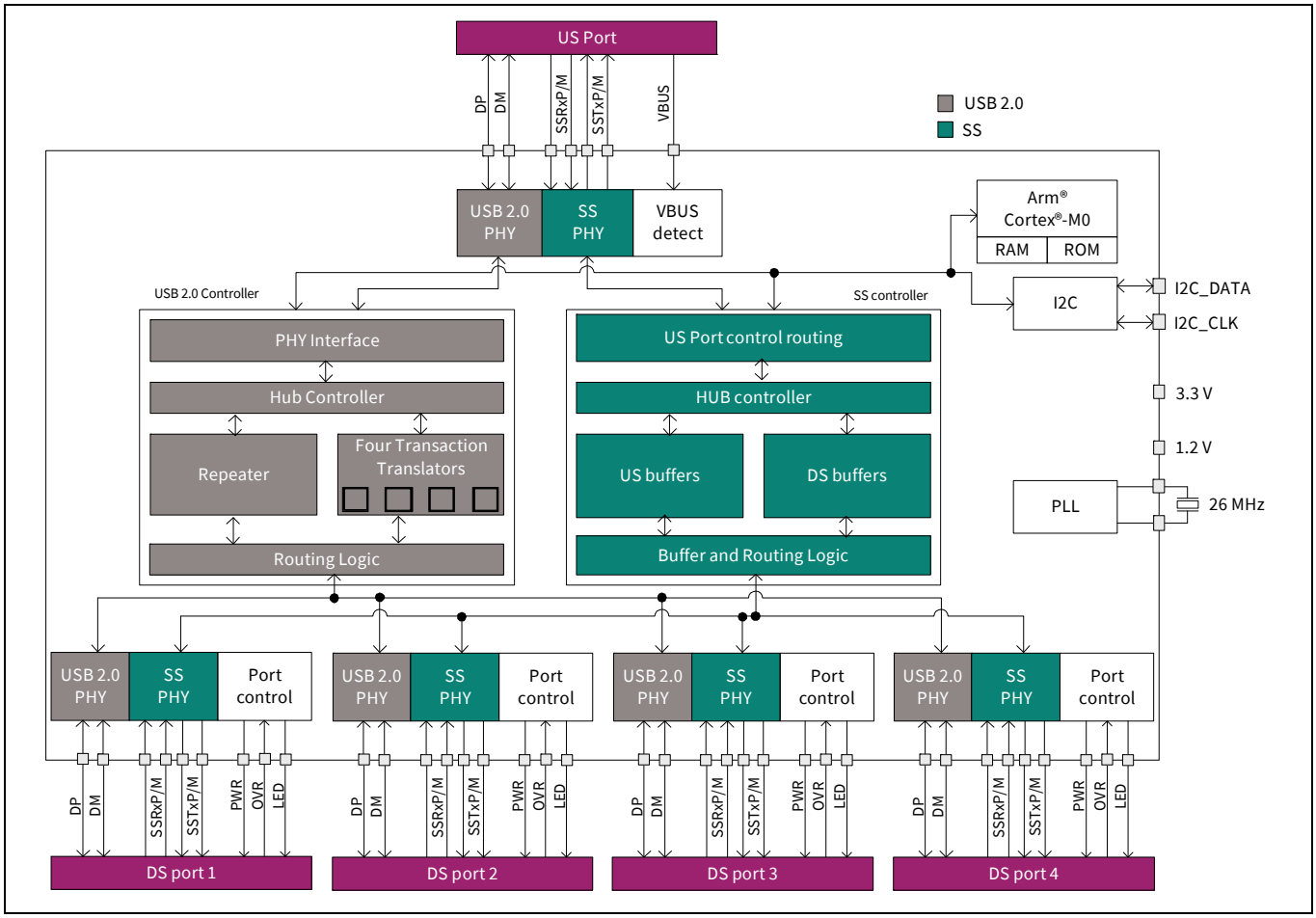

Figure 1 EZ-USB™ HX3-auto block diagram

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1 Architecture overview

The **“Block diagram”** on page 3 shows the HX3 architecture. EZ-USB™ HX3 consists of two independent hub controllers (SS and USB 2.0), the Cortex®-M0 CPU subsystem, an I^2C interface, and port controller blocks.

1.1 SuperSpeed (SS) hub controller

This block supports the SS hub functionality-based on the USB 3.1, Gen 1 specification. The SS hub controller supports the following:

- SS link power management (U0, U1, U2, U3 states)
- Full-duplex data transmission

1.2 USB 2.0 hub controller

This block supports the LS, FS, and HS hub functionalities. It includes the repeater, frame timer, and four transaction translators.

The USB 2.0 hub controller block supports the following:

- USB 2.0 link power management (L0, L1, L2, L3 states)
- Suspend, resume, and remote wake-up signaling
- Multi-TT (one TT for each DS port)

1.3 CPU

The Arm® Cortex®-M0 CPU subsystem is used for the following functions:

- System configuration and initialization
- Battery charging control
- Vendor-specific commands for the USB-to-I^2C bridge
- String-descriptor support
- Suspend status indicator
- Shared link support in embedded systems

1.4 I^2C interface

The I^2C interface in EZ-USB™ HX3 supports the following:

- I^2C slave, master, and multi-master configurations
  - Configure HX3 by an external I^2C Master in I^2C Slave mode
  - Configure HX3 from an I^2C EEPROM
  - Multimaster mode to share EEPROM with other I^2C masters
- In-system programming of the I^2C EEPROM from HX3’s US port

1.5 Port controller

The port controller block controls DS port power to comply with the BC v1.2 and USB 3.1 Gen 1 specifications. This block also controls the US port power in the ACA-Dock mode. The control signals for external power switches are implemented within the chip. HX3 controls the external power switches at power-on to reduce in-rush current.

The port controller block supports the following:

- Overcurrent detection
- SS and USB 2.0 port indicators for each DS port
- Ganged and individual power control modes
- Automatic port numbering based on active ports

2 Application

The automotive infotainment applications as shown in **Figure 2**.

EZ-USB™ HX3 Automotive with Power Delivery (PD) **Figure 2** illustrates the overview of Automotive head unit application with HX3 hub and Infineon PD (Power Delivery) controller. HX3 can be used for 2 to 4 downstream ports with data and various charging protocols.

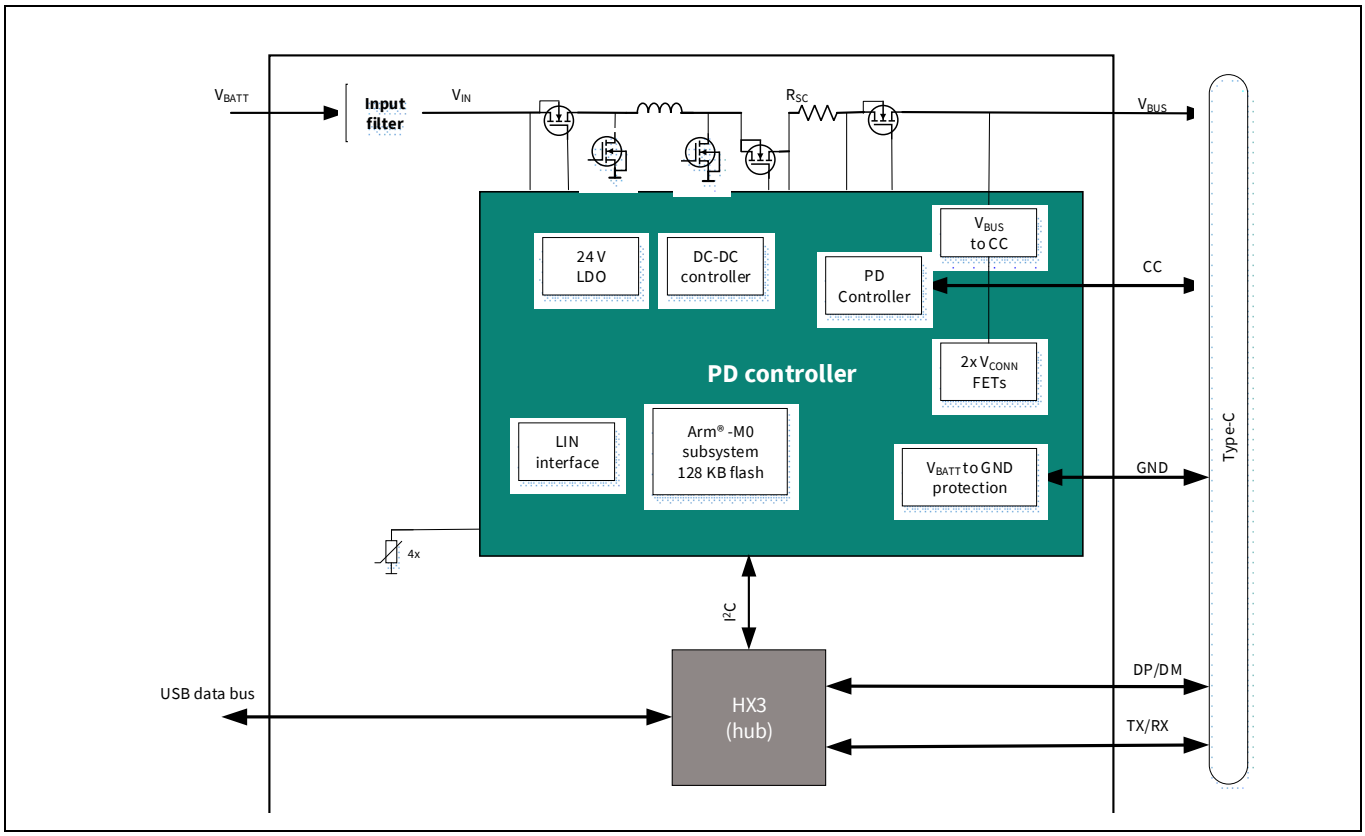


Figure 2 Automotive head unit application

3 HX3 Product options

Table 1 HX3 product options

Features	CYUSB3302	CYUSB3304	CYUSB3324	CYUSB3326	CYUSB2302	CYUSB2304	CYUSB3314	CYUSB2312
Number of DS ports	2 (USB 3.0)	4 (USB 3.0)	4 (USB 3.0)	6 (2 USB 3.0, 2 SS, 2 USB 2.0)	2 (USB 2.0)	4 (USB 2.0)	4	2 (USB 2.0)
Number of shared Link ports	0	0	0	2[1]	0	0	0	0
BC v1.2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACA-Dock	No	No	Yes	No	No	No	No	No
External power switch control	Ganged	Ganged	Individual and Ganged	Individual	Ganged	Ganged	Individual and Ganged	Individual
Pin-Strap support	No	No	Yes	Yes	No	No	Yes	Yes
I^2C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Vendor command	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Port indicators	No	No	Yes	No	No	No	Yes	Yes
Package[2]	100-ball BGA	100-ball BGA	100-ball BGA	100-ball BGA	68-QFN and 100-ball BGA	100-ball BGA	88-QFN and 100-ball BGA	88-QFN
Temperature range	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive	Automotive

Notes
1. DS1 and DS2 are shared link ports.
2. BGA Industrial grade packages are limited to 1 W of active power. For power calculations refer to **Table 11**.

4 Product features

4.1 EZ-USB™ HX3 with shared link feature

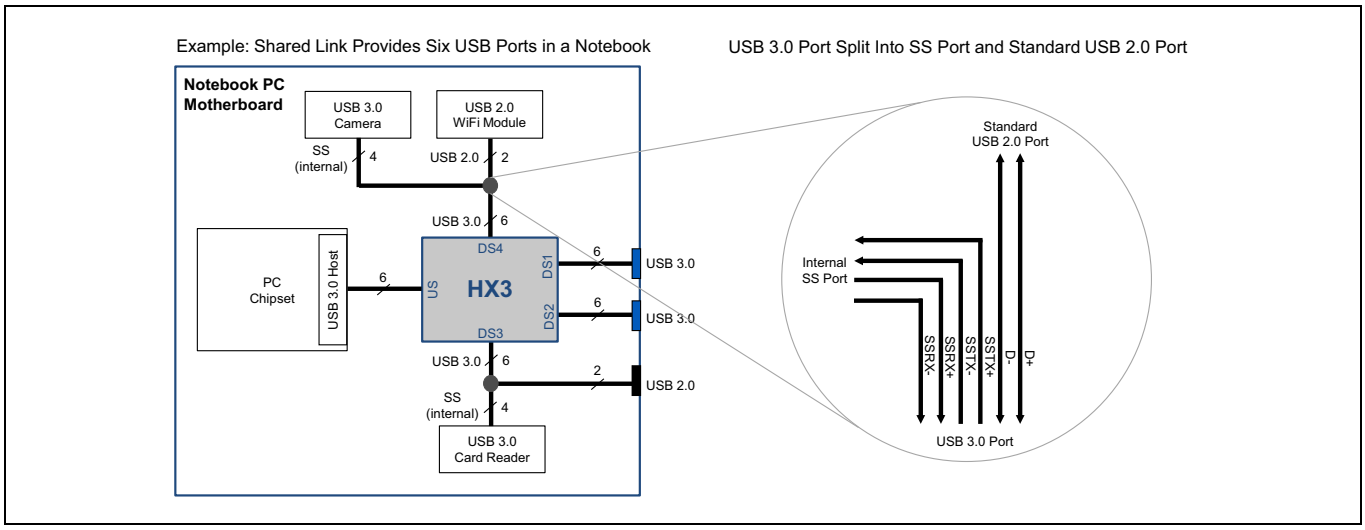


Figure 3 Application of Shared Link in a Notebook

The shared Link is a Infineon-proprietary feature that enables a USB 3.0 port to be split into an embedded SS port and a standard USB 2.0 port. The Shared Link enables a maximum of six DS ports from a four-port USB 3.0 hub.

For example, if one of the DS ports is connected to an embedded SS device, such as a USB 3.0 camera, HX3 enables the system designer to reuse the USB 2.0 signals of that specific port to connect to a standard USB 2.0 port. **Figure 3** shows how Shared Link can be used in an application.

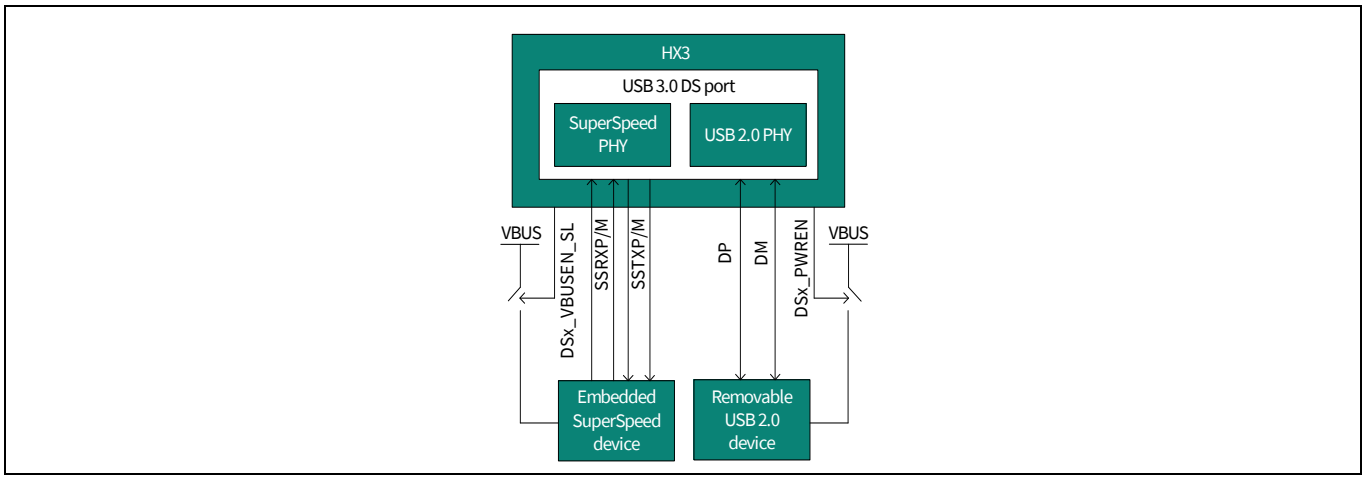


Figure 4 DS port VBUS control in shared link

The Shared Link mode requires a separate VBUS control for the removable USB 2.0 device and the embedded SS device. **Figure 2** shows the VBUS control implementation.

To ensure that the embedded SS device does not fall back to USB 2.0 operation, an external power switch is required. This switch is controlled by HX3, which generates an output signal called DSx_VBUSEN_SL. This signal controls the VBUS for the embedded device.

DSx_PWREN is another output signal generated by HX3 and controls VBUS for the removable USB 2.0 device. For example, when an overcurrent condition occurs, DSx_PWREN turns off the port power.

4.2 EZ-USB™ HX3 with ghost charging

The ghost charge is a Infineon-proprietary feature for charging USB devices on the DS port when the US port is not connected to a host. For example, in a docking station with HX3 as shown in **Figure 5**, when the laptop is undocked, HX3 will emulate a dedicated charging port (DCP) to provide charge to a phone connected on a DS port.

Charge a smartphone without docking the notebook

Figure 5 Ghost charge

When the US port is disconnected from the host, HX3 detects if any of the DS ports are connected to a device requesting charging. It determines the charging method and then switches to the appropriate signaling-based on the detected charging specification as shown in **Figure 6**. The hub either emulates a USB-compliant dedicated charging port by connecting DP and DM (see the BC v1.2 specification) or other supported proprietary charging schemes.

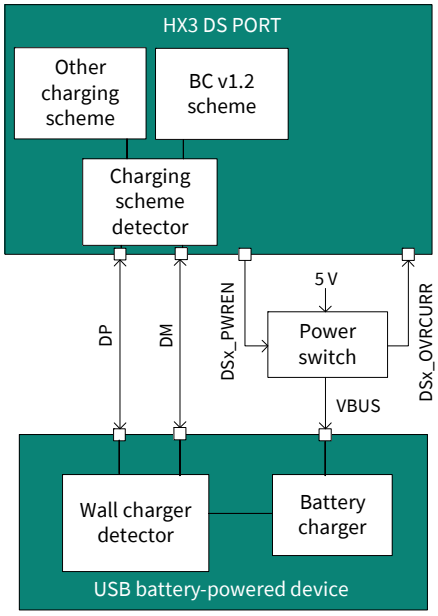


Figure 6 Ghost charge implementation in HX3

The ghost charging is enabled by default and can be disabled through configuration. See **"Configuration options"** on page 29.

4.3 Vendor-Command support

HX3 supports vendor-specific requests and can also enumerate as a vendor-specific device. The vendor-specific request can be used to (a) bridge USB and I^2C and (b) configure HX3. This feature can be used for the following applications:

- Firmware upgrade of an external ASSP connected to HX3 through USB
- In-System programming (ISP) of an EEPROM connected to HX3 through USB

4.4 ACA-Dock support

In traditional USB topologies, the host provides VBUS to enable and charge the connected devices. For OTG hosts, however, an ACA-Dock provides VBUS and a method to charge the host. HX3 supports the ACA-Dock standard (see BC v1.2 specification) by integrating the functions of the adapter controller.

Figure 7 shows the ACA-Dock system. If the ACA-Dock feature is enabled, HX3 turns ON the external power switch to drive VBUS on the US port. To inform the OTG host that it is connected to an ACA-Dock, the ID pin is tied to ground using a resistor RID_A,[3] as shown in **Figure 7**. The ACA-Dock feature can be disabled using the **"Configuration options"** on page 29.

For example, a BC v1.2 compliant phone such as a Sony Xperia (neo V) can be docked to a HX3-based ACA-Dock system. The phone acts as an OTG host and the ACA-Dock charges the phone connected to the US port while also powering the four DS ports.

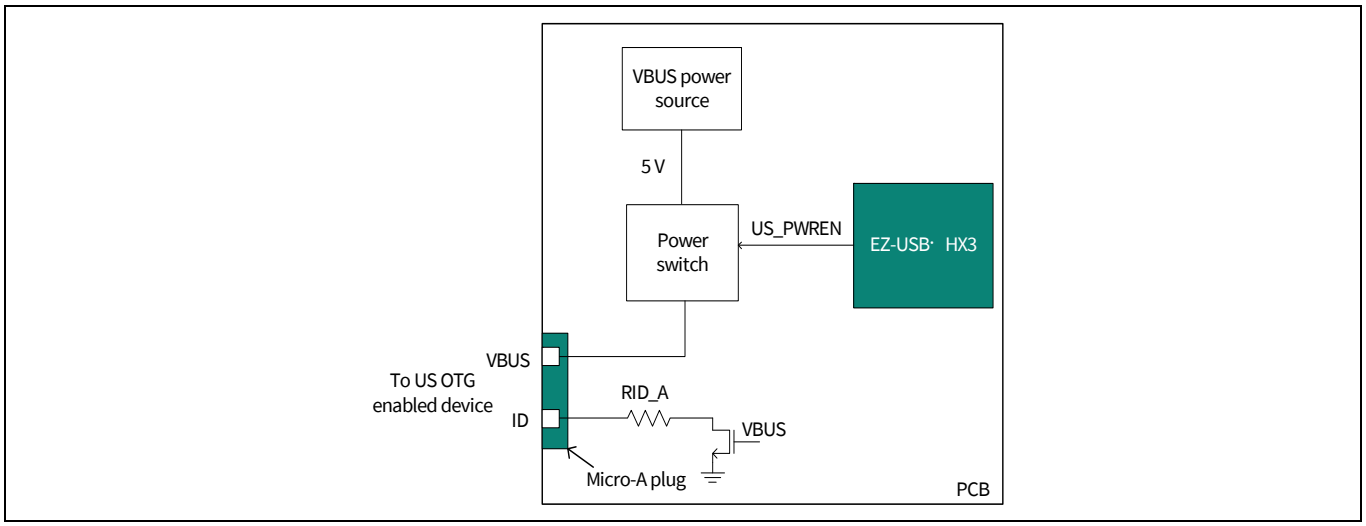


Figure 7 ACA-Dock support

Note

3. 124 kΩ is the recommended RID_A value as per BC v1.2 specification, but some portable devices use custom RID_A values.

5 Pin information

5.1 Pin information for 100-ball BGA

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B	NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C	US_TXM	NC	NC	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D	US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E	DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F	US_RXM	VSS	AVDD33	MODE_SEL[1]	DVDD12	OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G	US_RXP	VBUS_DS	SUSPEND	RESERVED2	MODE_SEL[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H	AVDD12	VBUS_US	VDD_EFUSE	RESERVED1	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J	VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K	NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Figure 8 100-ball BGA pinout for CYUSB3302

	1	2	3	4	5	6	7	8	9	10
A	NC	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B	NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C	US_TXM	NC	NC	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D	US_TXP	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E	DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F	US_RXM	VSS	AVDD33	MODE_SEL[1	DVDD12	OVRCURR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G	US_RXP	VBUS_DS	SUSPEND	RESERVED2	MODE_SEL[0	VDD_IO	PWR_EN	I2C_DATA	VSS	DS2_RXM
H	AVDD12	VBUS_US	DVDD12	RESERVED1	RREF_SS	VSS	DS2_TXM	DS2_TXP	NC	AVDD12
J	VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	DS3_RXM
K	DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	NC	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Figure 9 100-ball BGA pinout for CYUSB3304

Table 2 68-pin QFN, 100-ball BGA pinout for CYUSB2302 and CYUSB2304

Pin name		Type	100-ball BGA ball #	Description
CYUSB3302	CYUSB3304			
US port				
US_RXP		I	G1	SuperSpeed receive plus
US_RXM		I	F1	SuperSpeed receive minus
US_TXP		O	D1	SuperSpeed transmit plus
US_TXM		O	C1	SuperSpeed transmit minus
US_DP		I/O	A9	USB 2.0 data plus
US_DM		I/O	A8	USB 2.0 data minus
DS1 port				
DS1_RXP		I	D10	SuperSpeed receive plus
DS1_RXM		I	C10	SuperSpeed receive minus
DS1_TXP		O	F8	SuperSpeed transmit plus
DS1_TXM		O	E8	SuperSpeed transmit minus
DS1_DP		I/O	C7	USB 2.0 data plus
DS1_DM		I/O	C8	USB 2.0 data minus
DS2 port				
DS2_RXP		I	F10	SuperSpeed receive plus
DS2_RXM		I	G10	SuperSpeed receive minus
DS2_TXP		O	H8	SuperSpeed transmit plus
DS2_TXM		O	H7	SuperSpeed transmit minus
DS2_DP		I/O	A6	USB 2.0 data plus
DS2_DM		I/O	A5	USB 2.0 data minus
DS3 port				
NC	DS3_RXP	I	K10	SuperSpeed receive plus
NC	DS3_RXM	I	J10	SuperSpeed receive minus
NC	DS3_TXP	O	K7	SuperSpeed transmit plus
NC	DS3_TXM	O	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	C4	USB 2.0 data plus
NC	DS3_DM	I/O	C5	USB 2.0 data minus
DS4 port				
NC	DS4_RXP	I	K4	SuperSpeed receive plus
NC	DS4_RXM	I	K5	SuperSpeed receive minus
NC	DS4_TXP	O	K1	SuperSpeed transmit plus
NC	DS4_TXM	O	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	A3	USB 2.0 data plus
NC	DS4_DM	I/O	A2	USB 2.0 data minus
OVRCURR		I	F6	Ganged overcurrent input
PWR_EN		I/O	G7	Ganged power enable output
NC		I/O	NA	NC

Table 2 68-pin QFN, 100-ball BGA pinout for CYUSB2302 and CYUSB2304 *(continued)*

Pin name		Type	100-ball BGA ball #	Description
CYUSB3302	CYUSB3304			
RESERVED1		I/O	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO
RESERVED2		I	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO
Mode Select, Clock, and Reset				
MODE_SEL[0]		I	G5	Device operation mode select bit 0; see **Table 5**
MODE_SEL[1]		I	F4	Device operation mode select bit 1; see **Table 5**
XTL_OUT		A	E6	Crystal out
XTL_IN		A	E5	Crystal in
RESETN		I	F7	Active LOW reset input
I2C_CLK		I/O	J6	I^2C clock
I2C_DATA		I/O	G8	I^2C data
SUSPEND		I/O	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and ground				
VDD_EFUSE		PWR	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V.
AVDD12		PWR	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	G2	This pin is used to power the Apple-charging circuit in HX3. For BC v1.2 compliance testing, connect pin to GND. For normal operation, connect pin to local 5 V supply.
AVDD33		PWR	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	B4, E7, G6	3.3 V I/O supply
USB precision resistors				
RREF_USB2		A	E2	Connect pin to a precision resistor (6.04 kΩ ± 1%) to generate a current reference for USB 2.0 PHY
RREF_SS		A	H5	Connect pin to a precision resistor (200 Ω ± 1%) for SS PHY termination impedance calibration

	1	2	3	4	5	6	7	8	9	10
A	NC	NC	NC	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B	NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C	NC	NC	NC	NC	NC	VSS	DS1_DP	DS1_DM	AVDD12	NC
D	NC	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	NC
E	DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	NC	VSS	DVDD12
F	NC	VSS	AVDD33	MODE_SEL[1]	DVDD12	OVRCURR	RESETN	NC	AVDD12	NC
G	NC	VBUS_DS	SUSPEND	RESERVED2	MODE_SEL[0]	VDD_IO	PWR_EN	I2C_DATA	VSS	NC
H	AVDD12	VBUS_US	VDD_EFUSE	RESERVED1	RREF_SS	VSS	NC	NC	NC	AVDD12
J	VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K	NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Figure 10 100-ball BGA pinout for CYUSB2302

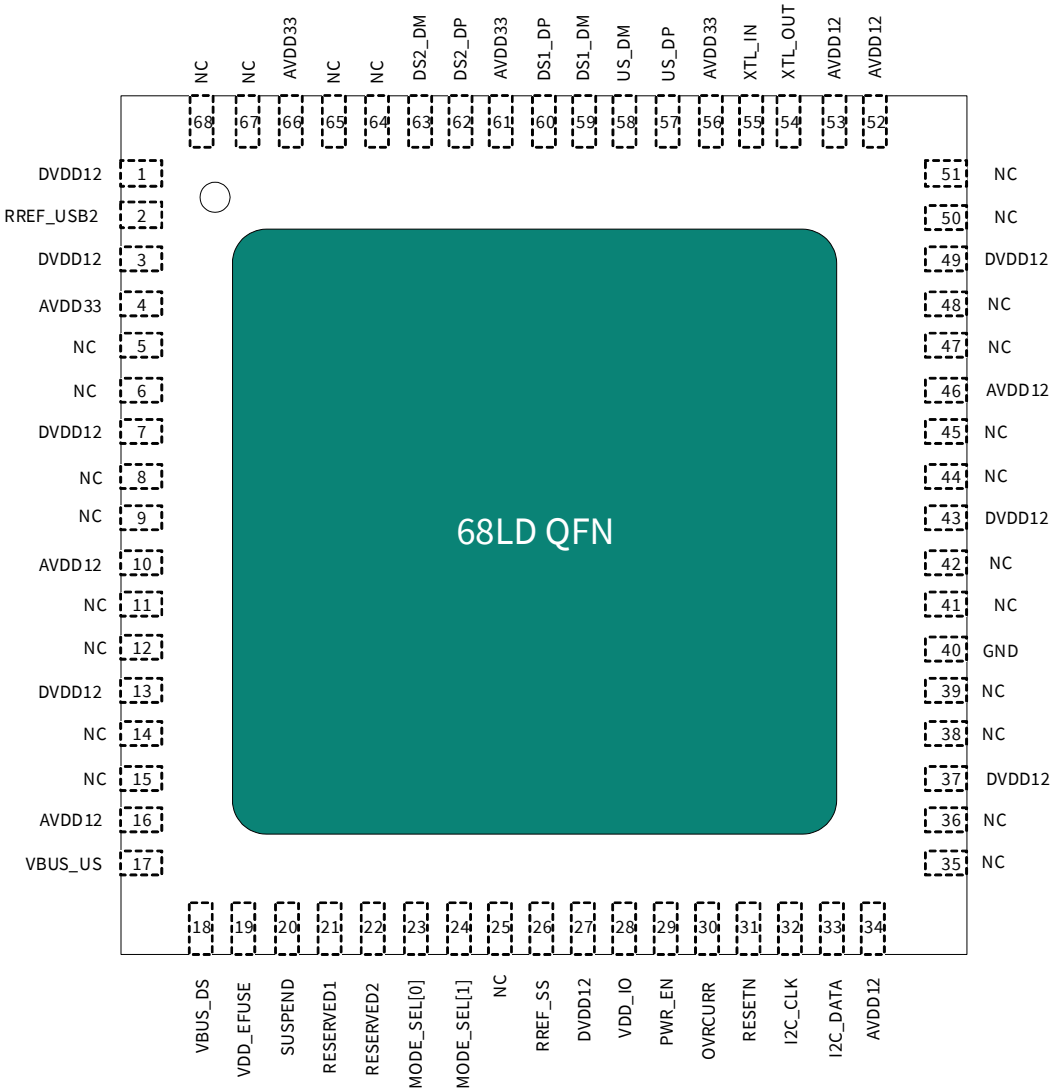


Figure 11 68LD QFN pinout for CYUSB2304

	1	2	3	4	5	6	7	8	9	10
A	NC	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B	NC	NC	NC	VDD_IO	VSS	AVDD33	NC	NC	NC	DVDD12
C	NC	NC	NC	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	NC
D	NC	NC	NC	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	NC
E	DVDD12	RREF_USB2	NC	NC	XTL_IN	XTL_OUT	VDD_IO	NC	VSS	DVDD12
F	NC	VSS	AVDD33	MODE_SEL[1	DVDD12	OVRCURR	RESETN	NC	AVDD12	NC
G	NC	VBUS_DS	SUSPEND	RESERVED2	MODE_SEL[0	VDD_IO	PWR_EN	I2C_DATA	VSS	NC
H	AVDD12	VBUS_US	VDD_EFUSE	RESERVED1	RREF_SS	VSS	NC	NC	NC	AVDD12
J	VSS	AVDD12	VSS	GPIO	NC	I2C_CLK	NC	NC	VSS	NC
K	NC	NC	DVDD12	NC	NC	NC	NC	NC	DVDD12	NC

Figure 12 100-ball BGA pinout for CYUSB2304

Table 3 68LD QFN, 100-ball BGA pinout for CYUSB2302 and CYUSB2304

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	**CYUSB2304**				
US port					
NC		I	9	G1	SuperSpeed receive plus
NC		I	8	F1	SuperSpeed receive minus
NC		O	6	D1	SuperSpeed transmit plus
NC		O	5	C1	SuperSpeed transmit minus
US_DP		I/O	57	A9	USB 2.0 data plus
US_DM		I/O	58	A8	USB 2.0 data minus
DS1 Port					
NC		I	51	D10	SuperSpeed receive plus
NC		I	50	C10	SuperSpeed receive minus
NC		O	47	F8	SuperSpeed transmit plus
NC		O	48	E8	SuperSpeed transmit minus
DS1_DP		I/O	60	C7	USB 2.0 data plus
DS1_DM		I/O	59	C8	USB 2.0 data minus
DS2 port					
NC		I	45	F10	SuperSpeed receive plus
NC		I	44	G10	SuperSpeed receive minus
NC		O	41	H8	SuperSpeed transmit plus
NC		O	42	H7	SuperSpeed transmit minus
DS2_DP		I/O	62	A6	USB 2.0 data plus
DS2_DM		I/O	63	A5	USB 2.0 data minus
DS3 port					
NC	NC	I	35	K10	SuperSpeed receive plus
NC	NC	I	36	J10	SuperSpeed receive minus
NC	NC	O	38	K7	SuperSpeed transmit plus
NC	NC	O	39	K8	SuperSpeed transmit minus
NC	DS3_DP	I/O	65	C4	USB 2.0 data plus
NC	DS3_DM	I/O	64	C5	USB 2.0 data minus
DS4 port					
NC	NC	I	15	K4	SuperSpeed receive plus
NC	NC	I	14	K5	SuperSpeed receive minus
NC	NC	O	11	K1	SuperSpeed transmit plus
NC	NC	O	12	K2	SuperSpeed transmit minus
NC	DS4_DP	I/O	67	A3	USB 2.0 data plus
NC	DS4_DM	I/O	68	A2	USB 2.0 data minus
OVRCURR		I	30	F6	Ganged overcurrent input
PWR_EN		I/O	29	G7	Ganged power enable output
NC		I/O	25	NA	NC

Table 3 68LD QFN, 100-ball BGA pinout for CYUSB2302 and CYUSB2304 *(continued)*

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	**CYUSB2304**				
RESERVED1		I/O	21	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
RESERVED2		I	22	H4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode select, clock, and reset					
MODE_SEL[0]		I	23	G5	Device operation mode select bit 0; see **Table 5**
MODE_SEL[1]		I	24	F4	Device operation mode select bit 1; see **Table 5**
XTL_OUT		A	54	E6	Crystal out
XTL_IN		A	55	E5	Crystal in
RESETN		I	31	F7	Active LOW reset input
I2C_CLK		I/O	32	J6	I^2C clock
I2C_DATA		I/O	33	G8	I^2C data
SUSPEND		I/O	20	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state
Power and ground					
VDD_EFUSE		PWR	19	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12		PWR	10, 16, 34, 46, 52, 53	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND		PWR	40	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12		PWR	1, 3, 7, 13, 27, 37, 43, 49,	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply
VBUS _US		PWR	17	H2	This pin must be connected to VBUS from US port
VBUS_DS		PWR	18	G2	This pin is used to power the Apple-charging circuit in HX3. For normal operation, connect pin to local 5 V supply to enable Apple charging and BC v1.2 charging modes (enable multi-charger mode). For BC v1.2 compliance testing or when Apple charging is not required, connect pin to GND to enable BC v1.2 charging mode (disable multi-charger mode).
AVDD33		PWR	4, 56, 61, 66	A4, A7, B6, F3	3.3 V analog supply
VDD_IO		PWR	28	B4, E7, G6	3.3 V I/O supply

Table 3 68LD QFN, 100-ball BGA pinout for CYUSB2302 and CYUSB2304 *(continued)*

Pin Name		Type	68-QFN Pin#	100-BGA Ball #	Description
CYUSB2302	**CYUSB2304**				
USB Precision Resistors					
RREF_USB2		A	2	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY
RREF_SS		A	26	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration

	1	2	3	4	5	6	7	8	9	10
A	DS3_PWREN	DS4_DM	DS4_DP	AVDD33	DS2_DM	DS2_DP	AVDD33	US_DM	US_DP	AVDD12
B	S2_OVRCUR	DS2_PWREN	DS3_AMBER	VDD_IO	VSS	AVDD33	S3_OVRCUR	DS3_GREEN	DS3_LED_SS	DVDD12
C	US_TXM	DS1_AMBER	DS2_LED_SS	DS3_DP	DS3_DM	VSS	DS1_DP	DS1_DM	AVDD12	DS1_RXM
D	US_TXP	DS1_LED_SS	DS1_GREEN	DVDD12	VSS	DVDD12	VSS	DVDD12	VSS	DS1_RXP
E	DVDD12	RREF_USB2	DS2_GREEN	DS2_AMBER	XTL_IN	XTL_OUT	VDD_IO	DS1_TXM	VSS	DVDD12
F	US_RXM	VSS	AVDD33	MODE_SEL[1	DVDD12	S4_OVRCUR	RESETN	DS1_TXP	AVDD12	DS2_RXP
G	US_RXP	VBUS_DS	SUSPEND	RESERVED2	MODE_SEL[0	VDD_IO	DS4_PWREN	I2C_DATA	VSS	DS2_RXM
H	AVDD12	VBUS_US	VDD_EFUSE	DS4_LED_SS	RREF_SS	VSS	DS2_TXM	DS2_TXP	DS4_GREEN	AVDD12
J	VSS	AVDD12	VSS	DS4_AMBER	US_PWREN	I2C_CLK	DS1_PWREN	S1_OVRCUR	VSS	DS3_RXM
K	DS4_TXP	DS4_TXM	DVDD12	DS4_RXP	DS4_RXM	JS_OVRCURI	DS3_TXP	DS3_TXM	DVDD12	DS3_RXP

Figure 13 100-ball BGA pinout for CYUSB332x

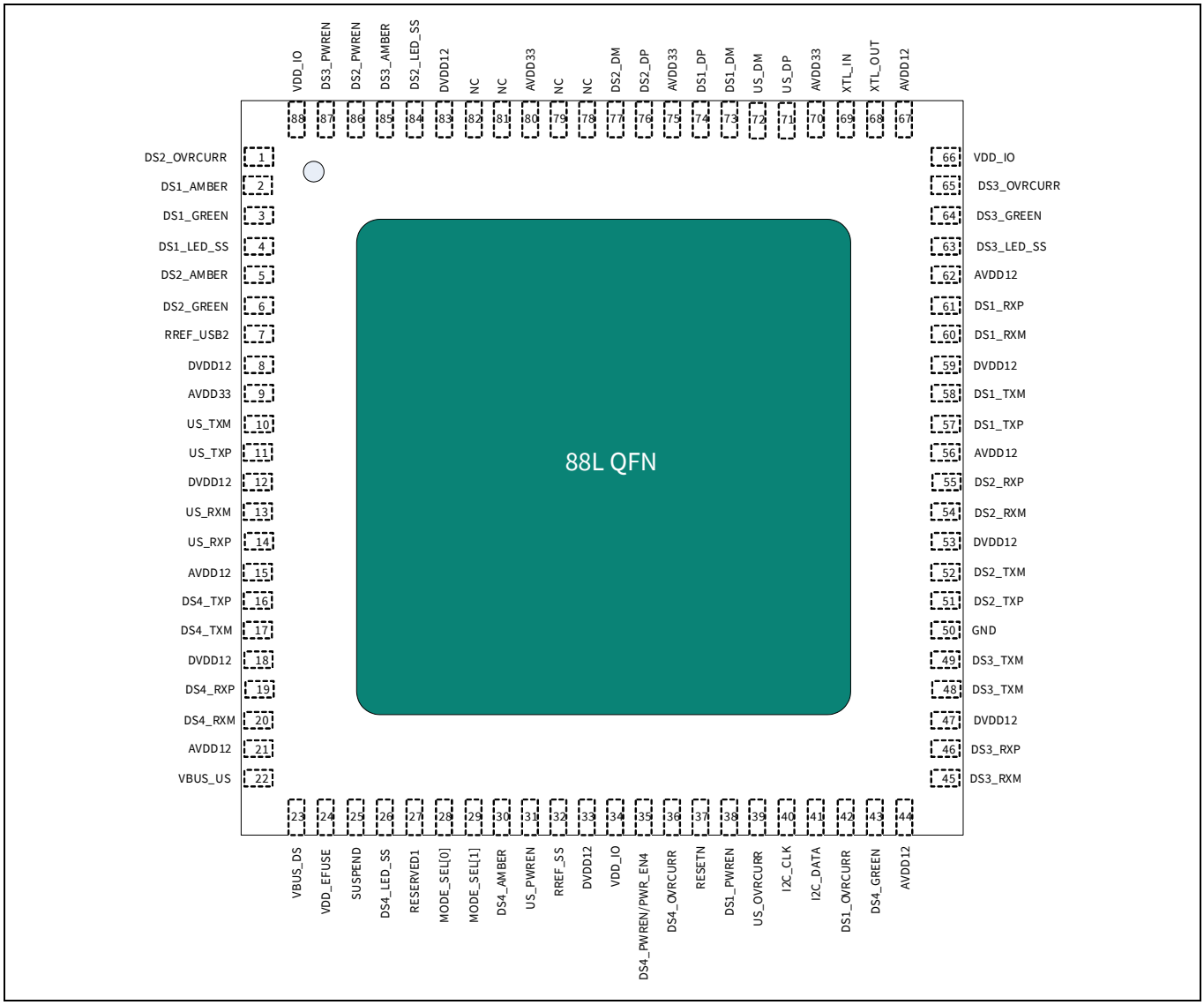


Figure 14 88L QFN pinout for CYUSB3314 and CYUSB2312

Table 4 88L QFN, 100-ball BGA Ppinout for CYUSB231X, CYUSB331X and CYUSB332X

Pin name			Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328	CYUSB2312				
US port						
US_RXP		NC	I	14	G1	SuperSpeed receive plus
US_RXM			I	13	F1	SuperSpeed receive minus
US_TXP			O	11	D1	SuperSpeed transmit plus
US_TXM			O	10	C1	SuperSpeed transmit minus
US_DP			I/O	71	A9	USB 2.0 data plus
US_DM			I/O	72	A8	USB 2.0 data minus
US_OVRCURR			I	39	K6	CYUSB3324/3328: Overcurrent detect input for US port in ACA-Dock mode. If ACA-Dock mode is disabled using **"Configuration options"** on page 29, this pin must be pulled HIGH using a 10 kΩ to VDD_IO. Other part numbers: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
US_PWREN[4]			I/O	31	J5	CYUSB3324/3328: VBUS power enable output for US port in ACA-Dock mode. If ACA-Dock mode is disabled using **"Configuration options"** on page 29, this pin can be left floating if Pin-Strap is not enabled. Other part numbers: This pin can be left floating if Pin-Strap (Pin# 63) is not enabled.
PWR_SW_POL[5]						This pin is called PWR_SW_POL in pin-strap configuration mode.
DS1 port						
DS1_RXP		NC	I	61	D10	SuperSpeed receive plus
DS1_RXM			I	60	C10	SuperSpeed receive minus
DS1_TXP			O	57	F8	SuperSpeed transmit plus
DS1_TXM			O	58	E8	SuperSpeed transmit minus
DS1_DP			I/O	74	C7	USB 2.0 data plus
DS1_DM			I/O	73	C8	USB 2.0 data minus
DS1_OVRCURR			I	42	J8	Overcurrent detect input for DS1 port

Notes

4. This pin can be configured as a GPIO using custom firmware. For more information go to **www.infineon.com/support**.
5. For pin-strap configuration details, see **Table 6**.

Table 4 88L QFN, 100-ball BGA Ppinout for CYUSB231X, CYUSB331X and CYUSB332X *(continued)*

Pin name			Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328	CYUSB2312				
DS1_PWREN[4]			I/O	38	J7	VBUS power enable output for DS1 port. When the port is disabled, this pin is in tristate.
DS1_CDP_EN[5]						This pin is called DS1_CDP_EN in pin-strap configuration mode
DS1_AMBER[4]			I/O	2	C2	LED_AMBER output for DS1 port
ACA_DOCK[5]						This pin is called ACA-DOCK in pin-strap configuration mode.
DS1_GREEN[4]			I/O	3	D3	CYUSB3312/3314/3324: LED_GREEN output for DS1 port
DS1_VBUSEN_SL[4]						CYUSB3326/3328: VBUS power enable output for SS port 1
PORT_DISABLE[0][5]						This pin is called PORT_DISABLE[0] in pin-strap configuration mode
DS1_LED_SS[4]			I/O	4	D2	LED_SS output for DS1 port
PORT_DISABLE[1][5]						This pin is called PORT_DISABLE[1] in pin-strap configuration mode
DS2 port						
DS2_RXP		NC	I	55	F10	SuperSpeed receive plus
DS2_RXM			I	54	G10	SuperSpeed receive minus
DS2_TXP			O	51	H8	SuperSpeed transmit plus
DS2_TXM			O	52	H7	SuperSpeed transmit minus
DS2_DP			I/O	76	A6	USB 2.0 data plus
DS2_DM			I/O	77	A5	USB 2.0 data minus
DS2_OVRCURR			I	1	B1	Overcurrent detect input for DS2 port
DS2_PWREN[4]			I/O	86	B2	VBUS power enable output for DS2 port. When the port is disabled, this pin is in tristate.
DS2_CDP_EN[5]						This pin is called DS2_CDP_EN in the pin-strap configuration mode.
DS2_AMBER[4]			I/O	5	E4	LED_AMBER output for DS2 port
NON_REMOVABLE[0][5]						This pin is called NON_REMOVABLE[0] in the pin-strap configuration mode.

Notes

4. This pin can be configured as a GPIO using custom firmware. For more information go to **www.infineon.com/support**.
5. For pin-strap configuration details, see **Table 6**.

Table 4 88L QFN, 100-ball BGA Ppinout for CYUSB231X, CYUSB331X and CYUSB332X *(continued)*

Pin name			Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328	CYUSB2312				
DS2_GREEN[4]			I/O	6	E3	CYUSB3312/3314/3324: LED_GREEN output for DS2 port
DS2_VBUSEN_SL[4]						CYUSB3326/3328: VBUS power enable output for SS port 2
NON_REMOVABLE[1][5]						This pin is called NON_REMOVABLE[1] in the pin-strap configuration mode.
DS2_LED_SS[4]			I/O	84	C3	LED_SS output for DS2 port
PWR_EN_SEL[5]						This pin is called PWR_EN_SEL in the pin-strap configuration mode.
DS3 port						
NC	DS3_RXP	NC	I	45	K10	SuperSpeed receive plus
NC	DS3_RXM		I	46	J10	SuperSpeed receive minus
NC	DS3_TXP		O	48	K7	SuperSpeed transmit plus
NC	DS3_TXM		O	49	K8	SuperSpeed transmit minus
NC	DS3_DP		I/O	79	C4	USB 2.0 data plus
NC	DS3_DM		I/O	78	C5	USB 2.0 data minus
DS3_OVRCURR			I	65	B7	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS3 port CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS3_PWREN[4]			I/O	87	A1	VBUS power enable output for DS3 port. When the port is disabled, this pin is in tristate.
DS3_CDP_EN[5]						This pin is called DS3_CDP_EN in the pin-strap configuration mode.
DS3_AMBER[4]			I/O	85	B3	LED_AMBER output for DS3 port
VID_SEL[2][5]						This pin is called VID_SEL[2] in the pin-strap configuration mode.
DS3_GREEN[4]			I/O	64	B8	CYUSB3312/3314/3324: LED_GREEN output for DS3 port
DS3_VBUSEN_SL[4]						CYUSB3328: VBUS power enable output for SS port 3
VID_SEL[1][5]						This pin is called VID_SEL[1] in the pin-strap configuration mode. For pin-strap configuration details, refer to **Table 6 on page 30**.

Notes

4. This pin can be configured as a GPIO using custom firmware. For more information go to **www.infineon.com/support**.
5. For pin-strap configuration details, see **Table 6**.

Table 4 88L QFN, 100-ball BGA Ppinout for CYUSB231X, CYUSB331X and CYUSB332X *(continued)*

Pin name			Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328	CYUSB2312				
DS3_LED_SS[4]			I/O	63	B9	LED_SS output for DS3 port
PIN_STRAP[5]						This pin is called PIN_STRAP in pin-strap configuration mode. When connected to VDD_IO through a 10-kΩ resistor, this pin enables pin-strap configuration mode for HX3.
DS4 port						
NC	DS4_RXP	NC	I	20	K4	SuperSpeed receive plus
NC	DS4_RXM		I	19	K5	SuperSpeed receive minus
NC	DS4_TXP		O	16	K1	SuperSpeed transmit plus
NC	DS4_TXM		O	17	K2	SuperSpeed transmit minus
NC	DS4_DP		I/O	81	A3	USB 2.0 data plus
NC	DS4_DM		I/O	82	A2	USB 2.0 data minus
DS4_OVRCURR			I	36	F6	CYUSB3314/3324/3326/3328: Overcurrent detect input for DS4 port. CYUSB3312: This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
DS4_PWREN/PWR_EN4			I/O	35	G7	VBUS power enable output for DS4 port. This pin is also used as power enable output when configured in ganged power mode using the Blaster Plus tool. When the port is disabled, this pin is in tristate.
DS4_CDP_EN[5]						This pin is called DS4_CDP_EN in the pin-strap configuration mode.
DS4_AMBER[4]			I/O	30	J4	LED_AMBER output for DS4 port
I2C_DEV_ID[5]						This pin is called I2C_DEV_ID in the pin-strap configuration mode.
DS4_GREEN[4]			I/O	43	H9	CYUSB3312/3314/3324: LED_GREEN output for DS4 port
DS4_VBUSEN_SL						CYUSB3328: VBUS power enable output for SS port 4
VID_SEL[0][5]						This pin is called VID_SEL[0] in the pin-strap configuration mode
DS4_LED_SS			I/O	26	H4	LED_SS output for DS4 port. The LED must be connected to GND as shown in **Figure 16**. If LED is not used, this pin must be pulled HIGH using a 10 kΩ to VDD_IO.

Notes

4. This pin can be configured as a GPIO using custom firmware. For more information go to **www.infineon.com/support**.
5. For pin-strap configuration details, see **Table 6**.

Table 4 88L QFN, 100-ball BGA Ppinout for CYUSB231X, CYUSB331X and CYUSB332X *(continued)*

Pin name			Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328	CYUSB2312				
RESERVED1			I	27	G4	This pin must be pulled HIGH using a 10 kΩ to VDD_IO.
Mode Select, clock, and reset						
MODE_SEL[0]			I	28	G5	Device operation mode select bit 0; see **Table 5**
MODE_SEL[1]			I	29	F4	Device operation mode select bit 1; see **Table 5**
XTL_OUT			A	68	E6	Crystal out
XTL_IN			A	69	E5	Crystal in
RESETN			I	37	F7	Active LOW reset input
I2C_CLK			I/O	40	J6	I^2C clock
I2C_DATA			I/O	41	G8	I^2C data
SUSPEND			I/O	25	G3	Hub suspend status indicator. This pin is asserted if both the SS and USB 2.0 hubs are in the suspend state and is de-asserted when either of the hubs comes out of the suspend state.
Power and ground						
VDD_EFUSE			PWR	24	H3	1.2 V normal operation, 2.5 V for programming. Customers should connect to 1.2 V
AVDD12			PWR	15, 21, 44, 56, 62, 67	A10, C9, F9, H1, H10, J2	1.2 V analog supply
GND			PWR	50	B5, C6, D5, D7, D9, E9, F2, G9, H6, J1, J3, J9	GND pin
DVDD12			PWR	8, 12, 18, 33, 47, 53, 59, 83	B10, D4, D6, D8, E1, E10, F5, K3, K9	1.2 V core supply

Notes

4. This pin can be configured as a GPIO using custom firmware. For more information go to **www.infineon.com/support**.
5. For pin-strap configuration details, see **Table 6**.

Table 4 88L QFN, 100-ball BGA Ppinout for CYUSB231X, CYUSB331X and CYUSB332X *(continued)*

Pin name			Type	Pin#	Ball#	Description
CYUSB3312	CYUSB3314 CYUSB3324 CYUSB3326 CYUSB3328	CYUSB2312				
VBUS _US			PWR	22	H2	CYUSB3324/3328: Connect the VBUS_US pin to the local 5 V supply. If ACA-Dock mode is disabled using **"Configuration options"** on page 29, this pin must be connected to VBUS from US port. Other part numbers: This pin must be connected to VBUS from US port.
VBUS_DS			PWR	23	G2	This pin is used to power the Apple-charging circuit in HX3. For normal operation, connect pin to local 5 V supply to enable Apple charging and BC v1.2 charging modes (enable multi-charger mode). For BC v1.2 compliance testing or when Apple charging is not required, connect pin to GND to enable BC v1.2 charging mode (disable multi-charger mode).
AVDD33			PWR	9, 70, 75, 80	A4, A7, B6, F3	3.3 V analog supply
VDD_IO			PWR	34, 66, 88	B4, E7, G6	3.3 V I/O supply
USB precision resistors						
RREF_USB2			A	7	E2	Connect pin to a precision resistor (6.04 kΩ ±1%) to generate a current reference for USB 2.0 PHY
RREF_SS			A	32	H5	Connect pin to a precision resistor (200 Ω ±1%) for SS PHY termination impedance calibration

Notes

4. This pin can be configured as a GPIO using custom firmware. For more information go to **www.infineon.com/support**.
5. For pin-strap configuration details, see **Table 6**.

6 System interfaces

6.1 Upstream Port (US)

This port is compliant with the USB 3.1 Gen 1 specifications and includes an integrated 1.5 kΩ pull-up and termination resistors. It also supports ACA-Dock to enable charging an OTG host connected on the US port.

6.2 Downstream Ports (DS1, 2, 3, 4)

DS ports are compliant with the USB 3.1 Gen 1 specification and integrate 15 kΩ pull-down and termination resistors. Ports can be disabled or enabled, and can be set to removable or non-removable options. BC v1.2 charging is enabled by default and can be disabled on each DS port using the configuration options (see **"Configuration options"** on page 29).

6.3 Communication interfaces (I^2C)

The interface follows the Inter-IC Bus specification, version 3.0, with support for the standard mode (100 kHz) and the fast mode (400 kHz) frequencies. HX3 supports I^2C in the Slave and Master modes. The I^2C interface supports the multi-master mode of operation. Both the SCL and SDA signals require external pull-up resistors based on the specification. VDD_IO for HX3 is 3.3 V and it is expected that the I^2C pull-up resistors will be connected to the same supply.

6.4 Oscillator

HX3 requires an external crystal with a frequency of 26 MHz and an accuracy of ±150 ppm in parallel resonant, fundamental mode. The crystal drive circuit is capable of a low-power drive level (< 200 µW). The crystal connection to the XTL_OUT and XTL_IN pins is shown in **Figure 15**.

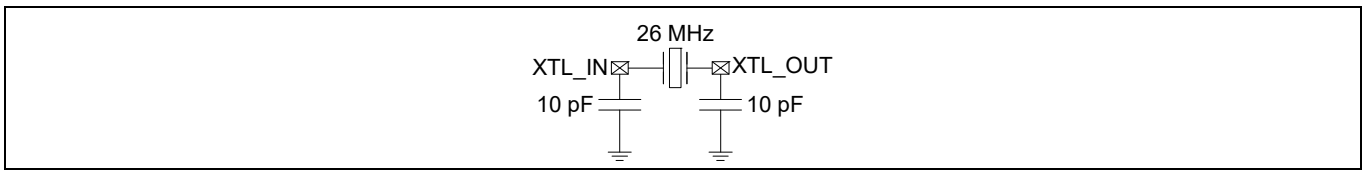


Figure 15 Crystal connection

6.5 GPIOs

HX3 GPIOs are used for overcurrent sensing, controlling external power switches, and driving LEDs. These pins can sink up to 4 mA current each. GPIOs also enable pin-straps for input configuration. See **Table 6** for more details.

6.6 Power control

The PWR_EN[1-4] and OV_CURR[1-4] pins interface HX3 to external power switches. These pins are used to control power switches for DS port power and monitor overcurrent conditions. The power switch polarity and the power control mode (individual and ganged) can be changed using the configuration options.

6.7 Reset

HX3 operates with two external power supplies, 3.3 V and 1.2 V. There is no power sequencing requirement between these two supplies. However, the RESETN pin should be held LOW until both these supplies become stable.

The RESETN pin can be tied to VDD_IO through an external resistor and to ground (GND) through an external capacitor (minimum 5 ms time constant), as shown in **Figure 16**. This creates a clean reset signal for power-on reset (POR).

HX3 does not support internal brownout detection. If the system requires this feature, an external reset should be provided on the RESETN pin when supplies are below their valid operating ranges.

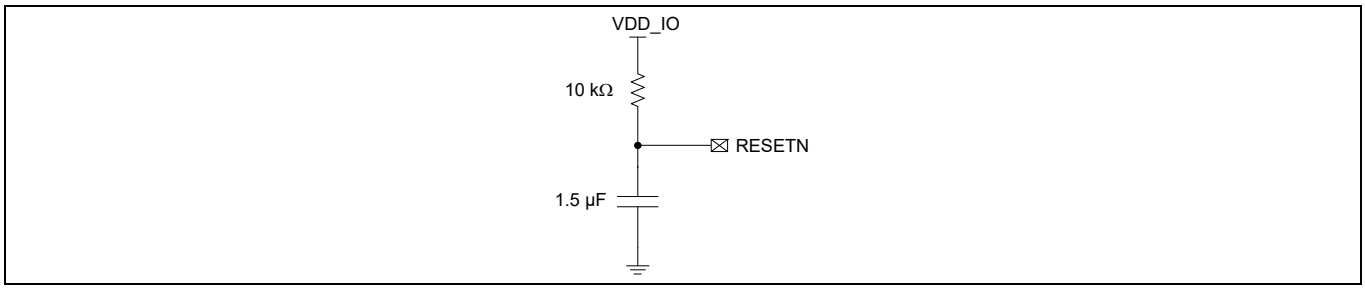


Figure 16 Reset connection

6.8 Configuration Mode select

Configuration options are selected through the MODE_SEL pins and the pin-strap enable pin (PIN_STRAP). After power-up, these pins are sampled by an on-chip bootloader to determine the configuration options (see **Table 5**).

Table 5 HX3 boot sequence

MODE SEL[1]	MODE SEL[0]	HX3 configuration modes
0	0	Reserved. Do not use this mode
1	1	Internal ROM configuration
0	1	I^2C master, read configuration from I^2C EEPROM[6]
1	0	I^2C slave, configure from an external I^2C master [6]

Note
6. Download the firmware from EZ -USB™ hub controller.

6.9 Configuration options

HX3 can be configured by using one of the following:

- eFuse (one-time programmable memory)
- Pin-Strap (read configuration from dedicated pins at power on)
- External I^2C slave such as an EEPROM
- External I^2C master

The I^2C master/slave configuration overrides the pin-strap configuration. Pin-straps override the eFuse configuration, and the eFuse configuration overrides the internal ROM configuration.

6.9.1 eFuse configuration

HX3 contains eFuses, which are OTP elements on the chip that can be electrically blown. The eFuses are read by the bootloader to determine the customer-specific configurations. eFuse programming is supported only at factory and distributor locations where programming conditions can be controlled. eFuse programming is supported under the following conditions: Temperature range of 25°Cto 70°C and programming voltage of 2.5 V–2.7 V.

6.9.2 Pin-Strap configuration

The pin-straps are supported for select product options (see **Table 1**) to provide reconfigurability without an additional EEPROM. The pin-strap configuration is enabled by pulling Pin #B9 HIGH. **Table 6** shows the configuration options supported through pin-straps and the GPIOs used for this purpose. **Figure 17** and **Figure 18** show how the GPIOs need to be connected if pin-strap and LED connection are required or only pin-strap is required.

HX3 samples pin-strap GPIOs at power-up. Floating straps are considered as invalid and the default configuration is used. If PIN_STRAP (Pin #B9) is floating, all strap inputs are considered invalid. A GPIO is considered strapped ’1’ or ’0’ when connected with a weak pull-up (10 kΩ) or pull-down (10 kΩ) respectively. After the initial sampling at power-up and reset, the GPIOs are used in their normal functions.

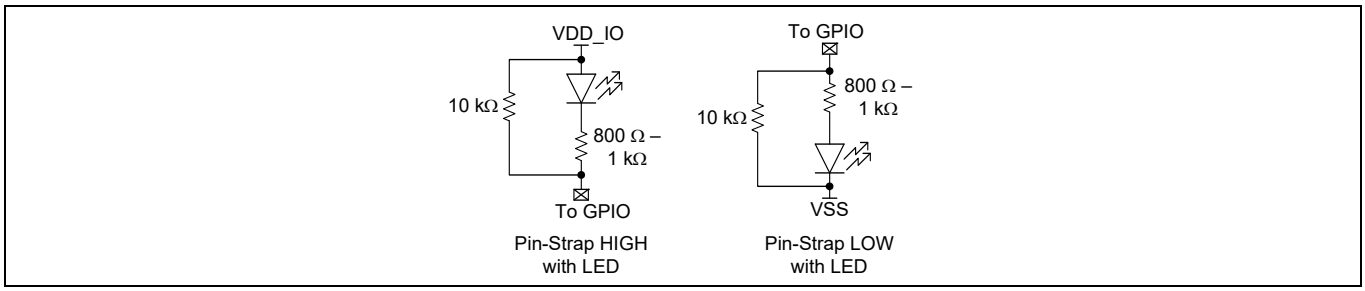


Figure 17 Pin-strap with LED or LED-only connection

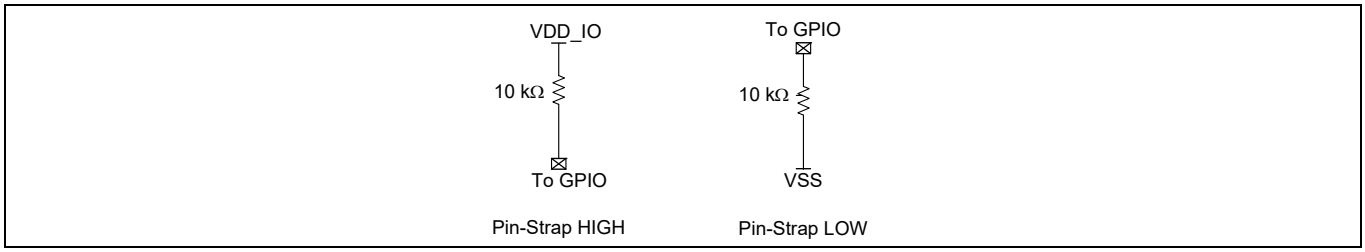


Figure 18 Pin-strap connection

Table 6 Pin-strap configuration

Pin #	Pin-strap name	Strapped '0'[10]		Strapped '1'[10]	
J4	I2C_DEV_ID[11]	ID 0: HX3 I^2C slave address (7 bits) is 0x60.		ID 1: HX3 I^2C slave address (7 bits) is 0x58	
J5	PWR_SW_POL	Power enable and overcurrent will be active LOW		Power enable and overcurrent will be active HIGH	
C2	ACA_DOCK	Disabled		Enabled	
C3	PWR_EN_SEL	Individual		Gang	
B9	PIN_STRAP[12]	No pin-strapping		Pin-strapping configuration enabled	
D2	PORT_DISABLE[1]	PORT_DISABLE[1:0] = b'00: DS1, DS2, DS3, DS4 active b'01: DS1, DS2, DS3 active b'10: DS1, DS2 active b'11: DS1 active Pin-straps cannot enable ports disabled by factory setting			
D3	PORT_DISABLE[0]				
E3	NON_REMOVABLE[1][13]	NON_REMOVABLE[1:0] = b'00: DS1, DS2, DS3, DS4 removable b'01: DS1, DS2, DS3 removable b'10: DS1, DS2 removable b'11: DS1 removable			
E4	NON_REMOVABLE[0][13]				
B3	VID[2]	Reserved: If PIN_STRAP is enabled and CY VID is required, strap VID[2:0] to '1'.			
B8	VID[1]				
H9	VID[0]				
J7	DS1_CDP_EN[14]	strapped '0'	strapped '1'	strapped '0'	strapped '1'
		DS1 CDP enabled	DS1 CDP disabled	DS1 CDP disabled	DS1 CDP enabled
B2	DS2_CDP_EN[14]	DS2 CDP enabled	DS2 CDP disabled	DS2 CDP disabled	DS2 CDP enabled
A1	DS3_CDP_EN[14]	DS3 CDP enabled	DS3 CDP disabled	DS3 CDP disabled	DS3 CDP enabled
G7	DS4_CDP_EN[14]	DS4 CDP enabled	DS4 CDP disabled	DS4 CDP disabled	DS4 CDP enabled

Notes

10. See **Figure 17** and **Figure 18**.
11. I2C_DEV_ID is valid only when HX3 is in I^2C Slave mode.
12. VID, PORT_DISABLE, NON_REMOVABLE are group straps. If one of the pins in a group strap is floating (INVALID), that group input will be INVALID and the default will not be overwritten.
13. These DS ports are exposed ports and the connected devices can be removed.
14. DSx_CDP_EN will be active LOW input when PWR_SW_POL is set to active LOW; similarly DSx_CDP_EN will be active HIGH input when PWR_SW_POL is set to active HIGH.

6.9.3 I²C configuration

When enabled for I²C configuration through the MODE_SEL pins (See **Table 5**), HX3 can be configured as an I²C master or as an I²C slave. HX3's configuration data is a maximum of 197 bytes and HX3's firmware is 10 KB. Note that HX3's firmware also includes configuration settings.

6.9.4 HX3 as I²C master

HX3 reads configurations from an external I²C EEPROM with sizes ranging from 16 to 64 KB. An example of a supported EEPROM is 24LC128. Based on the contents of the bSignature and bImageType fields in **Table 7**, HX3 performs one of the following actions:

- Loads custom configuration settings from the EEPROM when bSignature is "CY" and bImageType is 0xD4.
- Loads the Infineon-provided firmware from the EEPROM when bSignature is "CY" and bImageType is 0xB0. This firmware also includes configuration settings.
- If bSignature ≠ "CY", HX3 enumerates in the vendor-specific mode.

The contents of the EEPROM can be updated with the easy-to-use **Cypress Blaster Plus** tool. Blaster Plus is a GUI-based tool to configure HX3. Blaster Plus tool can be installed as part of **CY4609 RDK** or **CY4613 RDK**.

This tool allows to do the following:

- Download the Infineon-provided firmware from a PC via HX3's US port and store it on an EEPROM connected to HX3's I²C port.
- Read the configuration settings from the EEPROM. These settings are displayed in the Blaster Plus GUI. Modify settings as required.
- Write back the updated settings on to the EEPROM. In addition, an image file can be created for external use.

The Blaster Plus tool, user guide, and the Infineon-provided firmware are available at **EZ-USB™ HX3 USB 5 Gbps Hub Controller**.

6.9.5 HX3 as I²C Slave

An external I²C master can program the configuration settings into HX3 according to the EEPROM map in **Table 7**. Alternatively, the HX3 firmware (< 10 KB), which includes configuration settings, can also be programmed. It is recommended to use the Blaster Plus tool to create the HX3 firmware or configuration image file. HX3's I²C slave address needs to be provided while creating the image file. Refer to **Table 6** for HX3's I²C slave address.

Table 7 EEPROM map

I²C offset	Bits	Name	Default	Description
0	7:0	bSignature LSB ("C")	0x43	The first byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.
1	7:0	bSignature MSB ("Y")	0x59	The second byte of the 2-byte signature initialized with "CY" ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.

Note

15. When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
2	7:6	bImageCTL	b'00	Reserved
	5:4	I²C Speed	b'11	b'01: 400 kHz b'11: 100 kHz
	3:1	bImageCTL	b'000	Reserved
	0	bImageCTL	0	0: Execution binary file 1: Data file
3	7:0	bImageType	0xD4	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code.
4	7:0	bD4Length	40	bD4Length is defined in bytes as the length from offset 5. I²C offset bytes 0–4 are the header bytes. bD4Length = 6: Only update VID, PID, and DID bD4Length = 18: Configuration options (no PHY trim) bD4Length = 40: Configuration options with PHY trim options bD4Length > 40: User must provide valid string descriptors bD4Length > 192: Error
5	7:0	VID [7:0]	0xB4	Custom Vendor ID - LSB
6	7:0	VID [15:8]	0x04	Custom Vendor ID - MSB
7	7:0	PID [7:0]	0x04	Custom Product ID (PID) Default: 0x6504 If separate PID is used for USB 2.0, the USB 2.0 PID will be read from offset 35 and 36. Else, USB 2.0 PID = PID+2; Default: 0x6506
8	7:0	PID [15:8]	0x65	
9	7:0	DID [7:0]	00	Custom Device ID - revision - LSB
10	7:0	DID [15:8]	50	Custom Device ID - revision - MSB
11	7:0	Reserved	0	Reserved
12	7:4	SHARED_LINK_EN	b'0000	Enable shared link on DS port bit[7:4] = DS4, DS3, DS2, DS1 0: Shared link not enabled 1: Shared link enabled
	3:0	SHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a SuperSpeed port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active

Note

15.When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
13	7:0	POWER_ON_TIME	0x32	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)
14	7:4	REMOVABLE_PORTS [3:0]	b'1111	Indicates if the port is removable. bit[7:4] = DS4, DS3, DS2, DS1 0: Non-removable 1: Removable
	3:0	UHC_ACTIVE_PORTS [3:0]	b'1111	Indicates if a USB 2.0 port is active. bit[3:0] = DS4, DS3, DS2, DS1 0: Not active 1: Active
15	7	SS_LED_PIN_CONTROL	0	Port 1–4: SS LED disable 0: DS[1:4]_LED_SS are LEDs. The LED glows when the SS port is active and not in disabled state. 1: DS[1:4]_LED_SS are not LEDs
	6	GREEN_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Green LED disable 0: DS[1:4]_GREEN are LEDs 1: DS[1:4]_GREEN are not LEDs
	5	AMBER_LED_PIN_CONTROL	0	Port 1–4: USB 2.0 Amber LED disable 0: DS[1:4]_AMBER are LEDs 1: DS[1:4]_AMBER are not LEDs
	4	PORT_INDICATORS	1	Port indicators supported 0: Port indicators are not supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request has no effect. 1: Port indicators are supported on its DS-facing ports and the USB 2.0 PORT_INDICATOR request controls the indicators.
	3	COMPOUND_HUB	0	Identifies a compound device. 0: Hub is not part of a compound device. 1: Hub is part of a compound device.
	2:1	Reserved	0	Reserved
	0	GANG	0	1: Ganged power switch enable for all DS ports 0: Individual port power switch enable for each DS port

Note

15. When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
16	7	SUSPEND_INDICATOR_DISABLE	0	0: Suspend indicator enabled 1: Suspend indicator disabled
	6	SS_US_DISABLE	0	Hub mode of operation (USB 3.0 or USB 2.0) 0: USB 3.0 hub and USB 2.0 hub enabled 1: USB 3.0 hub disabled and USB 2.0 hub enabled
	5	PWR_EN_POLARITY	0	Power switch control output polarity 0: Active LOW 1: Active HIGH
	4:0	PORT_POLARITY	b'00000	USB 2.0 DP and DM swapped bit[4:0] = DS4, DS3, DS2, DS1, US 1: Port polarity swapped 0: Port polarity not swapped
17	7:5	Reserved	0	Reserved
	4	BC_ENABLE	1	0: BC v1.2 disabled 1: BC v1.2 enabled
	3	ACA_DOCK	0	If this bit is set, enable ACA-Dock on the US port
	2	APPLE_XA	0	0: Max limit for Apple charging 2.1 A 1: Max limit for Apple charging 1 A
	1	Reserved	0	Reserved
	0	GHOST_CHARGE_EN	1	0: Ghost charging disabled 1: Ghost charging enabled
18	7:4	CDP_EN[3:0]	b'1111	Per-port charging setting bit[7:4] = DS4, DS3, DS2, DS1 0: CDP disabled 1: CDP enabled
	3:0	DCP_EN[3:0]	b'0000	Per-port charging setting bit[3:0] = DS4, DS3, DS2, DS1 0: DCP disabled 1: DCP enabled

Note

15. When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
19	7	EMBEDDED_HUB	0	If this bit is set, the US is as an embedded port and VBUS connected to VBUS_US pin is ignored
	6	ILLEGAL_DESCRIPTOR	1	If this bit is set, the USB 2.0 hub controller will accept both 0x00 and 0x29 as valid descriptor types. If '0', only 0x29 will be accepted as a valid descriptor type
	5	Reserved	1	Reserved
	4	OC_POLARITY	0	Overcurrent input polarity 0: Active LOW 1: Active HIGH
	3:0	OC_TIMER	b'1000	Time in milliseconds for which the overcurrent inputs will be filtered.
20	7:0	Reserved	0	Reserved
21	7:4	Reserved	0	Reserved
	3	STRING_DESCRIPTOR_ENABLE[15]	0	0: String descriptor support is disabled 1: String descriptor support is enabled When string descriptors are not supported, the hub controller returns a non-zero index (compile-time programmable) for each string which is supported, and 0x00 for each string not supported, as indicated by this field.
	2:0	Reserved	0	Reserved
22	7:0	Reserved	0	Reserved
23	7:6	HS_AMPLITUDE_DS4	b'00	HS driver amplitude control; HS driver current: +0% to +7.5% b'00: Default b'01: +2.5% b'10: +5% b'11: +7.5%
	5:4	HS_AMPLITUDE_DS3	b'00	
	3:2	HS_AMPLITUDE_DS2	b'00	
	1:0	HS_AMPLITUDE_DS2	b'00	
24	7:6	HS_AMPLITUDE_US	b'00	
	5:2	HS_SLOPE	b'0100	HS driver slope control for all ports b'0000: +15% b'0001: +5% b'0100: Default b'0101: –5% b'1111: –7.5%
	1:0	HS_TX_VREF	b'10	Reference voltage for HS squelch (transmission envelope detector) for all ports b'00: 96 mV b'01: 108 mV b'10: 120 mV b'11: 132 mV

Note

15.When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
25	7:3	HS_PREEMP_EN[4:0]	b'00000	HS driver pre-emphasis enable – for ports DS4, DS3, DS2, DS1, and US 0: pre-emphasis is disabled 1: pre-emphasis is enabled
	2	HS_PREEMP_DEPTH_DS4[15]	0	HS driver pre-emphasis depth 0: +10% 1: +20%
	1	HS_PREEMP_DEPTH_DS3[15]	0	
	0	HS_PREEMP_DEPTH_DS2[15]	0	
26	7	HS_PREEMP_DEPTH_DS1[15]	0	
	6	HS_PREEMP_DEPTH_US[15]	0	
	5	Reserved	1	Reserved
	4:1	PCS_TX_DEEMPH_DS4	0x6	USB 3.0 Tx driver de-emphasis value 0x3: –2.75 dB 0x6: –3.4 dB (Default) 0x9: –4.0 dB
	0	Reserved	0	Reserved
27	7:4	PCS_TX_DEEMPH_DS3	0x6	USB 3.0 Tx driver de-emphasis value 0x3: –2.75 dB 0x6: –3.4 dB (Default) 0x9: –4.0 dB
	3:0	PCS_TX_DEEMPH_DS2	0x6	
28	7:4	PCS_TX_DEEMPH_DS1	0x6	
	3:0	PCS_TX_DEEMPH_US	0x6	
29	7	Reserved	0	Reserved
	6	Reserved	1	Reserved
	5:0	PCS_TX_SWING_FULL_DS4	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
30	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS3	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
31	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS2	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V

Note

15. When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
32	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_DS1	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
33	7:6	Reserved	0	Reserved
	5:0	PCS_TX_SWING_FULL_US	0x29	Adjust launch amplitude of the transmitter 0x1F – 0.9 V 0x29 – 1.0 V (Default) 0x35 – 1.1 V 0x3F – 1.2 V
34	7:0	Reserved	0	Reserved
35	7:0	UHC_PID [7:0]_LSB	0x06	USB 2.0 PID. If bD4Length ≥ 40, USB 2.0 PID will be read from this location.
36	7:0	UHC_PID [15:8]_MSB	0x65	
37–44	7:0	Reserved	0	Eight bytes reserved for future expansion
45	7:0	bLength: LangID	4	Size of LangID (defined by spec as N + 2)
46	7:0	DescType	3	String descriptor type (constant value)
47	7:0	LangID - MSB	9	String language ID - MSB of wLangID
48	7:0	LangID - LSB	4	String language ID - MSB of wLangID
49	7:0	bLength: Manufacturer (X)	54	Manufacturer string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). X ≤ 66.
50	7:0	DescType	3	String descriptor type (constant value)
51	7:0	bString: Manufacturer	‘2’, 0, ‘0’, 0, ‘1’, 0, ‘4’, 0, ‘ ‘, 0, ‘C’, 0, ‘y’, 0, ‘p’, 0, ‘r’, 0, ‘e’, 0, ‘s’, 0, ‘s’, 0, ‘ ‘, 0, ‘S’, 0, ‘e’, 0, ‘m’, 0, ‘i’, 0, ‘c’, 0, ‘o’, 0, ‘n’, 0, ‘d’, 0, ‘u’, 0, ‘c’, 0, ‘t’, 0, ‘o’, 0, ‘r’, 0	Manufacturer string: UNICODE UTF-16LE per USB 2.0 specification: “2014 Infineon Semiconductor”

Note

15. When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

Table 7 EEPROM map *(continued)*

I²C offset	Bits	Name	Default	Description
49 + X	7:0	bLength: Product (Y)	22	Product string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). Y ≤ 66.
50 + X	7:0	DescType	3	String descriptor type (constant value)
51 + X	7:0	bString: Product	‘C’, 0, ‘Y’, 0, ‘-’, 0, ‘H’, 0, ‘X’, 0, ‘3’, 0, ‘ ‘, 0, ‘H’, 0, ‘U’, 0, ‘B’, 0	Product string: UNICODE UTF-16LE per USB 2.0 specification: “CY-HX3 HUB”
49 + X + Y	7:0	bLength: Serial Number (Z)	22	Serial number string length (“bLength: LangID + bLength: Manufacturer + bLength: Product + bLength: Serial Number” should be less than or equal to 152 bytes). Z ≤ 66.
50 + X + Y	7:0	DescType	3	String descriptor type (constant value)
51 + X + Y	7:0	bString: Serial Number	‘1’, 0, ‘2’, 0, ‘3’, 0, ‘4’, 0, ‘5’, 0, ‘6’, 0, ‘7’, 0, ‘8’, 0, ‘9’, 0, ‘A’, 0	Serial number string: UNICODE UTF-16LE per USB 2.0 specification: “123456789A”

Note

15.When the string descriptor supports LangID, manufacturer, product and serial number, the serial number must be unique for each device.

7 EMI

EZ-USB™ HX3 meets the EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. EZ-USB™ HX3 tolerates EMI conducted by aggressors outlined by the above specifications and continues to function as expected.

8 ESD

EZ-USB™ HX3 has a built-in ESD protection on all pins. The ESD protection level provided on these ports is 2.2 kV Human Body Model (HBM) based on the JESD22-A114 specification.

9 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 8 Absolute maximum ratings

Parameter	Ratings
Storage temperature	–65°C to +150°C
Operating temperature	–40°C to +105°C for QFN package –40°C to +85°C for BGA package
Electrostatic discharge voltage	2200 V
Oscillator or crystal frequency	26 MHz ± 150 ppm
I/O voltage supply	3 V to 3.6 V
Maximum input sink current per I/O	4 mA

10 Electrical specifications

HX3 meets all USB-IF Electrical Compliance specifications.

10.1 DC electrical characteristics

Table 9 DC electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
DVDD12	1.2-V core supply	–	1.14	1.2	1.26	V
VDD_EFUSE	eFuse supply	Normal operation	1.14	1.2	1.26	V
		Programming	2.5	2.6	2.7	V
AVDD12	1.2-V analog supply	–	1.14	1.2	1.26	V
VDD_IO	3.3-V I/O supply	–	3	3.3	3.6	V
AVDD33	3.3-V analog supply	–	3	3.3	3.6	V
V_{IH}	Input HIGH voltage	–	0.7 × VDD_IO	–	VDD_IO	V
V_{IL}	Input LOW voltage	–	0	–	0.3 × VDD_IO	V
V_{OH}	Output HIGH voltage	Output high voltage at $I_{OH} \leq +4$ mA	2.4	–	–	V
V_{OL}	Output LOW voltage	Output low voltage at $I_{OL} \geq -4$ mA	–	–	0.4	V
I_{OS}	Input sink current	LED GPIO usage	–	–	4	mA
I_{IX}	Input leakage current	All I/O signals held at VDD_IO or GND	–1	–	1	µA
I_{OZ}	Output HI-Z leakage current	–	–	–	10	µA
I_{CC}	1.2-V supplies combined operating current	–	–	410	526	mA
I_{CC}	3.3-V supplies combined operating current	–	–	260	286	mA
V_{RAMP}	Voltage ramp rate on core and I/O supplies	Voltage ramp must be monotonic	0.2	–	50	V/ms
V_N	Noise level permitted on core and I/O supplies	Max p-p noise level permitted on all supplies except AVDD	–	–	100	mV
V_{N_USB}	Noise level permitted on AVDD12 and AVDD33 supply	Max p-p noise level permitted USB supply	–	–	20	mV

10.2 Power consumption

Table 10 provides the power consumption estimates for HX3 under different conditions. **Table 11** summarizes the power consumption for various combinations of devices connected to DS ports.

For example, to calculate the HX3 power consumption for three SS devices connected to DS ports (and no device connected to one DS port), and a US port connected to a USB 3.0 host:

Power consumption = [a] + 2*[g] = 492.5 + 2*76 = 644 mW

[a] is the active power consumption for the US port connected to a USB 3.0 host and the SS device connected to the DS port.

[g] is the incremental power consumption for an additional SS device connected to the DS port.

Table 10 Power consumption estimates for various usage scenarios

Device condition	Number and speed of DS ports connected	Typical consumption			Comment
		Supply current (mA)		Power (mW)	
		1.2 V	3.3 V		
Suspend [16]	NA	12.0	7.1	37.8	–
Active power with USB 3.0 host [17]	1 SS	204.1	75.0	492.5	[a]
	1 HS	51.2	45.2	210.7	[b]
	1 FS	51.2	34.0	173.7	[c]
	1 SS + 1 HS	218.0	103.4	602.9	[d]
Active power with USB 2.0 host [17, 18]	1 HS	51.2	45.2	210.7	[e]
	1 FS	51.2	34.0	173.7	[f]
Incremental active power for additional DS port	SS	39.4	8.7	76.0	[g]
	HS	7.0	19.8	73.7	[h]
	FS	7.0	14.2	55.2	[i]
Active power saving per disabled DS port [19]	–	10.6	9.6	44.4	[j]

Notes

16. US port in low-power state (SS in U3 and USB 2.0 in L2).
17. All four DS ports are enabled.
18. US SS disabled using configuration options. See **Table 7** for I^2C configuration options.
19. Power saving applicable only with a USB 3.0 host. DS ports can be disabled through configuration options. See **Table 6** for pin-strapping and **Table 7** for I^2C configuration options.

Table 11 Power consumption under various configurations

Configuration	Number of DS devices connected with data transfer	Typical consumption			Comment
		Supply current (mA)		Power (mW)	
		1.2 V	3.3 V		
USB 3.0 4-port hub (USB 3.0 host)	4 SS devices	322	101	720	[a] + 3*[g]
	3 SS + 1 HS devices	297	121	755	[d] + 2*[g]
	3 SS devices	283	92	644	[a] + 2*[g]
USB 3.0 4-port hub with one port disabled (USB 3.0 host)	3 SS devices	272	83	600	[a] + 2*[g] - [j]
	2 SS + 1 HS devices	247	103	634	[d] + [g] - [j]
Shared link with six DS ports	4 SS + 2 HS devices	343	149	904	[d] + 3*[g] +[h]
USB 2.0 4-port hub (USB 2.0 host)	4 HS devices	72	105	432	[e] + 3*[h]
	3 HS + 1 FS devices	72	99	413	[e] + 2*[h] + [i]

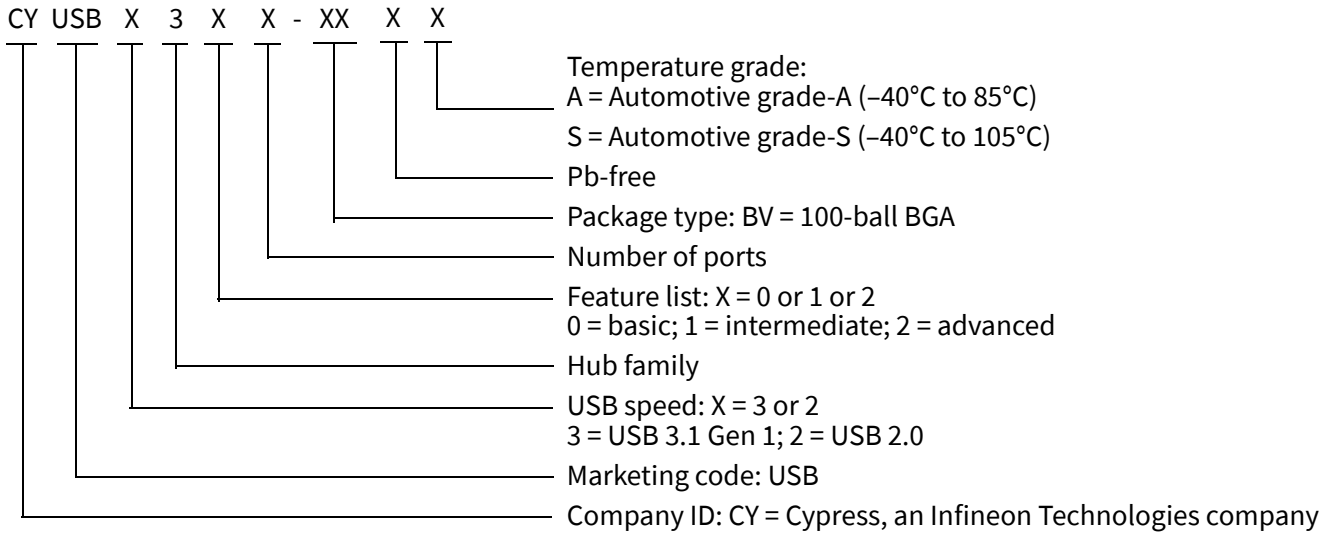
11 Ordering information

Table 12 lists HX3's ordering information. The table contains only the part numbers that are currently available for order. Additional part numbers for industrial temperature range can be made available on request. For more information, visit the Infineon **website** or contact the local sales representative.

Table 12 Ordering information

Product	Number of DS ports	Number of shared link ports	Ghost charge	ACA-Dock	Package
CYUSB3302-BVXA	2 (USB 3.0)	0	Yes	No	100-ball BGA
CYUSB3314-88LTXS	4 (USB 3v.0)	0	Yes	No	88L QFN
CYUSB3324-BVXA	4 (USB 3.0)	0	Yes	Yes	100-ball BGA
CYUSB2302-68LTXS	2 (USB 2.0)	0	Yes	No	68LD QFN
CYUSB2302-BVXA	2 (USB 2.0)	0	Yes	No	100-ball BGA
CYUSB2304-BVXA	4 (USB 2.0)	0	Yes	No	100-ball BGA
CYUSB2312-88LTXS	2 (USB 2.0)	0	Yes	No	88L QFN

11.1 Ordering code definitions



12 Packaging

Table 13 Package characteristics

Parameter	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	–40	–	85	°C
T_J	Operating junction temperature	–40	–	125	°C
T_{JA}	Package J_A (100-ball BGA)	–	35	–	°C/W
T_{JC}	Package J_C (100-ball BGA)	–	12	–	°C/W

Table 14 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
68LD QGN	260°C	30 s
88L QFN	260°C	30 s
100-ball BGA	260°C	30 s

Table 15 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68LD QFN	MSL 3
88LQFN	MSL 3
100-ball BGA	MSL 3

13 Package diagram

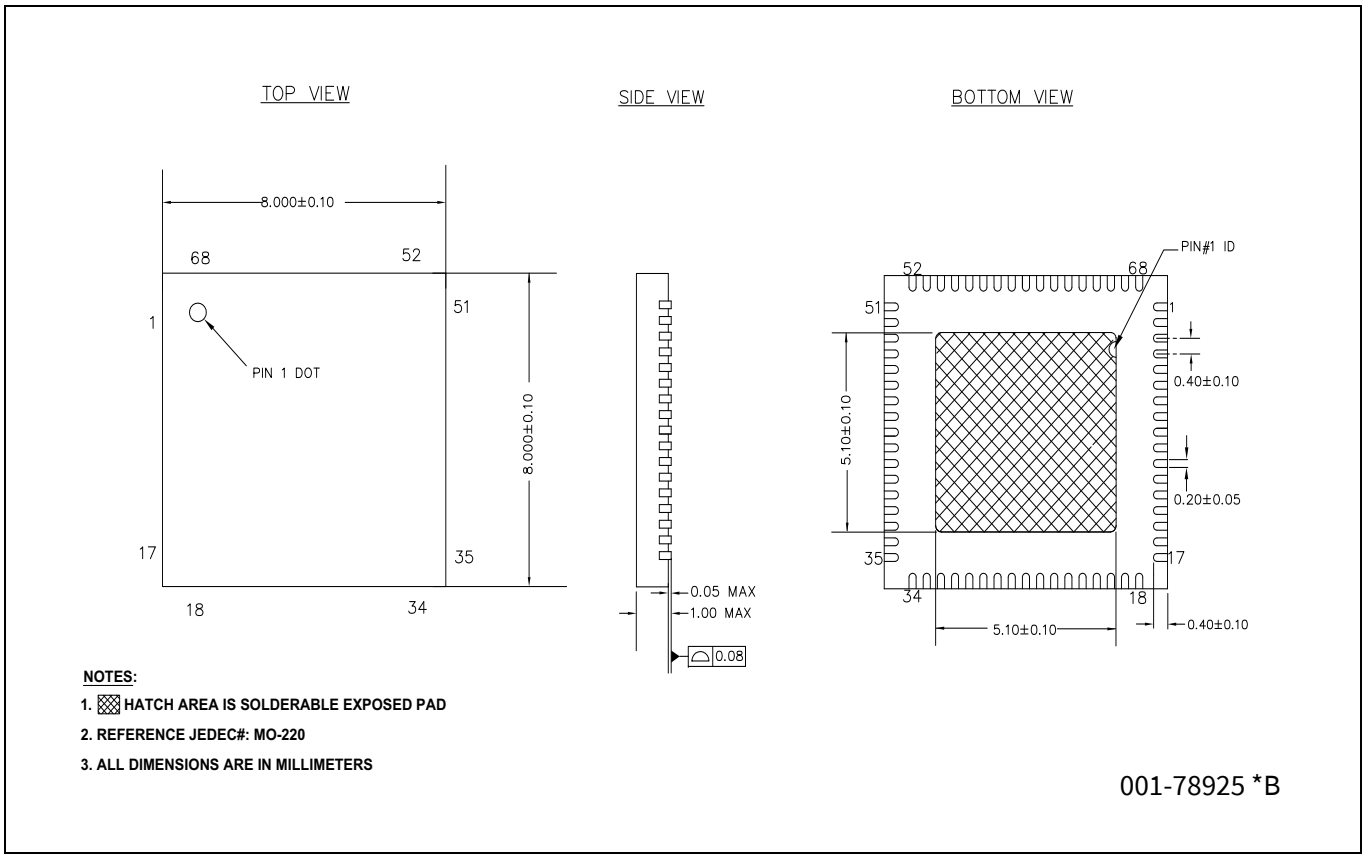


Figure 19 68LD QFN (8 × 8 × 1.0 mm) LT68B 5.1 × 5.1 mm EPAD (SAWN), Package outline (PG-VQFN-68)

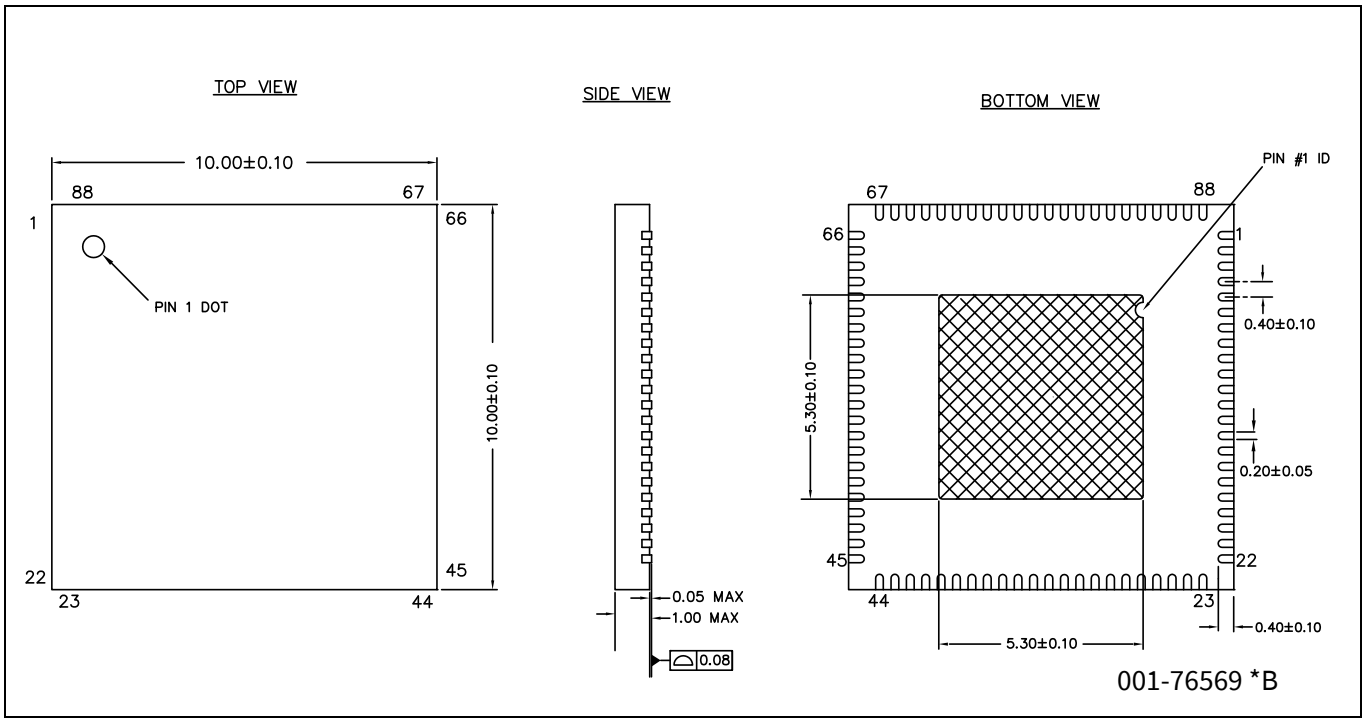
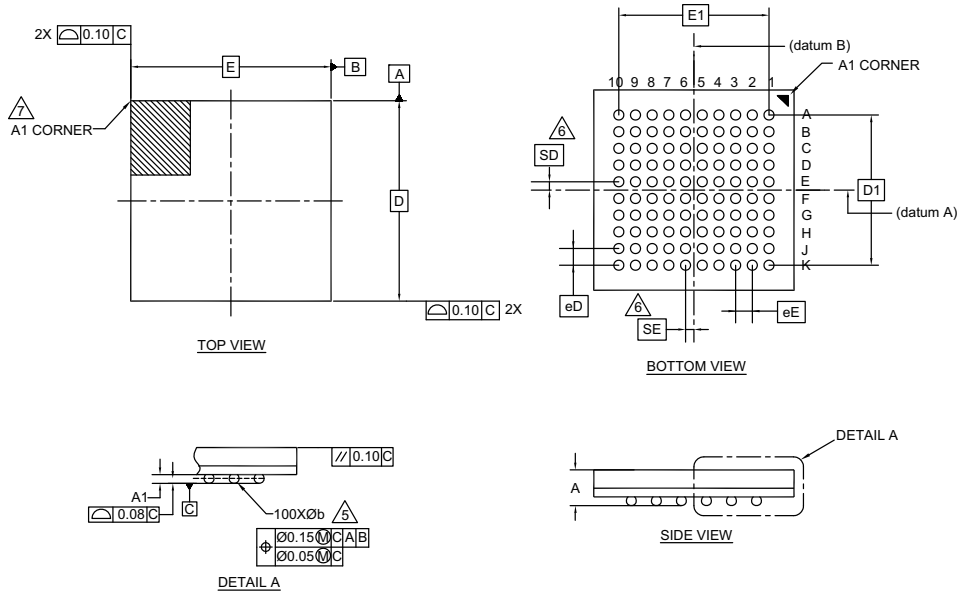


Figure 20 88L QFN (10 × 10 × 1.0 mm) LT88B 5.3 × 5.3 mm EPAD (SAWN), Package outline (PG-VQFN-88)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	4.50 BSC		
E1	4.50 BSC		
MD	10		
ME	10		
N	100		
Ø b	0.25	0.30	0.35
eD	0.50 BSC		
eE	0.50 BSC		
SD	0.25 BSC		
SE	0.25 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-195C.

51-85209 *F

Figure 21 100-ball VFBGA (6.0 × 6.0 × 1.0 mm) R2A100/BZ100, package outline (PG-VFBGA-100)

14 Acronyms

Table 16 Acronyms used in this document

Acronym	Description
ACA	Accessory Charging Adapter
ASSP	Application-Specific Standard Product
BC	Battery Charging
CDP	Charging Downstream Port
DS	Downstream
DCP	Dedicated Charging Port
DNU	Do Not Use
DWG	Device Working Group
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	Full-Speed
FW	FirmWare
GND	GrouND
GPIO	General-Purpose Input/Output
HS	Hi-Speed
ISP	In-system programming
I/O	Input/Output
LS	Low-speed
NC	No Connect
OTG	On-The-Go
PID	Product ID
POR	Power-on reset
ROM	Read-only memory
SCL	Serial clock
SDA	Serial data
SS	SuperSpeed
TT	Transaction translator
US	Upstream
VID	Vendor ID

15 Reference documents

[1] USB 2.0 specification

[2] USB 3.1 specification

[3] Battery Charging specification

16 Document conventions

16.1 Units of measure

Table 17 Units of measure

Symbol	Unit of measure
°C	degree celsius
W	ohm
Gbps	gigabit per second
KB	kilobyte
kHz	kilohertz
kΩ	kiloohm
Mbps	megabit per second
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
V	volt

Revision history

Document revision	Date	Description of changes
**	2016-05-05	New datasheet.
*A	2017-05-30	Changed datasheet status from Preliminary to Final. Updated document title to read as "HX3 Automotive SuperSpeed USB (USB 3.1 Gen 1) Hub". Updated temperature range for Automotive Grade-A and Automotive Grade-S devices in all instances across the document. Updated to new template. Completing Sunset Review.
*B	2017-11-29	Removed Automotive Grade-S devices related information in all instances across the document. Removed CYUSB3312, CYUSB3314, CYUSB3324, and CYUSB3328 parts related information in all instances across the document. Updated **Features** Updated description. Updated **Application** Updated description. Updated **Pin information** Updated **Table 3** (Removed 68-pin QFN related information). Removed figure "HX3 100-Ball BGA Pinout for CYUSB3312". Updated **System interfaces** Updated **Configuration options** Updated **Pin-Strap configuration** Updated description. Updated **Electrical specifications** Updated **Power consumption** Updated **Table 11**. Updated **Ordering information** Updated **Table 12** (Updated part numbers).
*C	2017-12-14	Updated **Package diagram** Updated **Table 13**.
*D	2023-07-22	Updated **Features** Updated description. Updated **Ordering information** Updated **Table 12** (Updated part numbers). Migrated to Infineon template. Completing Sunset Review.

Document revision	Date	Description of changes
*E	2024-03-04	Updated the title to “EZ-USB™ HX3 Automotive USB 3.1 Gen 1 (5 Gbps) Hub” Replaced SuperSpeed with USB 3.1 Gen 1 (5 Gbps) throughout the datasheet. Added Automotive qualification, Package options, Temperature range in the **Features** section. Added **Figure 2**. Added CYUSB3314 in **Table 1**. Added the title **“Pin information for 100-ball BGA”** on page 12. Added links in **“HX3 as I2C master”** on page 31. Updated **Figure 1**, **Figure 4**, **Figure 6** and **Figure 7**. Updated **Table 12**. Added links in **Reference documents**. Updated HX3 to EZ-USB™ HX3 throughout the datasheet. Updated all the cypress links to Infineon links. Updated the **Table 3** and **Table 4**. Added CYUSB3314-88LTXS and CYUSB2302-68LTXS in **Table 12**. Updated **“Ordering code definitions”** on page 45. Added **Figure 19** and **Figure 20**. Updated **Figure 8** through **Figure 14**. Updated **Figure 14** title to 88L QFN pinout for CYUSB3314 and CYUSB2312. Added CYUSB2312 and updated **Table 4**.

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