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High-performance SiC MOSFET technology for power electronics design

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The performance potential of SiC (https://www.powerelectronicsnews.com/?s=CoolSic+technology) is indisputable. The key challenge to be mastered is to determine which design approach achieves the biggest success in applications.

By Dr. Peter Friedrichs, Infineon Technologies

Advanced design activities are focusing on the field of specific on-resistance as the major benchmark parameter for a given technology. However, it is essential to find the right balance between the primary performance indicators like resistance and switching losses and the additional aspects relevant for actual power electronics designs, e.g. sufficient reliability.

Device design philosophy

A suitable device concept should allow a certain design freedom in order to adapt to the needs of various mission profiles without significant changes in processing and layout. However, the key performance indicator will still be a low area-specific resistance of a chosen device concept, ideally in combination with the other listed parameters. Figure 1 lists a few parameters that are considered essential, more could be added.

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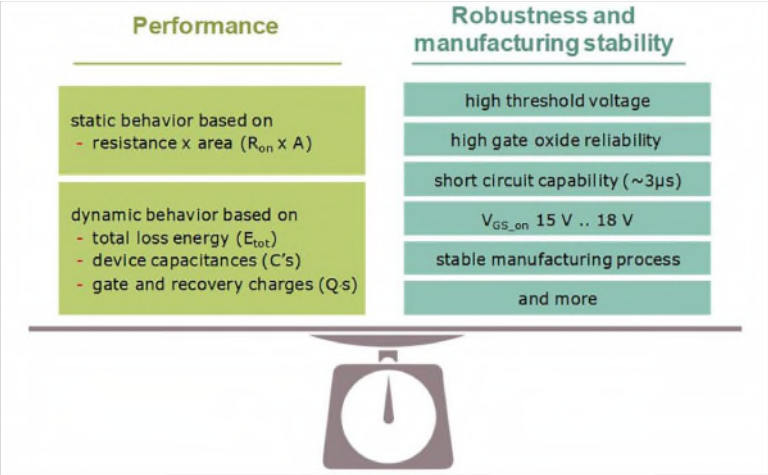

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Figure 1: selected parameters (right) which have to be balanced with performance indicators (left) of a SiC MOSFET

One of the most important acceptance criteria is the reliability of the device under the operating conditions of its target applications. The major difference to the established silicon device world is the fact that SiC components operate at much higher internal electric fields. Related mechanisms need to be analyzed carefully. What they have in common is that the total resistance of a device is defined by the series connection of contact resistances at drain and source, including the highly doped areas close to the contact, the channel resistance, the resistance of the JFET area, and the drift zone resistance (see figure 2). Note that in high-voltage silicon MOSFETs, the drift zone clearly dominates the total resistance; in SiC devices, the part can be designed with a significantly higher conductivity as stated above.

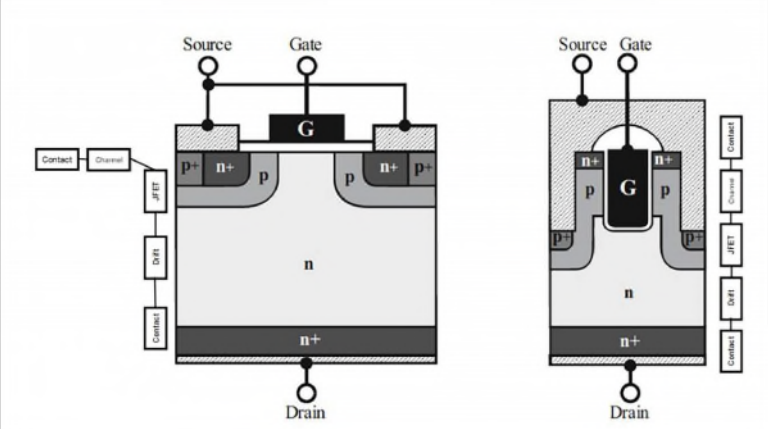

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Figure 2: Sketch of planar DMOS SiC MOSFETs (left), and vertical trench, TMOS SiC MOSFETs, and the corresponding location of resistance-relevant contributions

Regarding the key MOSFET element, the SiC-SiO_2 interface, the following differences as compared to silicon have to be considered:

- SiC has a higher surface density of atoms per unit area compared to Si, resulting in a higher density of dangling Si- and C- bonds; defects located in the gate oxide layer near the interface may appear in the energy gap, and act as traps for electrons [1].
- The thickness of thermally grown oxides strongly depends on the crystal plane.
- SiC devices operate at much higher drain-induced electric fields in the blocking mode compared to their Si counterparts (MV instead of kV), which requires measures to limit the electric field in the gate oxide to maintain reliability of the oxide in blocking stage [2]. See also figure 3: for TMOS, the critical point is the trench corner, and for DMOS, the center of a cell.
- SiC MOS structures show for a given electric field a higher Fowler-Nordheim current injection compared to Si devices due to a smaller barrier height. Consequently, the electric field on the SiC side of the interface must be limited [3,4].

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The above-mentioned interface defects result in a very low channel mobility. Therefore, they cause a high contribution of the channel to the total on-resistance. Thus, the advantage of SiC versus silicon in the form of a very low drift zone resistance is diminished due to the high channel contribution. An observed way to overcome this dilemma is to increase the electric field applied across the oxide in on-state, either higher gate source (V_{GS}) bias for turn-on or comparably thin gate oxides. The applied electric fields exceed the values usually used in silicon-based MOSFET devices (4 to 5 MV/cm vs. 3 MV/cm max. in silicon). Such high fields in the oxide in the on-state can potentially accelerate wear, and limit the capability of screening remaining extrinsic oxide defects [1].

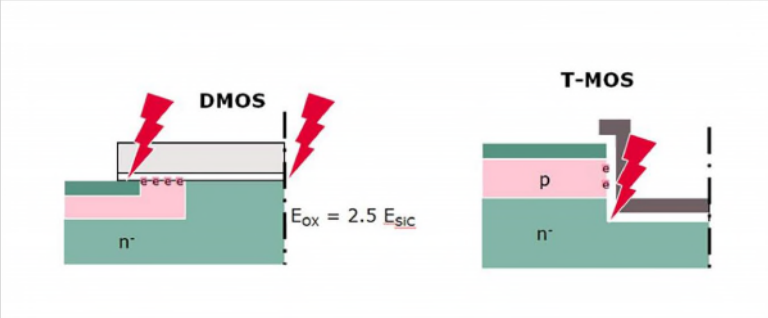

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Figure 3: Left: Typical structure of a planar MOSFET (half-cell) revealing two sensitive areas with respect to oxide field stress. Right: Typical structure of a trench MOSFET (half-cell), critical issue is the oxide field stress at the trench's corners.

Based on these considerations, it is clear that planar MOSFET devices in SiC actually have two sensitive areas with respect to oxide field stress, as sketched in the left part of figure 3. First, the discussed stress in reverse mode in the highest electric field area close to the interface between drift region and gate oxide, and secondly, the overlap between gate and source which is stressed in on-state.

A high electric field in on-state is seen as more dangerous, since no device design measures are in place which could reduce the field stress during on-state as long as the on-resistance performance has to be guaranteed. Infineon's overall goal is to combine the low R_{DSon} offered by SiC with a working mode in which the part operates in the well-known safe oxide field-strength conditions. Hence, it was decided to forgo DMOS technology and to focus on trench-based devices from the beginning. Moving away from the planar surface with its high-defect density towards other more favorable surface orientations enables a low channel resistance at low oxide fields. These boundary conditions are the baseline for transferring quality assurance methodologies established in the silicon power semiconductor world in order to guarantee FIT rates expected in industrial and automotive applications.

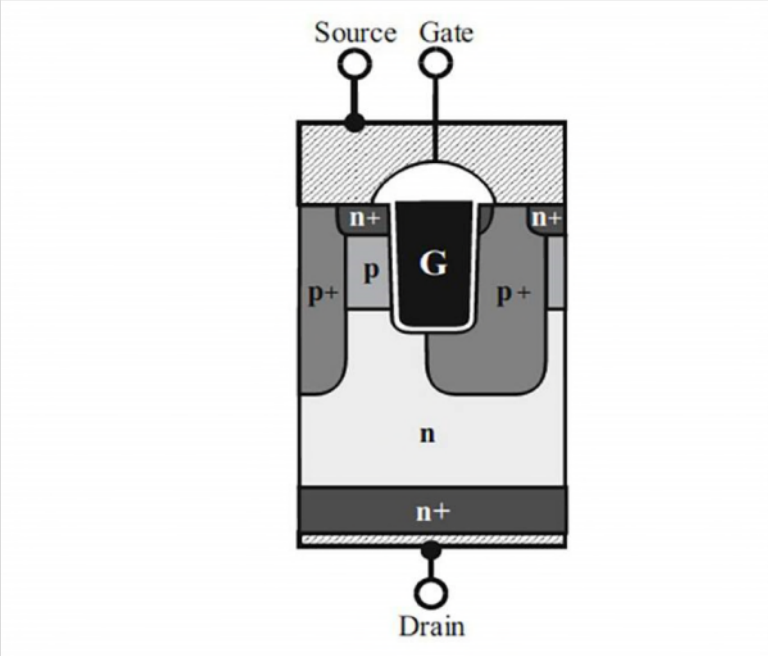

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Figure 4: Sketch of the CoolSiC™ MOSFET cell structure

The CoolSiC™ MOSFET cell design was developed to limit the electric field in the gate oxide in on-state as well as in off-state (see figure 4). At the same time, an attractive specific on-resistance for the 1200 V class is provided, achievable even in mass production in a stable and reproducible way. The low on-resistance is ensured driving voltage levels of only V_{GS} = 15 V combined with a sufficiently high gate-source-threshold voltage of 4.5 V typically, being a benchmark in the landscape of SiC transistors. Special features of the design include the orientation of the channel at a single crystallographic orientation via a self-aligned process. This ensures highest channel mobility and narrow threshold voltage distributions. Another feature is the deep p-trenches intersecting the actual MOS trench in the center in order to allow narrow p+ to p+ pitch sizes for effective screening of the lower oxide corner.

Static performance – first quadrant operation

The key parameter of the static output characteristic of a MOSFET is the total resistance $R_{DS(ON)}$.The typical on-resistance of the CoolSiC™ MOSFET is defined at room temperature and for a V_{GS} = 15 V (figure 5, left). The threshold voltage V_{GS_TH} follows the physics of the device, and drops with temperature as shown in figure 5 on the right.

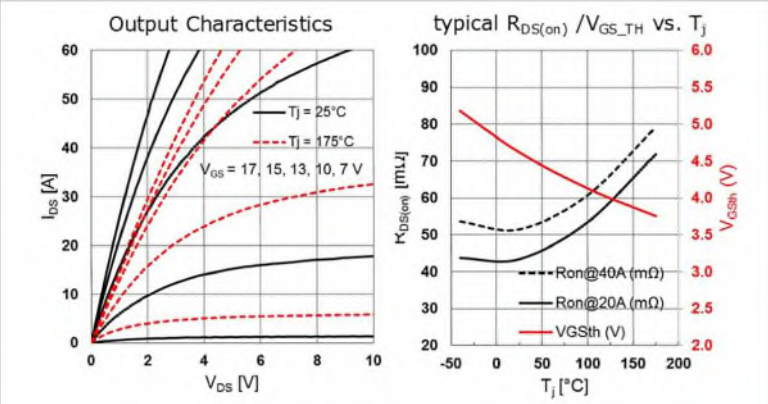

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Figure 5: CoolSiC™ MOSFET output characteristics (example 45 mOhm 1200 V type) for room temperature and 175°C (left) and dependence of Ron and VGS_TH on temperature (right)

The positive temperature coefficient of the on-resistance (figure 5, right) as an outcome of the low-channel defect density makes the devices predestined for use in paralleling. This is another significant difference to DMOS devices, which usually show a weaker dependence of the resistance on temperature due to the high density of defects in the channel.

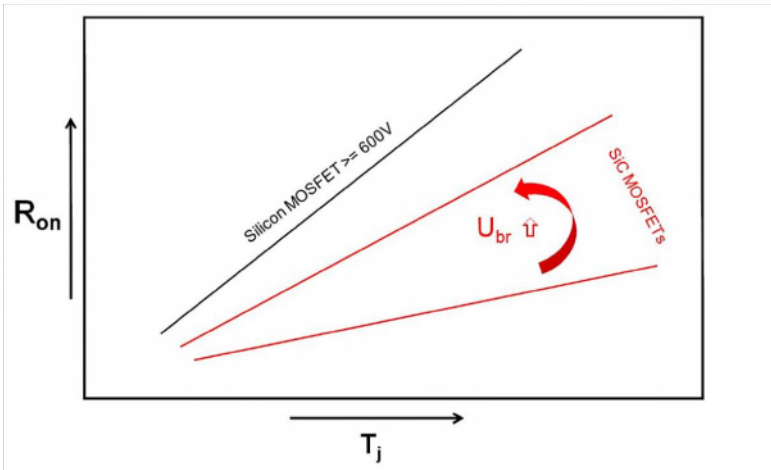

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Figure 6: Principal behavior of the on-resistance for MOSFETs as a function of temperature, comparison between Si and SiC as well as impact of the blocking voltage

This DMOS "feature" at first glance sounds attractive; however, with progress towards lower on-resistances, the physically justified temperature dependence of the drift zone will increasingly dominate the total on-resistance. Thus, SiC MOSFETs will become more

silicon-like. However, it should be noted that even in a mature state the actual temperature coefficient of SiC MOSFETs would be lower than for silicon devices at the same blocking voltage due to the higher absolute doping densities. Furthermore, the temperature dependence of the on-resistance will be more pronounced for higher blocking voltages due to the increasing contribution of the drift zone to the total resistance. The qualitative behavior is summarized in figure 6.

Static performance – third quadrant operation

In contrast to IGBTs, a vertical MOSFET such as the CoolSiC™ device offers conduction in reverse mode via the body diode, practically a freewheeling diode. However, due to the band gap of SiC, the knee voltage of this diode is relatively high (around 3 V), so that a continuous operation would result in high conduction losses. Consequently, it is mandatory to use the well- known synchronous rectification concept. The diode works just for a short dead time as a diode (see above sections). After this period, the channel is turned on again by applying a positive V_{GS} (like in the first quadrant mode).

This operation scheme offers very low conduction losses in the third quadrant mode, since no knee voltage is in place achieving the same resistance as in first quadrant mode. In fact, the resistance is even slightly lower, since the JFET impact is reduced due to a negative feed-forward impact of the now inverted current flow direction. Figure 6 illustrates the third quadrant operation (I-V characteristic for different gate voltages). Please note that due to the p-n diode structure also a certain pulse current handling capability (higher than in forward mode) can be achieved.

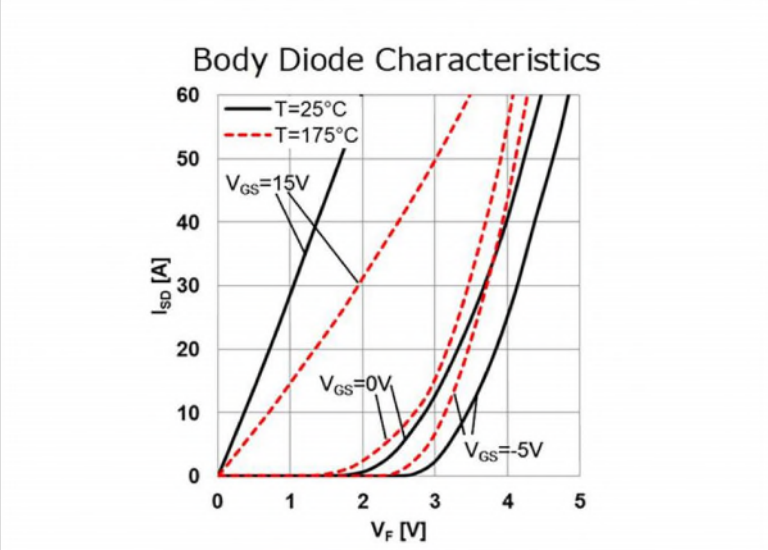

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Figure 7: Body diode I-V behavior for a 45 mOhm CoolSiC™ MOSFET

Dynamic performance

Being a unipolar device, the dynamic performance of the SiC-MOSFET is largely governed by its capacitances. The device was designed to have a small gate-drain reverse capacity C_{rss} compared to the input capacity C_{iss}. This is beneficial for suppressing parasitic turn-on, which can prevent the use of sophisticated gate driver circuitry when operated in a half-bridge configuration. Many CoolSiC™ MOSFET products can be turned off safely even with 0 V at the gate, since in addition to the favorable capacitance ratio the threshold voltage is sufficiently high. The total device capacitances as a function of temperature are summarized in figure 8 (left).

Figure 8 (right) displays the typical switching losses of a half bridge with single devices mounted in a 4-pin TO-247 housing as a function of drain current. The turn-off energy E_{off} depends only slightly on the load current, since it is dominated by capacities, whereas the turn-on energy E_{on} increases linearly with current, and dominates the total losses E_{tot}. Based on the status from mid-2019, it should be emphasized that the CoolSiC™ MOSFET shows the lowest E_{on} among the commercially available 1200 V SiC MOSFETs. E_{on} and E_{off} are practically independent of temperature. Important to note is the fact that the actual housing design has a significant impact on switching losses, mainly on turn-on losses.

Especially effective is the use of Kelvin contacts, which practically separate the load path from the control path in terms of current, and thus, help to prevent di/dt induced feedback loops to the gate signal increasing the dynamic losses.

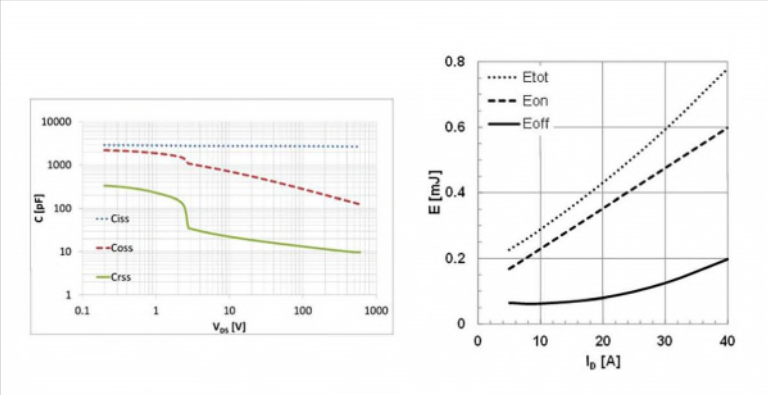

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Figure 8: Typical device capacitance vs. drain-source voltage for a 45 mOhm CoolSiC™ MOSFET (left) and related switching energies (right) as a function of drain current (for VGS = 15 / -5 V, RGext = 4.5 Ω, VDS = 800 V, Tvj =175°

In general, it is essential to implement fast-switching SiC transistors with low capacitances and gate charges in certain packages only. Major criteria include good thermal performance due to the high-loss power density (absolute losses are reduced with SiC of course, but the remaining ones are concentrated in very small areas). Another criterion is a low stray inductance for managing high di/dt slopes without critical voltage peaks. Finally, especially in the case of multichip packages with more die in parallel, a symmetric inner module design based on the strip line concept [5] is mandatory. Current module packages offering such features are the EASY platform by Infineon for modules, or the TO247 family, respectively TO263-7, for discrete housing.

The gate charge curve for CoolSiC™ MOSFETs is usually different from the typical shape of silicon power devices; in particular, there is no clear Miller plateau visible, as indicated in figure 9 left. The total gate charge Q_{tot} amounts to typically 75 nC for I_D = 30 A, V_{DS} = 800 V and R_G = 3.3 kΩ at $V_{GS(off)}$=-5 V to $V_{GS(on)}$ = 15 V.

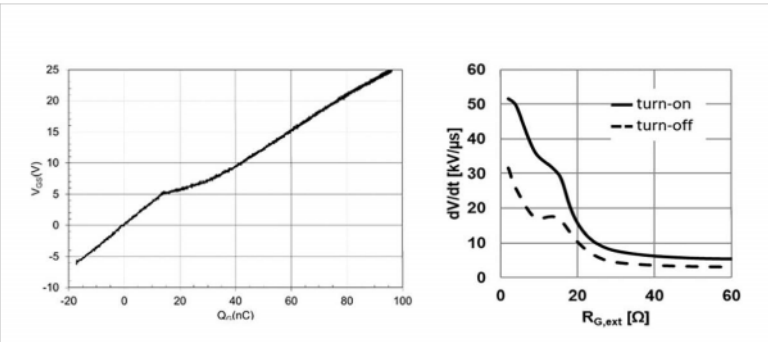

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Figure 9: Typical gate charge curve for a 45 mOhm 1200 V CoolSiC™ MOSFET (left) and controllability of the switching speed via Rg (right)

In many cases, there might be a need to adjust the switching speed (dv/dt) in order to deal with oscillations, etc. One benefit of MOSFETs is the simple way of adjusting the slopes via the gate resistor. Combined with the right driver circuit, it may even be different for turn-on and turn-off. Figure 9 on the right shows the corresponding behavior for Infineon's 45 mOhm 1200 V CoolSiC™ MOSFET.

Figure 10 depicts the short-circuit waveforms for 45 mOhm 1200 V CoolSiC™ MOSFET in TO-247 4-pin and TO-247 3-pin, at a DC voltage of V_{DS} = 800 V, which differs significantly from the IGBT. Initially, the drain current increases rapidly and reaches the peak current level. Because of fast turn-on with the Kelvin-source design, the TO-247 4-pin current rises faster, and has less self-heating at the beginning of the SC event with high peak current exceeding 300 A, while the TO-247 3-pin has a smaller peak current. The major

reason is a negative feedback induced by the di/dt against the applied V_{GS} in the case of the 3-pin device. Since this effect is eliminated in the Kelvin connection solution, which enables faster switching, the current can also rise to higher values for the 4-pin device before the saturation effect takes place.

After peak current, the drain current is significantly decreased to about 150 A. This is due to the reduction in carrier mobility and JFET effect with temperature increase and self-heating. The test waveform shows clean, robust behavior, which proves the typical 3 µs SC capability for both packaged TO-247 CoolSiC™ MOSFET and power modules (currently 2 µs according to the related target application requirements). Infineon's CoolSiC™ MOSFET is the first device with a guaranteed short circuit in the data sheet.

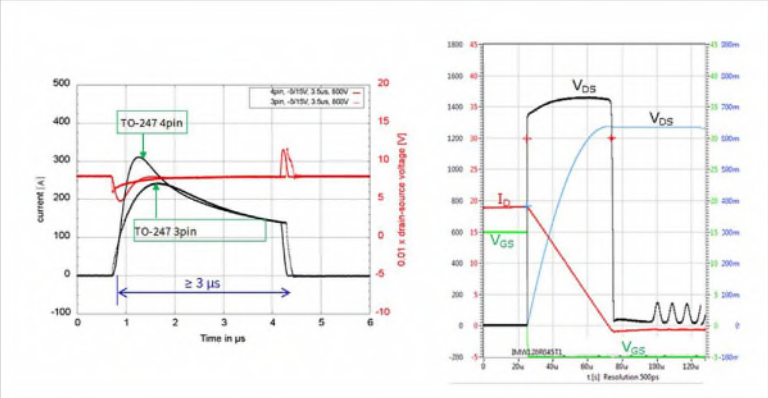

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Figure 10: Typical short circuit as a function of duration time at 25°C (left); avalanche behavior of a 1200 V device, turn-off of an unclamped inductive load of 3.8 5mH at 60 V (right)

The new 650 V class devices are accompanied with an avalanche rating in the data sheet to meet the requirements of the target-application power supplies. In general, the CoolSiC™ MOSFET technology shows high ruggedness under avalanche; figure 10, on the right, depicts the typical behavior of a 1200 V component

FIT rates and gate-oxide reliability

Besides performance, reliability and ruggedness are the most discussed topics for SiC MOSFETs. Ruggedness is defined as the capability of a device to withstand certain extraordinary stress events, for example, short-circuit performance or pulse-current handling capability. Reliability covers the stability of the device under nominal operating conditions over the targeted application lifetime. The effects relevant to reliability include the drift of certain electrical parameters or catastrophic failures. For hard failures, the quantification is usually done in the form of FIT rates, which actually state how many devices of a certain type are allowed to fail over a certain period. FIT rates in high-power silicon devices are mostly governed today by cosmic ray effects.

In the case of SiC, an additional influence from gate-oxide reliability needs to be considered due to the oxide field stress as discussed earlier. Thus, as indicated in figure 11, the total FIT rate is the sum of cosmic ray FIT rates and oxide FIT rates. For cosmic ray stability, a similar approach can be applied such as the one typical in the silicon sector. Here, FIT rates are obtained experimentally for a certain type of technology, and based on the results, in combination with the application targets, a design can be implemented that meets the FIT rates, usually achieved by optimizing the electric field distribution in the drift zone. For the oxides FIT rates, a screening process needs to be applied to reduce the FIT rates, as defect densities in SiC are still quite high compared to silicon (in the case of Infineon's Si power devices, the screening of gate oxides still takes place as a quality assurance measure).

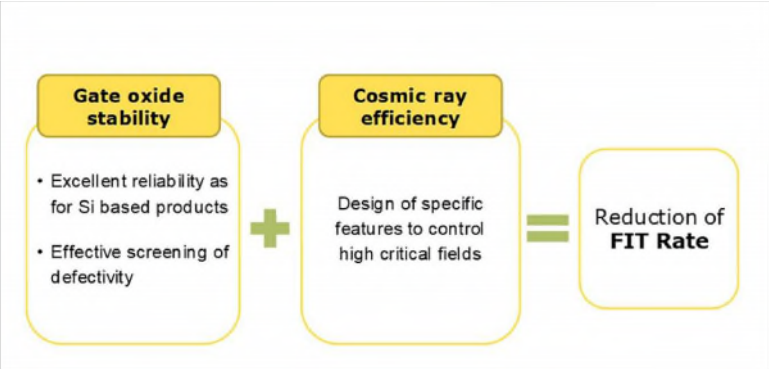

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Figure 11: FIT rate constitution in the case of SiC MOSFETs

The challenge of the gate-oxide reliability of SiC MOS devices is for example to guarantee a maximum failure rate of less than 1 FIT under given operation conditions in industrial applications (as is available today for IGBTs). Since the intrinsic quality and properties of SiO_2 on SiC and on Si are almost identical, Si MOSFETs and SiC MOSFETs of the same area and oxide thickness can withstand roughly the same oxide field for the same time (same intrinsic lifetime). Of course, this is only valid if the devices do not contain defect-related impurities, i.e., extrinsic defects. In contrast to Si MOSFETs, SiC MOSFETs exhibit a much higher extrinsic defect density in the gate oxide.

Devices with extrinsic defects break down earlier in comparison to devices that are free of defects. Defect-free devices will fail much later due to intrinsic wear. Typically, intrinsic failure times are far less frequent under normal application conditions if the bulk oxide thickness is sufficient. Consequently, the oxide FIT rate within the typical chip lifetime is exclusively determined by extrinsic defects.

The challenge of guaranteeing a sufficient reliability of the gate oxide of silicon carbide MOSFETs is to reduce the number of devices being affected by extrinsic defects from an initially high number at the end of process (e.g. 1 %) to an acceptably low number when the products are shipped to the customer (e.g. 10 ppm). One well-established way to achieve this is to apply electrical screening [2].

During electrical screening, each device is subjected to a gate-stress pattern. The stress pattern is selected to destroy devices with critical extrinsic defects, while devices without extrinsic defects, or those with only non-critical ones, survive. Devices that do not pass the screening test are removed from the distribution. In this way, a potential reliability risk is converted to yield loss.

To be able to stress-test devices at a sufficiently high stress level, the bulk gate oxide needs to have a specified minimum thickness. In case the gate oxide thickness is too low, devices will either fail intrinsically during screening because of wear or show a degraded threshold voltage and channel mobility after screening. As a result, a nominal oxide thickness is needed that is much higher than what is typically needed to fulfill the intrinsic lifetime targets for efficient gate-oxide screening. Unfortunately, a thicker gate oxide increases the threshold voltage, and decreases the channel conductance at a given $V_{GS(on)}$. The trade-off between gate oxide FIT rate and device performance is illustrated in Fig. 12 and was also discussed in [6].

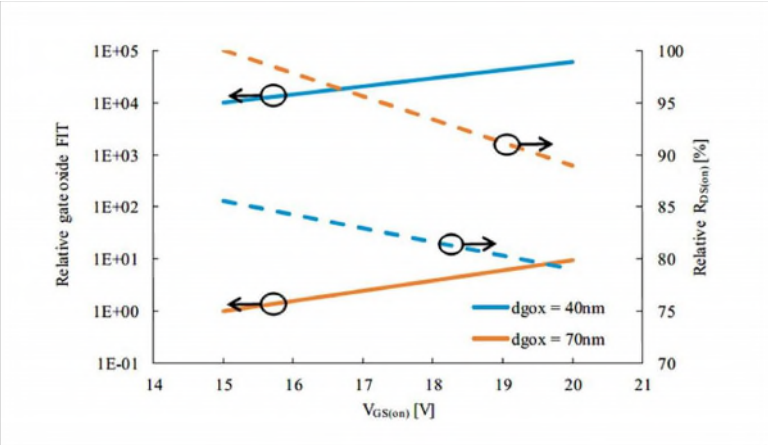

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Figure 12: Impact of gate-oxide thickness and gate voltage on failure probability and on-state properties (Rdson data for 650V devices)

Infineon has invested a significant amount of time and material samples to develop a complete picture regarding the MOS reliability for SiC MOSFETs. As an example, we have tested the on-state reliability of electrically screened SiC MOSFETs for 100 days at 150°C using three individual stress runs at different positive and negative gate-stress biases. Each sample group consisted of 1000 pieces. Figure 13 indicates the results for the different gate-oxide process conditions, sketching the technology improvement towards the finally released process. Using the initial processing conditions, at twice the recommended gate bias of 30 V, less than 10 out of 1000 devices failed. The implemented technology progress reduced this number to only one fail at 30 V, and zero fails at 25 V and -15 V. This one remaining failure is still an extrinsic failure, but it is not critical, as it will occur far beyond the specified product lifetime under the nominal gate-bias use conditions.

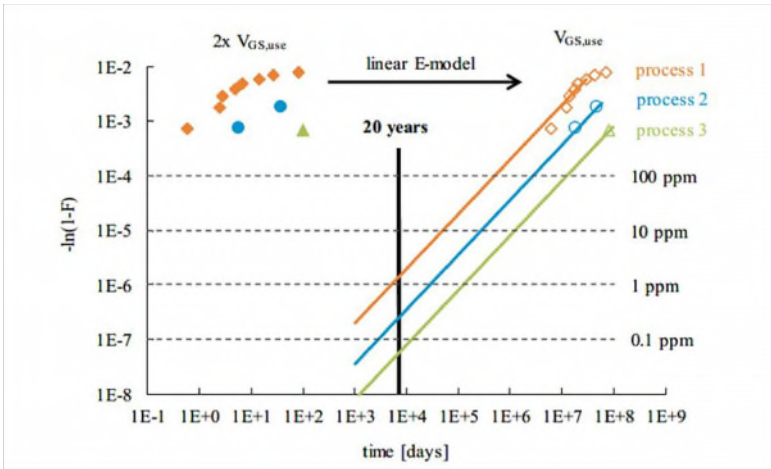

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Figure 13: Evaluation of on-state failure rate for different processing conditions

It is of course also important to assess the off-state oxide stress in addition to the on-state oxide reliability due to the electric field conditions in SiC power devices being much closer to the limits of SiO_2 than in silicon power MOS components. The key strategy is an efficient shielding of the sensitive oxide areas by a proper design of deep p-regions. The efficiency of the shielding is again a trade-off between on-resistance and reliability. In the case of the trench MOSFET, the deep p-regions which form JFET-like structures below the channel zone of the MOSFET can facilitate the shielding effectively [7]. This JFET adds an additional component to the on-resistance that mainly depends on the distance and the doping between the buried p-regions. This shielding structure design feature is crucial to avoid gate-oxide degradation or gate oxide breakdown in the off-state.

To verify the off-state reliability of the CoolSiC™ MOSFETs, we have stress-tested over 5000 1200 V SiC MOSFETs for 100 days at 150°C, V_{GS} = -5 V and V_{DS} = 1000 V. These conditions correspond to the most critical point of the mission profile for industrial applications. A further acceleration is very difficult due to restrictions in the applied drain voltage with respect to the breakdown voltage of the device. Running the tests at even higher drain

voltages will falsify the results, as other failure mechanisms such as cosmic-ray induced failures would become more likely. The result was that none of the tested devices failed during this off-state reliability test. As the 650 V device follows the same design criteria as the 1200 V device, the same reliability is expected.

Conclusion

The CoolSiC™ MOSFET features superior performance in terms of switching behavior and total losses.. One of the highlights is the possibility to turn off the device with zero gate bias, which makes the CoolSiC™ transistor concept the only true "normally-off" device at the moment.

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