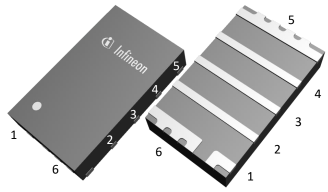
# CoolGaN™

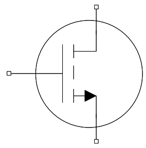
## CoolGaN™ Transistor 100 V G3

PG-VSON-6



## Features

- Ultra fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Moisture rating MSL1
- Industrial grade 3x5 package




## Potential applications

- Telecom & Datacenter 48V IBC
- Sync Rectification for AC-DC and DC-DC converters
- Robotics and drones
- Battery powered tools
- 48V servo drive
- e-Mobility, UAVs
- Class D Audio
- Solar & Energy storage systems
- Point of Load Converters

## Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key performance parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 100 | V |
| $R_{DS(on)}$ | 2.4 | mΩ |
| $I_D$ | 76 | A |
| $Q_{oss}$ | 43 | nC |
| $Q_G$ | 11 | nC |
| $Q_{rr}$ | 0 | nC |

| Type / Ordering code | Package | Marking | Related links |
|---|---|---|---|
| IGC033S101 | PG-VSON-6 | 33SA1 | see Appendix A |

# Table of contents

# 1 Maximum ratings

at $T_j$ = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

**Table 2 Maximum ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain-source voltage | $V_{DS}$ | - | - | 100 | V | $V_{GS}$=0 V |
| Pulsed drain-source voltage [1] | $V_{DS,\ pulse}$ | - | - | 120 | V | $V_{GS}$=0 V, 1 h total time |
| Continuous drain current | $I_D$ | - | - | 76<br>21 | A | $V_{GS}$=5 V, $T_C$=25 °C<br>$V_{GS}$=5 V, $T_A$=25 °C, $R_{thJA}$=38 °C/W [2] |
| Pulsed drain current [3] | $I_{D,pulse}$ | - | - | 700<br>330 | A | $T_j$=25 °C<br>$T_j$=150 °C |
| Pulsed gate-source voltage [1] | $V_{GS}$ | -6.5 | - | 6.5 | V | Pulsed 100 h total time |
| Power dissipation | $P_{tot}$ | - | - | 45<br>3.3 | W | $T_C$=25 °C<br>$T_A$=25 °C, $R_{thJA}$=38 °C/W [2] |
| Storage temperature | $T_{stg}$ | -55 | - | 150 | °C | - |
| Junction temperature | $T_j$ | -40 | - | 150 | °C | |

1) Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

2) Device on 4-layer FR4 PCB, vertical in still air.

3) Pulse current limited by transfer characteristic.

# 2 Recommended operating conditions

**Table 3 Recommended operating conditions**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate-source voltage | $V_{GS}$ | -4.0 | 5.0 | 5.5 | V | - |

# 3 Thermal characteristics

**Table 4 Thermal characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, top | $R_{thJC}$ | - | 15 | 18 | °C/W | - |
| Thermal resistance, junction - case, bottom | $R_{thJC}$ | - | 1.9 | 2.8 | °C/W | |
| Thermal resistance, junction - ambient 1s0p | $R_{thJA}$ | - | 60 | - | °C/W | On 1 layer PCB, vertical in still air. |
| Thermal resistance, junction - ambient 2s2p | $R_{thJA}$ | - | 38 | - | °C/W | With vias on 4 layer PCB, vertical in still air. |

# 4 Electrical Characteristics

at $T_j$=25 °C, unless otherwise specified

### Table 5 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate threshold voltage | $V_{GS(th)}$ | 1.2 | 1.9 | 2.9 | V | $V_{DS}$=$V_{GS}$, $I_D$=8.0 mA |
| Drain-source leakage current | $I_{DSS}$ | - | 0.3<br>6.0 | 1.5<br>50 | µA | $V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 16<br>0.01<br>120<br>0.01 | 150<br>0.03<br>1100<br>0.04 | µA | $V_{GS}$=5 V, $T_j$=25 °C<br>$V_{GS}$=-4 V, $T_j$=25 °C<br>$V_{GS}$=5 V, $T_j$=125 °C<br>$V_{GS}$=-4 V, $T_j$=125 °C |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 2.4 | 3.3 | mΩ | $V_{GS}$=5 V, $I_D$=20 A |
| Gate resistance [4] | $R_G$ | - | 0.5 | - | Ω | - |

4) Defined by design. Not subject to production test.

### Table 6 Capacitance characteristics [5]

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 1200 | 1400 | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Output capacitance | $C_{oss}$ | - | 540 | 590 | pF | |
| Reverse transfer capacitance | $C_{rss}$ | - | 6.1 | 8.0 | pF | |

5) Defined by design. Not subject to production test.

### Table 7 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 2.8 | - | nC | $V_{DS}$=50 V, $I_D$=20 A, $V_{GS}$=0 to 5 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 2.1 | - | nC | |
| Gate to drain charge [6] | $Q_{gd}$ | - | 2.6 | - | nC | |
| Switching charge | $Q_{sw}$ | - | 3.3 | - | nC | |
| Gate charge total [6] | $Q_g$ | - | 11 | 14 | nC | |
| Gate plateau voltage | $V_{plateau}$ | - | 2.6 | - | V | |
| Output charge [6] | $Q_{oss}$ | - | 43 | 47 | nC | $V_{DS}$=50 V, $V_{GS}$=0 V |

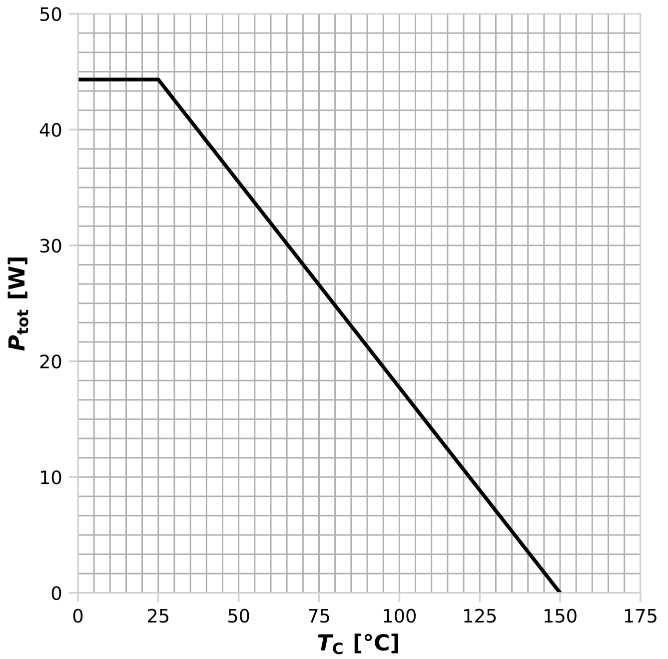
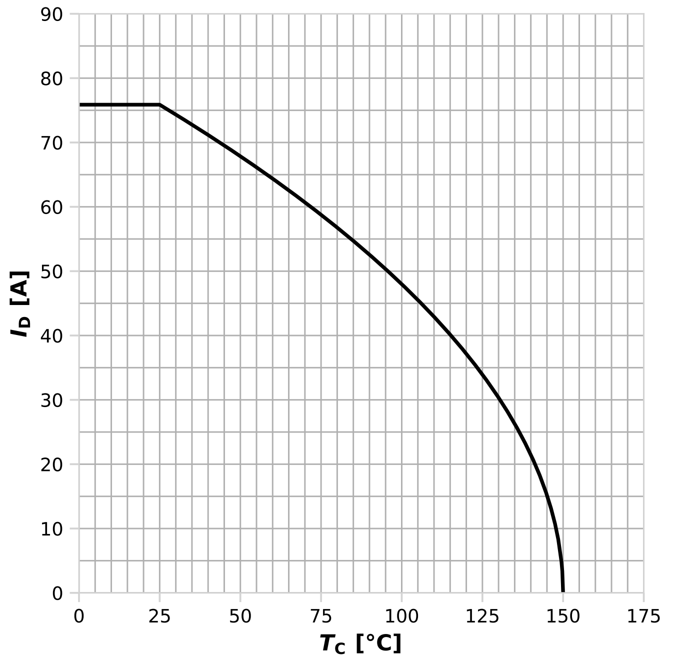
6) Defined by design. Not subject to production test.

### Table 8 Reverse operation

| Parameter | Symbol | Values | | | Unit | Note / Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Reverse continuous current | $I_S$ | - | - | 16 | A | $T_C$=25 °C |
| Pulsed current, reverse | $I_{S,pulse}$ | - | - | 304 | A | |
| Source-Drain reverse voltage | $V_{SD}$ | - | 2.4<br>2.0 | 3.1<br>- | V | $V_{GS}$=0 V, $I_{S,pulse}$=20 A, $T_j$=25 °C<br>$V_{GS}$=0 V, $I_{S,pulse}$=0.5 A, $T_j$=25 °C |
| Reverse recovery charge [7)] | $Q_{rr}$ | - | 0 | - | nC | $V_R$=50 V, $I_{S,pulse}$=20 A, $di_{S,pulse}/dt$ =100 A/µs |

7) Defined by design. Not subject to production test.

# 5 Electrical characteristics diagrams

| Diagram 1: Power dissipation | Diagram 2: Drain Current |
|---|---|
|  |  |
| $P_{tot}$=f($T_C$) | $I_D$=f($T_C$) |



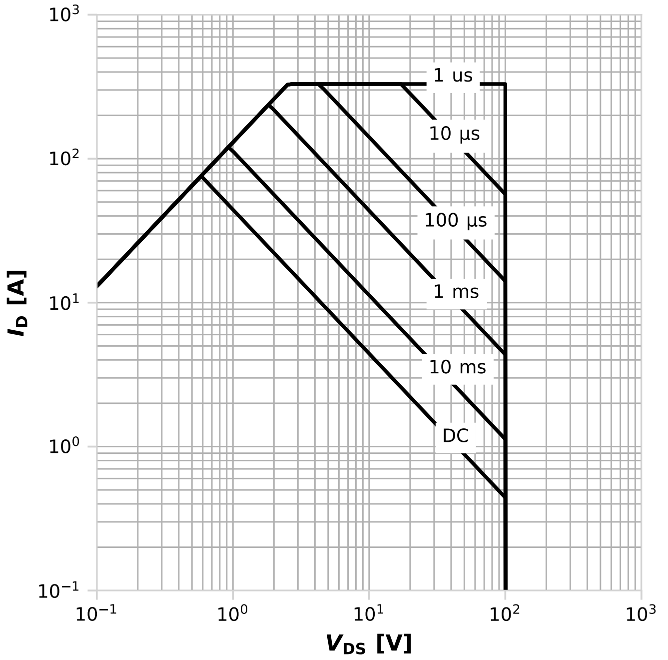
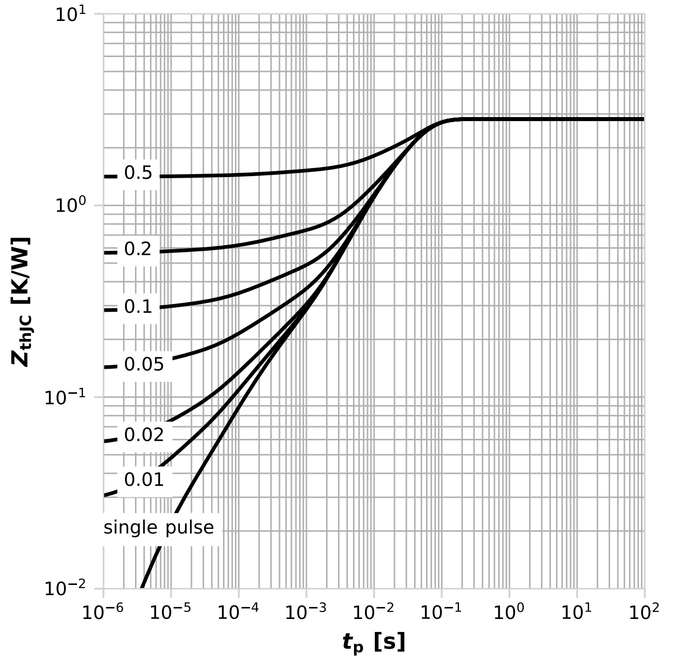
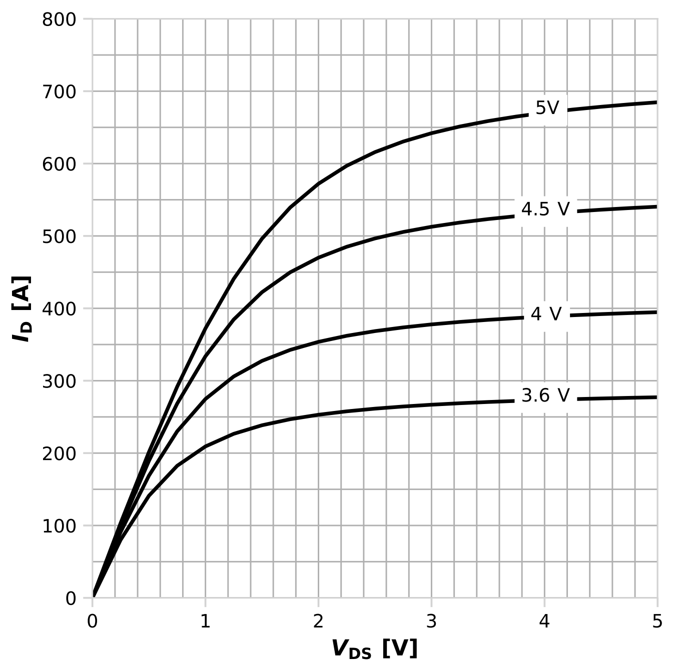
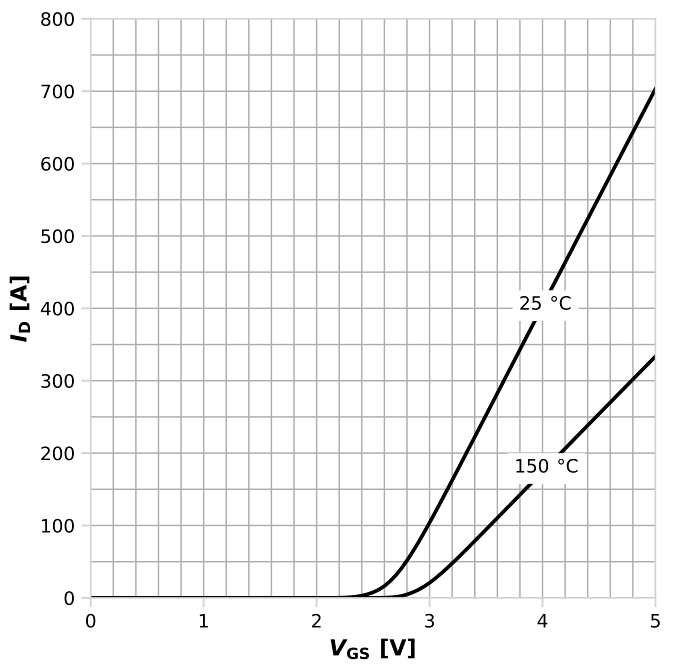
| Diagram 3: Safe operating area | Diagram 4: Max. transient thermal impedance |
|---|---|
|  |  |
| $I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0; parameter: $t_p$ | $Z_{thJC}$ =f($t_p$); parameter: $D$=$t_p$/$T$ |

**Diagram 5: Typ. output characteristics**



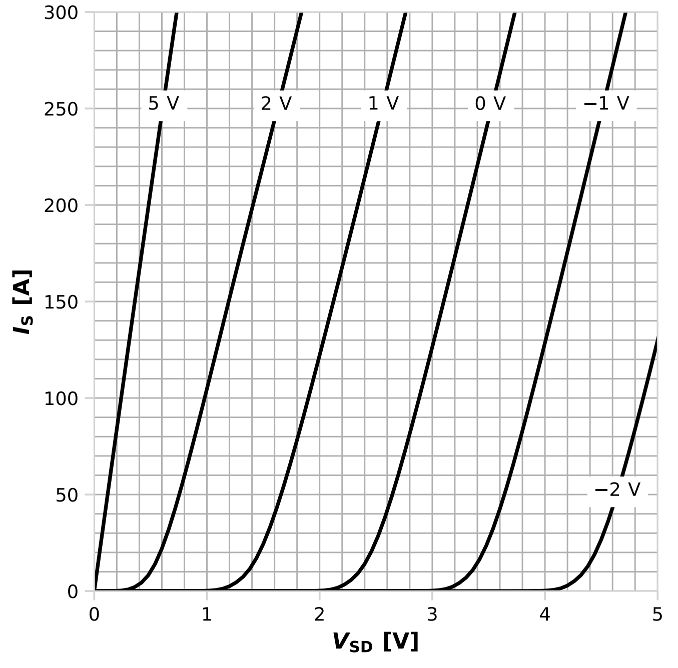

$I_D$=f($V_{DS}$); $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. transfer characteristics**



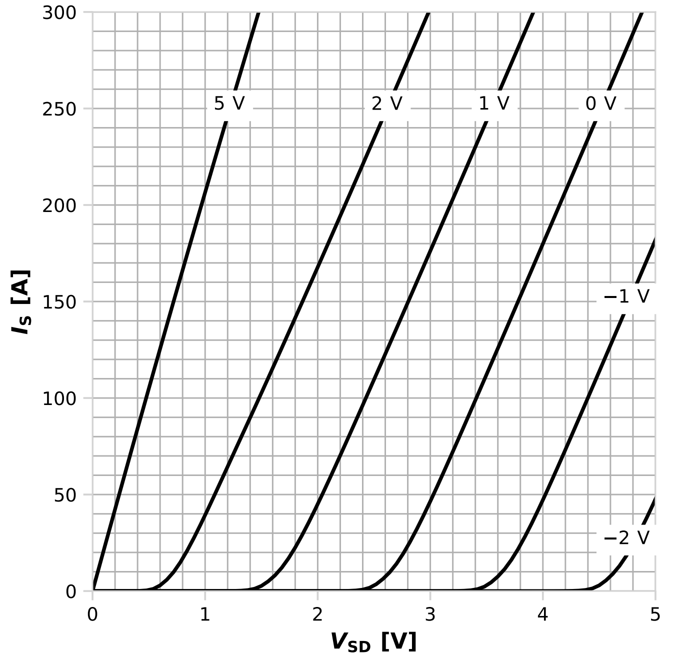

$I_D$=f($V_{GS}$); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: $T_j$

**Diagram 7: Typ. channel reverse characteristics**



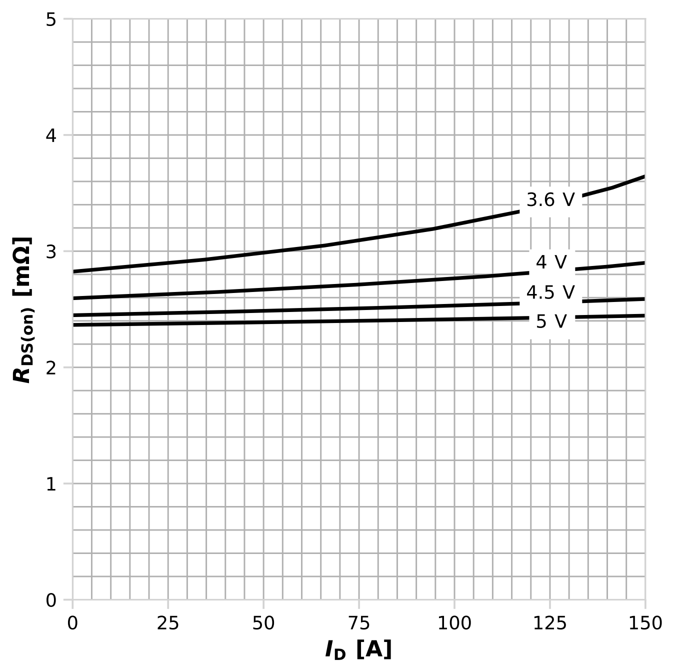

$I_S$=f($V_{SD}$); $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 8: Typ. channel reverse characteristics**



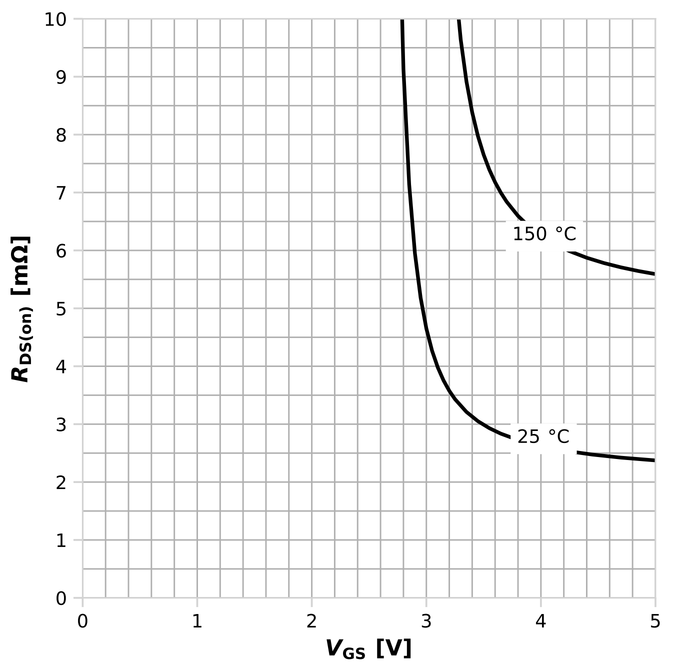

$I_S$=f($V_{SD}$); $T_j$=125 °C; parameter: $V_{GS}$

**Diagram 9: Typ. drain-source on-state resistance**



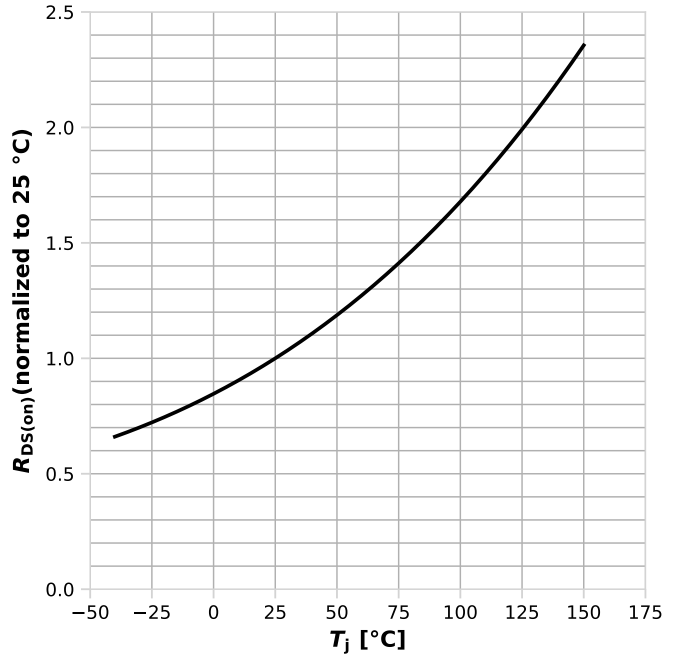

$R_{DS(on)}$=f($I_D$); $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 10: Typ. Drain-source on-state resistance**



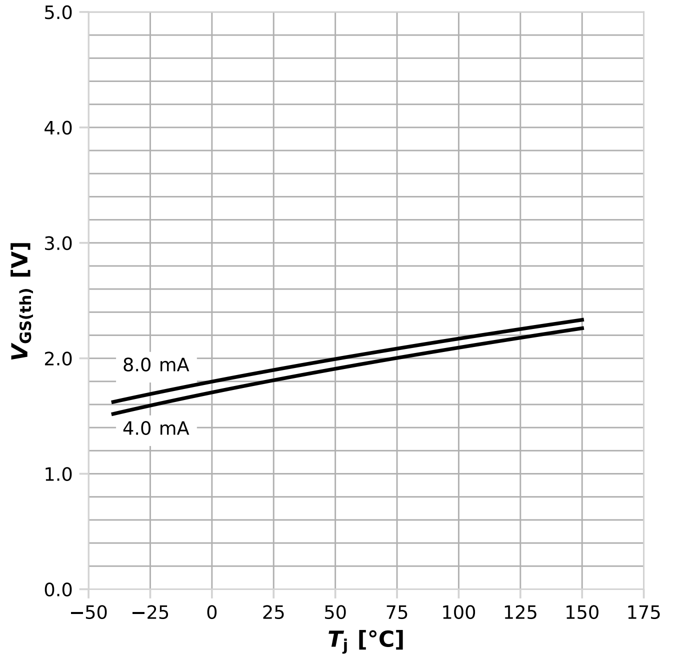

$R_{DS(on)}$=f($V_{GS}$); $I_D$=20 A; parameter: $T_j$

**Diagram 11: Drain-source on-state resistance**



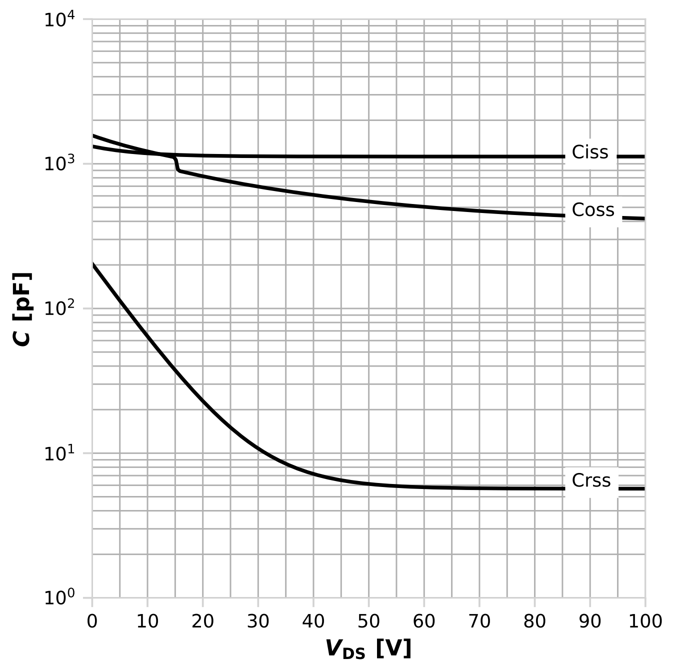

$R_{DS(on)}$=f($T_j$); $I_D$=20 A, $V_{GS}$=5V

**Diagram 12: Typ. gate threshold voltage**



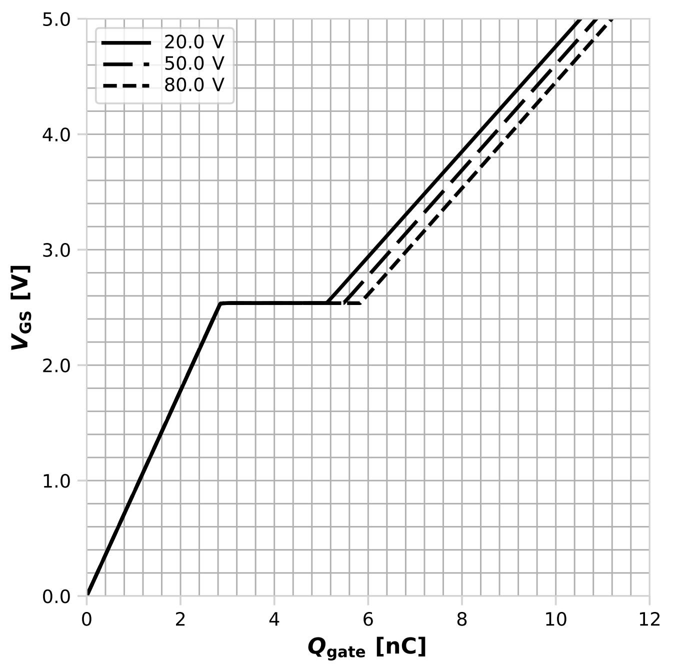

$V_{GS(th)}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 13: Typ. capacitances**



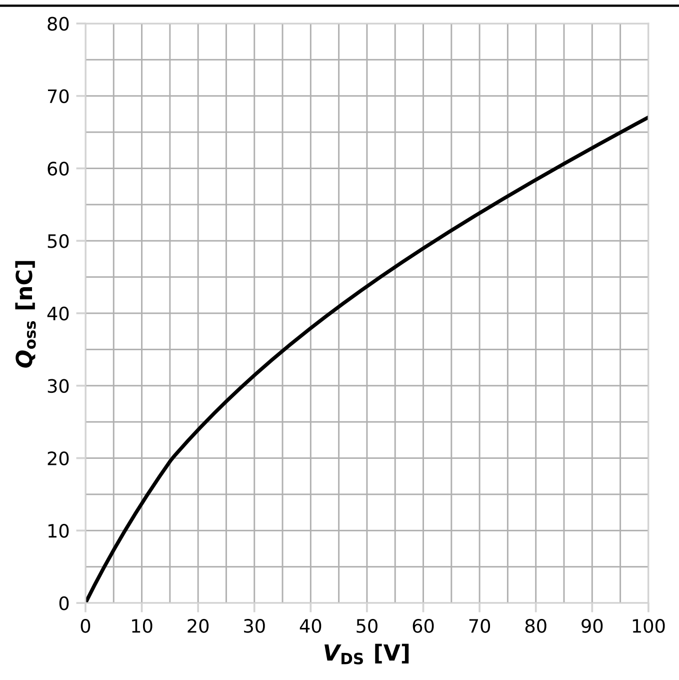

$C=f(V_{DS})$; $V_{GS}=0$ V

**Diagram 14 Typ. gate charge**



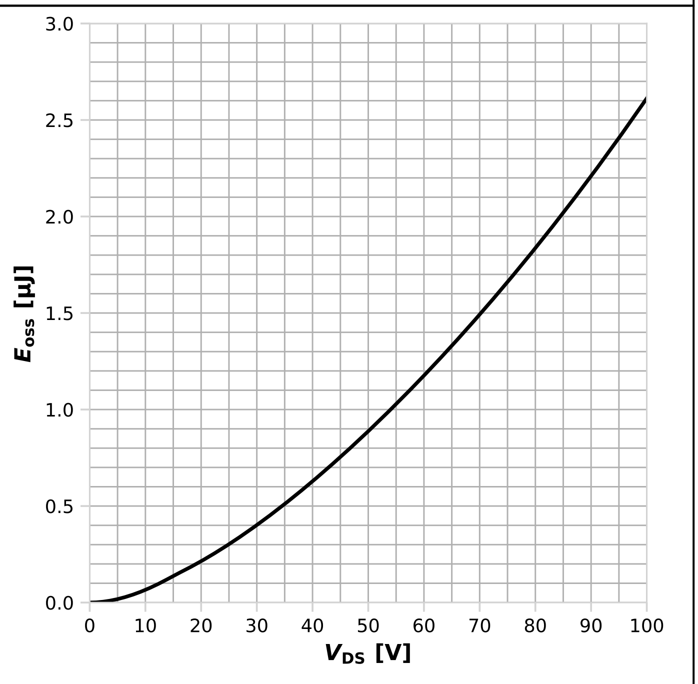

$V_{GS}=f(Q_{gate})$; $I_D=20$ A pulsed; parameter: $V_{DS}$

**Diagram 15: Typ. output charge**

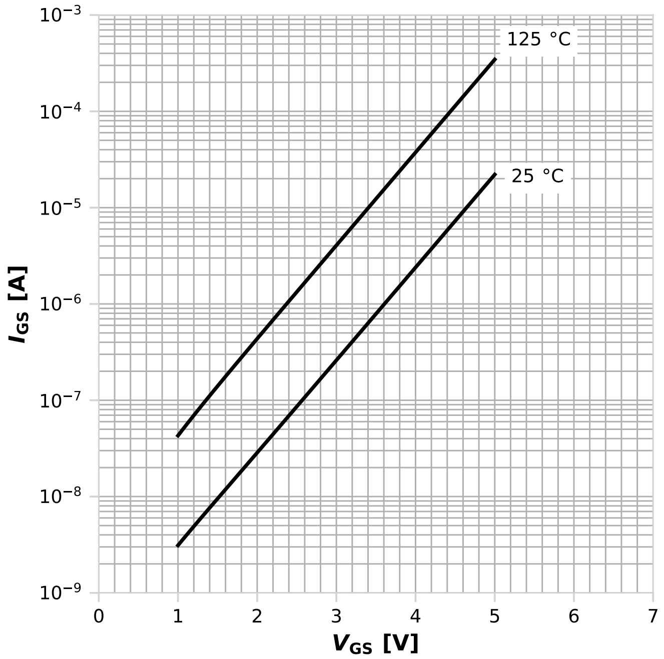



$Q_{oss}=f(V_{DS})$, $V_{GS}=0$ V

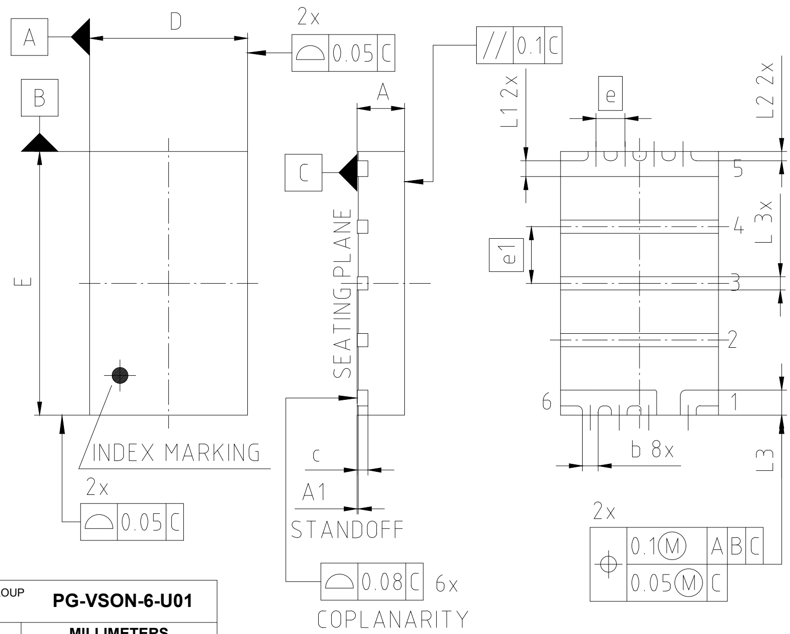
**Diagram 16: Typ. Coss stored Energy**




$E_{oss}=f(V_{DS})$, $V_{GS}=0$ V

| Diagram 17: Typ. gate characteristics forward |
| --- |
|  |
| $I_{GS}$=f($V_{GS}$); $V_{DS}$=0 V; parameter: $T_j$ |

# 6 Package outlines




| PACKAGE - GROUP NUMBER: | PG-VSON-6-U01 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | | 1.00 |
| A1 | | 0.05 |
| b | 0.20 | 0.40 |
| c | | 0.20 |
| D | 2.90 | 3.10 |
| E | 4.90 | 5.10 |
| L | 0.20 | 0.30 |
| L1 | 0.25 | 0.35 |
| L2 | 0.125 | 0.225 |
| L3 | 0.425 | 0.525 |
| e | 0.55 | |
| e1 | 1.075 | |
| N | 6 | |

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

**Figure 1 Outline PG-VSON-6, dimensions in mm**

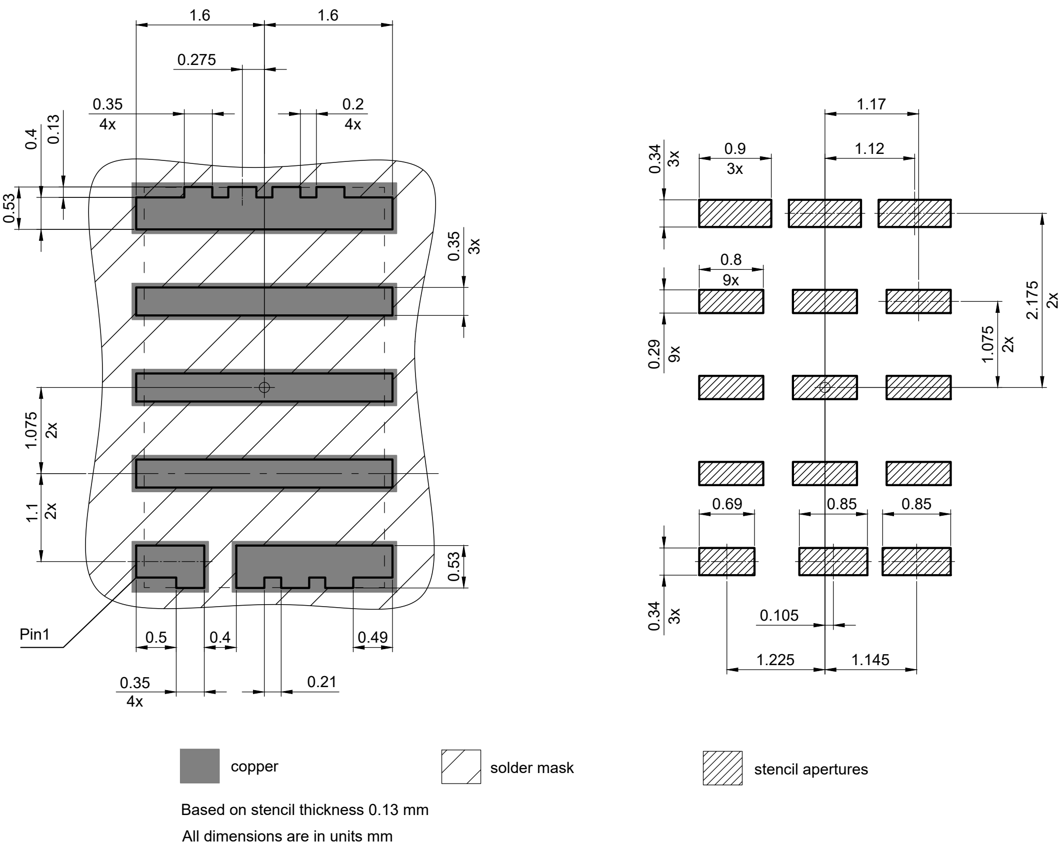
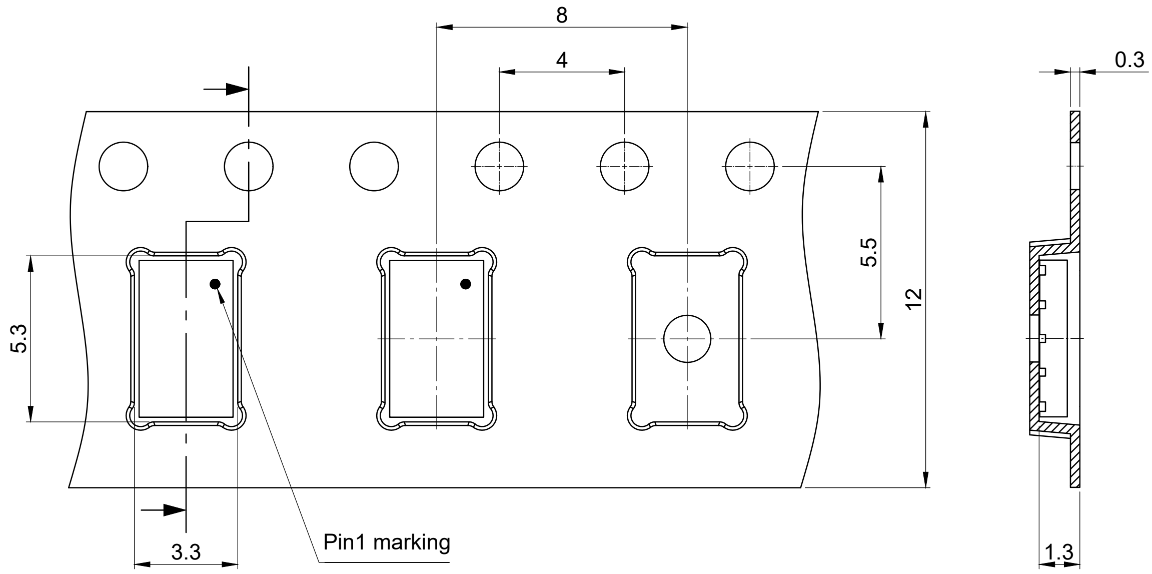



**Figure 2** Footprint drawing PG-VSON-6, dimensions in mm




All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

**Figure 3 Packaging variant PG-VSON-6, dimensions in mm**

# 7 Appendix A

**Table 9 Related links**

- IFX CoolGaN™ GaN webpage
- IFX CoolGaN™ reliability white paper
- IFX CoolGaN™ gate driver application note
- IFX CoolGaN™ Evaluation Boards
- IFX Packages Description-PG-VSON-6-3

## Revision history

IGC033S101

### Revision 2024-12-12, Rev. 1.1

Previous revisions

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 1.0 | 2024-12-10 | Release of final |
| 1.1 | 2024-12-12 | Updated Features |

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