

Features

- $V_{CES} = 650\text{ V}$
- $I_{Cn} = 200\text{ A}$
- 650 V trench & field stop technology
- High short circuit capability, self limiting short circuit current
- Positive temperature coefficient
- Easy paralleling

Potential applications

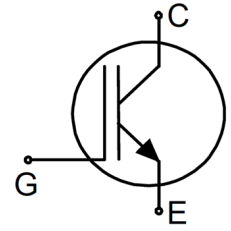
- Drives

Product validation

- Technology qualified for industrial applications. Ready for validation in industrial applications according to the relevant tests of IEC 60747 and 60749 or alternatively JEDEC47/20/22

Description

- Recommended for power modules



Type	Die size	Delivery form
IGC100T65T8RM	9.73 mm x 10.23 mm	Sawn on foil

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1 Mechanical parameters

Table 1 Mechanical parameters

Parameter	Values
Die size	9.73 mm x 10.23 mm
Area total	99.54 mm ²
Emitter pad size	See chip drawing
Gate pad size	See chip drawing
Silicon thickness	80 μm
Wafer size	200 mm
Maximum possible chips per wafer	259
Passivation frontside	Photoimide
Pad metal	3.2 μm AlSiCu
Backside metal	Ni Ag - system
Die attach	Electrically conductive epoxy glue and soft solder
Frontside interconnect	Wire bond: Al ≤ 500 μm
Reject ink dot size (valid for inked delivery form only)	Ø 0.65 mm; max. 1.2 mm
Storage environment (<12 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<12 months) for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C

2 Characteristics

Table 2 Maximum ratings

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Collector-emitter voltage	V_{CES}		$T_{vj} = 25\text{ °C}$	650			V
DC collector current, limited by T_{vjmax}	I_C			-1)			A
Pulsed collector current, t_p limited by T_{vjmax} 2)	I_{Cpulse}			600			A
Gate-emitter voltage	V_{GE}			±20			V
Operating junction temperature	T_{vjop}			-40...175			°C
Short-circuit withstand time 2) 3)	t_{SC}	$V_{CC} = 360\text{ V}, V_{GE} = 15\text{ V}$	$T_{vj} = 150\text{ °C}$	10			µs

1) depending on thermal properties of assembly

2) not subject to production test - verified by design/characterization

3) allowed number of short circuits: <1000; time between short circuits: >1s

Table 3 Static characteristics (tested on wafer), $T_{vj} = 25\text{ °C}$

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Collector-emitter breakdown voltage	V_{BRCES}	$I_C = 4\text{ mA}, V_{GE} = 0\text{ V}$		650			V
Collector-emitter saturation voltage	V_{CESat}	$V_{GE} = 15\text{ V}, I_C = 60\text{ A}$		0.89	1.06	1.23	V
Gate-emitter threshold voltage	V_{GEth}	$I_C = 3.2\text{ mA}, V_{GE} = V_{CE}$		5.1	5.8	6.4	V
Zero gate-voltage collector current	I_{CES}	$V_{CE} = 650\text{ V}, V_{GE} = 0\text{ V}$				1.08	µA
Gate-emitter leakage current	I_{GES}	$V_{CE} = 0\text{ V}, V_{GE} = 20\text{ V}$				600	nA
Internal gate resistance	$R_{G,int}$				2		Ω

Table 4 Electrical characteristics

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Collector-emitter saturation voltage	V_{CESat}	$V_{GE} = 15\text{ V}, I_C = 200\text{ A}$	$T_{vj} = 25\text{ °C}$		1.55		V
			$T_{vj} = 150\text{ °C}$		1.75		
Input capacitance	C_{ies}	$V_{CE} = 25\text{ V}, V_{GE} = 0\text{ V}, f = 1000\text{ kHz}, T_{vj} = 25\text{ °C}$			12335		pF
Reverse transfer capacitance	C_{res}	$V_{CE} = 25\text{ V}, V_{GE} = 0\text{ V}, f = 1000\text{ kHz}, T_{vj} = 25\text{ °C}$			366		pF

4 Bare die product specifics

- Switching characteristics and thermal properties are dependent on module design and mounting technology and can therefore not be specified for a bare die.
- AQL 0.65 for visual inspection according to failure catalogue.
- Electrostatic discharge sensitive device according to MIL-STD 883.
- The example application may be subject to change without prior notice. It is intended for information purposes only, and should not be interpreted as a commitment.
- Example application: FS200R07N3E4R

Revision history

Document revision	Date of release	Description of changes
1.00	2023-04-28	Final datasheet ***Legacy Revisions*** V1.2 2014-08-12

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