CoolGaN(TM) Bidirectional Transistor 40 V G3

Features

- E-mode bidirectional transistor - normally OFF switch
- Drain-to-Drain configuration
- Bidirectional blocking capability
- Low on-resistance, low gate charge, low output charge
- Qualified according to JEDEC for target applications

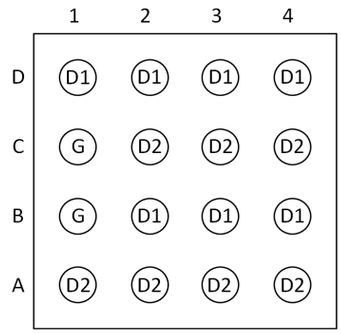
RoHS Pb-Free

Applications

- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power supply system

Product Summary

$V_{DD.max}$	40	V
$R_{DD(on),Typ}$	6.0	mΩ
I_D	14	A
$Q_{oss,Typ}$	4.8	nC
$Q_{G,Typ}$	5.5	nC
Q_{rr}	0	nC



Type	Package	Marking
IGK080B041S	SG-UFWLB-16	BF1

Maximum ratings

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Continuous drain-to-drain voltage[1]	V_{DD}	V_{GD}=0 V, I_D=0 A			40	V
Pulsed drain-to-drain voltage[2]	$V_{DD,pulse}$	V_{GD}=0 V, I_D= 0 A			48	
Drain to gate voltage	V_{DG}				40	
Continuous drain current	I_D	V_{GD}=5 V, T_C=25 °C			14	A
Pulsed drain current	$I_{D,pulse}$	T_J=25 °C			70	
Gate-drain voltage	V_{GD}	Continuous			6	V

[1] For both directions of current flow: from D1 to D2 and D2 to D1.

[2] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation

Maximum ratings

Parameter	Symbol	Conditions	Value			Unit
Storage temperature	T_{stg}		-40 ... 150			°C
Operating temperature	T_j		-40	-	125	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	top	-	26	-	°C/W
Thermal resistance, junction - bottom	R_{thJC}	bottom	-	4	-	
Thermal resistance, junction - ambient	R_{thJA}		-	62	-	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

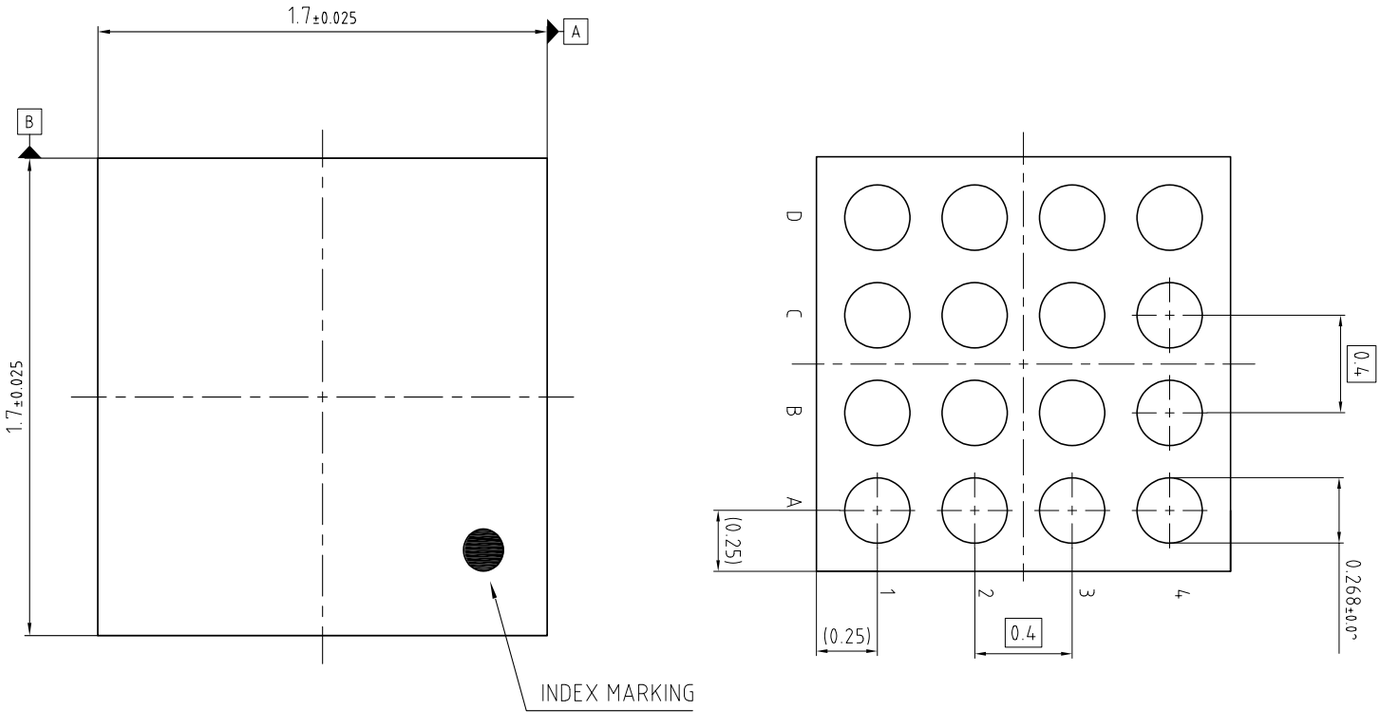
Static characteristics

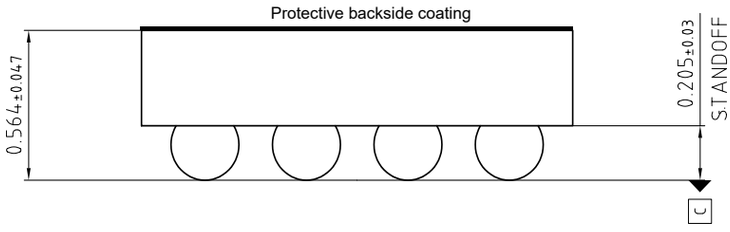
Gate threshold voltage	$V_{GD(th)}$	V_{DD}=V_{GD}	1.2	2.3	2.9	V
Drain-Drain leakage current	I_{DDS}	V_{DD}=40 V, V_{GD}=0 V, T_j=25 °C	-	19	-	nA
Gate-Drain leakage current	I_{GDS}	V_{GD}=5 V, T_j=25 °C	-	17	-	µA
		V_{GD}= 5 V, T_j=85 °C	-	43	-	
		V_{GD}=-4 V, T_j=25 °C	-	0.7	-	nA
		V_{GD}=-4 V, T_j=85 °C	-	0.9	-	
Drain-drain on-state resistance	$R_{DD(on)}$	V_{GD}=5 V, I_D=10 A	-	6.0	8.0	mΩ
Gate resistance[5)]	R_G		-	1.2	-	Ω

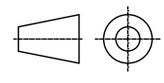
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[5]						
Input capacitance	C_{iss}	V_{GD}=0 V, V_{DD}=20 V, f=1 MHz	-	387	-	pF
Output capacitance	C_{oss}		-	154	-	
Reverse transfer capacitance	C_{rss}		-	98	-	
Gate Charge Characteristics						
Gate to Drain 1 charge	Q_{gd1}	V_{D1D2}=20 V, I_{D1D2}=10 A	-	2.9	-	nC
Gate to Drain 1 charge	Q_{gd1}	V_{D2D1}=20 V, I_{D2D1}=10 A	-	0.7	-	
Gate to Drain 2 charge	Q_{gd2}	V_{D2D1}=20 V, I_{D2D1}=10 A	-	2.9	-	
Gate to Drain 2 charge	Q_{gd2}	V_{D1D2}=20 V, I_{D1D2}=10 A	-	0.7	-	
Gate charge total	Q_g	V_{DD}=20 V, I_D=10 A	-	5.5	-	nC
Output charge[5]	Q_{oss}	V_{DD}=20 V, V_{GD}=0 V	-	4.8	-	nC

[5] Defined by design. Not subject to production test.

Package Outlines



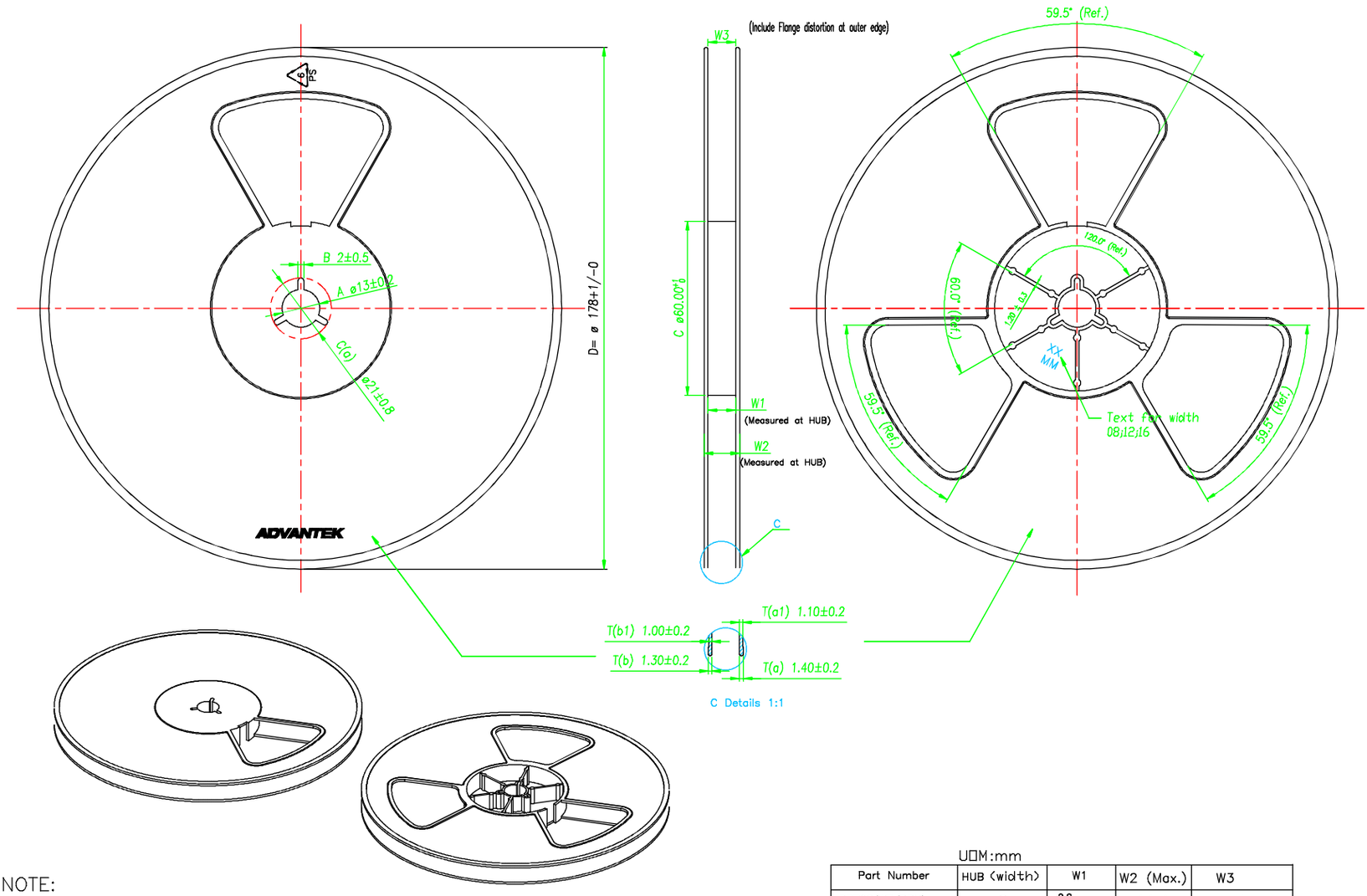


DOCUMENT NO.
Draft
REVISION
01
Drawing according to ISO 8015 General tolerances ISO 2768-mK
EUROPEAN PROJECTION

ISSUE DATE
17.01.2024

Outline SG-UFWLB-16, dimensions in mm

Tape and Reel

REVISIONS			
REV.	DESCRIPTION	DATE	INT
0	Release product drawing(CCD 12-0094(3 width type(08, 12 and 16mm;"WT'&"RBK' type));CO 12-00xx)	11/02/2012	NSU



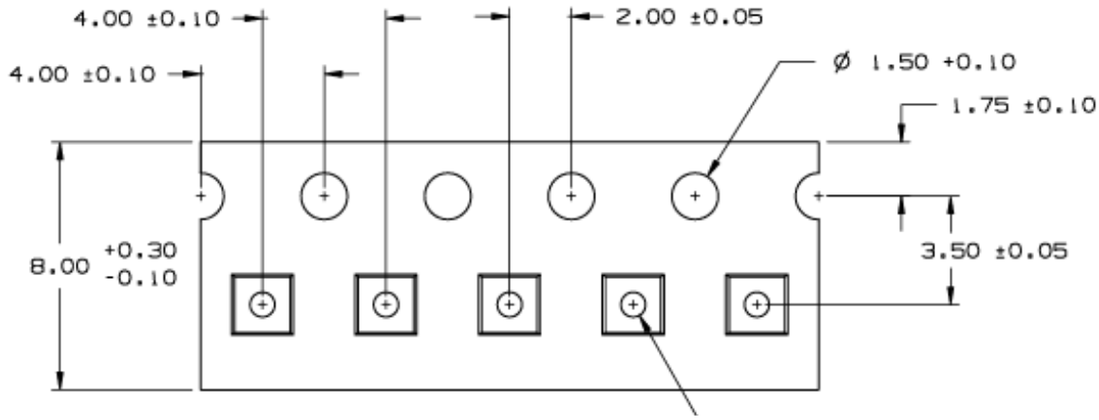
UOM:mm

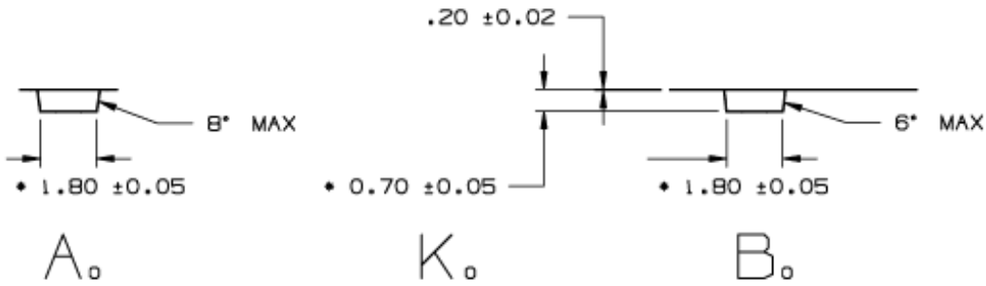
Part Number	HUB (width)	W1	W2 (Max.)	W3
RE708(WT/RBK)	8	9.0 +0.9/-0.0	14.4	9 +1.5/-0.0
RE712(WT/RBK)	12	12.4 +2.0/-0.0	18.4	13 +1.5/-0.0
RE716(WT/RBK)	16	16.4 +2.0/-0.0	22.4	17 +2.0/-0.0

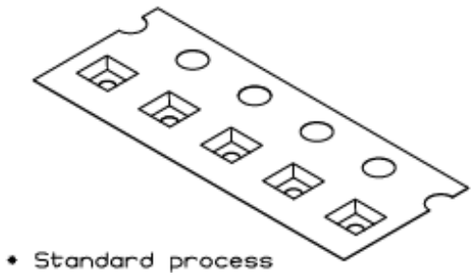
NOTE:
1. Suffix with "WT": standard for White
2. Suffix with "RBK": standard for Regrind Black
3. Related propteries refer to Tech Bulletins

TOLERANCES UNLESS - SPECIFIED
1 PL +/-0.2 2 PL +/-0.10
DIA./ RAD. +/-.003

Carrier Outline



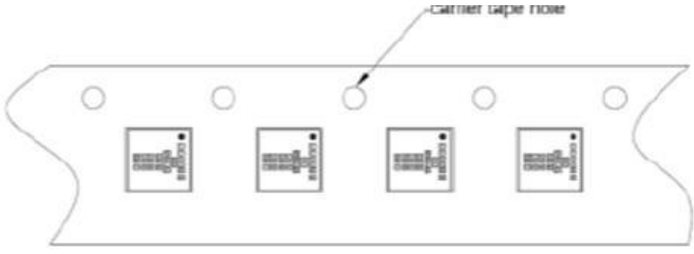


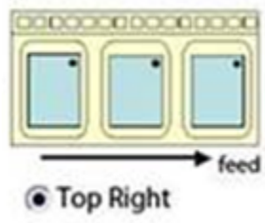


• Standard process

REV	ISSUE DATE AND CHANGE RECORD	DRFT	CHKD
A	JAN 17, 20	MZL	MZL

Pin 1 Orientation





Revision History
IGK080B041S
Revision: Rev 0.2 - 28.06.2024

Previous Revision

Revision	Date	Subjects (major changes since last revision)
-	-	-

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