

## CoolGaN™ G5

### CoolGaN™ Transistor 650 V G5

Infineon's CoolGaN™ is a highly efficient gallium nitride (GaN) transistor designed for power conversion at 650 V. It enables higher power density, supports reduced system BOM cost, and facilitates miniaturized form factors. Produced using 200 mm (8 inch) wafer technology and fully automated production lines, it features narrow production tolerances and the highest product quality. This makes it suitable for a wide range of applications, from consumer electronics to industrial applications.

### Features

- Enhancement mode transistor
- Ultra-fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate and output charge
- Superior commutation ruggedness
- 2 kV HBM ESD standards

### Benefits

- Normally OFF transistor technology ensures safe operation
- Enables rapid and precise power delivery control
- Improves system efficiency and reliability
- Ensures robust performance under challenging conditions

These features collectively make CoolGaN™ a game-changer in the realm of power conversion, offering a compelling combination of efficiency, compactness, and reliability.

### Potential applications

Industrial, telecom, datacenter SMPS based on half-bridge hard and soft switching topologies such as totem pole PFC and high frequency LLC, as well as charger and adapter.

### Product validation

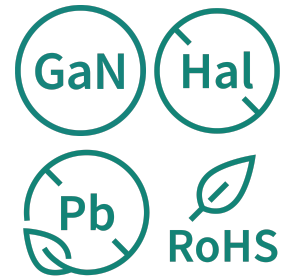
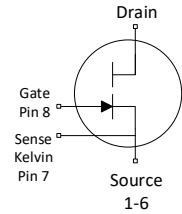
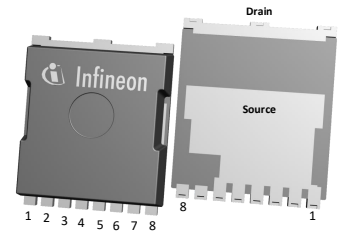
Fully qualified according to JEDEC for Industrial Applications

**Table 1** Key performance parameters

| Parameter          | Value | Unit |
|--------------------|-------|------|
| $V_{DS,max}$       | 650   | V    |
| $V_{DS,trans-max}$ | 900   | V    |
| $R_{DS(on),max}$   | 30    | mΩ   |
| $Q_{g,typ}$        | 11    | nC   |
| $I_{D,pulse}$      | 120   | A    |
| $Q_{oss} @ 400 V$  | 82    | nC   |
| $Q_{rr}$           | 0     | nC   |

| Type / Ordering code | Package   | Marking  | Related links  |
|----------------------|-----------|----------|----------------|
| IGT65R025D2          | PG-HSOF-8 | 65R025D2 | see Appendix A |

TOLL



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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80% of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

**Table 2 Maximum ratings**

| Parameter   | Symbol          | Values      |      |            | Unit             | Note / Test condition  |
|---|-----------------|-------------|------|------------|------------------|--|
|   |                 | Min.        | Typ. | Max.       |                  |  |
| Drain source voltage, continuous                  | $V_{DS,max}$    | -           | -    | 650        | V                | $V_{GS} = 0\text{ V}$ , derating recommendation according JEDEC JEP198   |
| Leakage current at drain source transient voltage | $I_{DS,trans}$  | -           | -    | 28         | mA               | $V_{GS} = 0\text{ V}$ , $V_{DS,trans} = 900\text{ V}$  |
| Drain source voltage transient                    | $V_{DS,trans}$  | -           | -    | 900        | V                | <1% duty cycle, <1 $\mu\text{s}$ , 1 million pulses  |
| Drain source voltage, pulsed                      | $V_{DS,pulsed}$ | -           | -    | 750<br>650 | V                | $T_j = 25^\circ\text{C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$<br>$T_j = 125^\circ\text{C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$        |
| Switching surge voltage, pulsed                   | $V_{DS,surge}$  | -           | -    | 750        | V                | DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$ ; turn on $I_{D,pulse} = 63\text{ A}$ ; $T_j = 105^\circ\text{C}$ ; $f \leq 100\text{ kHz}$ , $t \leq 100\text{ s}$ (10 million pulses) |
| Continuous current, drain source <sup>1)</sup>    | $I_D$           | -           | -    | 70         | A                | $T_C = 25^\circ\text{C}$ ; $T_j = T_{j,max}$   |
| Pulsed current, drain source                      | $I_{D,pulse}$   | -120<br>-84 | -    | 120<br>84  | A                | $T_j = 25^\circ\text{C}$ ; $I_G = 60\text{ mA}$ ; See Diagram 3, 5<br>$T_j = 125^\circ\text{C}$ ; $I_G = 60\text{ mA}$ ; See Diagram 4, 6  |
| Gate current, continuous <sup>2)</sup>            | $I_{G,avg}$     | -           | -    | 46         | mA               | $T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; See Table 9   |
| Gate current, pulsed <sup>2)</sup>                | $I_{G,pulsed}$  | -4.6        | -    | 4.6        | A                | $T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; $t_{pulse} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; See Table 9   |
| Gate source voltage, continuous <sup>2)</sup>     | $V_{GS}$        | -10         | -    | -          | V                | $T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; See Diagram 12  |
| Gate source voltage, pulsed <sup>2)</sup>         | $V_{GS,pulse}$  | -25         | -    | -          | V                | $T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; $t_{pulse} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; open drain  |
| Power dissipation                                 | $P_{tot}$       | -           | -    | 236        | W                | $T_C = 25^\circ\text{C}$   |
| Operating junction temperature                    | $T_j$           | -55         | -    | 150        | $^\circ\text{C}$ | -  |
| Storage temperature                               | $T_{stg}$       | -55         | -    | 150        | $^\circ\text{C}$ | Max shelf life depends on storage conditions   |
| Drain-source voltage slew-rate                    | $dv/dt$         | -           | -    | 200        | V/ns             | -  |

- 1) Limited by  $T_{j,max}$ . Maximum duty cycle  $D = 0.75$
- 2) We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

| Parameter  | Symbol     | Values |      |      | Unit | Note / Test condition   |
|--|------------|--------|------|------|------|---|
|  |            | Min.   | Typ. | Max. |      |   |
| Thermal resistance, junction - case                    | $R_{thJC}$ | -      | -    | 0.53 | °C/W | -   |
| Thermal resistance, junction - ambient                 | $R_{thJA}$ | -      | -    | 86   | °C/W | Device on PCB, minimum footprint  |
| Thermal resistance, junction - ambient for SMD version | $R_{thJA}$ | -      | -    | 62   | °C/W | Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm <sup>2</sup> (one layer, 70 μm thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling. |
| Reflow soldering temperature                           | $T_{sold}$ | -      | -    | 260  | °C   | MSL1  |

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless specified otherwise

**Table 4 Static characteristics**

| Parameter                            | Symbol          | Values   |                |            | Unit          | Note / Test condition   |
|--------------------------------------|-----------------|----------|----------------|------------|---------------|---|
|                                      |                 | Min.     | Typ.           | Max.       |               |   |
| Gate threshold voltage               | $V_{GS(th)}$    | 0.9<br>- | 1.2<br>1       | 1.6<br>-   | V             | $I_{DS}=6.1\text{ mA}; V_{DS}=10\text{ V}; T_j=25^\circ\text{C}$<br>$I_{DS}=6.1\text{ mA}; V_{DS}=10\text{ V}; T_j=150^\circ\text{C}$ |
| Gate-Source reverse clamping voltage | $V_{GS, clamp}$ | -        | -              | -8         | V             | $I_{GS}=-1\text{ mA}$   |
| Drain-Source leakage current         | $I_{DSS}$       | -        | 2.3<br>46      | 230<br>-   | $\mu\text{A}$ | $V_{DS}=650\text{ V}, V_{GS}=0\text{ V}, T_j=25^\circ\text{C}$<br>$V_{DS}=650\text{ V}, V_{GS}=0\text{ V}, T_j=150^\circ\text{C}$     |
| Drain-Source on-state resistance     | $R_{DS(on)}$    | -        | 0.025<br>0.053 | 0.030<br>- | $\Omega$      | $I_G=60\text{ mA}; I_D=18\text{ A}; T_j=25^\circ\text{C}$<br>$I_G=60\text{ mA}; I_D=18\text{ A}; T_j=150^\circ\text{C}$               |
| Gate resistance                      | $R_{G,int}$     | -        | 0.7            | -          | $\Omega$      | LCR impedance measurement;<br>$f=f_{res}$ , open drain;   |

**Table 5 Dynamic characteristics**

| Parameter  | Symbol       | Values |      |      | Unit          | Note / Test condition  |
|--|--------------|--------|------|------|---------------|--|
|  |              | Min.   | Typ. | Max. |               |  |
| Input capacitance  | $C_{iss}$    | -      | 780  | -    | pF            | $V_{GS}=0\text{ V}; V_{DS}=400\text{ V}, f=1\text{ MHz}$   |
| Output capacitance   | $C_{oss}$    | -      | 130  | -    | pF            | $V_{GS}=0\text{ V}, V_{DS}=400\text{ V}, f=1\text{ MHz}$   |
| Reverse transfer capacitance                               | $C_{rss}$    | -      | 1.8  | -    | pF            |  |
| Effective output capacitance, energy related <sup>3)</sup> | $C_{o(er)}$  | -      | 150  | -    | pF            | $V_{DS}=0\text{ to }400\text{ V}$  |
| Effective output capacitance, time related <sup>4)</sup>   | $C_{o(tr)}$  | -      | 204  | -    | pF            | $V_{GS}=0\text{ V}; V_{DS}=0\text{ to }400\text{ V}; I_D=const$  |
| Output charge  | $Q_{oss}$    | -      | 82   | -    | nC            | $V_{DS}=0\text{ to }400\text{ V}$  |
| Coss stored energy   | $E_{oss}$    | -      | 12   | -    | $\mu\text{J}$ |  |
| Turn-on delay time   | $t_{d(on)}$  | -      | 11   | -    | ns            | $I_D=18\text{ A}; R_{ON}=2.2\text{ Ohm}; R_{OFF}=2.2\text{ Ohm}; R_{SS}=150\text{ Ohm}; C_C=6.8\text{ nF}; V_{DRV}=12\text{ V};$ see Table 8 |
| Turn-off delay time  | $t_{d(off)}$ | -      | 18   | -    | ns            |  |
| Rise time  | $t_r$        | -      | 12   | -    | ns            |  |
| Fall time  | $t_f$        | -      | 9    | -    | ns            |  |

<sup>3)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

<sup>4)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

**Table 6 Gate charge characteristics**

| Parameter   | Symbol | Values |      |      | Unit | Note / Test condition   |
|-------------|--------|--------|------|------|------|---|
|             |        | Min.   | Typ. | Max. |      |   |
| Gate charge | $Q_G$  | -      | 11   | -    | nC   | $V_{GS}=0\text{ to }3\text{ V}; V_{DS}=400\text{ V}, I_D=18\text{ A}$ |

**Table 7 Reverse conduction characteristics**

| Parameter                             | Symbol         | Values |      |      | Unit | Note / Test condition                     |
|---------------------------------------|----------------|--------|------|------|------|---|
|                                       |                | Min.   | Typ. | Max. |      |   |
| Source-Drain reverse voltage          | $V_{SD}$       | -      | 2.0  | 2.4  | V    | $V_{GS}=0\text{ V}; I_{SD}=18\text{ A}$   |
| Pulsed current, reverse               | $I_{SD,pulse}$ | -      | -    | 120  | A    | $I_G=60\text{ mA}$                        |
| Reverse recovery charge <sup>5)</sup> | $Q_{rr}$       | -      | 0    | -    | nC   | $I_{SD}=18\text{ A}; V_{DS}=400\text{ V}$ |

<sup>5)</sup> Excluding  $Q_{oss}$

## 4 Electrical characteristics diagrams

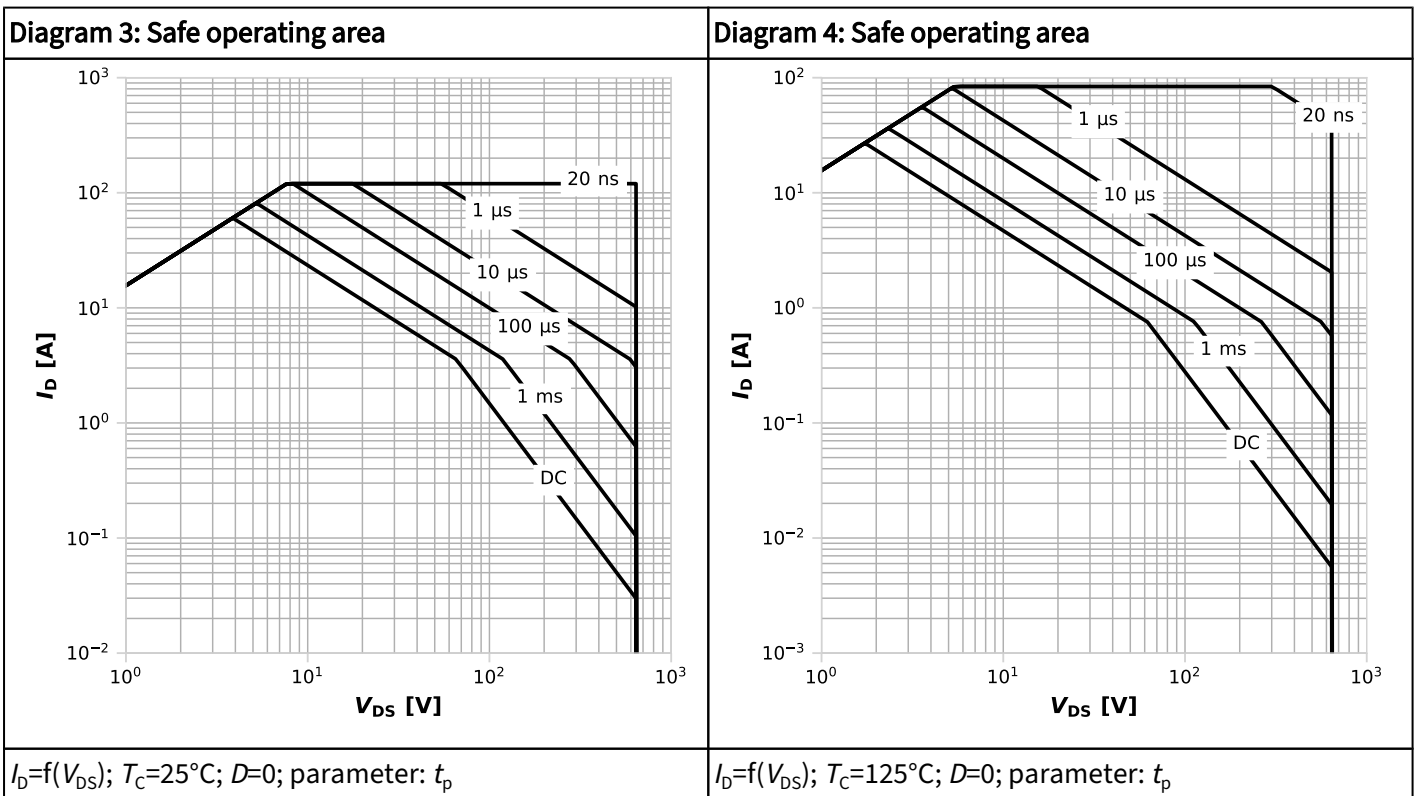
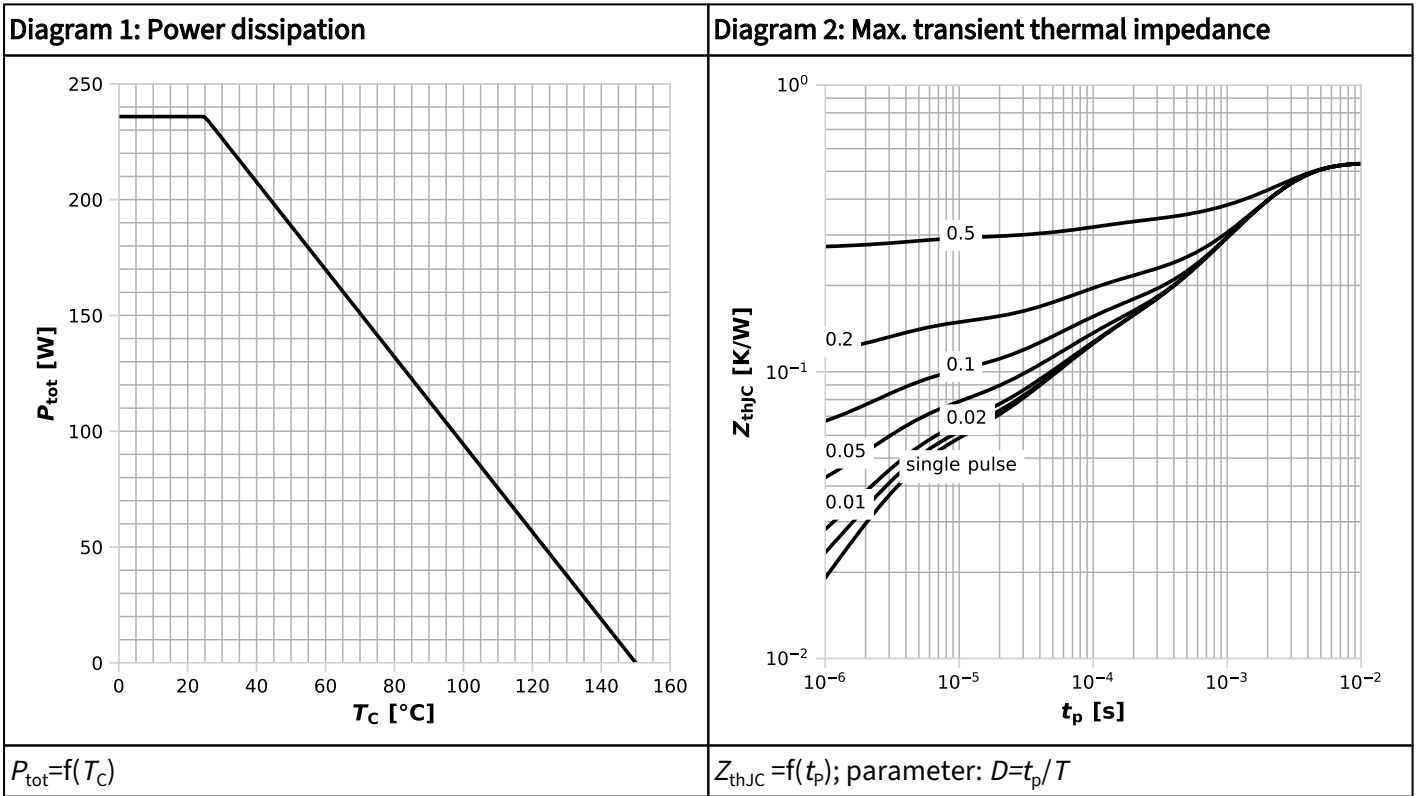
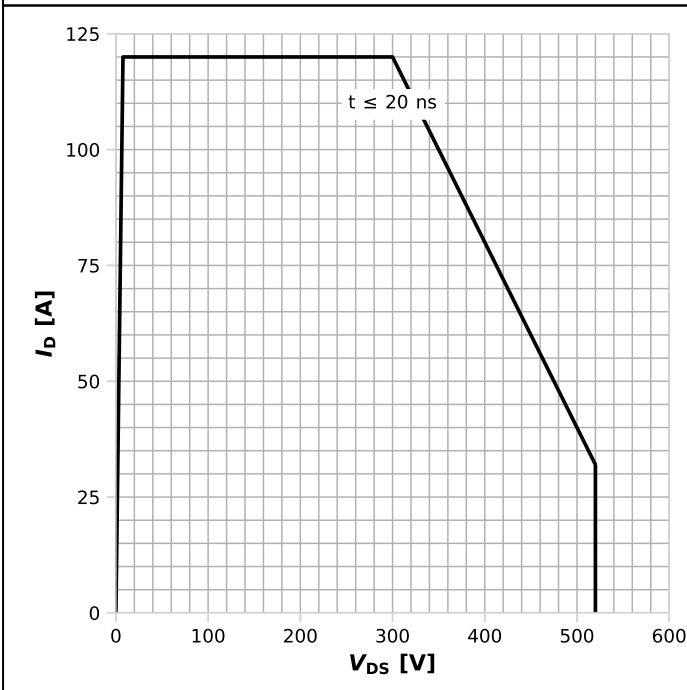


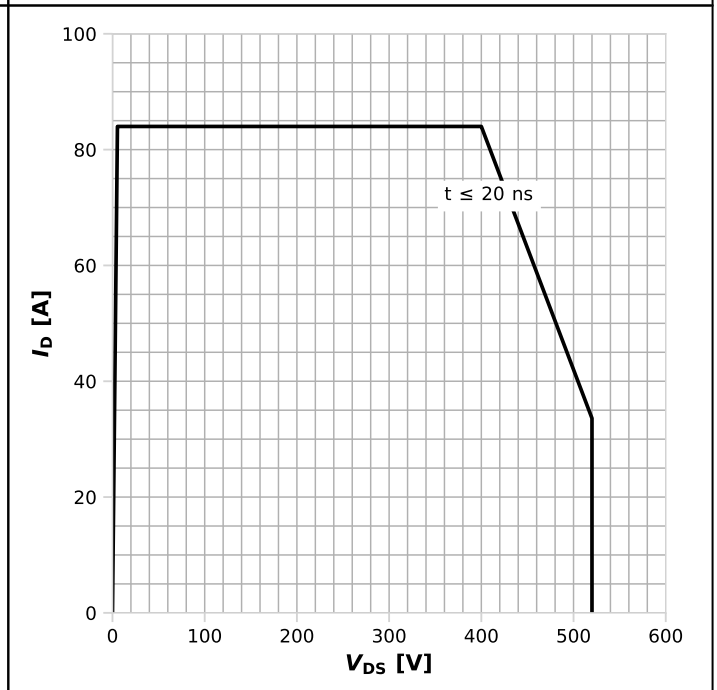


Diagram 5: Repetitive safe operating area



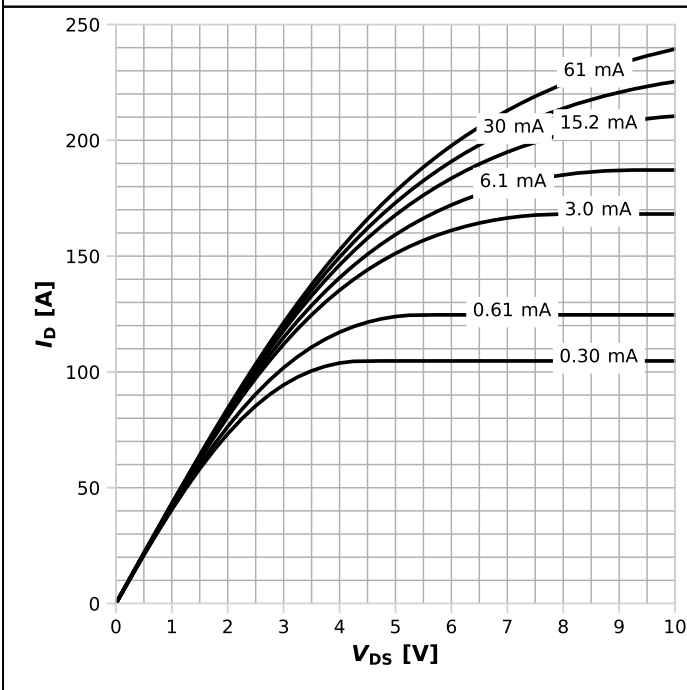
$I_D=f(V_{DS}); T_C=25^\circ\text{C}; T_J\leq 150^\circ\text{C};$  parameter:  $t_p$

Diagram 6: Repetitive safe operating area



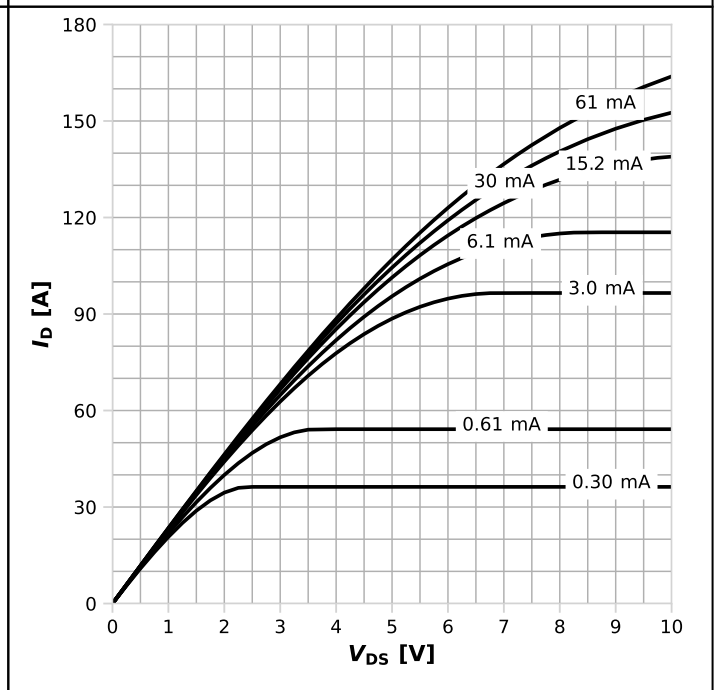
$I_D=f(V_{DS}); T_C=125^\circ\text{C}; T_J\leq 150^\circ\text{C};$  parameter:  $t_p$

Diagram 7: Typ. output characteristics



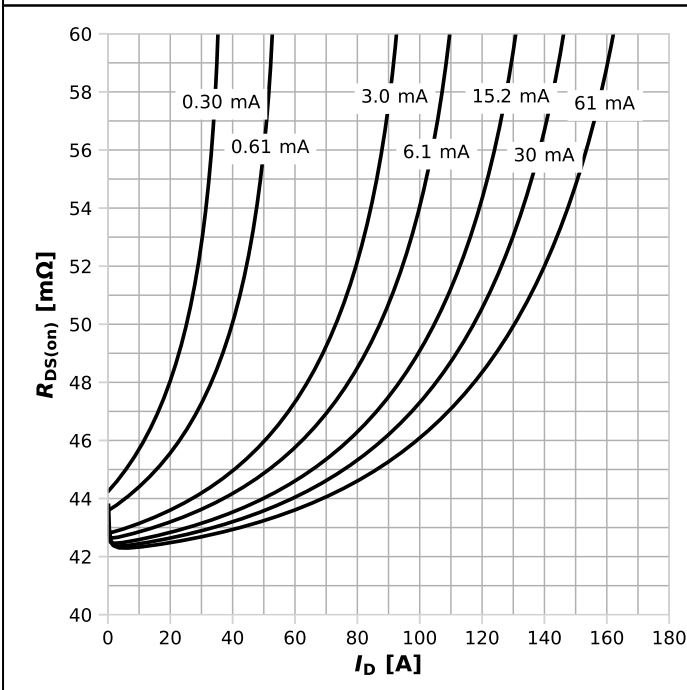
$I_D=f(V_{DS}); T_J=25^\circ\text{C};$  parameter:  $I_{GS}$

Diagram 8: Typ. output characteristics



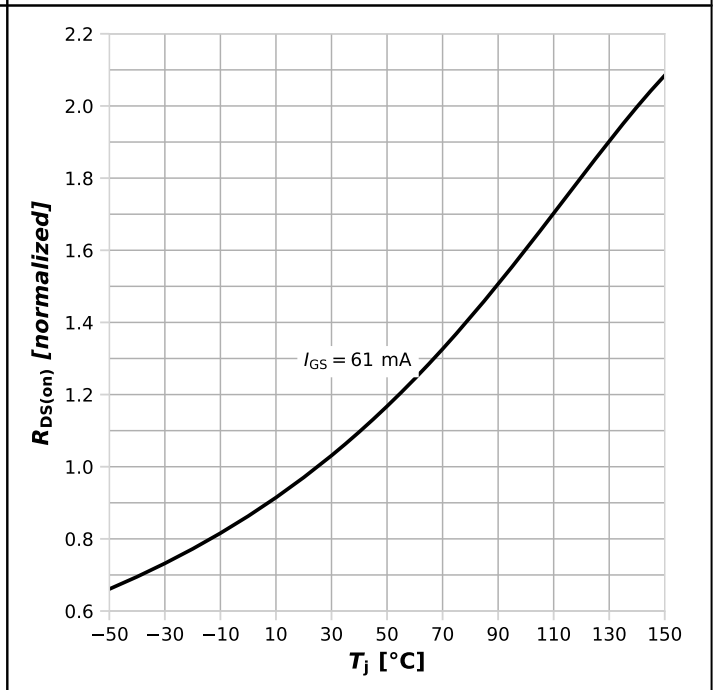
$I_D=f(V_{DS}); T_J=125^\circ\text{C};$  parameter:  $I_{GS}$

Diagram 9: Typ. Drain-source on-state resistance



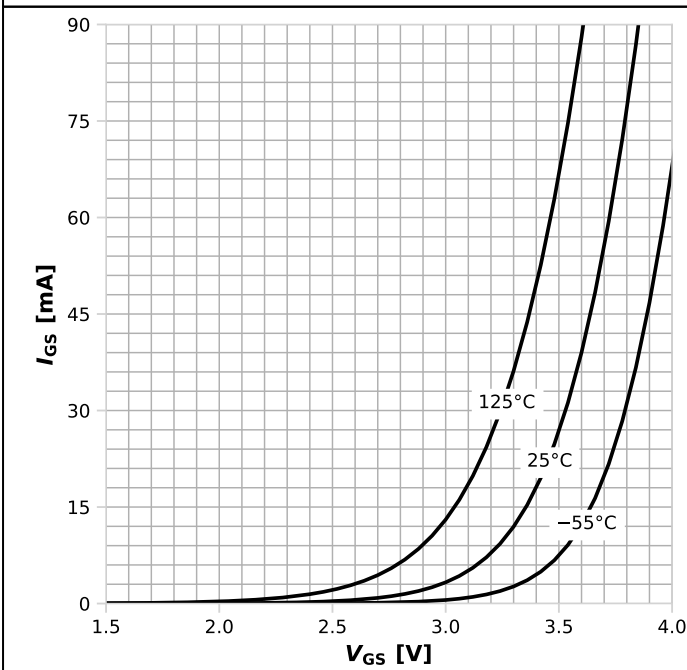
$R_{DS(on)}=f(I_D); T_j=125^\circ\text{C}; \text{parameter: } I_{GS}$

Diagram 10: Drain-source on-state resistance



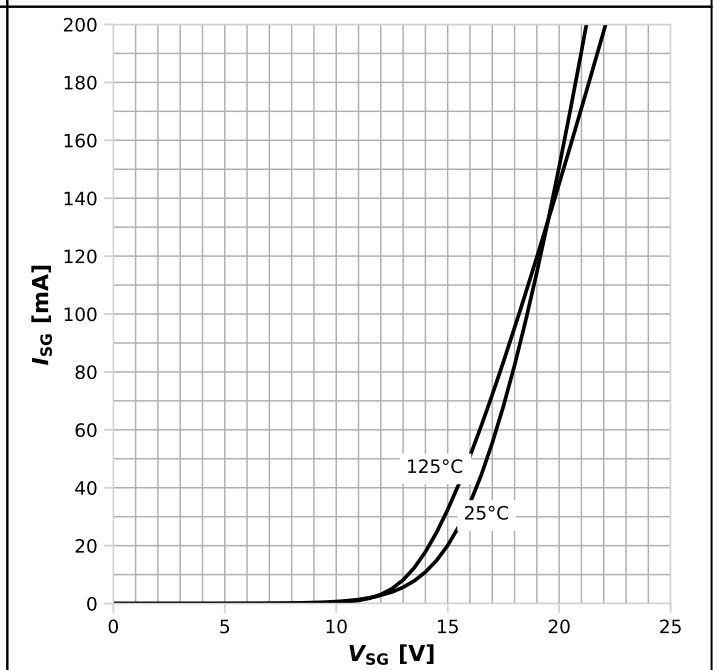
$R_{DS(on)}=f(T_j); I_D=18 \text{ A}$

Diagram 11: Typ. gate characteristics forward



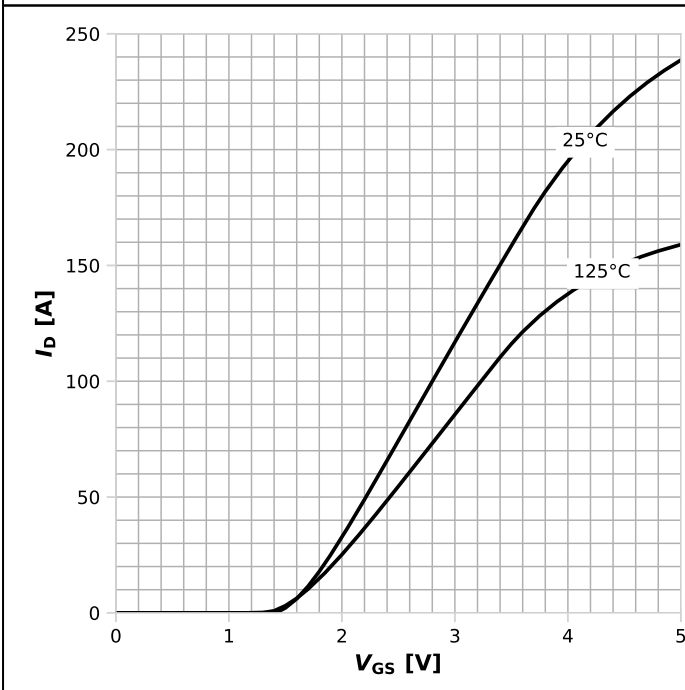
$I_{GS}=f(V_{GS}); \text{open drain}; \text{parameter: } T_j$

Diagram 12: Typ. gate characteristics reverse



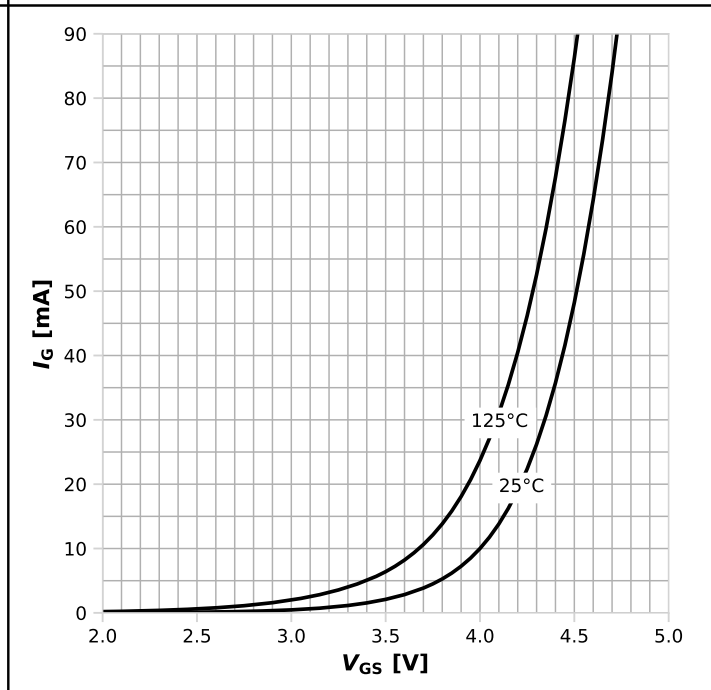
$I_{SG}=f(V_{SG}); \text{parameter: } T_j$

Diagram 13: Typ. transfer characteristics



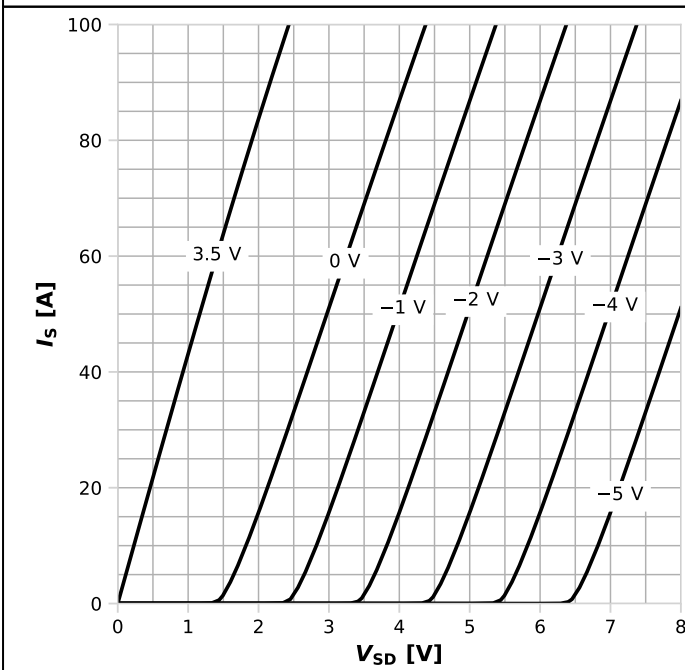
$I_D = f(V_{GS}); V_{DS} = 8V; \text{parameter: } T_j$

Diagram 14: Typ. transfer gate current characteristic



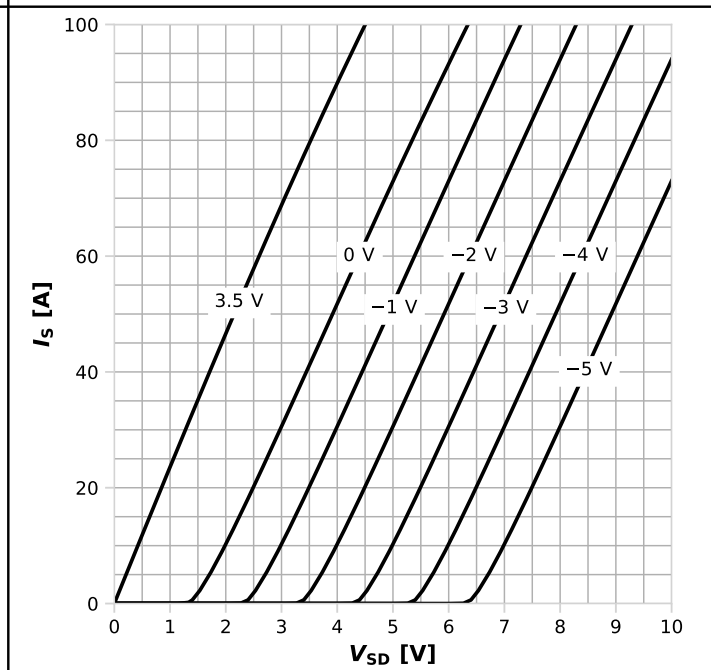
$I_G = f(V_{GS}); V_{DS} = 8V; \text{parameter: } T_j$

Diagram 15: Typ. channel reverse characteristics



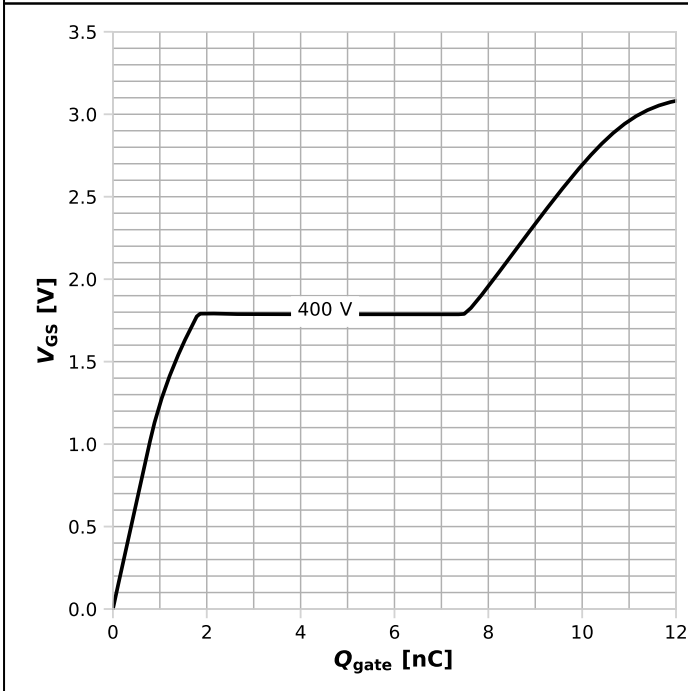
$I_S = f(V_{SD}); T_j = 25^\circ C; \text{parameter: } V_{GS}$

Diagram 16: Typ. channel reverse characteristics



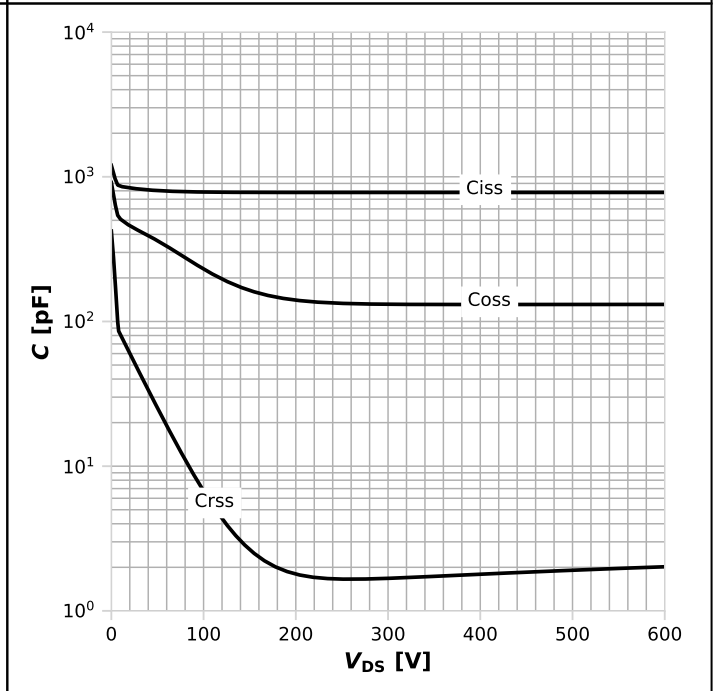
$I_S = f(V_{SD}); T_j = 125^\circ C; \text{parameter: } V_{GS}$

Diagram 17 Typ. gate charge



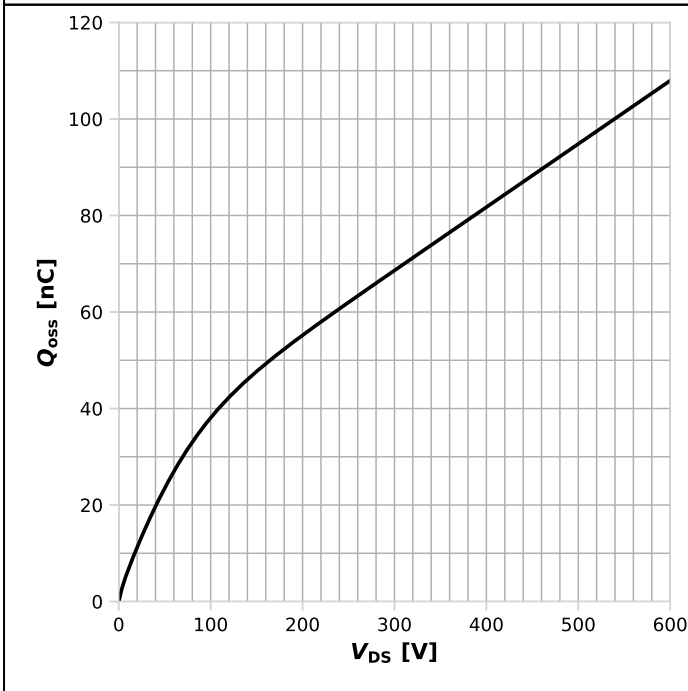
$V_{GS}=f(Q_{gate})$ ;  $I_D=18$  A pulsed;  $I_G=4.5$  mA; parameter:  $V_{DD}$

Diagram 18: Typ. capacitances



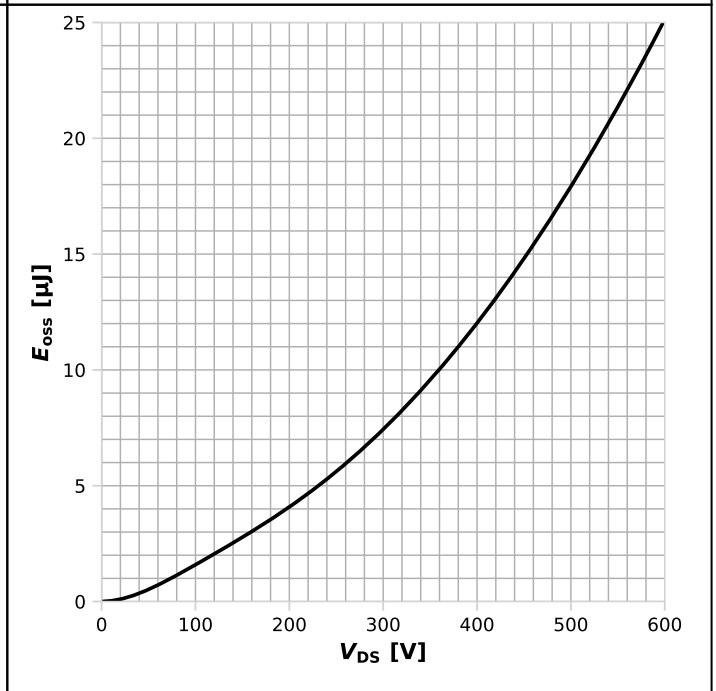
$C=f(V_{DS})$ ;  $V_{GS}=0$  V

Diagram 19: Typ. output charge



$Q_{oss}=f(V_{DS})$

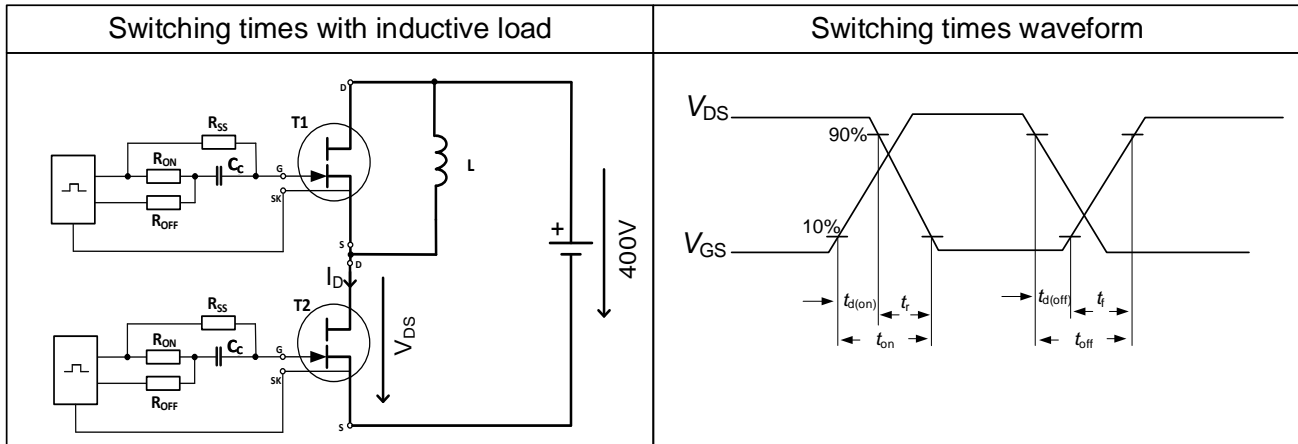
Diagram 20: Typ. Coss stored energy



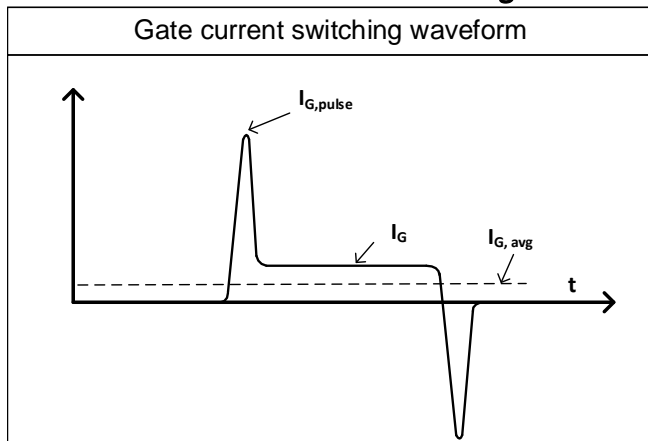
$E_{oss}=f(V_{DS})$

## 5 Test circuits

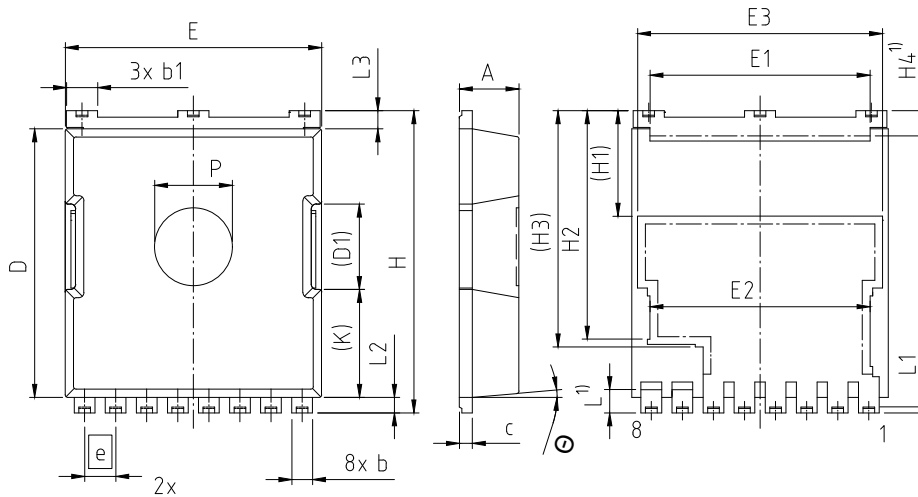
**Table 8 Reverse channel characteristics test**



**Table 9 Gate current switching waveform**



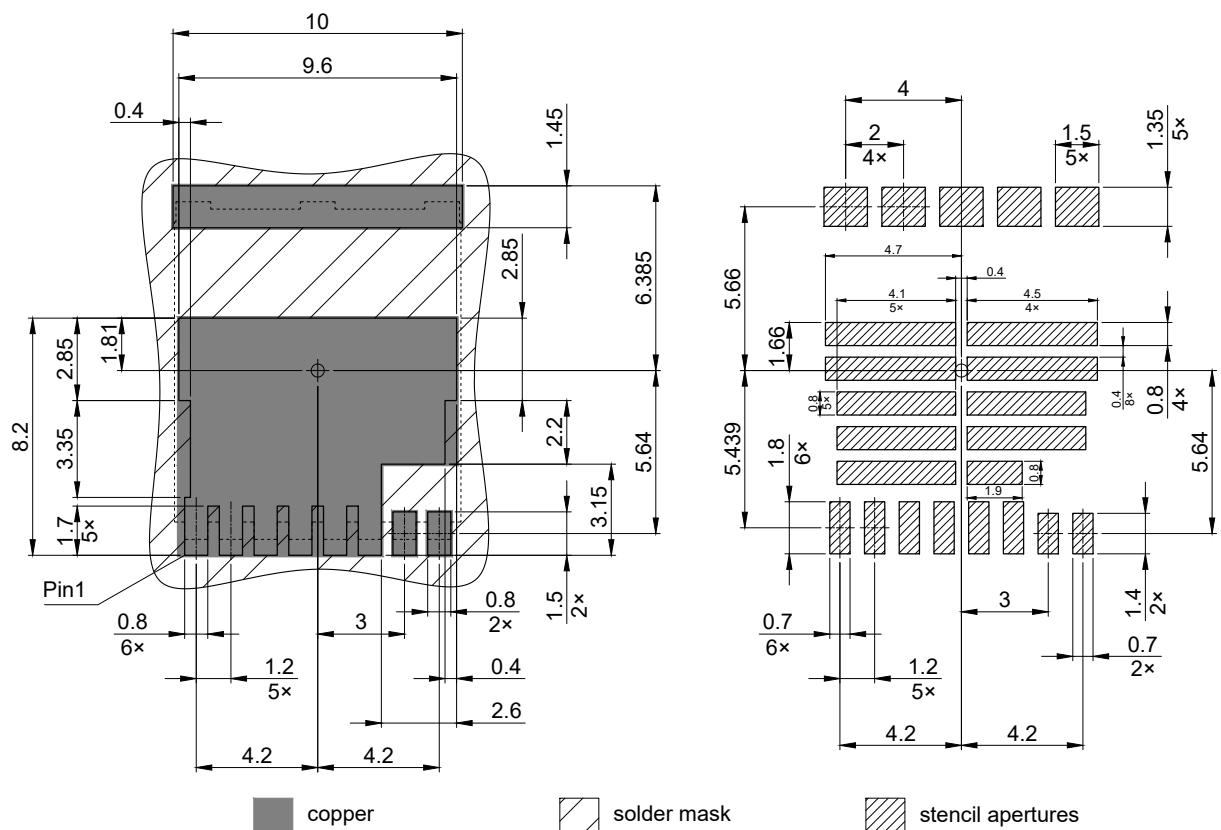
## 6 Package outlines



| PACKAGE - GROUP NUMBER: PG-HSOF-8-U04 |             |        |
|---------------------------------------|-------------|--------|
| DIMENSIONS                            | MILLIMETERS |        |
|                                       | MIN.        | MAX.   |
| A                                     | 2.20        | 2.40   |
| b                                     | 0.70        | 0.90   |
| b1                                    | 1.10        | 1.30   |
| c                                     | 0.40        | 0.60   |
| D                                     | 10.275      | 10.575 |
| D1                                    | (3.20)      | (3.40) |
| E                                     | 9.70        | 10.10  |
| E1                                    | 8.40        | 8.60   |
| E2                                    | 8.40        | 8.60   |
| E3                                    | 9.36        | 9.56   |
| e                                     | 1.20        |        |
| H                                     | 11.475      | 11.875 |
| H1                                    | (3.98)      | (4.18) |
| H2                                    | 8.73        | 8.93   |
| H3                                    | (9.03)      | (9.23) |
| H4                                    | 0.88        | 1.08   |
| N                                     | 8           |        |
| K                                     | (4.07)      | (4.27) |
| L                                     | 0.80        | 1.00   |
| L1                                    | 0.13        | 0.33   |
| L2                                    | 0.50        | 0.70   |
| L3                                    | 0.60        | 0.80   |
| P                                     | 2.90        | 3.10   |
| Θ                                     | 3.5°        | 6.5°   |

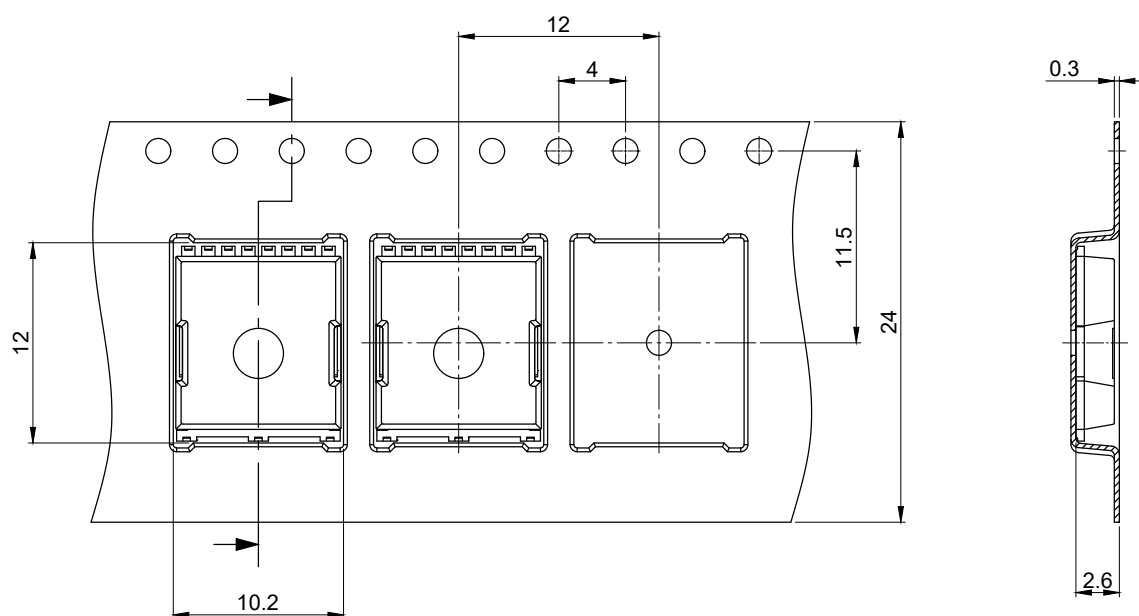
NOTES:  
1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED

Figure 1 Outline PG-HSOF-8, dimensions in mm



Based on stencil thickness 0.130 mm  
 All dimensions are in units mm

**Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm**



All dimensions are in units mm  
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥]

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm



## 7 Appendix A

Table 10 Related links

- [CoolGaN™ GaN 650 V webpage](#)
- [CoolGaN™ GaN 650 V reliability white paper](#)
- [CoolGaN™ GaN 650 V gate driver application note](#)
- [CoolGaN™ GaN 650 V applications information](#)

## Revision history

IGT65R025D2

### Revision 2024-11-28, Rev. 1.0

Previous revisions

| Revision | Date       | Subjects (major changes since last revision) |
|----------|------------|--|
| 1.0      | 2024-11-28 | Release of final                             |

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#### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.