

# CIPOS™ Mini IPM

## IM06B15AC1, 600 V 15 A

### Description

The CIPOS™ Mini IPM product family offers the chance for integrating various power and control components to increase reliability and optimize PCB size and system cost. It is designed to control 3-phase motors in variable speed drives. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also less EMI and overload protection. To deliver excellent electrical performance, Infineon's leading-edge TRENCHSTOP™ IGBTs and anti-parallel diodes are combined with an optimized SOI gate driver.

### Features

#### Package

- Fully isolated dual in-line molded module
- Lead-free terminal plating; RoHS compliant

#### Inverter

- 650 V TRENCHSTOP™ IGBT7 T7
- 600 V rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative  $V_S$  potential up to -11 V for signal transmission at  $V_{BS} = 15$  V
- Integrated bootstrap functionality
- Overcurrent shutdown
- Built-in NTC thermistor for temperature monitor
- Undervoltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection



### Potential applications

- Air-conditioners, home appliances, motor drives

**Product validation**

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

**Table 1 Product Information**

Base part number	Package type	Standard pack		Remarks
		Form	MOQ	
IM06B15AC1	DIP 36x21	14 pcs / Tube	280 pcs	

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# 1 Internal electrical schematic

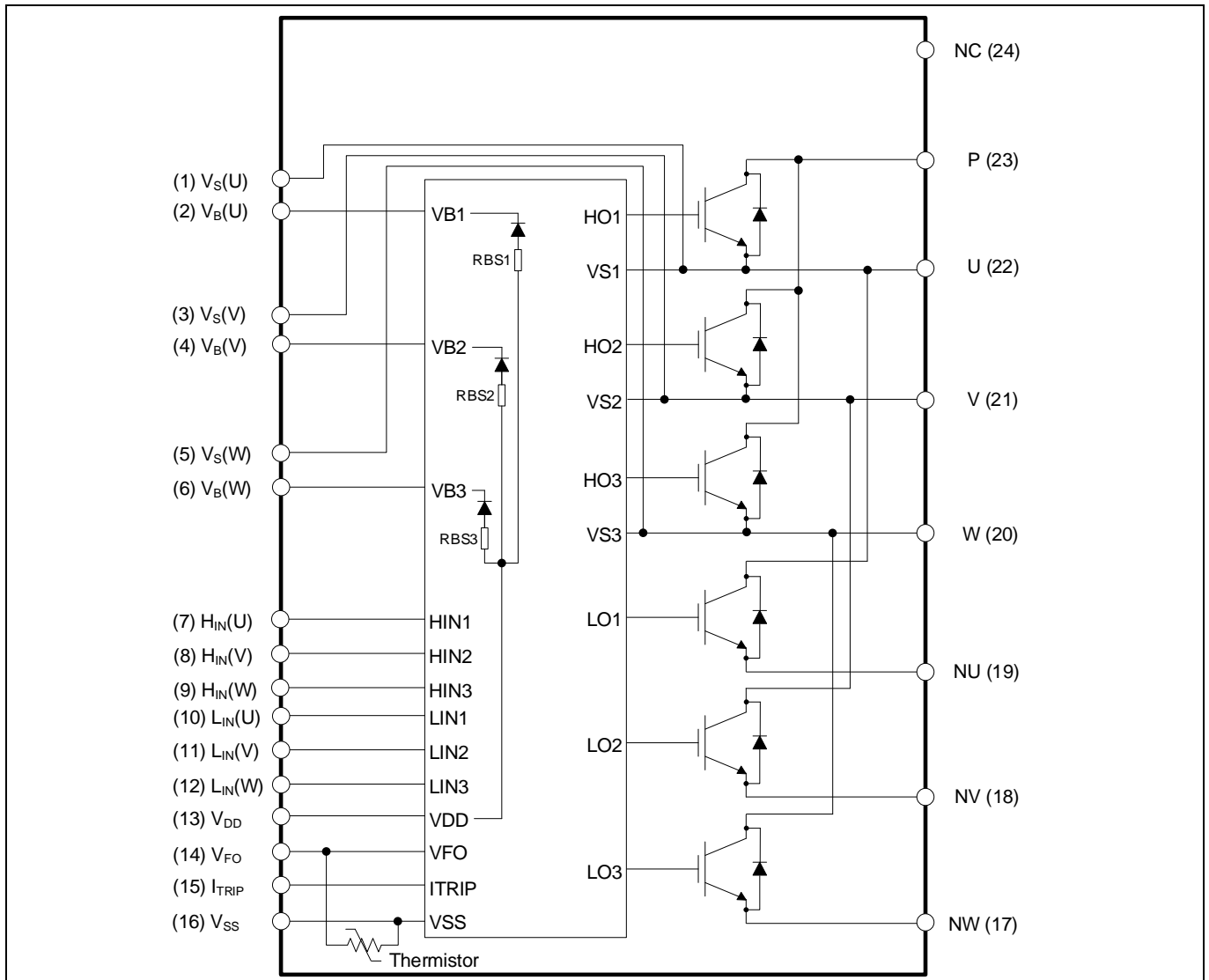


Figure 1 Internal electrical schematic

Pin description

## 2 Pin description

### 2.1 Pin assignment

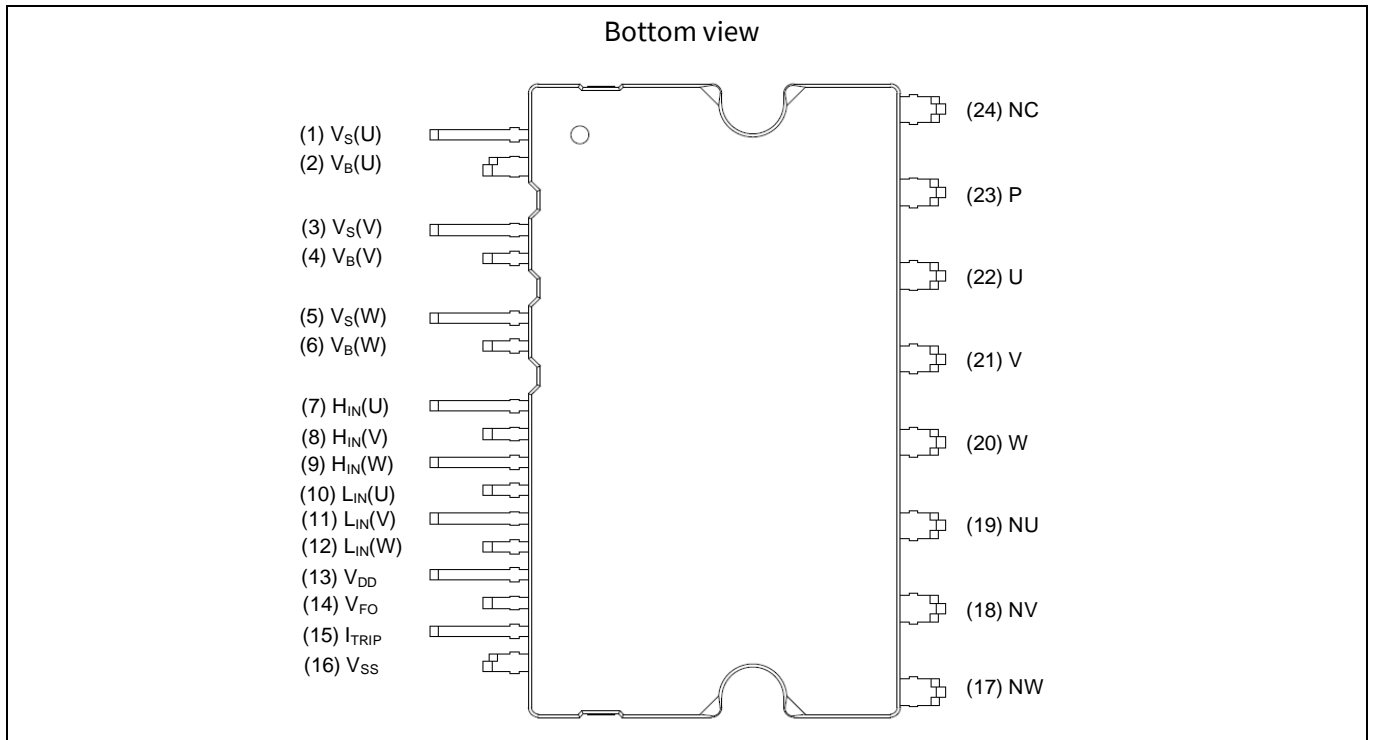


Figure 2 Internal electrical schematic

Table 2 Pin assignment

Pin number	Pin name	Pin description
1	$V_S(U)$	U-phase high-side floating IC supply offset voltage
2	$V_B(U)$	U-phase high-side floating IC supply voltage
3	$V_S(V)$	V-phase high-side floating IC supply offset voltage
4	$V_B(V)$	V-phase high-side floating IC supply voltage
5	$V_S(W)$	W-phase high-side floating IC supply offset voltage
6	$V_B(W)$	W-phase high-side floating IC supply voltage
7	$H_{IN}(U)$	U-phase high-side gate driver input
8	$H_{IN}(V)$	V-phase high-side gate driver input
9	$H_{IN}(W)$	W-phase high-side gate driver input
10	$L_{IN}(U)$	U-phase low-side gate driver input
11	$L_{IN}(V)$	V-phase low-side gate driver input
12	$L_{IN}(W)$	W-phase low-side gate driver input
13	$V_{DD}$	Low-side control supply
14	$V_{FO}$	Fault output / temperature monitor
15	$I_{TRIP}$	Overcurrent shutdown input
16	$V_{SS}$	Low-side control negative supply
17	NW	W-phase low-side emitter

Pin description

Pin number	Pin name	Pin description
18	NV	V-phase low-side emitter
19	NU	U-phase low-side emitter
20	W	Motor W-phase output
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No connection

2.2 Pin description

**H<sub>IN</sub> (U, V, W) and L<sub>IN</sub> (U, V, W) (Low-side and high-side control pins, Pin 7 - 12)**

These pins are positive logic, and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up, and a zener clamp is provided to protect the pins. Negative pulses down to an absolute minimum of -5.5 V are allowed that offers an outstanding robustness. Input Schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses shorter than the filter time  $t_{FIL, IN}$ . The Figure 4 describes how the filter works. An input pulse-width shorter than 1 μs is not recommended.

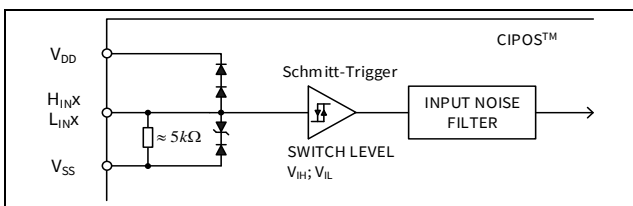


Figure 3 Input pin structure

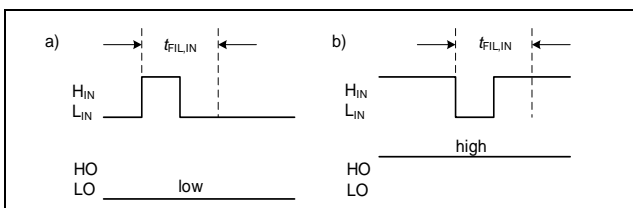


Figure 4 Input filter timing diagram

The integrated gate driver additionally provides a shoot-through prevention capability that avoids the simultaneous on-states of the same leg. When both

inputs of the same leg are activated, only formerly activated one remained activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 360 ns is also provided by driver to reduce cross-conduction of the IGBTs.

**V<sub>FO</sub> (Fault-output and NTC, Pin 14)**

The V<sub>FO</sub> pin indicates a module failure in case of undervoltage at pin V<sub>DD</sub> or in case of triggered overcurrent detection at I<sub>TRIP</sub>. An external pull-up resistor is required.

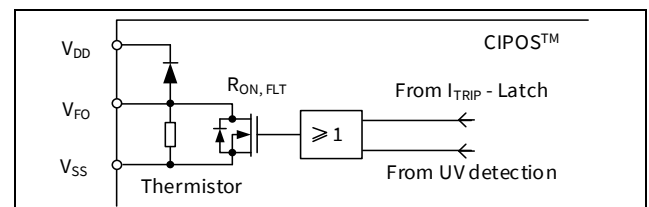


Figure 5 Internal circuit at pin V<sub>FO</sub>

The sleep function is activated after each trigger of I<sub>TRIP</sub> or undervoltage lockout. A new edge input signal is mandatory to activate gate drives after fault-clear time.

**I<sub>TRIP</sub> (Overcurrent detection function, Pin 15)**

This product family provides an overcurrent detection function by connecting the I<sub>TRIP</sub> input with the IGBT current feedback. The I<sub>TRIP</sub> comparator threshold (typ. 0.525 V) is referenced to V<sub>SS</sub>. An input noise filter ( $t_{TRIP} = \text{typ. } 530 \text{ ns}$ ) prevents the driver to detect false overcurrent events.

Overcurrent detection generates a shutdown of outputs of the gate driver. Fast track shutdown function allows low-side outputs to be turned off faster than high side outputs about 200 ns.

The fault-clear time is set to minimum 100 μs.

## Pin description

### **$V_{DD}$ , $V_{SS}$ (Low-side control supply and reference, Pin 13, 16)**

$V_{DD}$  is the control supply, and it provides power both to input logic and to output stage. Input logic is referenced to  $V_{SS}$  ground.

The undervoltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of  $V_{DDUV+} = 12.4$  V is present.

The gate driver shuts down all the outputs, when the  $V_{DD}$  supply voltage is below  $V_{DDUV-} = 11.5$  V. This prevents the IGBTs from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

### **$V_B$ (U, V, W) and $V_S$ (U, V, W) (High-side supplies, Pin 1 - 6)**

$V_B$  to  $V_S$  is the high-side supply voltage. The high-side circuit can float with respect to  $V_{SS}$  following the high-side IGBT emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typical  $V_{BSUV+} = 11.5$  V and a falling threshold of  $V_{BSUV-} = 10.7$  V.

$V_S$  (U, V, W) provide a high robustness against negative voltage in respect of  $V_{SS}$  of -50 V transiently. This ensures very stable designs even under harsh conditions.

### **NW, NV, NU (Low-side emitter, Pin 17 - 19)**

The low-side emitters are available for current measurement of each phase leg. It is recommended to keep the connection to pin  $V_{SS}$  as short as possible to avoid unnecessary inductive voltage drops.

### **W, V, U (High-side emitter and low-side collector, Pin 20 - 22)**

These pins are connected to motor U, V, W input pins.

### **P (Positive bus input voltage, Pin 23)**

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

Absolute maximum ratings

### 3 Absolute maximum ratings

( $V_{DD} = 15\text{ V}$  and  $T_J = 25^\circ\text{C}$ , if not stated otherwise)

#### 3.1 Module section

Description	Symbol	Condition	Value	Unit
Storage temperature range	$T_{STG}$		-40 ~ 125	$^\circ\text{C}$
Operating case temperature	$T_C$	Refer to Figure 7	-40 ~ 125	$^\circ\text{C}$
Operating junction temperature	$T_J$		-40 ~ 150	$^\circ\text{C}$
Maximum junction temperature <sup>1</sup>	$T_{J, \text{switch, max}}$		175	$^\circ\text{C}$
Isolation test voltage	$V_{ISO}$	1 min, RMS, $f = 60\text{ Hz}$	2000	V

#### 3.2 Inverter section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	$V_{CES}$		650	V
DC link supply voltage of P-N	$V_{PN}$	Applied between P-N	450	V
DC link supply voltage (surge) of P-N	$V_{PN(\text{surge})}$	Applied between P-N	500	V
Output current <sup>2</sup>	$I_O$	$T_C = 25^\circ\text{C}, T_J < 150^\circ\text{C}$	$\pm 15$	A
		$T_C = 80^\circ\text{C}, T_J < 150^\circ\text{C}$	$\pm 10$	
Maximum peak output current	$I_{O(\text{peak})}$	$T_C = 25^\circ\text{C}, T_J < 150^\circ\text{C}$ less than 1 ms	$\pm 30$	A
Power dissipation per IGBT	$P_{\text{tot}}$		30.5	W
Short circuit withstand time	$t_{SC}$	$V_{DC} \leq 360\text{V}, T_J = 150^\circ\text{C}$	3	$\mu\text{s}$

#### 3.3 Control section

Description	Symbol	Condition	Value	Unit
High side offset voltage	$V_S$		600	V
Repetitive peak reverse voltage of bootstrap diode	$V_{RRM}$		600	V
Module supply voltage	$V_{DD}$		-1 ~ 20	V
High-side floating supply voltage ( $V_B$ reference to $V_S$ )	$V_{BS}$		-1 ~ 20	V
Input voltage ( $L_{IN}, H_{IN}, I_{TRIP}$ )	$V_{IN}$		-1 ~ $V_{DD} + 0.3$	V

<sup>1</sup>The maximum junction temperature rating of built in power chips is  $175^\circ\text{C}$  under condition: max. 10 sec, every 10 min, max. 1 hrs cumulative over lifetime.

<sup>2</sup> Pulse width and period are limited by junction temperature.



Thermal characteristics

#### 4 Thermal characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single IGBT thermal resistance, junction to case	$R_{thJC}$	See Figure 7 for $T_c$ measurement point	-	-	4.1	K/W
Single diode thermal resistance, junction-case	$R_{thJC,D}$		-	-	5.4	K/W

**Recommended operation conditions**

## 5 Recommended operation conditions

All voltages are absolute voltages referenced to  $V_{SS}$  -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	$V_{PN}$	0	300	400	V
Low-side supply voltage	$V_{DD}$	13	15	18.5	V
High-side floating supply voltage ( $V_B$ vs. $V_S$ )	$V_{BS}$	13	-	18.5	V
Logic input voltages $L_{IN}$ , $H_{IN}$ , $I_{TRIP}$	$V_{IN}$ $V_{ITRIP}$	0	-	5	V
Inverter PWM carrier frequency	$f_{PWM}$	-	-	20	kHz
External deadtime between $H_{IN}$ and $L_{IN}$	DT	1.5	-	-	$\mu s$
Voltage between $V_{SS}$ – N (including surge)	$V_{COMP}$	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$ $PW_{IN(OFF)}$	1	-	-	$\mu s$
Control supply variation	$\Delta V_{BS}$ , $\Delta V_{DD}$	-1 -1	- -	1 1	V/ $\mu s$

Static parameters

## 6 Static parameters

( $V_{DD} = V_{BS} = 15\text{ V}$  and  $T_J = 25^\circ\text{C}$ , if not stated otherwise)

### 6.1 Inverter section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter voltage	$V_{CE(Sat)}$	$I_C = 15\text{ A}, T_J = 25^\circ\text{C}$ $I_C = 15\text{ A}, T_J = 150^\circ\text{C}$	-	1.35 1.50	1.70 -	V
Collector-emitter leakage current	$I_{CES}$	$V_{CE} = 600\text{ V}$	-	-	1.00	mA
Diode forward voltage	$V_F$	$I_F = 15\text{ A}, T_J = 25^\circ\text{C}$ $I_F = 15\text{ A}, T_J = 150^\circ\text{C}$	-	1.75 1.75	2.20 -	V

### 6.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage ( $L_{IN}, H_{IN}$ )	$V_{IH}$		1.7	2.0	2.3	V
Logic "0" input voltage ( $L_{IN}, H_{IN}$ )	$V_{IL}$		0.7	0.9	1.1	V
$I_{TRIP}$ positive going threshold	$V_{IT, TH+}$		475	525	570	mV
$I_{TRIP}$ input hysteresis	$V_{IT, HYS}$		45	70	-	mV
$V_{DD}$ and $V_{BS}$ supply undervoltage positive going threshold	$V_{DDUV+}$		11.5	12.4	13.1	V
	$V_{BSUV+}$		10.6	11.5	12.2	
$V_{DD}$ and $V_{BS}$ supply undervoltage negative going threshold	$V_{DDUV-}$		10.6	11.5	12.3	V
	$V_{BSUV-}$		9.7	10.7	11.7	
$V_{DD}$ and $V_{BS}$ supply undervoltage lockout hysteresis	$V_{DDUVH}$ $V_{BSUVH}$		0.5	0.9	-	V
Quiescent $V_{Bx}$ supply current ( $V_{Bx}$ only)	$I_{QBS}$	$H_{IN} = 0\text{ V}$	-	-	300	$\mu\text{A}$
Quiescent $V_{DD}$ supply current ( $V_{DD}$ only)	$I_{QDD}$	$L_{IN} = 0\text{ V}, H_{INX} = 5\text{ V}$	-	-	1.1	mA
Input bias current for $L_{IN}, H_{IN}$	$I_{IN+}$	$V_{IN} = 5\text{ V}$	-	1.1	1.7	mA
Input bias current for $I_{TRIP}$	$I_{ITRIP+}$	$V_{ITRIP} = 5\text{ V}$	-	68	185	$\mu\text{A}$
Input bias current for $V_{FO}$	$I_{FO}$	$V_{FO} = 5\text{ V}, V_{ITRIP} = 0\text{ V}$	-	60	-	$\mu\text{A}$
$V_{FO}$ output voltage	$V_{FO}$	$I_{FO} = 10\text{ mA}, V_{ITRIP} = 1\text{ V}$	-	0.35	-	V
Bootstrap diode forward voltage	$V_{F\_BSD}$	$I_F = 0.3\text{ mA}$	-	1.0	-	V
Bootstrap diode resistance	$R_{BSD}$	Between $V_{F1} = 4\text{ V}$ and $V_{F2} = 5\text{ V}$	-	37	-	$\Omega$

Dynamic parameters

## 7 Dynamic parameters

( $V_{DD} = 15\text{ V}$  and  $T_J = 25^\circ\text{C}$ , if not stated otherwise)

### 7.1 Inverter section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	$t_{on}$	$V_{LIN, HIN} = 5\text{ V}$ , $I_C = 15\text{ A}$ , $V_{DC} = 300\text{ V}$	-	795	-	ns
Turn-on rise time	$t_r$		-	25	-	ns
Turn-on switching time	$t_{c(on)}$		-	135	-	ns
Reverse recovery time	$t_{rr}$		-	105	-	ns
Turn-off propagation delay time	$t_{off}$	$V_{LIN, HIN} = 0\text{ V}$ , $I_C = 15\text{ A}$ , $V_{DC} = 300\text{ V}$	-	985	-	ns
Turn-off fall time	$t_f$		-	30	-	ns
Turn-off switching time	$t_{c(off)}$		-	80	-	ns
Short circuit propagation delay time	$t_{SCP}$	From $V_{IT, TH+}$ to 10% $I_{SC}$	-	1430	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	$E_{on}$	$V_{DC} = 300\text{ V}$ , $I_C = 15\text{ A}$ $T_J = 25^\circ\text{C}$ $T_J = 150^\circ\text{C}$	-	375	-	$\mu\text{J}$
			-	625	-	
IGBT turn-off energy	$E_{off}$	$V_{DC} = 300\text{ V}$ , $I_C = 15\text{ A}$ $T_J = 25^\circ\text{C}$ $T_J = 150^\circ\text{C}$	-	205	-	$\mu\text{J}$
			-	355	-	
Diode recovery energy	$E_{rec}$	$V_{DC} = 300\text{ V}$ , $I_C = 15\text{ A}$ $T_J = 25^\circ\text{C}$ $T_J = 150^\circ\text{C}$	-	55	-	$\mu\text{J}$
			-	145	-	

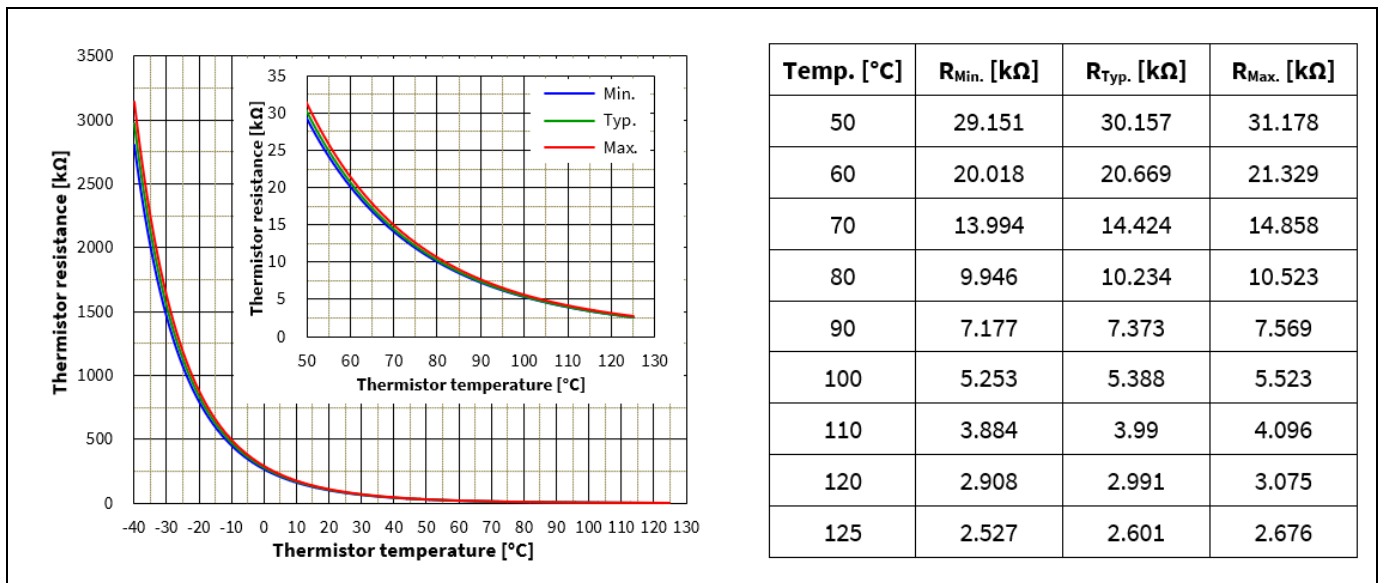
### 7.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input filter time $I_{TRIP}$	$t_{TRIP}$	$V_{ITRIP} = 1\text{ V}$	-	530	-	ns
Input filter time at $L_{IN}$ , $H_{IN}$ for turn on and off	$t_{FIL, IN}$	$V_{LIN, HIN} = 0\text{ V}$ or $5\text{ V}$	-	290	-	ns
Fault clear time after $I_{TRIP}$ -fault	$t_{FLTCLR}$		100	280	-	$\mu\text{s}$
$I_{TRIP}$ to fault propagation delay	$t_{FLT}$	$V_{LIN, HIN} = 0$ or $V_{LIN, HIN} = 5\text{ V}$ , $V_{ITRIP} = 1\text{ V}$	-	680	1000	ns
Internal deadtime	$DT_{IC}$		-	360	-	ns
Matching propagation delay time (on and off) all channels	$M_T$	External dead time > 500 ns	-	20	-	ns

Thermistor

## 8 Thermistor

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Resistance	$R_{NTC}$	$T_{NTC} = 25^{\circ}\text{C}$	-	85	-	$\text{k}\Omega$
B-constant of NTC (negative temperature coefficient) thermistor	B (25/100)		-	4092	-	K



**Figure 6 Thermistor resistance - temperature curve and table**  
(For more information, please refer to the application note)

## 9 Mechanical characteristics and ratings

Description	Condition		Value			Unit
			Min.	Typ.	Max.	
Mounting torque	M3 screw and washer		0.59	0.69	0.78	Nm
Terminal strength pull	Control terminal: Load 5 N Power terminal: Load 10 N	JEITA-ED-4701	10	-	-	S
Terminal strength bendong	Control terminal: Load 2.5 N Power terminal: Load 5 N	JEITA-ED-4701	2	-	-	times
Backside curvature	Refer to Figure 8		-50	-	100	μm
Weight			-	5.92	-	g

**Qualification information**

## 10 Qualification information

<b>UL certification</b>	File number: E314539	
<b>Moisture sensitivity level (SOP23 only)</b>	-	
<b>RoHS compliant</b>	Yes (Lead-free terminal plating)	
<b>ESD</b>	HBM (human body model)	2
	CDM (charged device model)	C2a

## 11 Diagrams and tables

### 11.1 $T_c$ measurement point (top View)

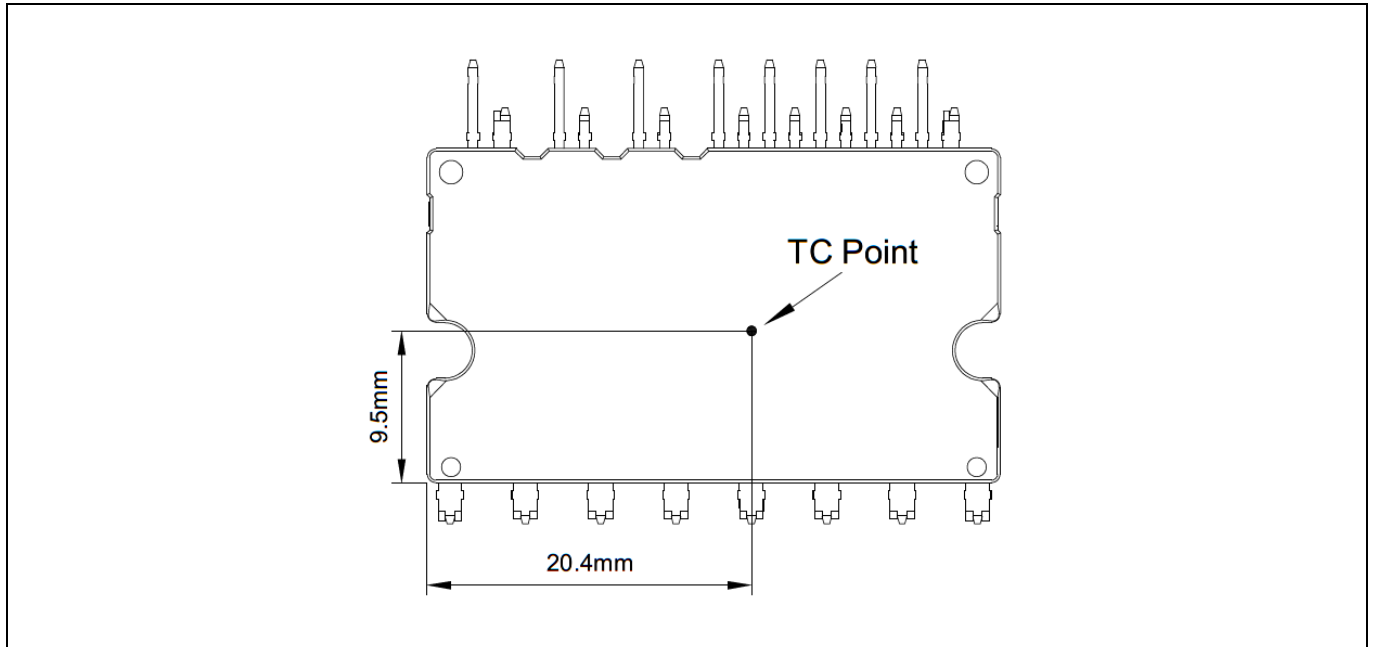
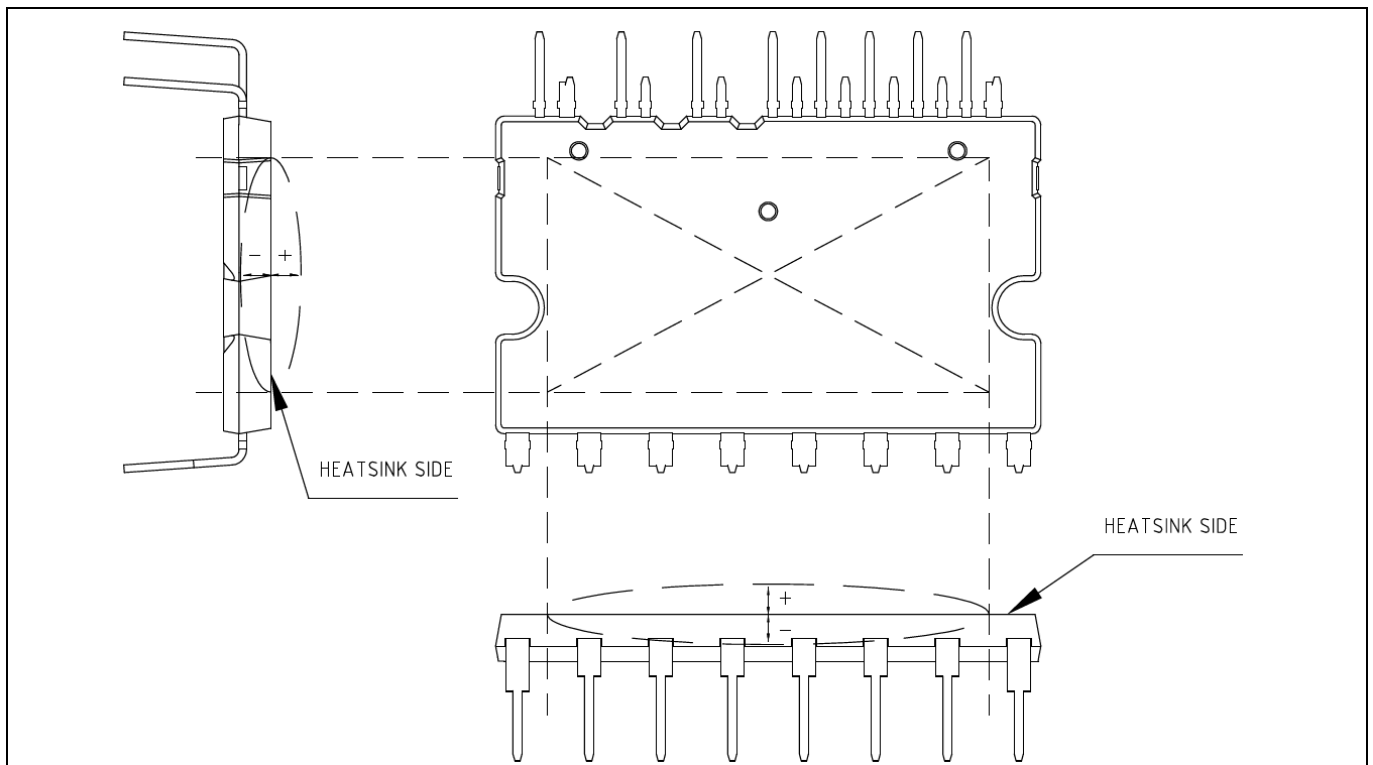


Figure 7  $T_c$  measurement point<sup>1</sup>

### 11.2 Backside curvature measurement point



<sup>1</sup>Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.



Figure 8 Backside curvature measurement position

### 11.3 Switching test circuit

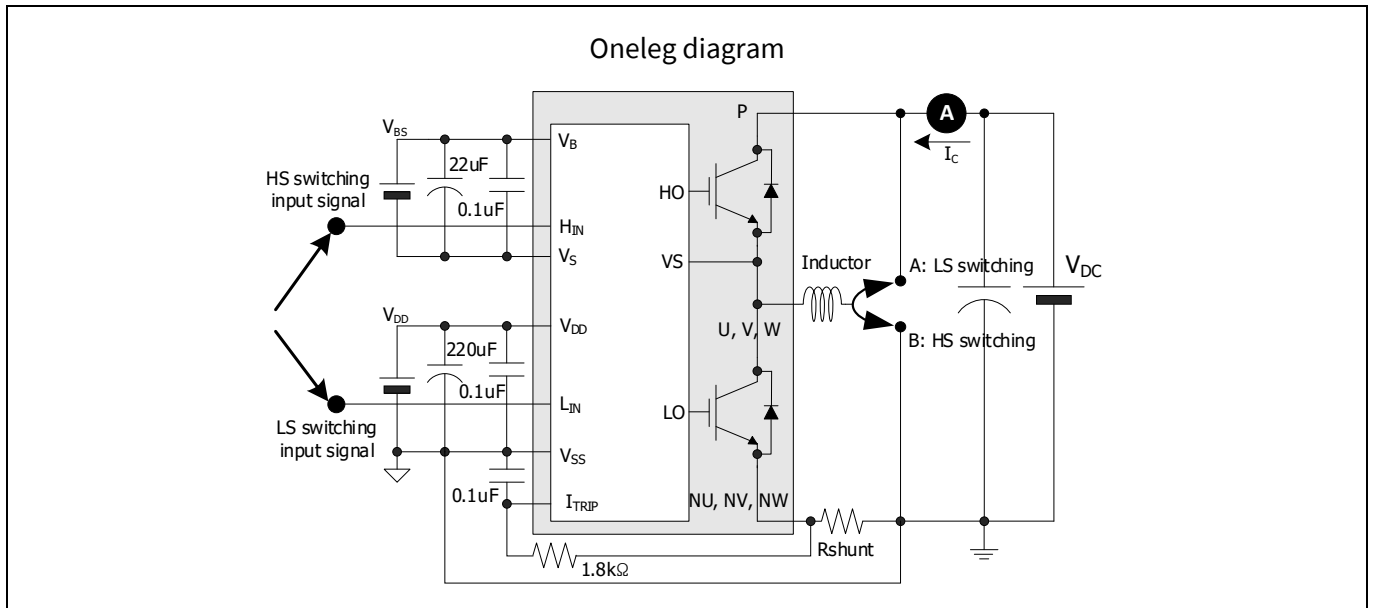


Figure 9 Switching test circuit

### 11.4 Switching time definition

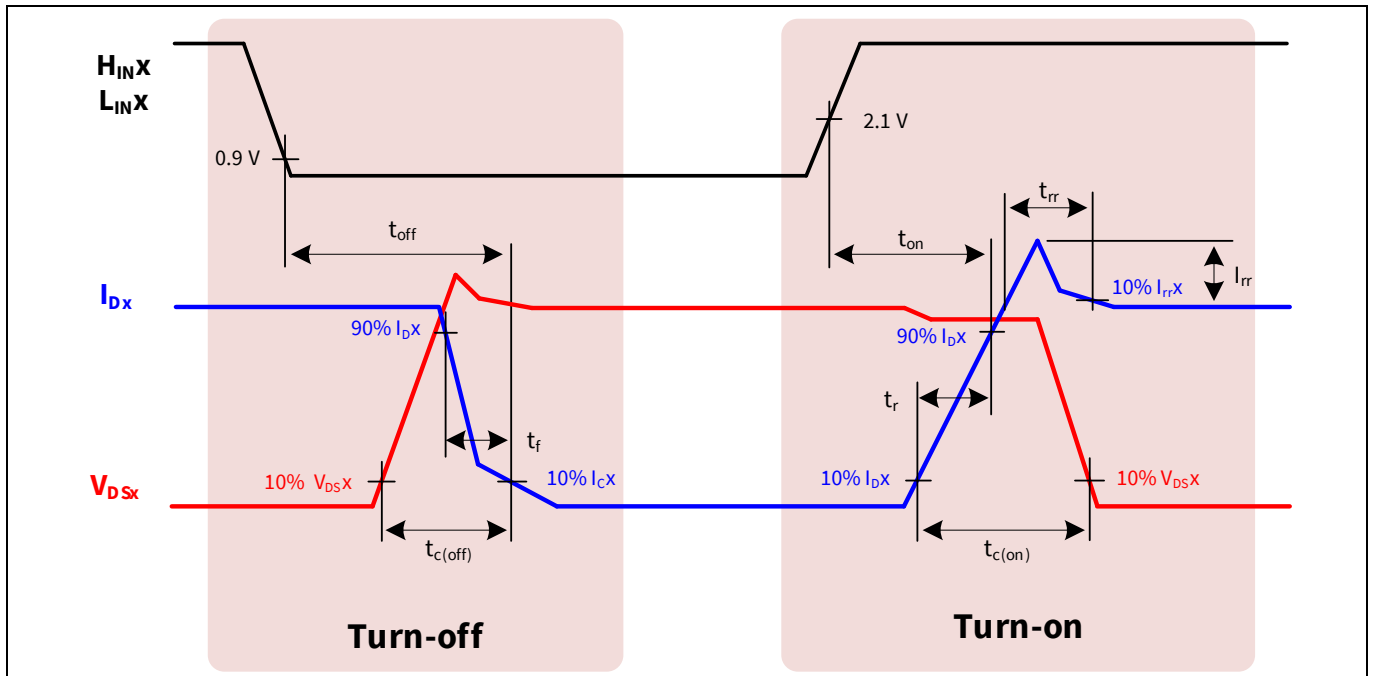
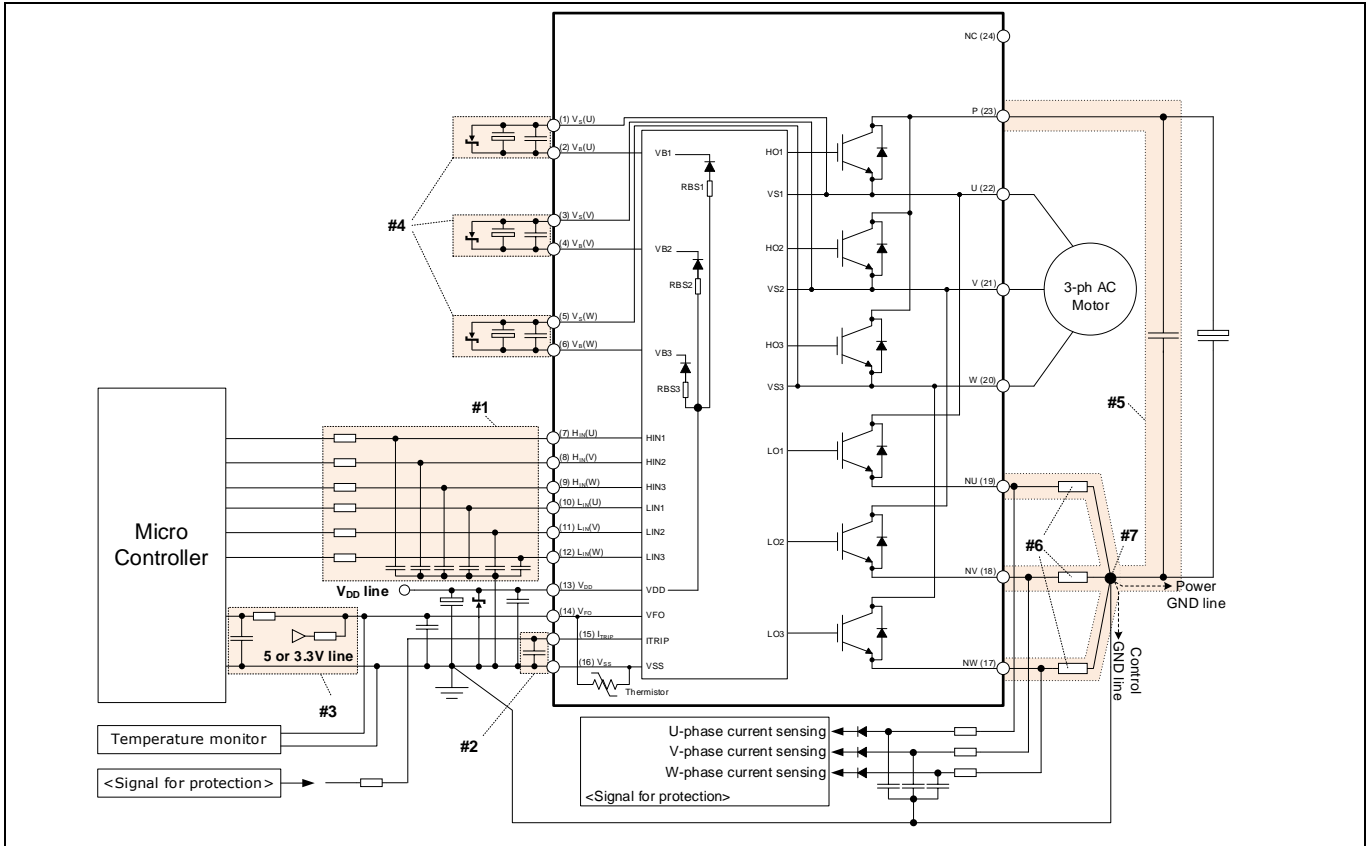


Figure 10 Switching time definition

## 12 Application guide

### 12.1 Typical application schematic



**Figure 11 Typical application circuit**

- #1 Input circuit
  - RC filter circuit can be used to reduce input signal noise (e.g. 100  $\Omega$ , 1 nF).
  - The filter capacitors should be placed close to the IPM (to  $V_{SS}$  pin especially).
- #2  $I_{TRIP}$  circuit
  - To prevent protection function errors, RC filter (1.5~ 2.0  $\mu$ s, e.g. 68  $\Omega$ , 22 nF) circuit is recommended.
  - The filter capacitor should be placed close to  $I_{TRIP}$  and  $V_{SS}$  pins.
- #3  $V_{F0}$  circuit
  - $V_{F0}$  pin is an open-drain output. This signal line should be pulled up to the bias voltage of the 5 V/3.3 V with a proper resistor.
  - It is recommended that RC filter circuit is placed close to the controller.
- #4  $V_B$ - $V_S$  circuit
  - Capacitors for high-side floating supply voltage should be placed close to  $V_B$  and  $V_S$  pins.
- #5 Snubber capacitor
  - The wiring among the IPM, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor
  - SMD-type resistors are strongly recommended to minimize stray inductance.
- #7 Ground pattern
  - Power ground and signal ground should be connected at a single point. It is recommended to connect them at the end of shunt resistor.

12.2 Performance chart

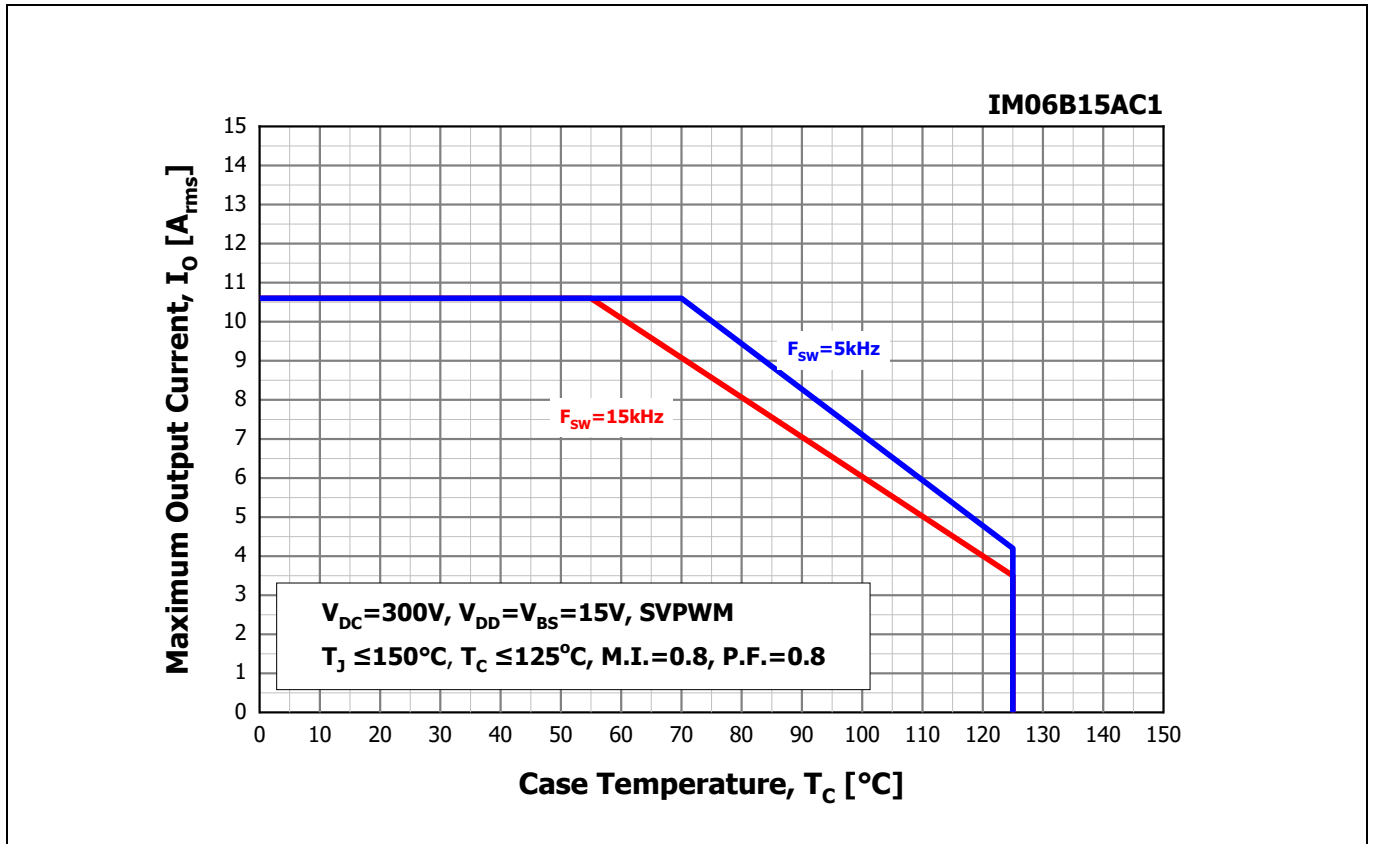


Figure 12 Maximum operating current SOA<sup>1</sup>

<sup>1</sup>This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

Package outline

13 Package outline

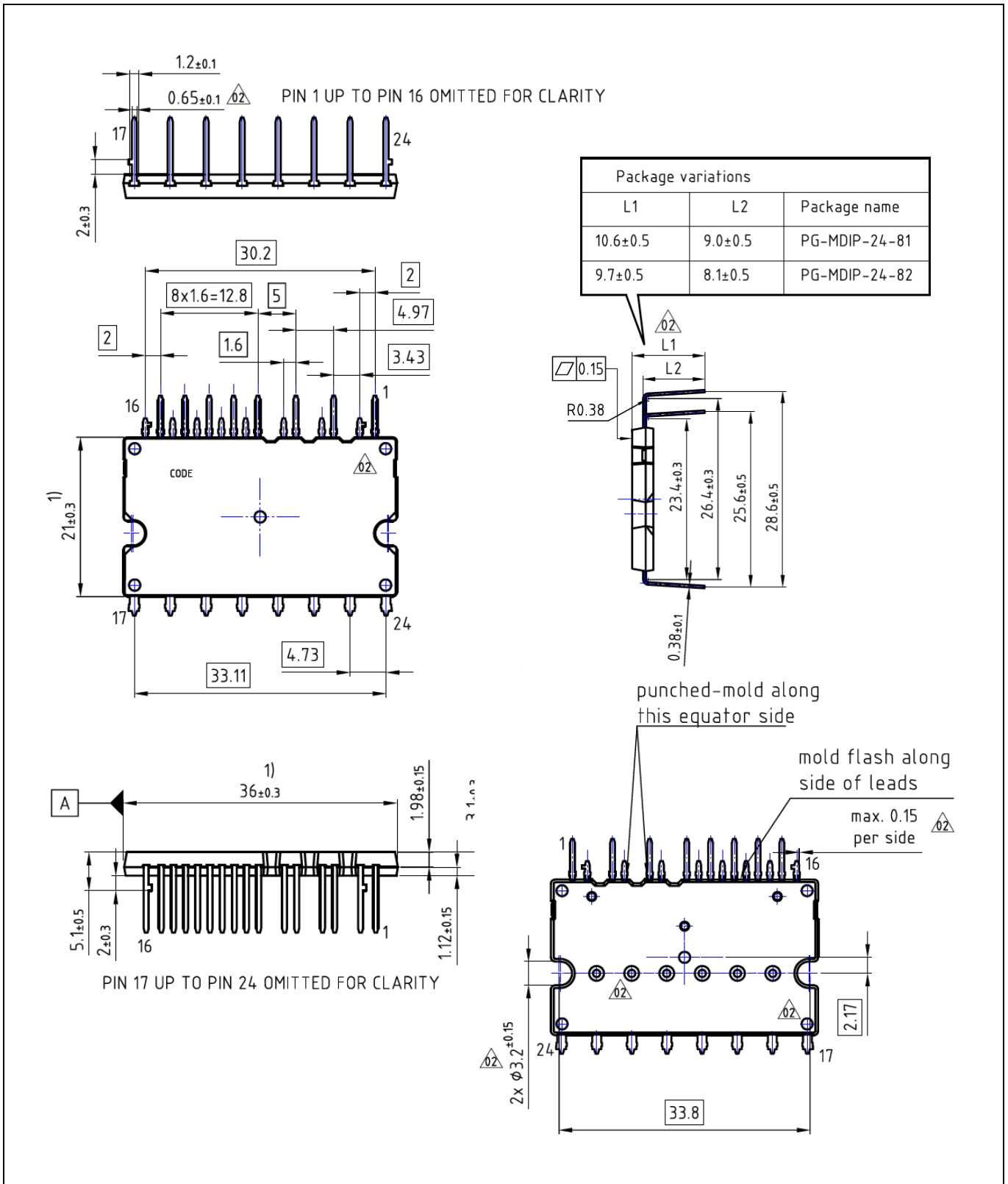


Figure 13 IM06B15AC1

**Revision history**

**Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
V 1.00	2024-08-16	Initial release
V1.10	2024-12-16	Updated Figure 7 and typo

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