CIPOS™ Maxi IPM

IM12B20EC1, 1200 V 20 A

Description

The CIPOS™ Maxi IM12B20EC1 product offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs. It is designed to control three phase AC motors and permanent magnet motors in variable speed drives applications such as low power motor drives (GPI, Servo drives), pumps, fan drives and active filter for HVAC (Heating, Ventilation, and Air Conditioning). The product concept is specially adapted to power applications, which need good thermal performance and electrical isolation as well as EMI save control and overload protection. Three phase inverter with 1200 V TRENCHSTOP™ IGBTs and Emitter Controlled diodes are combined with an optimized 6-channel SOI gate driver for excellent electrical performance.

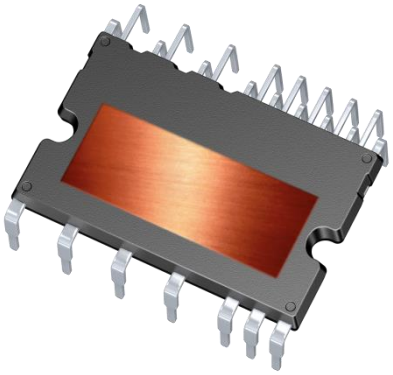
Features

Package

- Fully isolated Dual In-Line molded module
- Very low thermal resistance due to DCB substrate
- Lead-free terminal plating; RoHS compliant

Inverter

- 1200 V TRENCHSTOP™ IGBT7 S7
- Rugged 1200 V SOI gate driver technology with stability against transient and negative voltage
- Allowable negative V_S potential up to -11 V for signal transmission at V_{BS} = 15 V
- Integrated bootstrap functionality
- Overcurrent shutdown
- Built-in NTC thermistor for temperature monitoring
- Undervoltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection
- Programable fault clear timing and enable input



Potential applications

Fan drives and pumps
Active filter for HVAC
Low power motor drives (GPI, Servo drives)

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product information

Base part number	Package type	Standard pack		Remark
		Form	MOQ	
IM12B20EC1	DIP 36x23D	14 pcs / Tube	280 pcs	

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1 Internal electrical schematic

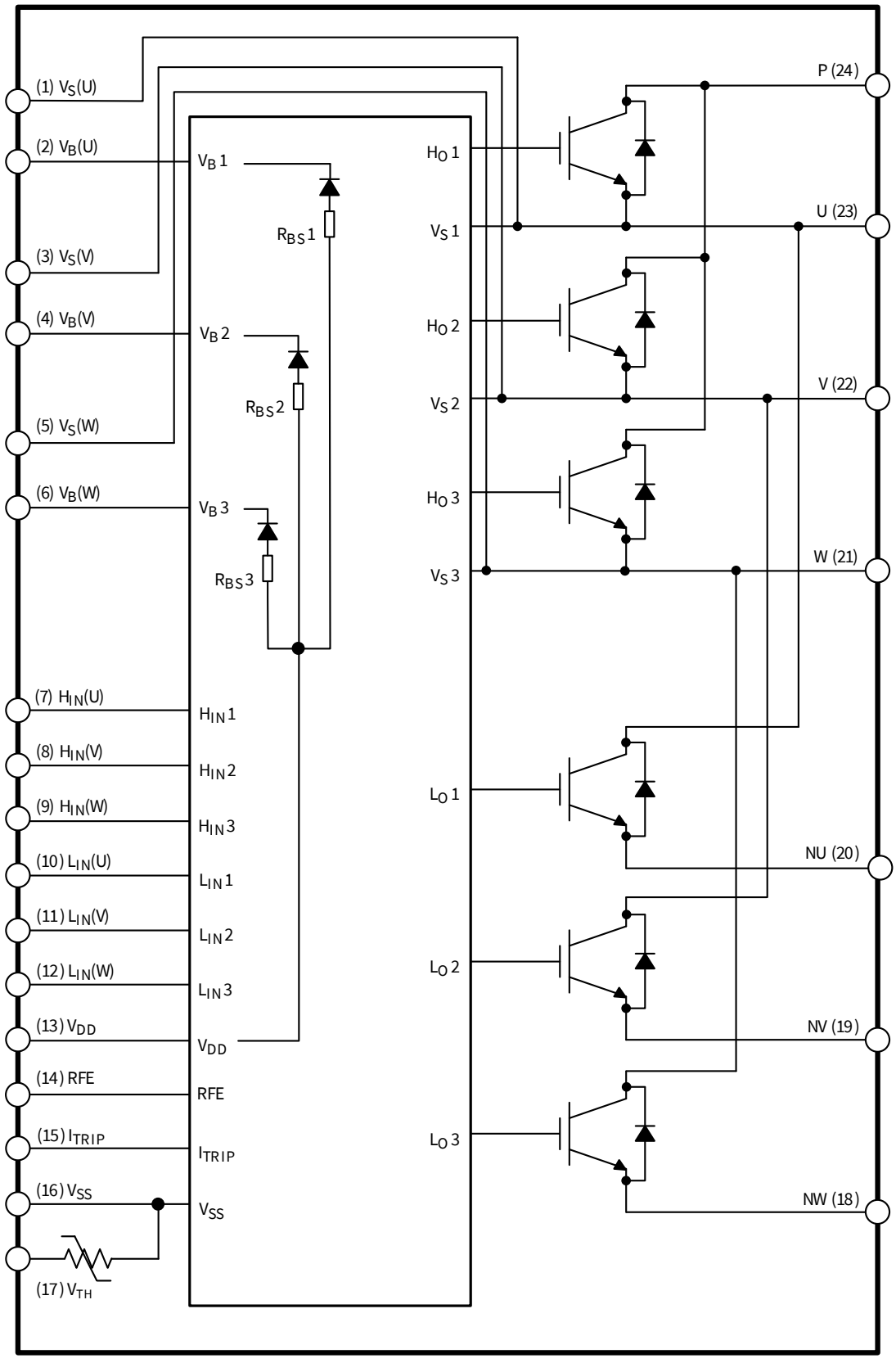


Figure 1 Internal electrical schematic

2 Pin description

2.1 Pin assignment

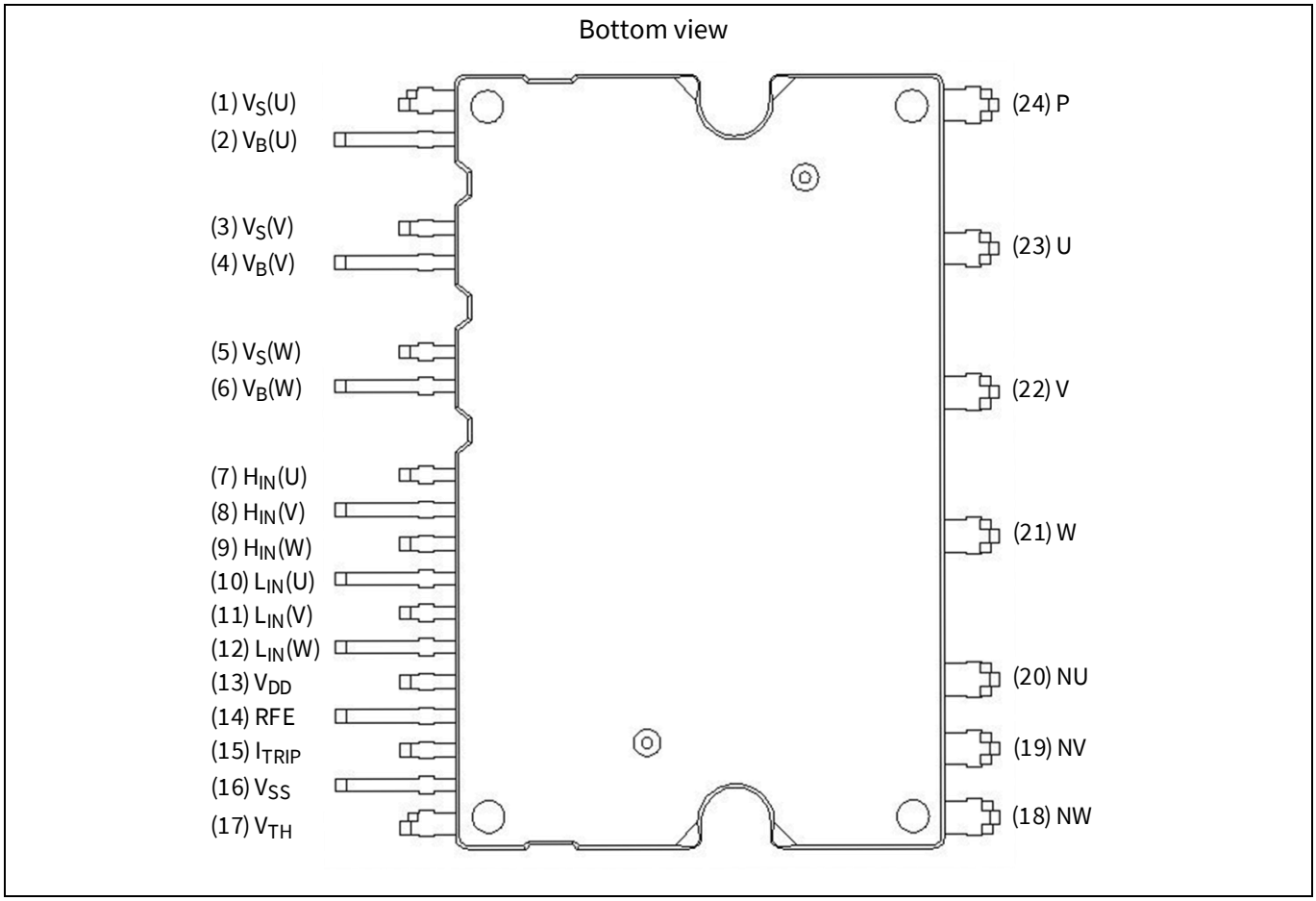


Figure 2 Pin configuration

Table 2 Pin assignment

Pin number	Pin name	Pin description
1	V_S(U)	U-phase high-side floating IC supply offset voltage
2	V_B(U)	U-phase high-side floating IC supply voltage
3	V_S(V)	V-phase high-side floating IC supply offset voltage
4	V_B(V)	V-phase high-side floating IC supply voltage
5	V_S(W)	W-phase high-side floating IC supply offset voltage
6	V_B(W)	W-phase high-side floating IC supply voltage
7	H_{IN}(U)	U-phase high-side gate driver input
8	H_{IN}(V)	V-phase high-side gate driver input
9	H_{IN}(W)	W-phase high-side gate driver input
10	L_{IN}(U)	U-phase low-side gate driver input
11	L_{IN}(V)	V-phase low-side gate driver input
12	L_{IN}(W)	W-phase low-side gate driver input
13	V_{DD}	Low-side control supply

Pin description

Pin number	Pin name	Pin description
14	RFE	Programmable fault clear time, fault output, enable input
15	I_{TRIP}	Overcurrent shutdown input
16	V_{SS}	Low-side control negative supply
17	V_{TH}	Temperature output
18	NW	W-phase low-side emitter
19	NV	V-phase low-side emitter
20	NU	U-phase low-side emitter
21	W	Motor W-phase output
22	V	Motor V-phase output
23	U	Motor U-phase output
24	P	Positive bus input voltage

2.2 Pin description

H_{IN} (U, V, W) and L_{IN} (U, V, W) (High-side pins, Pin 7 – 9 and Low-side pins, Pin 10 - 12)

These pins are positive logic, and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time $t_{FIL,IN}$ The filter acts according to Figure 4. It is not recommended for proper work to provide input pulse-width lower than 1 µs.

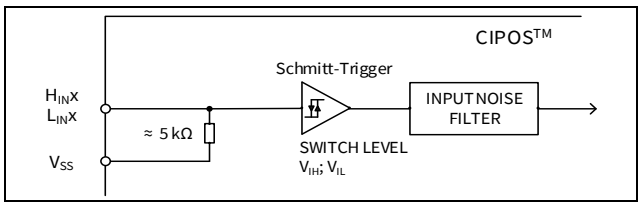


Figure 3 Input pin structure

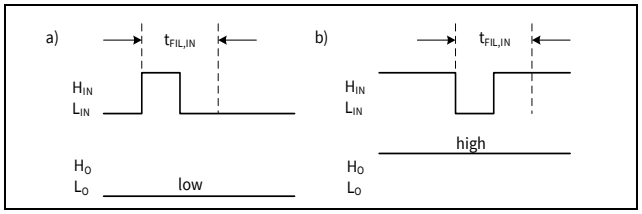


Figure 4 Input filter timing diagram

The integrated gate driver provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e., H_O1 and L_O1, H_O2 and L_O2, H_O3 and L_O3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 360 ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

RFE (Fault / Fault-clear time / Enable, Pin 14)

The RFE pin combines three functions in one pin: programmable fault clear time by RC network, fault out and enable input.

The programmable fault-clear time can be adjusted by RC network, which is external pull-up resistor and capacitor. For example, typical value is about 1 ms at 1 MΩ and 2 nF. The fault-out indicates a module failure in case of undervoltage at pin V_{DD} or in case of triggered overcurrent detection at I_{TRIP}. The microcontroller can pull this pin low to disable the IPM functionality. This is enabling function.

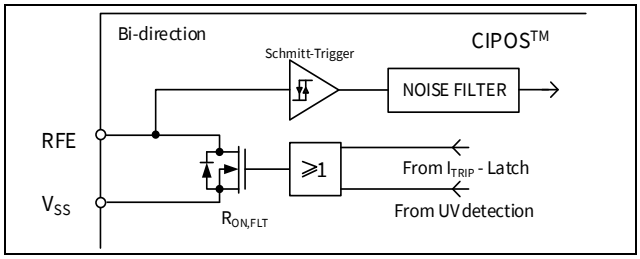


Figure 5 Internal circuit at pin RFE

V_{TH} (Thermistor temperature output, Pin 17)

The V_{TH} pin provides direct access to the NTC thermistor, which is referenced to V_{SS}. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

I_{TRIP} (Overcurrent detection function, Pin 15)

The IM12B20EC1 product provides an overcurrent detection function by connecting the I_{TRIP} input with the IGBT current feedback. The I_{TRIP} comparator threshold (typical 0.5 V) is referenced to V_{SS} ground. An input noise filter (t_{ITRIP} = typ. 500 ns) prevents the driver to detect false overcurrent events.
Overcurrent detection generates a shutdown of outputs of the gate driver. After the shutdown propagation delay of typically 1 µs.
The fault-clear time is set to typical 1.1 ms at R_{RCIN} = 1 MΩ and C_{RCIN} = 2 nF.

V_{DD}, V_{SS} (Control supply and reference, Pin 13 and reference, Pin 16)

V_{DD} is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to V_{SS} ground.

The undervoltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.2 V is present.

The IC shuts down all the gate drivers power outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 11.2 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B (U, V, W) and V_S (U, V, W) (High-side supplies, Pin 1 - 6)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to V_{SS} following the external high-side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typical V_{BSUV+} = 11.2 V and a falling threshold of V_{BSUV-} = 10.2 V.

V_S (U, V, W) provide a high robustness against negative voltage in respect of V_{SS} of -50 V transiently. This ensures very stable designs even under rough conditions.

NW, NV, NU (Low-side emitter, Pin 18 - 20)

The low-side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin V_{SS} as short as possible in order to avoid unnecessary inductive voltage drops.

W, V, U (High-side emitter and low-side collector, Pin 21 - 23)

These pins are connected to motor U, V, W input pins.

P (Positive bus input voltage, Pin 24)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 900 V.

3 Absolute maximum ratings

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

3.1 Module section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Isolation voltage	V_{ISO}	1 min, RMS, f = 60 Hz	2500	V

3.2 Inverter section

Description	Symbol	Condition	Value	Unit
Maximum blocking voltage	V_{CES}/V_{RRM}	I_C = 250 µA	1200	V
DC link supply voltage of P - N	V_{PN}	Applied between P - N	900	V
DC link supply voltage (surge) of P - N	$V_{PN(Surge)}$	Applied between P - N	1000	V
Collector current[1]	I_C	T_C = 25°C, T_J < 150°C	±30	A
		T_C = 80°C, T_J < 150°C	±20	
Maximum peak collector current	I_{CP}	T_C = 25°C, T_J < 150°C, limited by $T_{Jmax.}$	±35	A
Power dissipation per IGBT	P_{tot}		156	W
Short circuit withstand time	t_{SC}	V_{DD} = 15 V, V_{DC} ≤ 800 V, T_J ≤ 150°C	5	µs

3.3 Control section

Description	Symbol	Condition	Value	Unit
High-side offset voltage	V_S		1200	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		1200	V
Module control supply voltage	V_{DD}	Applied between V_{DD} - V_{SS}	-1 ~ 20	V
High-side floating supply voltage (V_B reference to V_S)	V_{BS}	Applied between V_B - V_S	-1 ~ 20	V
Input voltage (L_{IN}, H_{IN}, I_{TRIP}, RFE)	V_{IN}		-1 ~ V_{DD} + 0.3	V

[1]Limited by junction temperature.

4 Thermal characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single IGBT thermal resistance, junction-case	R_{thJC}	High-side V-phase (See Figure 7 for T_C measurement point)	-	-	0.80	K/W
Single diode thermal resistance, junction-case	$R_{thJC, D}$		-	-	1.55	K/W

5 Recommended operation conditions

All voltages are absolute voltages referenced to V_{SS}-potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P - N	V_{PN}	350	600	800	V
Low-side supply voltage	V_{DD}	13.5	15	18.5	V
High-side floating supply voltage (V_B vs. V_S)	V_{BS}	12.5	-	18.5	V
Logic input voltages L_{IN}, H_{IN}, I_{TRIP}, RFE	V_{IN} V_{ITRIP} V_{RFE}	0	-	5	V
Inverter PWM carrier frequency	f_{PWM}	-	-	20	kHz
External dead time between H_{IN} & L_{IN}	DT	1	-	-	µs
Voltage between V_{SS} - N (including surge)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$, $PW_{IN(OFF)}$	1	-	-	µs
Control supply variation	ΔV_{BS} ΔV_{DD}	-1 -1	- -	1 1	V/µs

6 Static parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

6.1 Inverter section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter saturation voltage	$V_{CE(Sat)}$	I_C = 20 A, T_J = 25°C I_C = 20 A, T_J = 150°C	- -	2.25 2.80	2.65 -	V
Collector-emitter leakage current	I_{CES}	V_{CE} = 1200 V	-	-	1	mA
Diode forward voltage	V_F	I_F = 20 A, T_J = 25°C I_F = 20 A, T_J = 150°C	- -	2.40 2.40	2.75 -	V

6.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (L_{IN}, H_{IN})	V_{IH}		-	1.9	2.3	V
Logic "0" input voltage (L_{IN}, H_{IN})	V_{IL}		0.7	0.9	-	V
I_{TRIP} positive going threshold	$V_{IT, TH+}$		475	500	525	mV
I_{TRIP} input hysteresis	$V_{IT, HYS}$		-	55	-	mV
V_{DD} and V_{BS} supply undervoltage positive going threshold	V_{DDUV+}		11.5	12.2	13.0	V
	V_{BSUV+}		10.5	11.2	12.0	
V_{DD} and V_{BS} supply undervoltage negative going threshold	V_{DDUV-}		10.5	11.2	12.0	V
	V_{BSUV-}		9.5	10.2	11.0	
V_{DD} and V_{BS} supply undervoltage lockout hysteresis	V_{DDUVH}, V_{BSUVH}		-	1.0	-	V
Quiescent V_{BSx} supply current (V_{BSx} only)	I_{QBS}	V_{HIN} = 0 V	-	175	-	µA
Quiescent V_{DD} supply current (V_{DD} only)	I_{QDD}	V_{LIN} = 0 V, V_{HINX} = 5 V	-	1.0	-	mA
Input bias current for L_{IN}, H_{IN}	I_{IN+}	V_{IN} = 5 V	-	1.0	-	mA
Input bias current for I_{TRIP}	I_{ITRIP+}	V_{ITRIP} = 5 V	-	30	100	µA
Input bias current for RFE	I_{RFE}	V_{RFE} = 5 V, V_{ITRIP} = 0 V	-	-	5	µA
RFE output voltage	V_{RFE}	I_{RFE} = 10 mA, V_{ITRIP} = 1 V	-	0.4	-	V
V_{RFE} positive going threshold	$V_{RFE, TH+}$		-	1.9	2.3	V
V_{RFE} negative going threshold	$V_{RFE, TH-}$		0.7	0.9	-	V
Bootstrap diode forward voltage	$V_{F, BSD}$	I_F = 0.3 mA	-	0.9	-	V
Bootstrap diode resistance	R_{BSD}	Between V_F = 4 V and V_F = 5 V	-	120	-	Ω

7 Dynamic parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

7.1 Inverter section

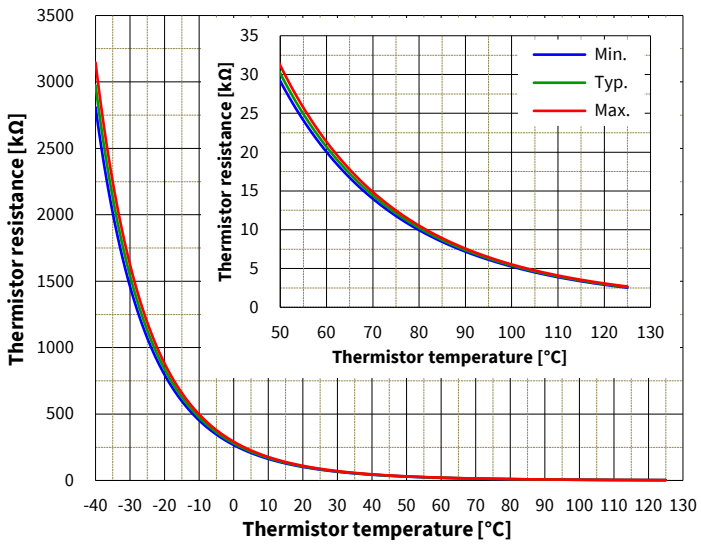
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 5 V, I_C = 20 A, V_{DC} = 600 V	-	815	-	ns
Turn-on rise time	t_r		-	50	-	ns
Turn-on switching time	$t_{c(on)}$		-	225	-	ns
Reverse recovery time	t_{rr}		-	250	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 0 V, I_C = 20 A, V_{DC} = 600 V	-	1015	-	ns
Turn-off fall time	t_f		-	115	-	ns
Turn-off switching time	$t_{c(off)}$		-	210	-	ns
Short circuit propagation delay time	t_{SCP}	From $V_{IT, TH+}$ to 10% I_{SC}	-	1575	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 600 V, I_C = 20 A T_J = 25°C 150°C	- -	2.06 3.18	- -	mJ
IGBT turn-off energy	E_{off}	V_{DC} = 600 V, I_C = 20 A T_J = 25°C 150°C	- -	0.99 1.57	- -	mJ
Diode recovery energy	E_{rec}	V_{DC} = 600 V, I_C = 20 A T_J = 25°C 150°C	- -	0.34 0.75	- -	mJ

7.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input filter time I_{TRIP}	t_{ITRIP}	V_{ITRIP} = 1 V	-	500	-	ns
Input filter time at L_{IN}, H_{IN} for turn on and off	$t_{FIL, IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	350	-	ns
Fault clear time after I_{TRIP}-fault	$t_{FLT, CLR}$	V_{ITRIP} = 1 V, $V_{pull-up}$ = 5 V (R = 1 MΩ, C = 2 nF)	-	1.1	-	ms
I_{TRIP} to fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 V or 5 V, V_{ITRIP} = 1 V	-	650	900	ns
Internal deadtime	DT_{IC}	V_{IN} = 0 or V_{IN} = 5 V	300	-	-	ns
Matching propagation delay time (On & Off) all channels	M_T	External dead time > 500 ns	-	-	130	ns

8 Thermistor characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Resistance	R_{NTC}	T_{NTC} = 25°C	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient) thermistor	B (25/100)		-	4092	-	K



Temp. [°C]	$R_{Min.}$ [kΩ]	$R_{Typ.}$ [kΩ]	$R_{Max.}$ [kΩ]
50	29.151	30.157	31.178
60	20.018	20.669	21.329
70	13.994	14.424	14.858
80	9.946	10.234	10.523
90	7.177	7.373	7.569
100	5.253	5.388	5.523
110	3.884	3.99	4.096
120	2.908	2.991	3.075
125	2.527	2.601	2.676

Figure 6 Thermistor resistance – temperature curve and table

(For more information, please refer to application note 'AN-2024-05 CIPOS™ Maxi IPM IM12BxxxC1 Series application note'.)

9 Mechanical characteristics and ratings

Description	Condition	Value			Unit
		Min.	Typ.	Max.	
Comparative Tracking Index (CTI)		600	-	-	
Mounting torque	M3 screw and washer	0.49	-	0.78	N·m
Backside curvature	Refer to Figure 8	0	-	150	µm
Weight		-	7.1	-	g

10 Qualification information

UL certification	File number: E314539	
Moisture sensitivity level	-	
RoHS compliant	Yes (Lead-free terminal plating)	
ESD (Electrostatic Discharge)	HBM (Human body model) class	2
	CDM (Charged device model) class	C3

11 Diagrams and tables

11.1 T_C measurement point

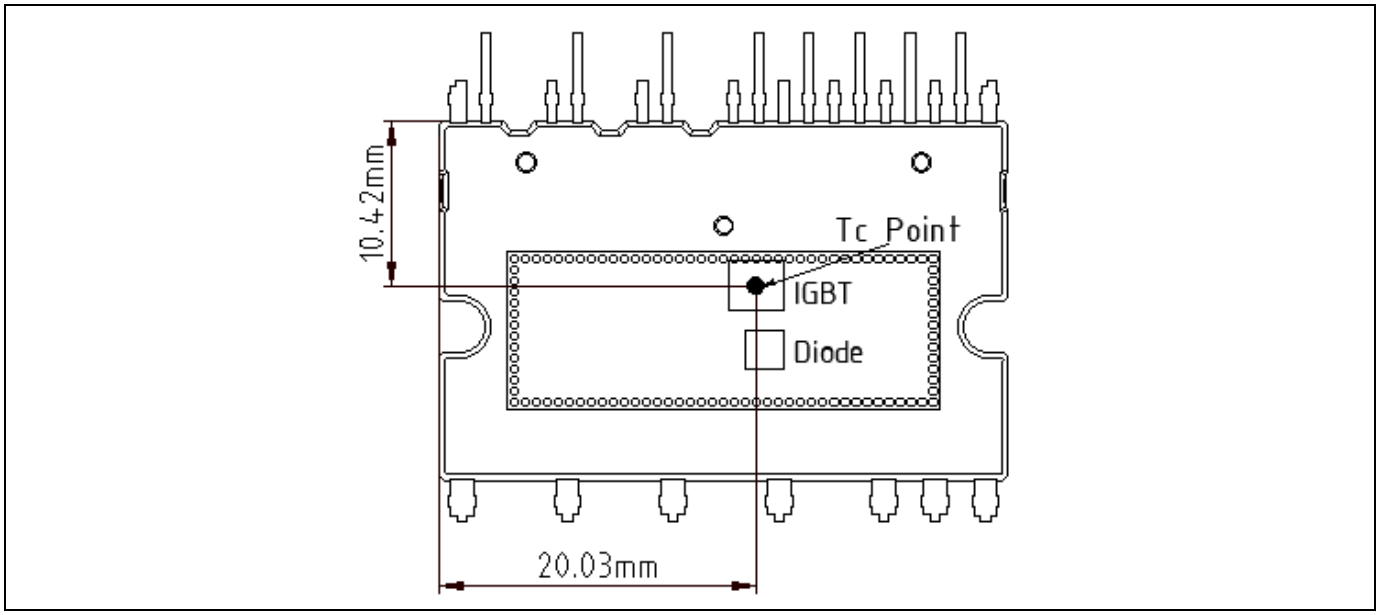


Figure 7 T_C measurement point[1]

11.2 Backside curvature measurement point

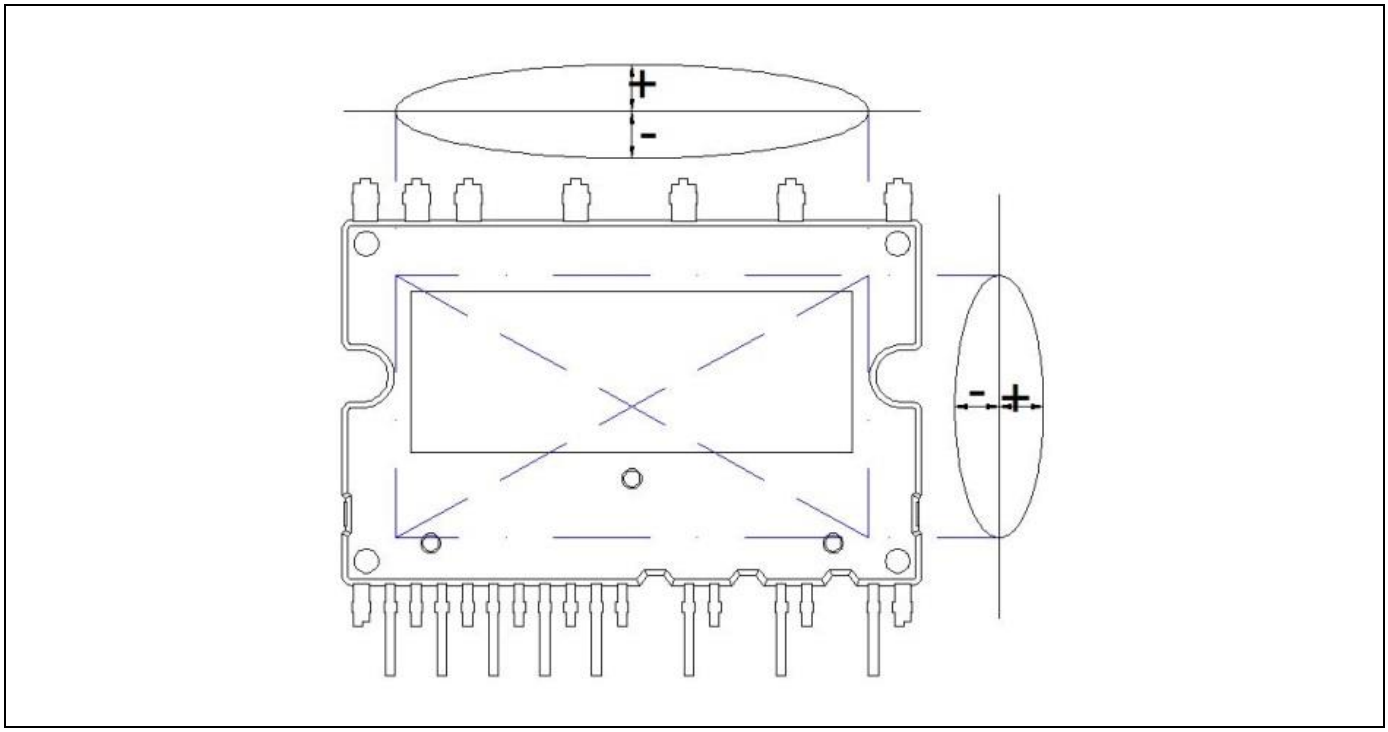


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching time definition

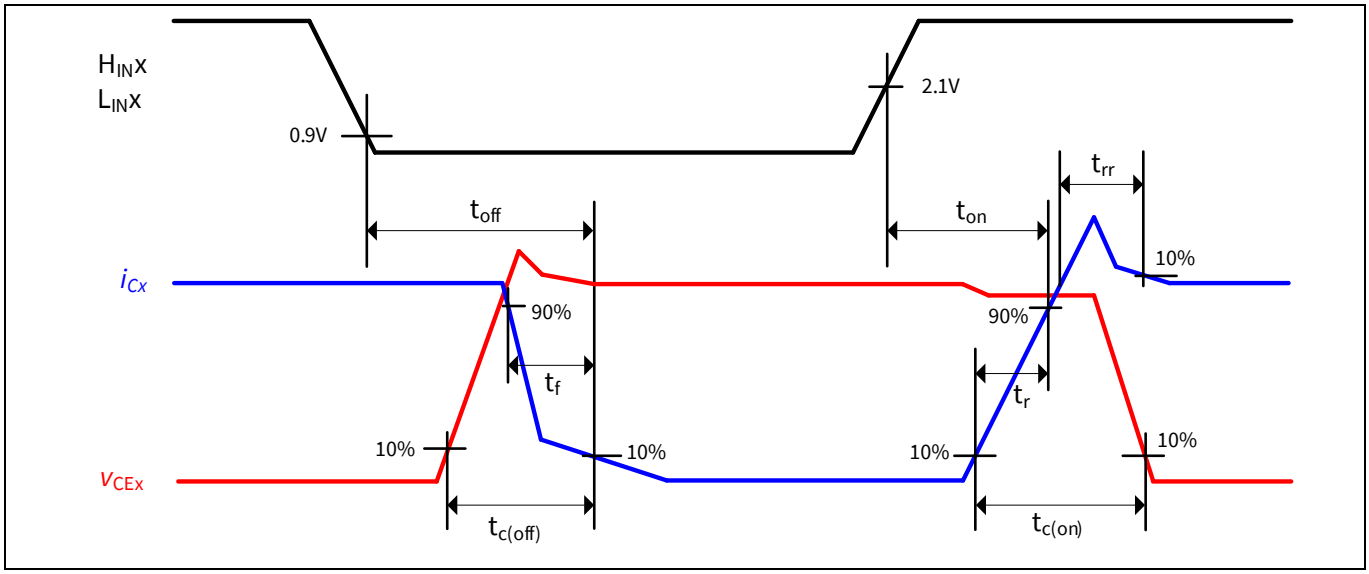


Figure 9 Switching times definition

11.4 Sleep function timing diagram

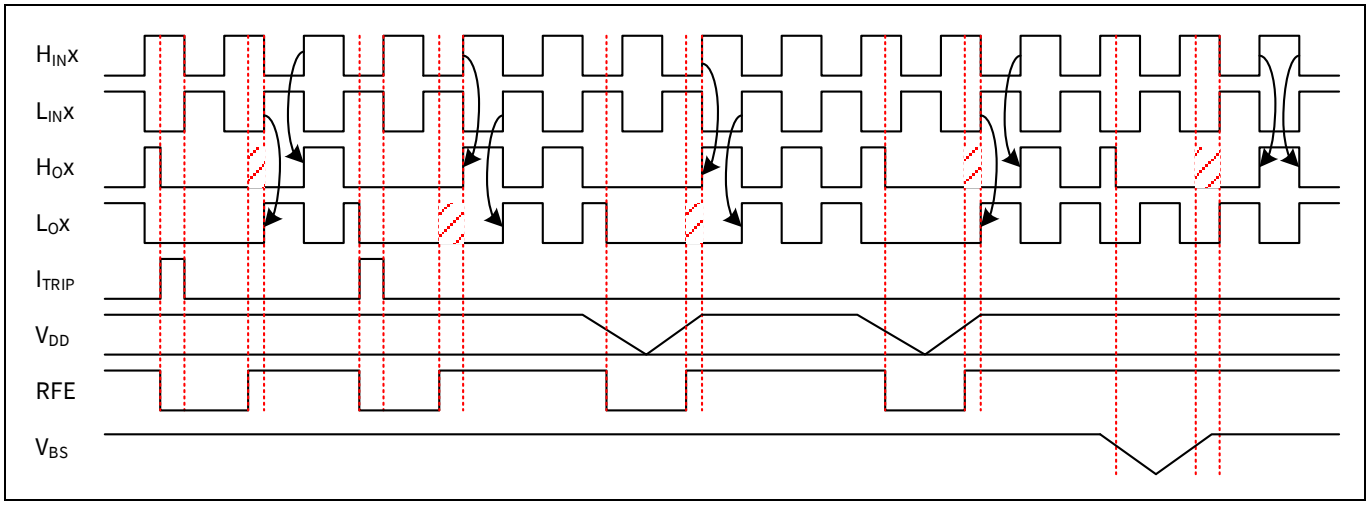


Figure 10 Sleep function timing diagram

12 Application guide

12.1 Typical application schematic

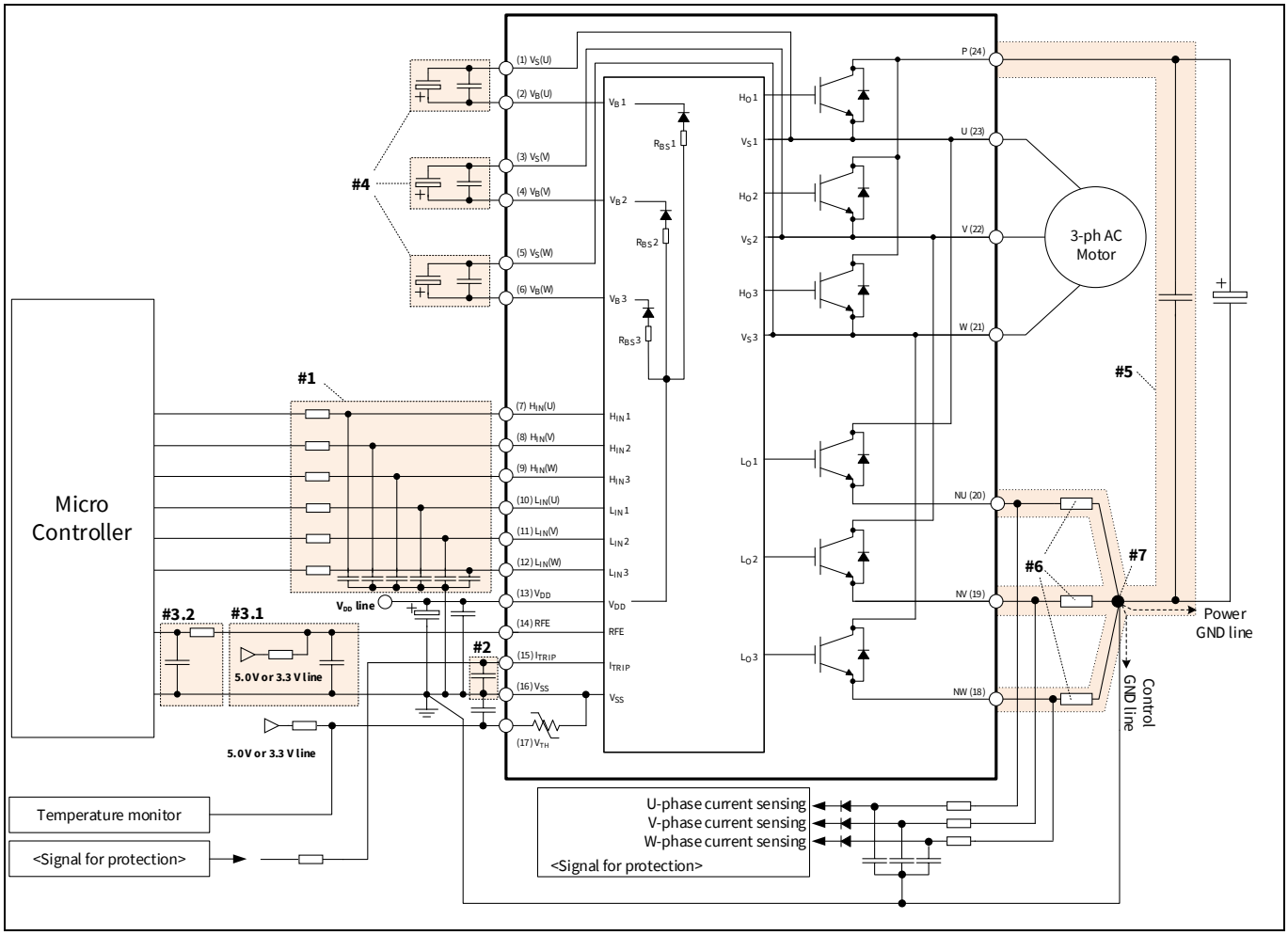


Figure 11 Typical application circuit

1. Input circuit
   - To reduce input signal noise by high speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100 Ω, 1 nF)
   - C_{IN} should be placed as close to V_{SS} pin as possible.

2. I_{TRIP} circuit
   - To prevent protection function errors, C_{ITRIP} should be placed as close to I_{TRIP} and V_{SS} pins as possible.
   - To prevent fault operation of the protection function, an RC filter is recommended around 1.5~2.0 µs (68 Ω, 22 nF, “Signal for protection” in the schematic leads the signal into the microcontroller”).

3. RFE circuit

   3.1 Pull-up resistor and pull-down capacitor
   - RFE output is an open drain output. This signal line should be pulled up to the positive side of the 5.0 V / 3.3 V logic power supply with a proper resistor R_{PU}.
   - The fault-clear time is adjusted by RC network of a pull-up resistor, a pull-down capacitor and pull-up voltage.
     - $t_{FLT,CLR} = -R_{pull\text{-}up} \cdot C_{pull\text{-}down} \cdot \ln(1 - V_{RFE,TH+}/V_{pull\text{-}up})$ + internal fault-clear time 160 µs
     - $t_{FLT,CLR}$ = -1 MΩ x 2 nF x ln(1 - 1.9 / 5 V) + 160 µs ≅ 1.1 ms at R = 1 MΩ, C = 2 nF and $V_{pull\text{-}up}$ = 5 V
     - A pull-up resistor is limited to max. 2 MΩ

   3.2 RC filter
   - It is recommended that RC filter be placed as close to the controller as possible.

Application guide

4. V_B-V_S circuit
   - Capacitor for high side floating supply voltage should be placed as close to V_B and V_S pins as possible.

5. Snubber capacitor
   - The wiring between IPM and snubber capacitor including shunt resistor should be as short as possible.

6. Shunt resistor
   - The shunt resistor of SMD type should be used for reducing its stray inductance.

7. Ground pattern
   - Ground pattern should be separated at only one point of shunt resistor as short as possible.

12.2 Performance chart

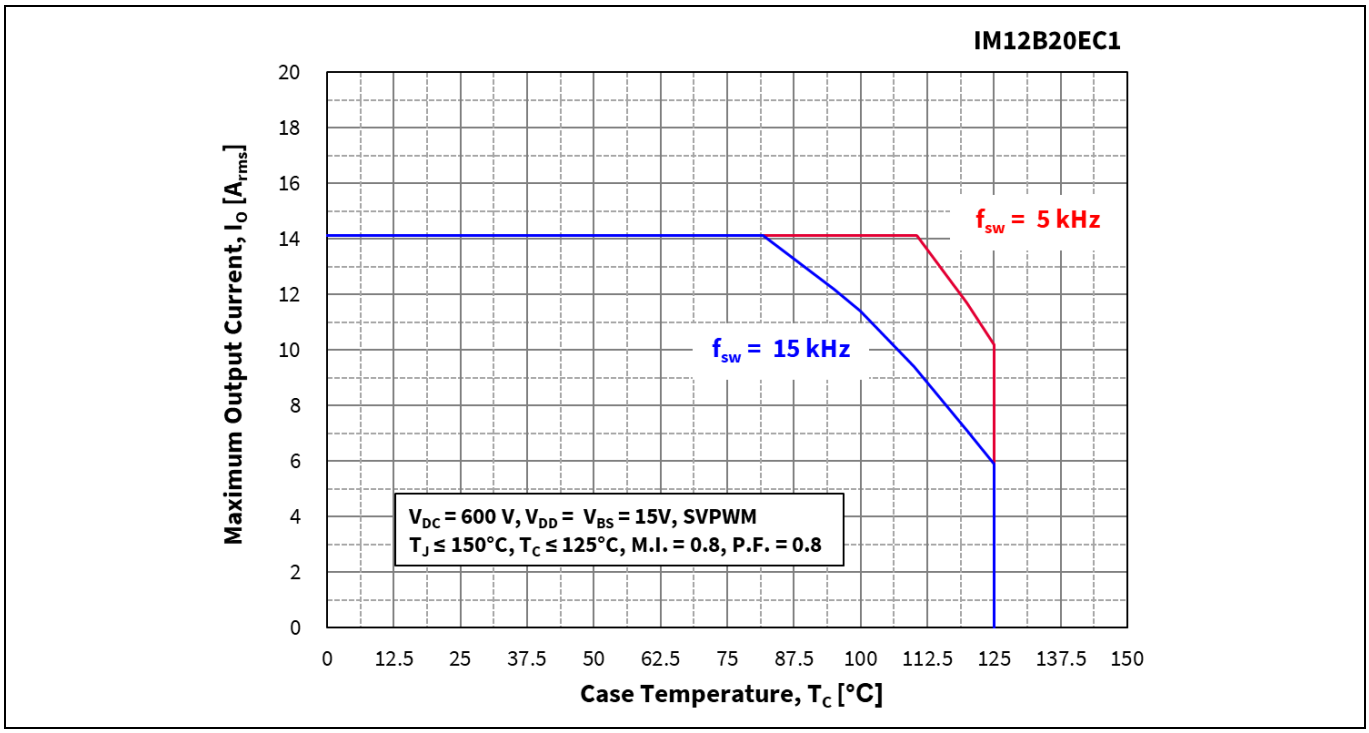


Figure 12 Maximum operating current SOA[1]

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

13 Package outline

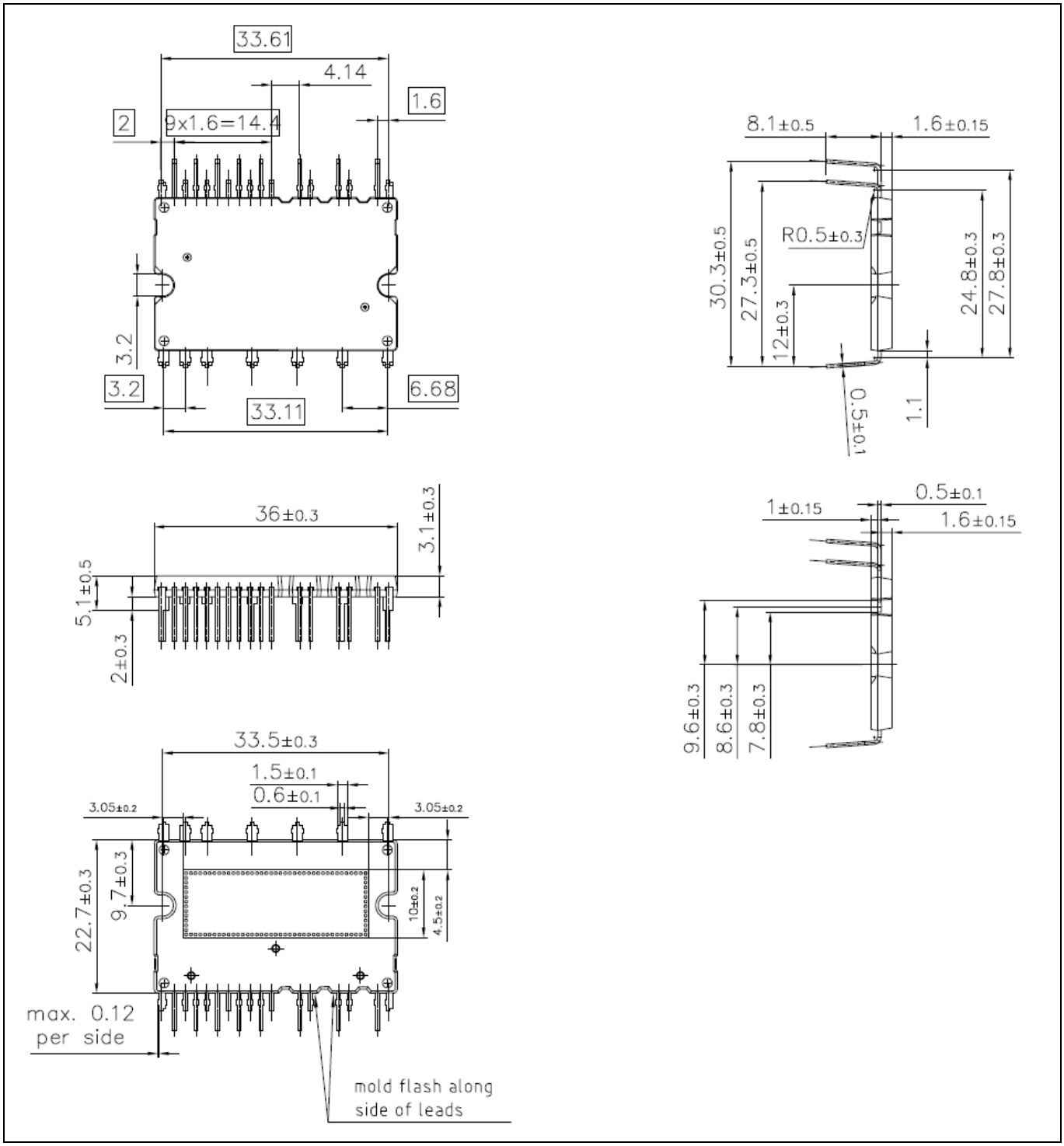


Figure 13 IM12B20EC1

Revision history

Document version	Date of release	Description of changes
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V 1.01	2024-06-03	Changed Figure 10

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