

CoolSiC™
400V CoolSiC™ G2 MOSFET

Features

- Ideal for high frequency switching and synchronous rectification
- Commutation robust fast body diode with low Q_{fr}
- Low $R_{DS(on)}$ dependency on temperature
- Benchmark gate threshold voltage, $V_{GS(th)} = 4.5\text{ V}$
- Recommended gate driving voltage 0 V to 18 V
- .XT interconnection technology for best-in-class thermal performance
- 100% avalanche tested

Potential applications

- SMPS
- Solar PV inverters
- Energy storage, UPS and battery formation
- Class-D audio
- Motor drives

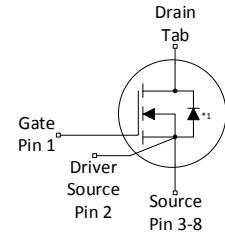
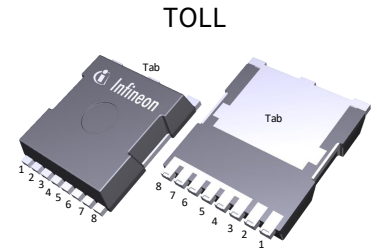
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	400	V
$R_{DS(on),typ}$	44.9	mΩ
I_D	43	A
Q_{oss}	34	nC
E_{oss}	2.4	μJ
Q_G	21	nC

Type/Ordering Code	Package	Marking	Related Links
IMT40R045M2H	PG-HSOF-8	40R045M2	-



*1: Internal body diode

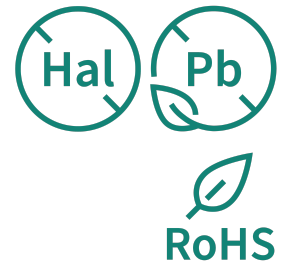




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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	43 30 6.8	A	$V_{GS}=18\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=18\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=18\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	129	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	53	mJ	$I_D=8.9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Avalanche energy, repetitive	E_{AR}	-	-	0.27	mJ	$I_D=8.9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage (static)	$V_{GS,DC}$	-7	-	23	V	-
Gate source voltage (transient)	$V_{GS,AC}$	-10	-	25	V	$t_{pulse} \leq 500\text{ ns}$, duty cycle $\leq 1\%$
Power dissipation	P_{tot}	-	-	150 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{THJA}=40\text{ °C/W}^2)$
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information.

⁴⁾ See Diagram 19 for more detailed information.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	40	°C/W	-

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

4 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	400	-	-	V	$V_{GS}=0\text{ V}$, $I_D=0.32\text{ mA}$
Gate threshold voltage ⁶⁾	$V_{GS(th)}$	3.5	4.5	5.6	V	$V_{DS}=V_{GS}$, $I_D=3.2\text{ mA}$
Zero gate voltage drain current	I_{DSS}	-	1 2	75 -	μA	$V_{DS}=400\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=400\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=175\text{ °C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	44.9 64.5 55.0	56.2 - -	m Ω	$V_{GS}=18\text{ V}$, $I_D=8.9\text{ A}$, $T_j=25\text{ °C}$ $V_{GS}=18\text{ V}$, $I_D=8.9\text{ A}$, $T_j=175\text{ °C}$ $V_{GS}=15\text{ V}$, $I_D=8.9\text{ A}$, $T_j=25\text{ °C}$
Gate resistance	R_G	-	5.8	8.7	Ω	-

⁶⁾ Tested after 1ms pulse at $V_{GS} = +20\text{V}$.

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	710	910	pF	$V_{GS}=0\text{ V}$, $V_{DS}=200\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	100	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=200\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	9	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=200\text{ V}$, $f=1\text{ MHz}$
Effective output capacitance, energy related ⁷⁾	$C_{o(er)}$	-	121	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=0\dots200\text{ V}$
Effective output capacitance, time related ⁸⁾	$C_{o(tr)}$	-	170	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{ V}$, $V_{DS}=0\dots200\text{ V}$
Turn-on delay time ⁹⁾	$t_{d(on)}$	-	12.0	-	ns	$V_{DD}=200\text{ V}$, $V_{GS}=0\dots18\text{ V}$, $I_D=8.9\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Rise time ⁹⁾	t_r	-	10.7	-	ns	$V_{DD}=200\text{ V}$, $V_{GS}=0\dots18\text{ V}$, $I_D=8.9\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Turn-off delay time ⁹⁾	$t_{d(off)}$	-	17.3	-	ns	$V_{DD}=200\text{ V}$, $V_{GS}=18\dots0\text{ V}$, $I_D=8.9\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$
Fall time ⁹⁾	t_f	-	8.3	-	ns	$V_{DD}=200\text{ V}$, $V_{GS}=18\dots0\text{ V}$, $I_D=8.9\text{ A}$, $R_{G,ext}=1.8\text{ }\Omega$

⁷⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 200 V.

⁸⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 200 V.

⁹⁾ Refer to Table 9 for test setup.

Table 7 Gate Charge Characteristics ¹⁰⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5.6	-	nC	$V_{DD}=200\text{ V}$, $I_D=8.9\text{ A}$, $V_{GS}=0\text{ to }18\text{ V}$
Gate to drain charge	Q_{gd}	-	4.4	-	nC	$V_{DD}=200\text{ V}$, $I_D=8.9\text{ A}$, $V_{GS}=0\text{ to }18\text{ V}$
Gate charge total	Q_g	-	21	-	nC	$V_{DD}=200\text{ V}$, $I_D=8.9\text{ A}$, $V_{GS}=0\text{ to }18\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	19	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }18\text{ V}$
Output charge	Q_{oss}	-	34	-	nC	$V_{DS}=200\text{ V}$, $V_{GS}=0\text{ V}$
Output Energy	E_{oss}	-	2.4	-	μJ	$V_{DS}=200\text{ V}$, $V_{GS}=0\text{ V}$

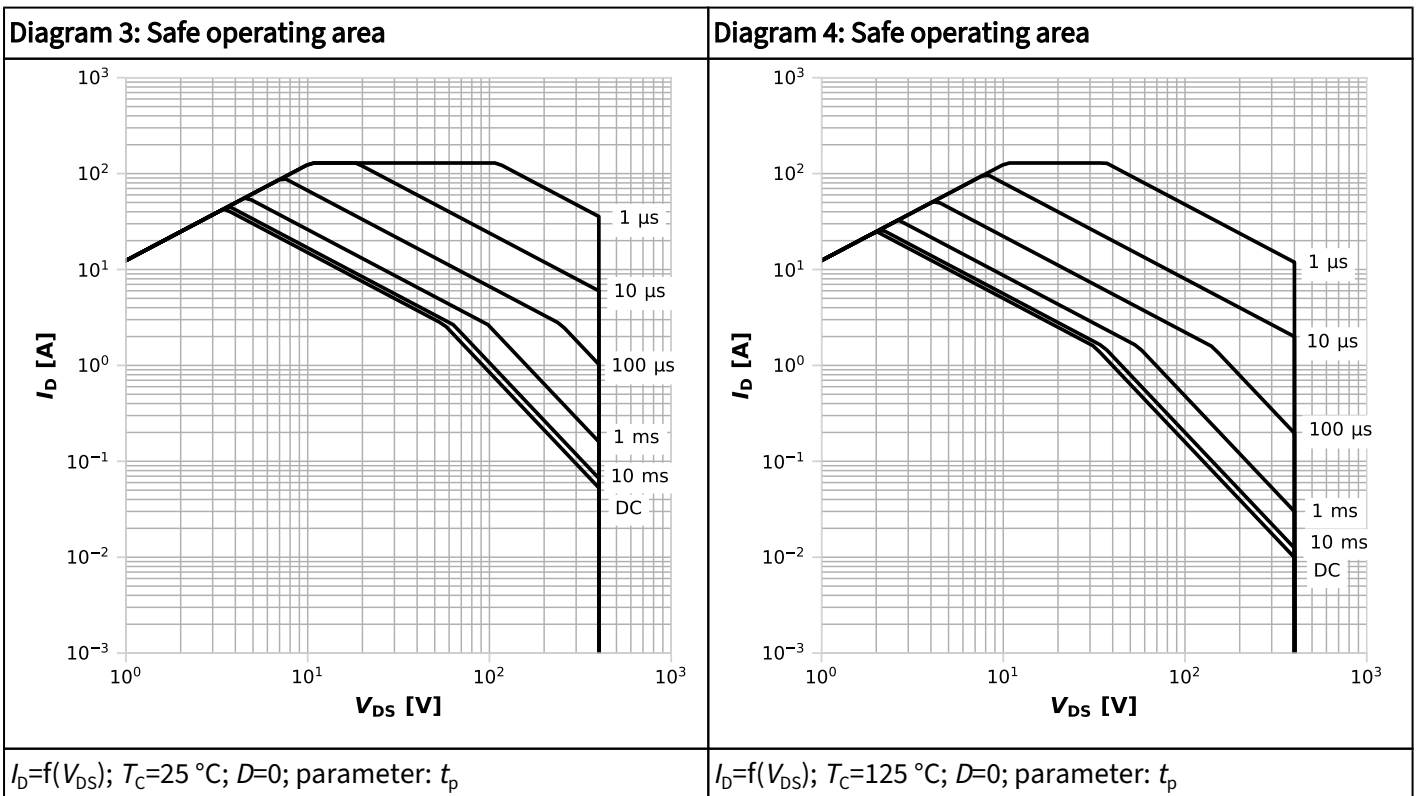
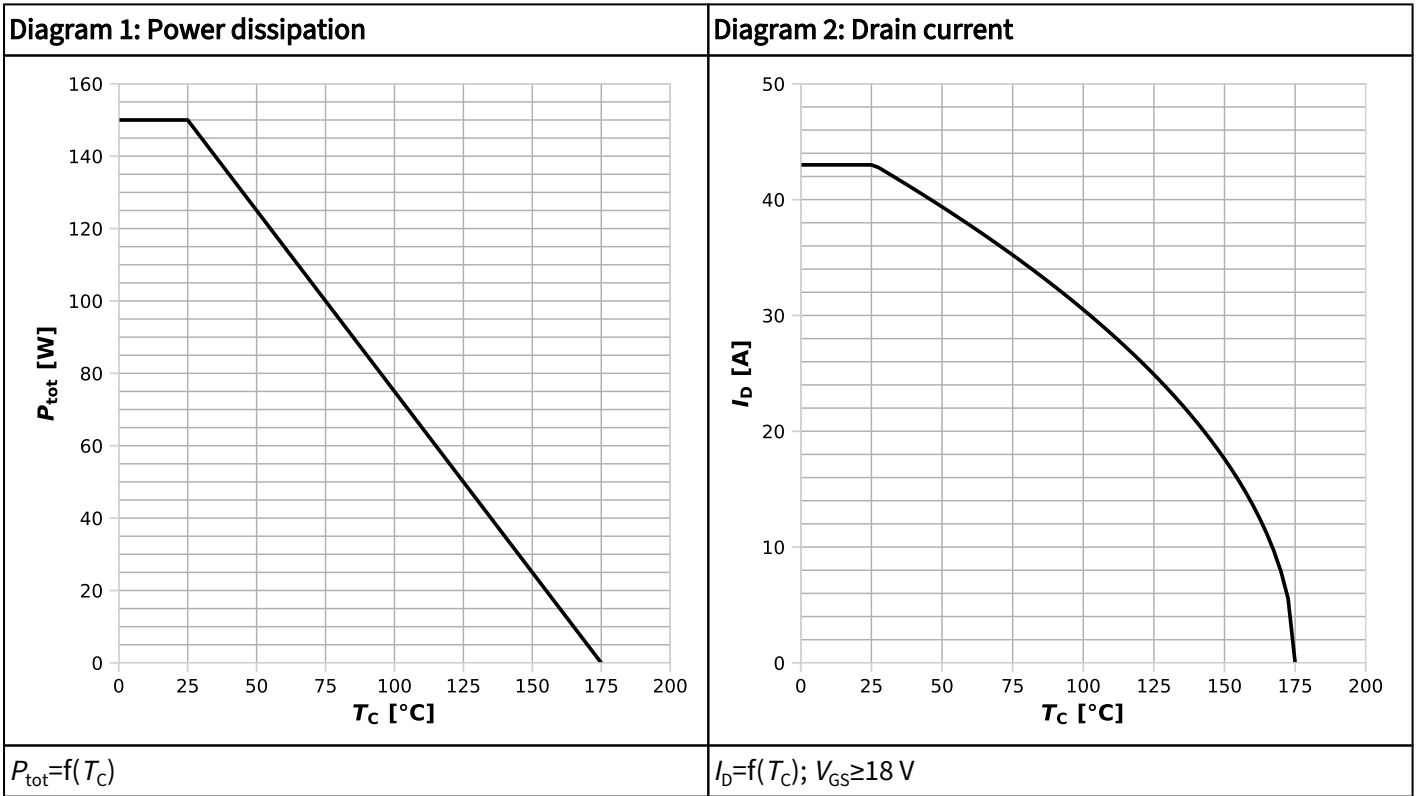
¹⁰⁾ As per JEP192, Guidelines for Gate Charge (Q_g) Test Method for SiC MOSFET.

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	21	A	$T_c=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	129	A	$T_c=25\text{ °C}$, $t_{pulse}\leq 250\text{ ns}$
Diode forward voltage	V_{SD}	-	3.5	4.3	V	$V_{GS}=0\text{ V}$, $I_S=8.9\text{ A}$, $T_j=25\text{ °C}$
MOSFET forward recovery time	t_{fr}	-	11.1 8.7	-	ns	$V_R=200\text{ V}$, $I_S=8.9\text{ A}$, $di_S/dt=1000\text{ A}/\mu\text{s}$ $V_R=200\text{ V}$, $I_S=8.9\text{ A}$, $di_S/dt=3000\text{ A}/\mu\text{s}$
MOSFET forward recovery charge ¹¹⁾	Q_{fr}	-	38 74	-	nC	$V_R=200\text{ V}$, $I_S=8.9\text{ A}$, $di_S/dt=1000\text{ A}/\mu\text{s}$ $V_R=200\text{ V}$, $I_S=8.9\text{ A}$, $di_S/dt=3000\text{ A}/\mu\text{s}$

¹¹⁾ Q_{fr} includes Q_{oss} . Refer to Table 10 for test setup.

5 Electrical characteristics diagrams



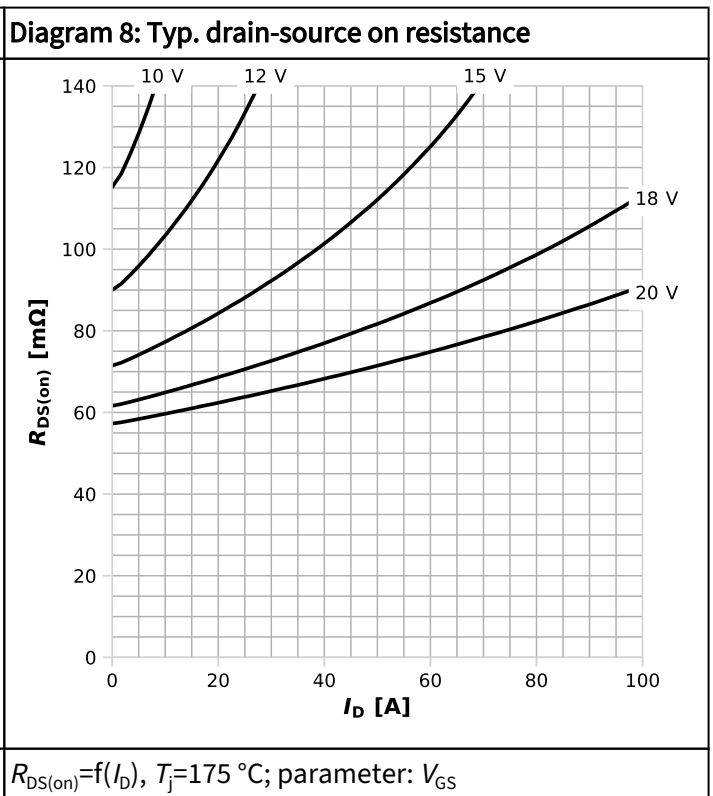
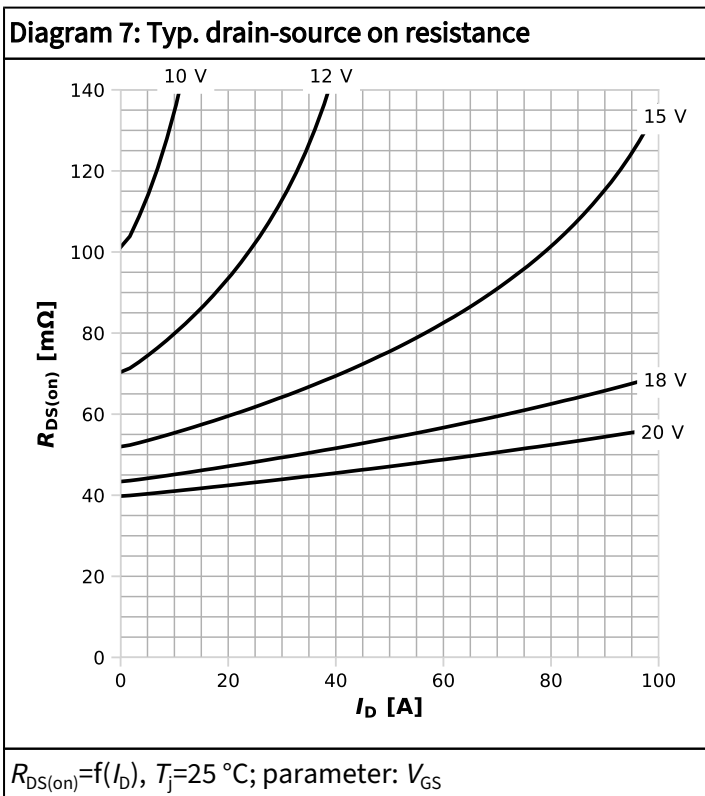
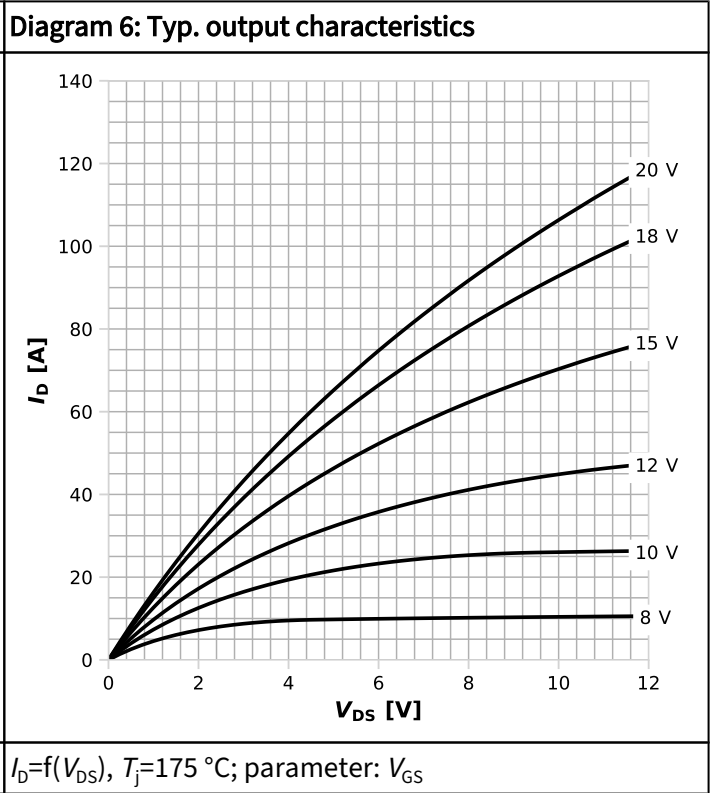
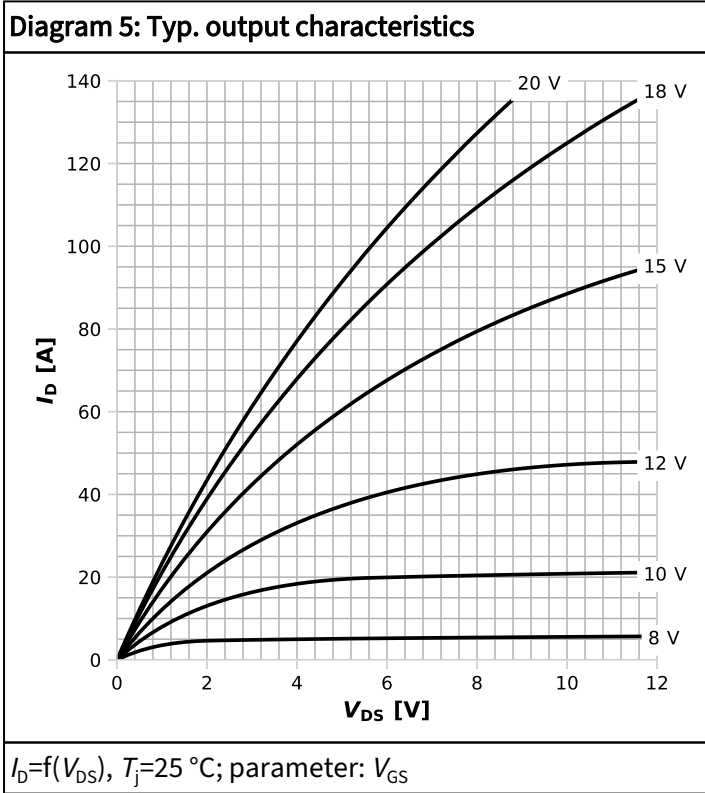
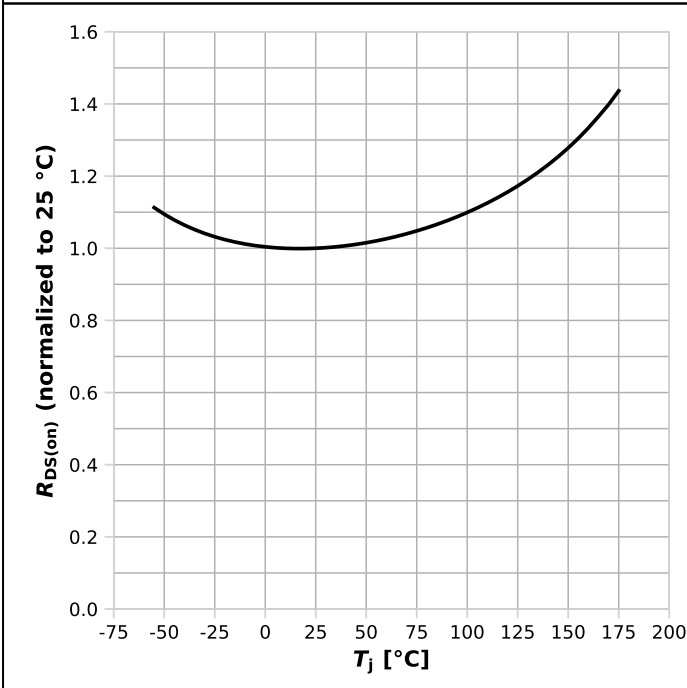
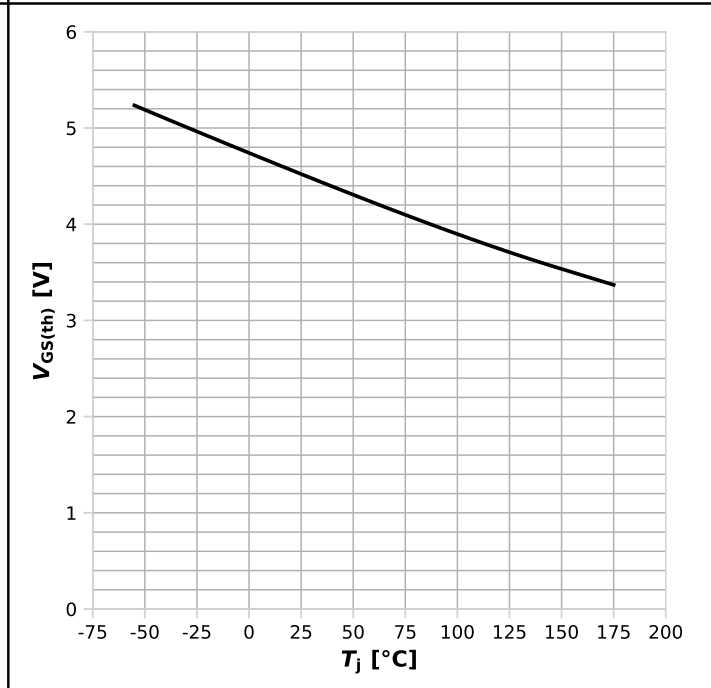


Diagram 9: Normalized drain-source on resistance



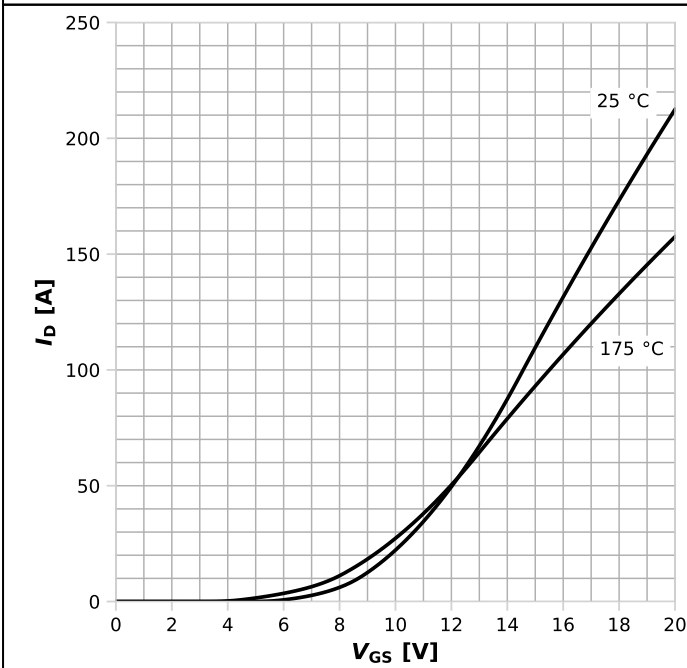
$R_{DS(on)}=f(T_j), I_D=8.9\text{ A}, V_{GS}=18\text{ V}$

Diagram 10: Typ. gate threshold voltage



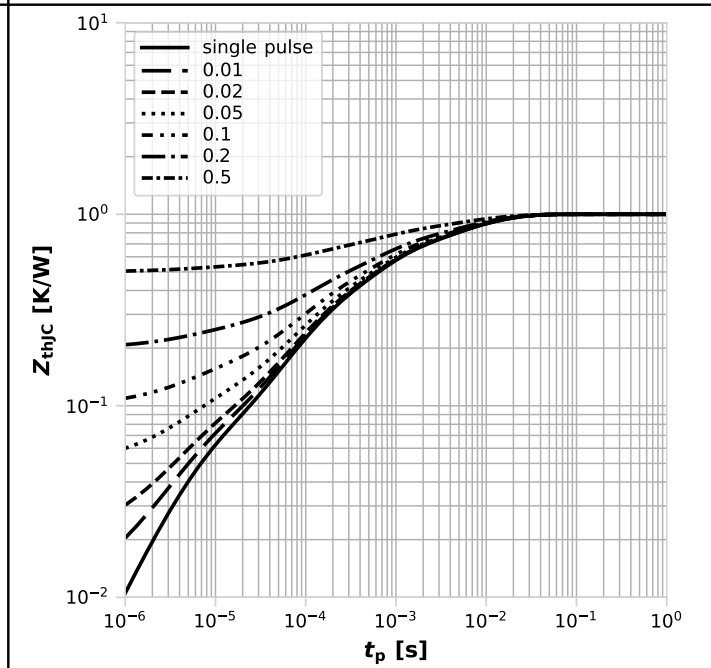
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}, I_D=3.2\text{ mA}$

Diagram 11: Typ. transfer characteristics



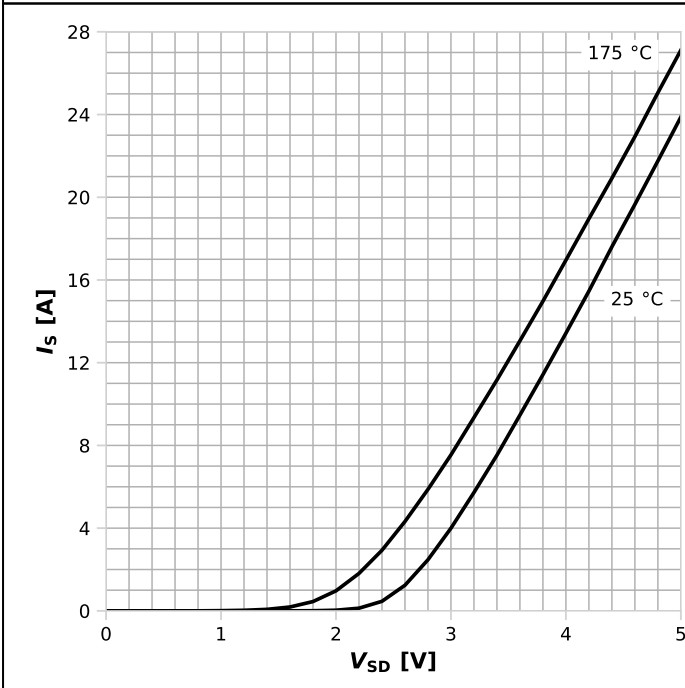
$I_D=f(V_{GS}), |V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 12: Max. transient thermal impedance



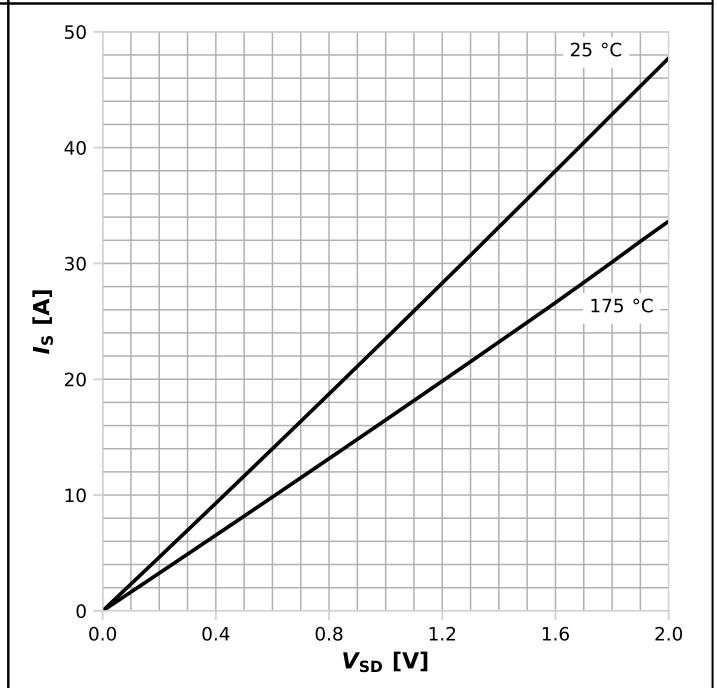
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 13: Reverse output characteristics



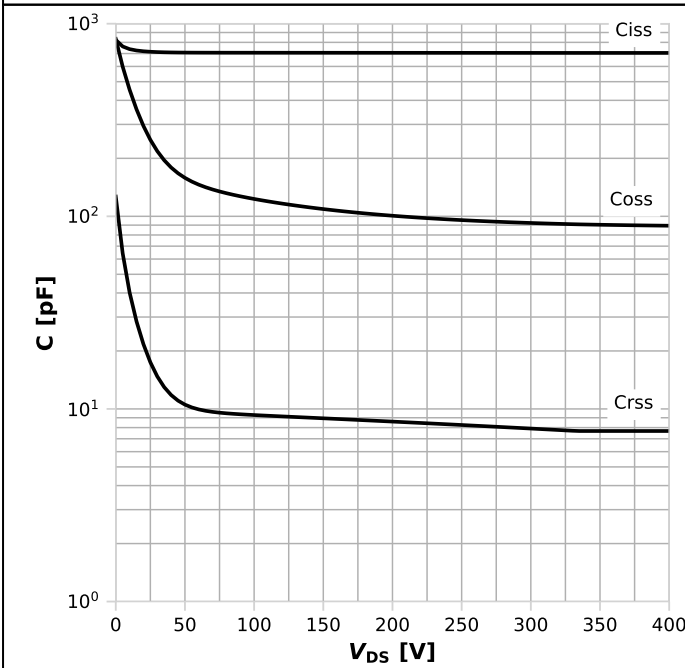
$I_F=f(V_{SD}), V_{GS}=0\text{ V}; \text{parameter: } T_j$

Diagram 14: Reverse output characteristics



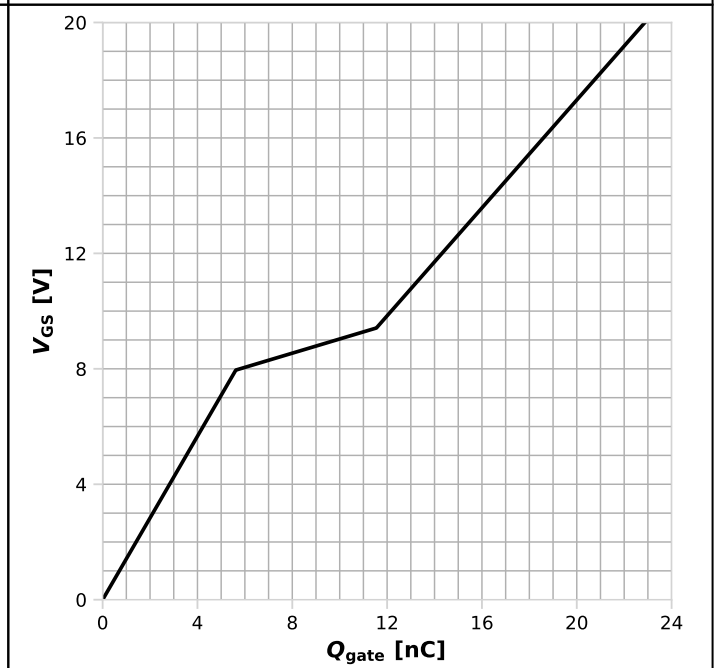
$I_F=f(V_{SD}), V_{GS}=18\text{ V}; \text{parameter: } T_j$

Diagram 15: Typ. capacitances



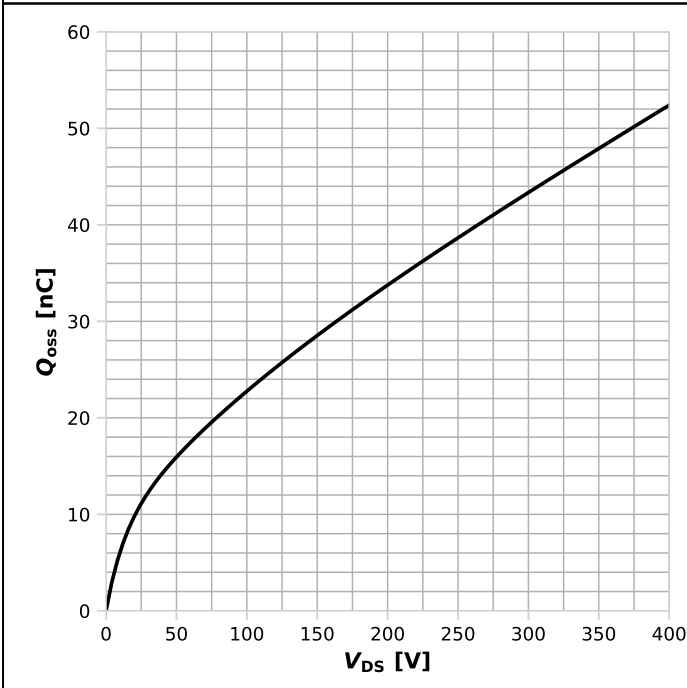
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 16: Typ. gate charge



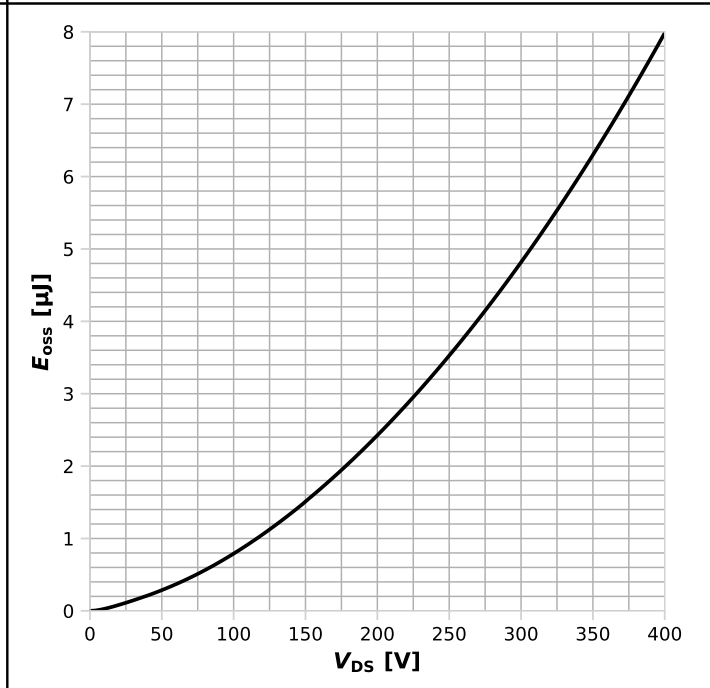
$V_{GS}=f(Q_{\text{gate}}), V_{DD}=200\text{ V}, I_D=8.9\text{ A pulsed}, T_j=25\text{ °C}$

Diagram 17: Typ. output charge



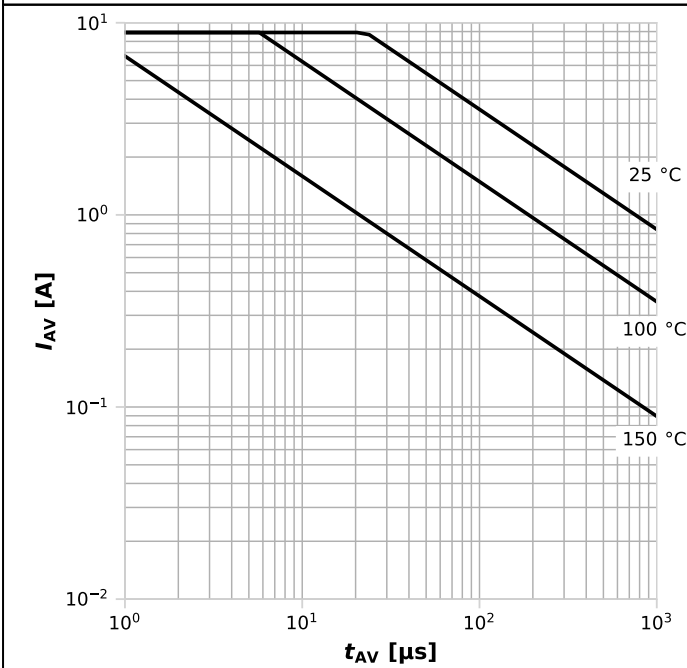
$Q_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$

Diagram 18: Typ. output energy



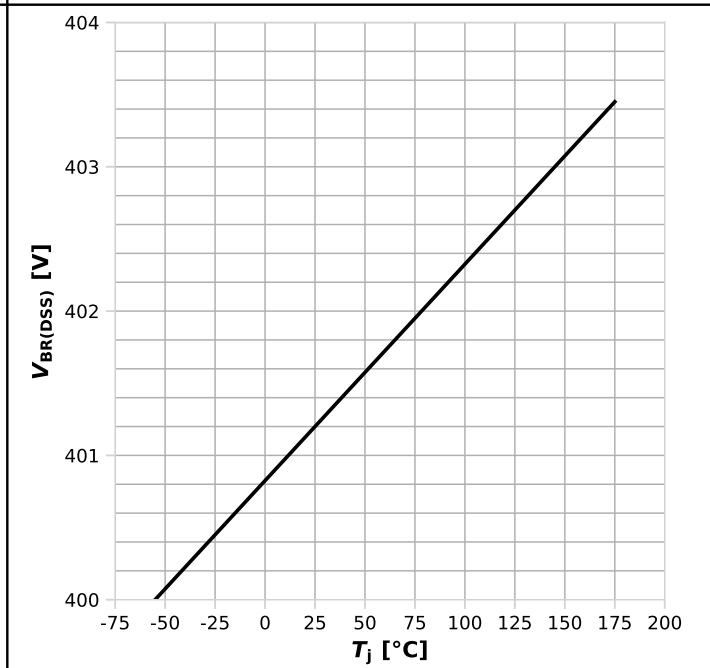
$E_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$

Diagram 19: Avalanche characteristics

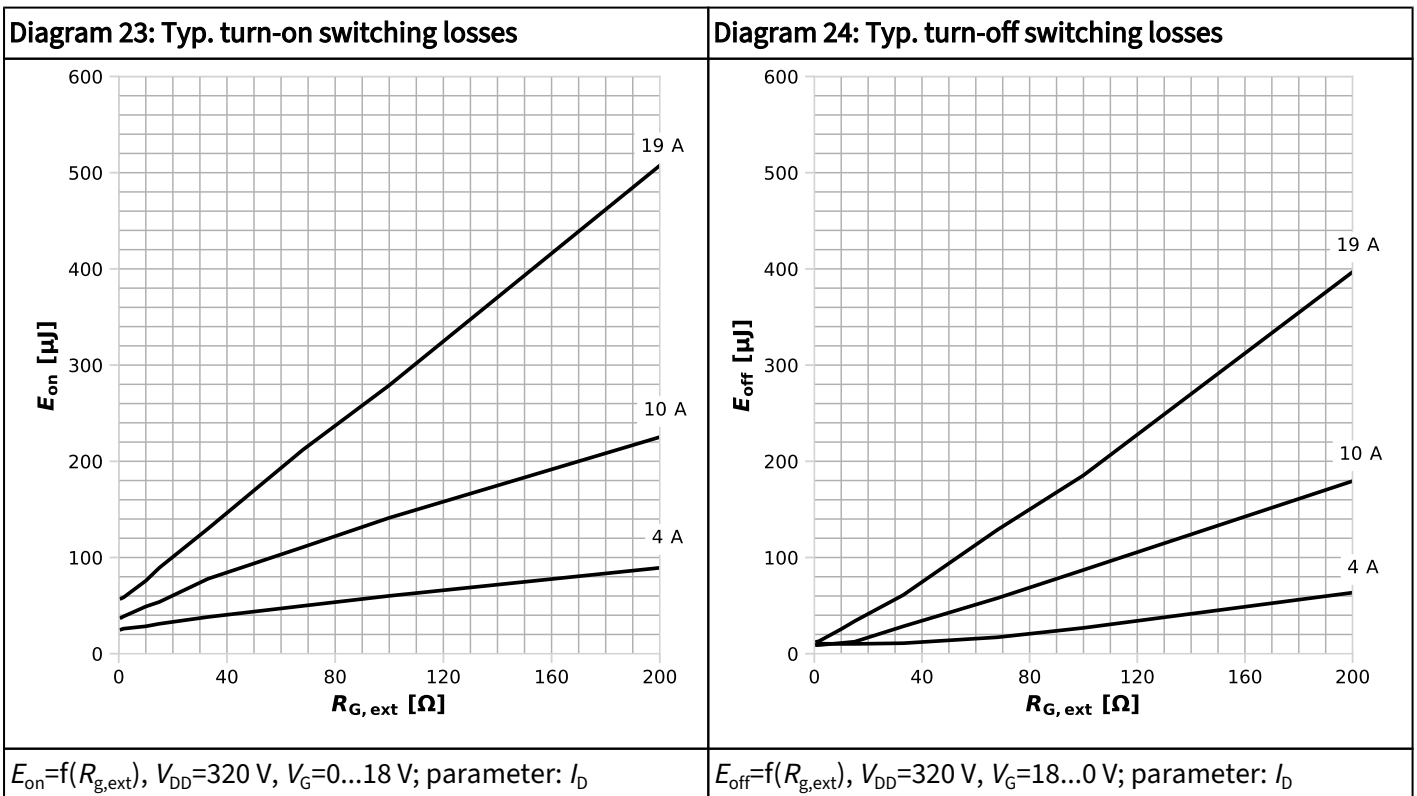
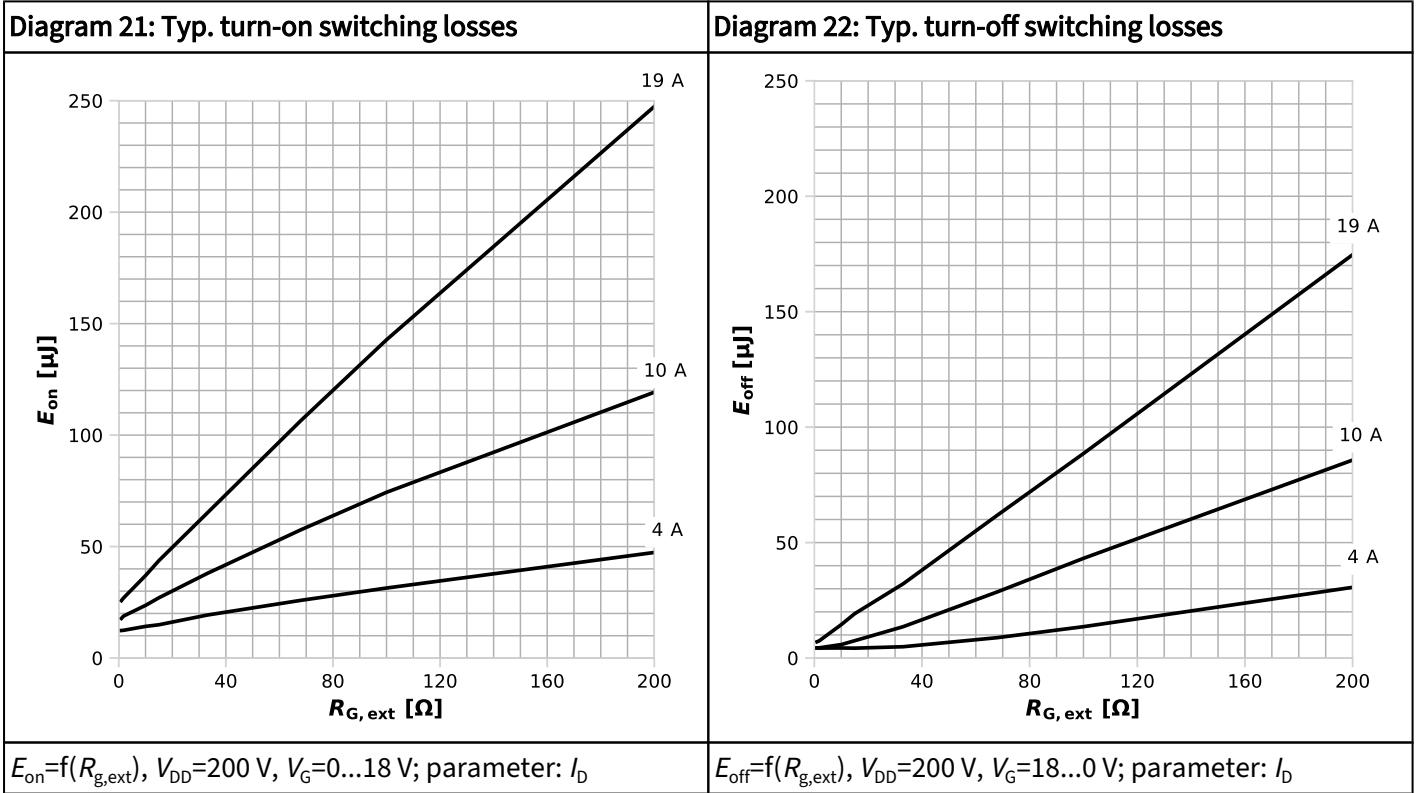


$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega; \text{parameter: } T_{j,\text{start}}$

Diagram 20: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=0.32\text{ mA}$



6 Test Circuits

Table 9 Switching times (CoolSiC)

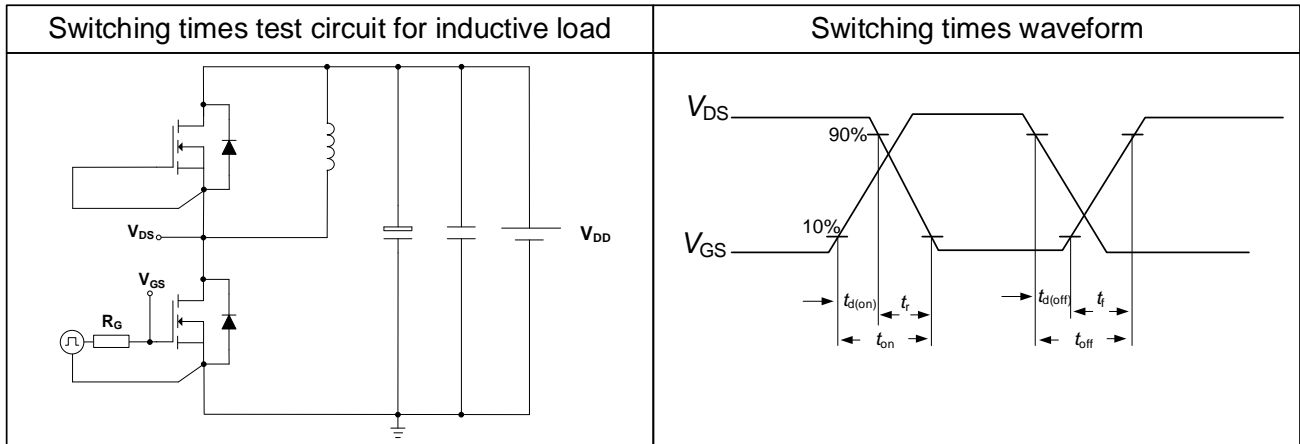
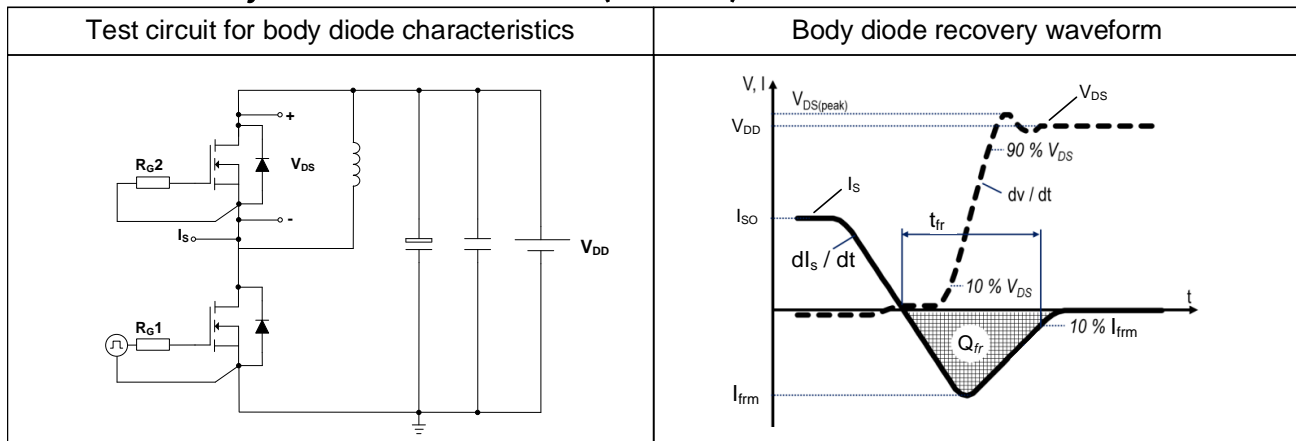
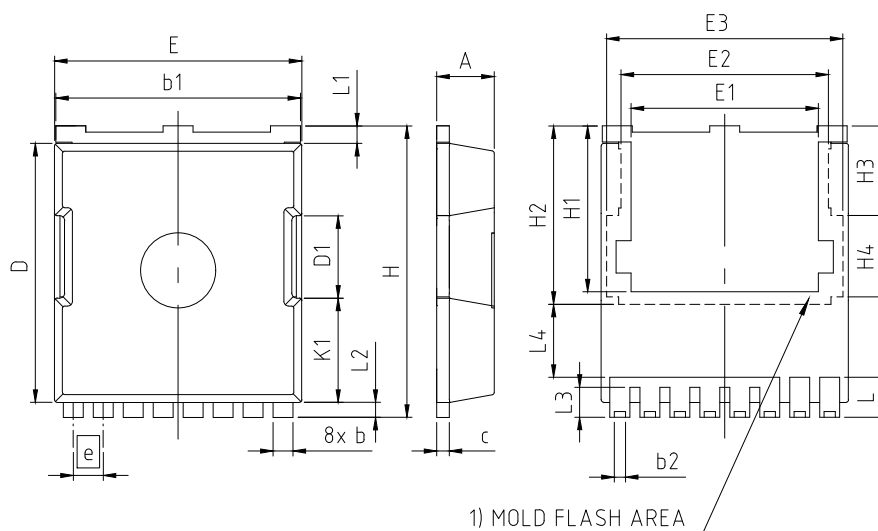


Table 10 Body diode characteristics (CoolSiC)



7 Package Outlines



PACKAGE - GROUP NUMBER: PG-HSOF-8-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

Revision History

IMT40R045M2H

Revision 2024-04-27, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-04-26	Release of preliminary version
2.0	2024-04-27	Release of final

Trademarks

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