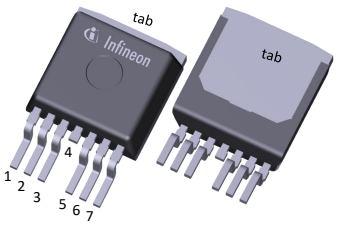
MOSFET

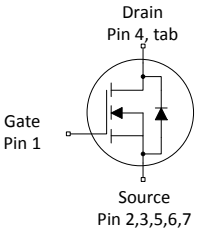
OptiMOS™ 6 Power-Transistor, 150 V

D²-PAK 7pin



Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

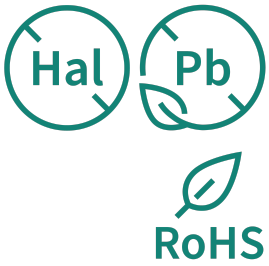


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	2.6	mΩ
I_D	239	A
Q_{oss}	310	nC
Q_G	105	nC
Q_{rr} (500A/µs)	220	nC



Type/Ordering Code	Package	Marking	Related Links
IPF026N15NM6	PG-TO263-7	026N15N6	-

Table of Contents

Description 1
Maximum ratings 3
Thermal characteristics 3
Electrical characteristics 4
Electrical characteristics diagrams 6
Package Outlines 10
Revision History 12
Trademarks 12
Disclaimer 12

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	239 183 172 25	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=8 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	956	A	T_C=25 °C
Avalanche current, single pulse [4]	I_{AS}	-	-	100	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	1012	mJ	I_D=60 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	395 3.8	W	T_C=25 °C T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.38	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5]	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.5	4.0	V	V_{DS}=V_{GS}, I_D=276 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1 2.3 2.5	2.5 2.6 3.0	mΩ	V_{GS}=15 V, I_D=100 A V_{GS}=10 V, I_D=100 A V_{GS}=8 V, I_D=50 A
Gate resistance	R_G	-	1.04	1.56	Ω	-
Transconductance	g_{fs}	91	180	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [6)]	C_{iss}	-	7600	9900	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance [6)]	C_{oss}	-	2300	3000	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance [6)]	C_{rss}	-	25	38	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	18	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	34	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	20	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

6) Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [7]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge [8]	Q_{gs}	-	40	52	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	26	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge [8]	Q_{gd}	-	23	35	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	37	-	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total [8]	Q_g	-	105	137	nC	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	V_{DD}=75 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	89	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge [8]	Q_{oss}	-	310	403	nC	V_{DS}=75 V, V_{GS}=0 V

[7] See "Gate charge waveforms" for parameter definition

[8] Defined by design. Not subject to production test.

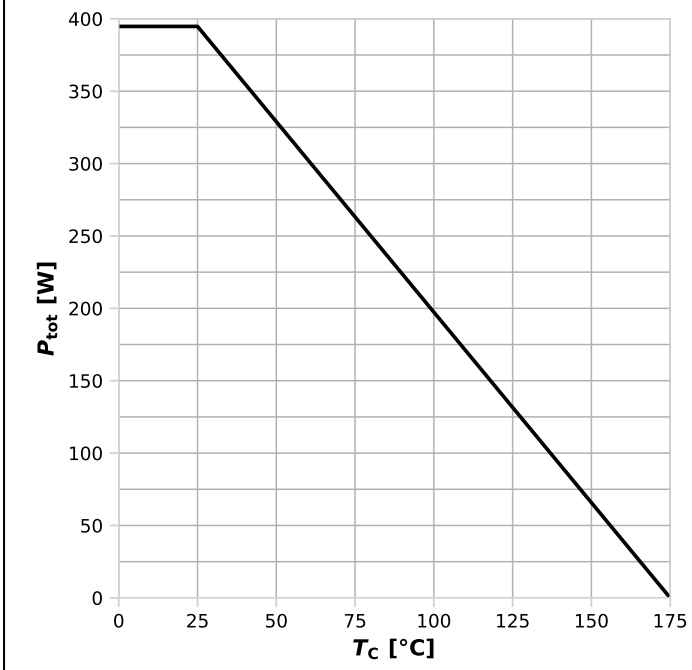
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	239	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	956	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.86	1.0	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time [9]	t_{rr}	-	42	84	ns	V_R=75 V, I_F=50 A, di_F/dt=500 A/µs
Reverse recovery charge [9]	Q_{rr}	-	220	440	nC	V_R=75 V, I_F=50 A, di_F/dt=500 A/µs
Reverse recovery time [9]	t_{rr}	-	39	78	ns	V_R=75 V, I_F=50 A, di_F/dt=1000 A/µs
Reverse recovery charge [9]	Q_{rr}	-	410	820	nC	V_R=75 V, I_F=50 A, di_F/dt=1000 A/µs

[9] Defined by design. Not subject to production test.

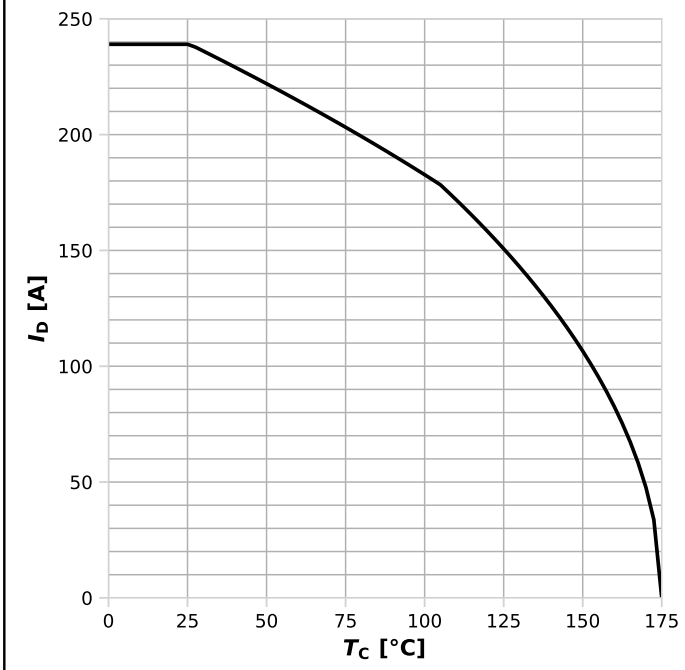
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



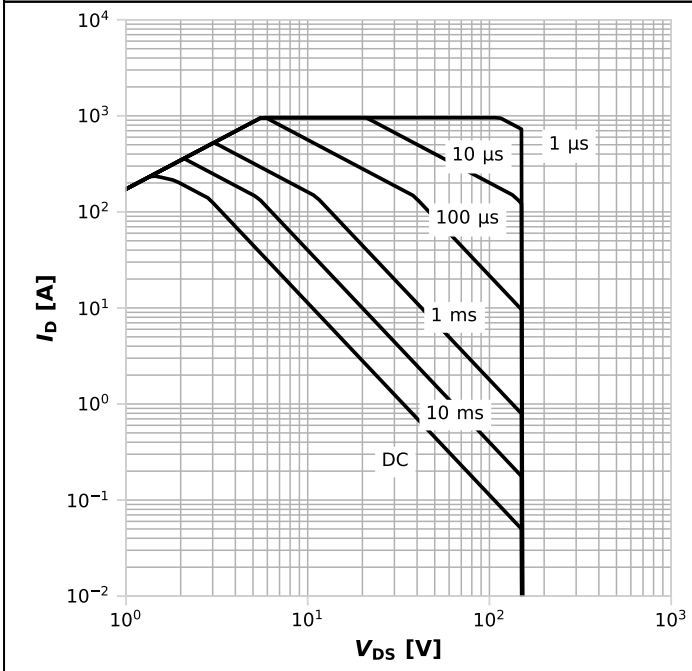
P_{tot}=f(T_C)

Diagram 2: Drain current



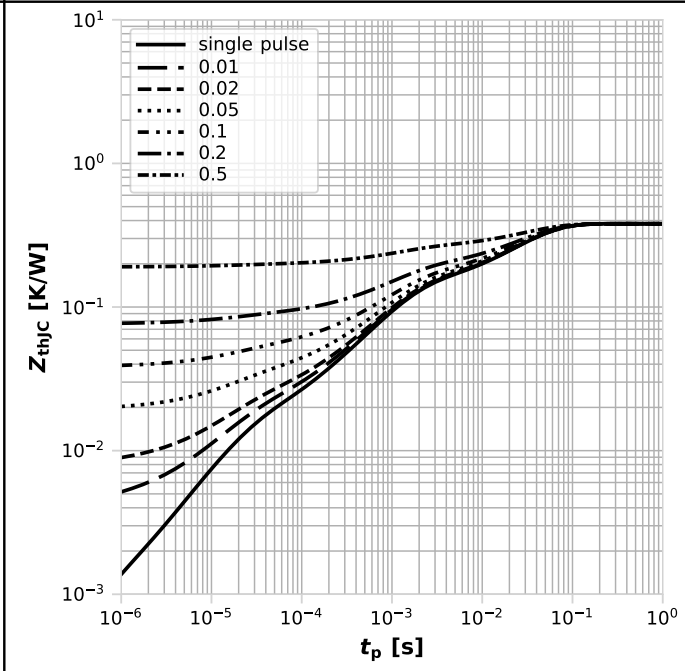
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



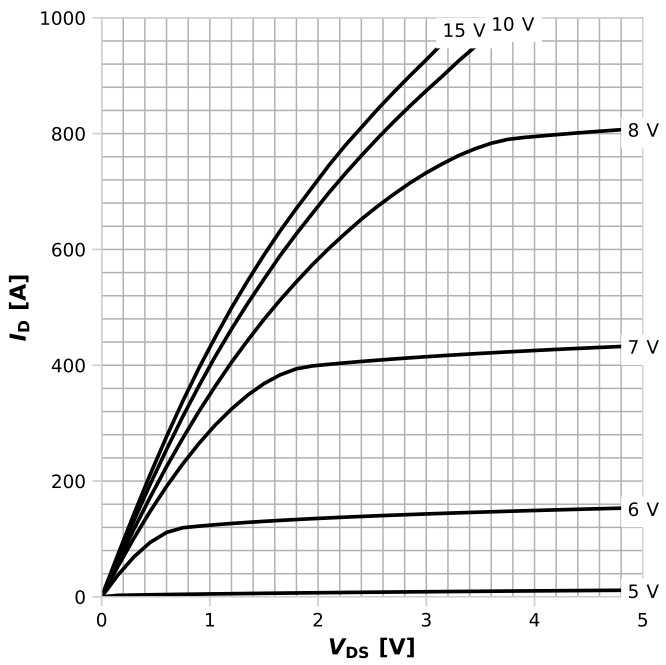
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



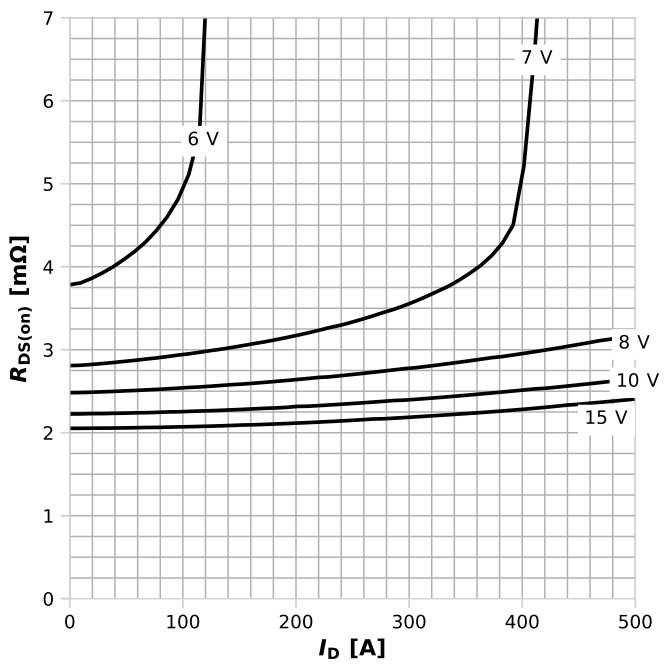
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



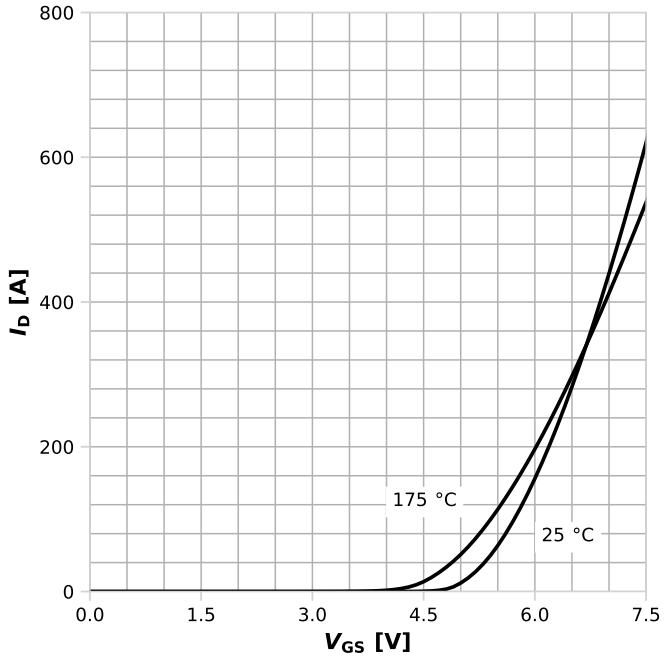
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



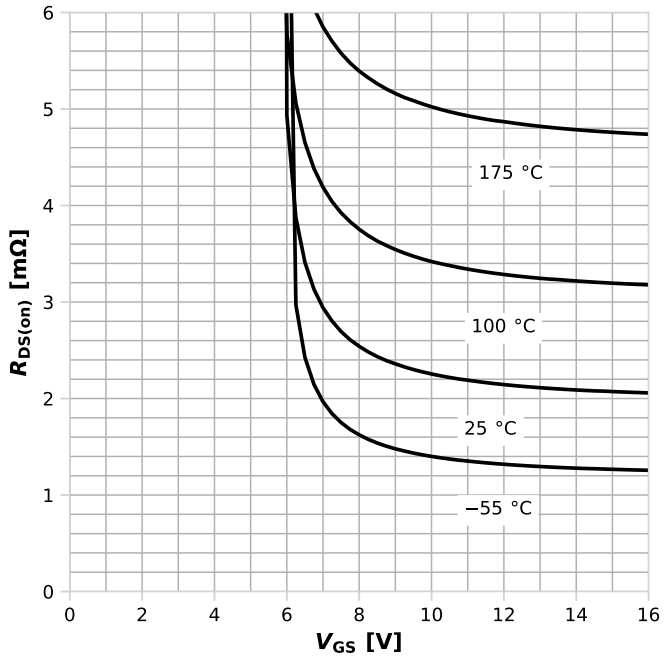
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}=f(V_{GS})$, $I_D=100$ A; parameter: T_j

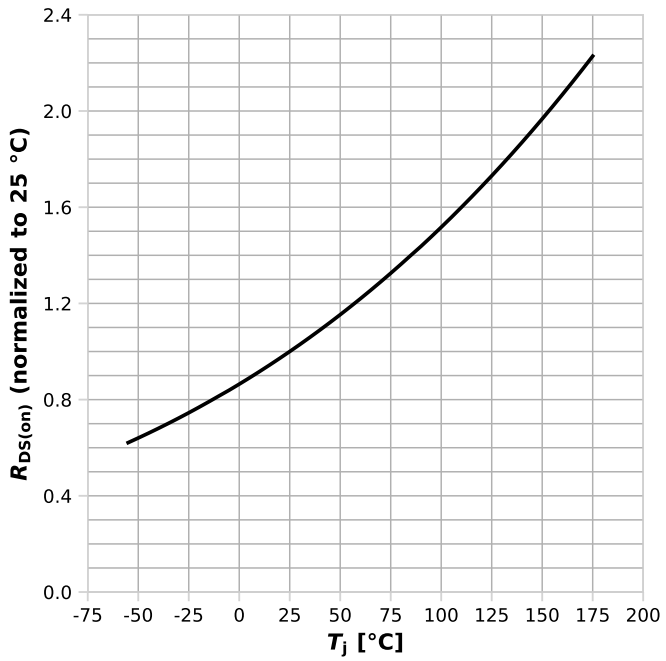
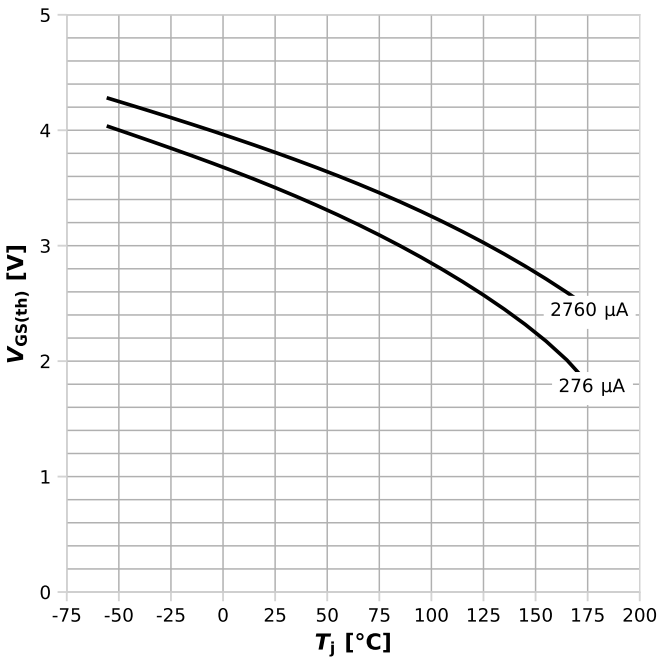
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

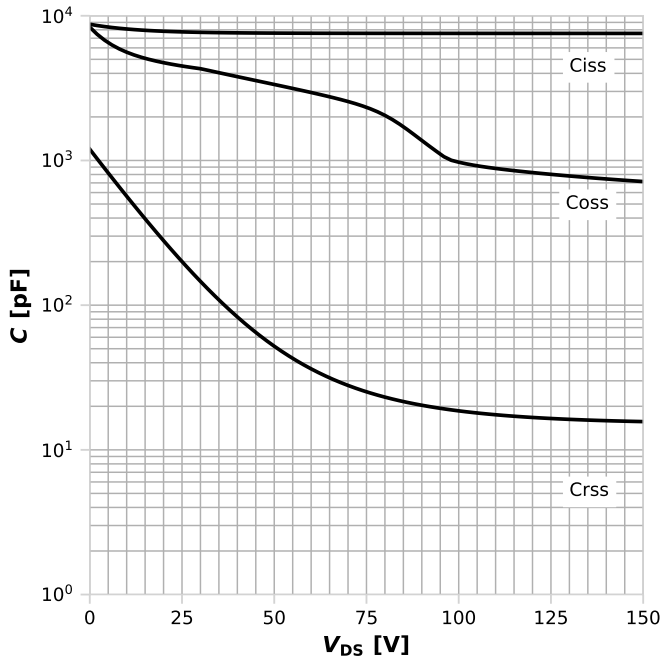
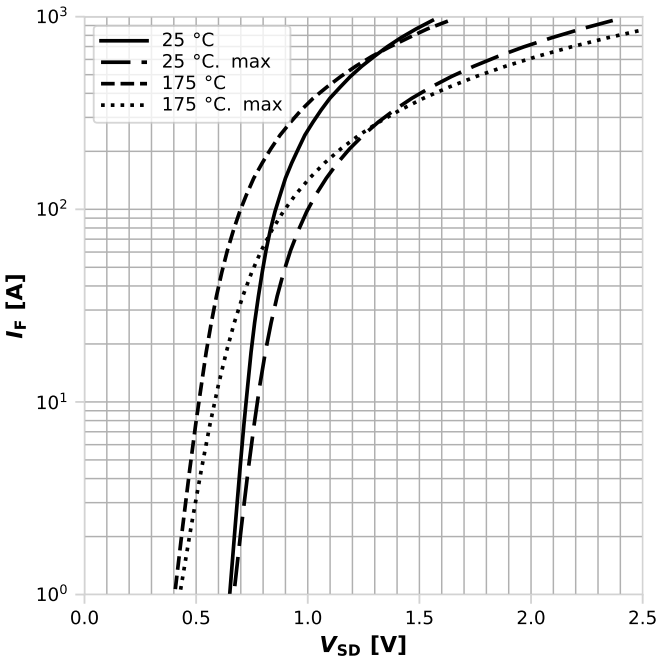
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

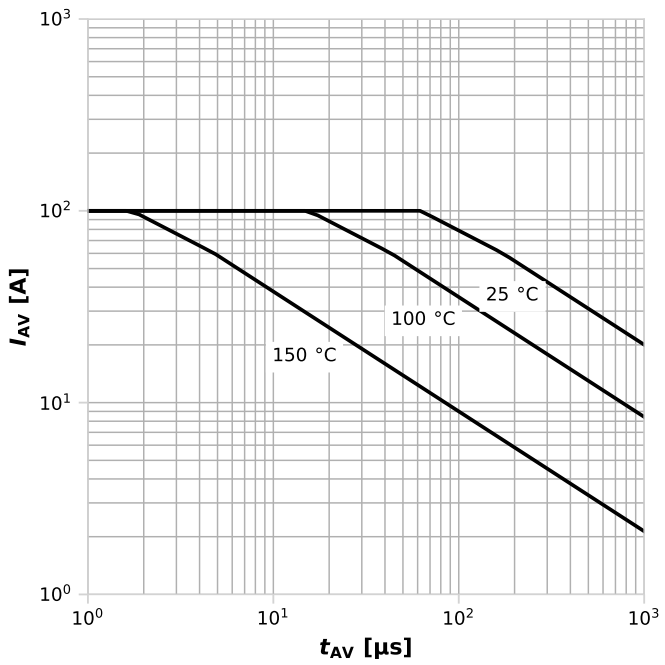
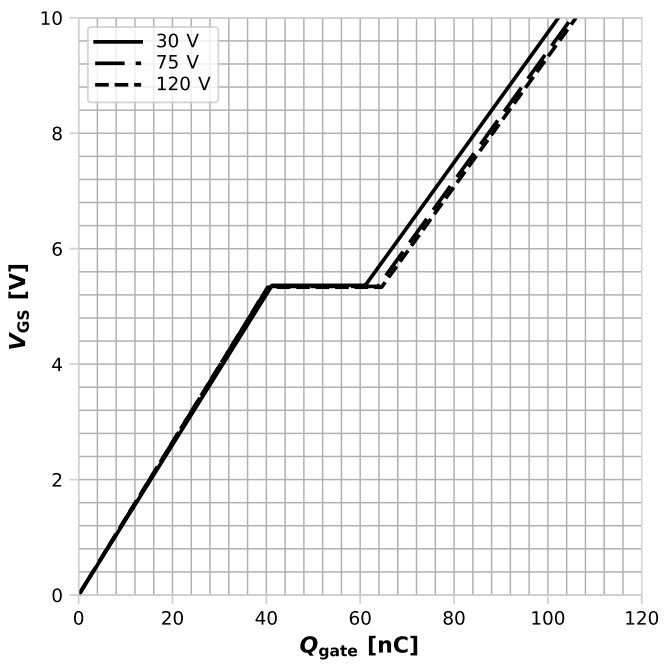
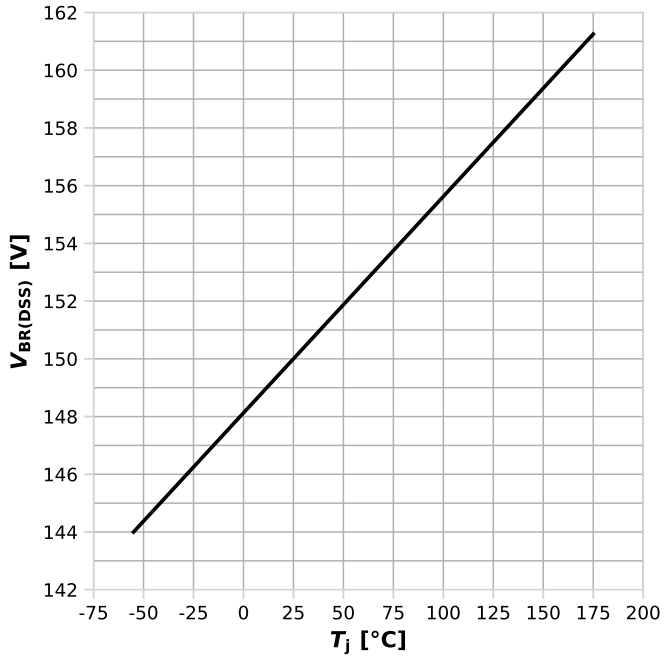
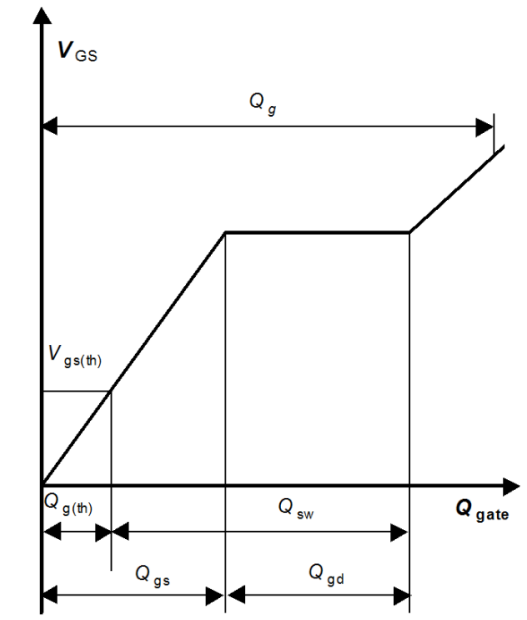
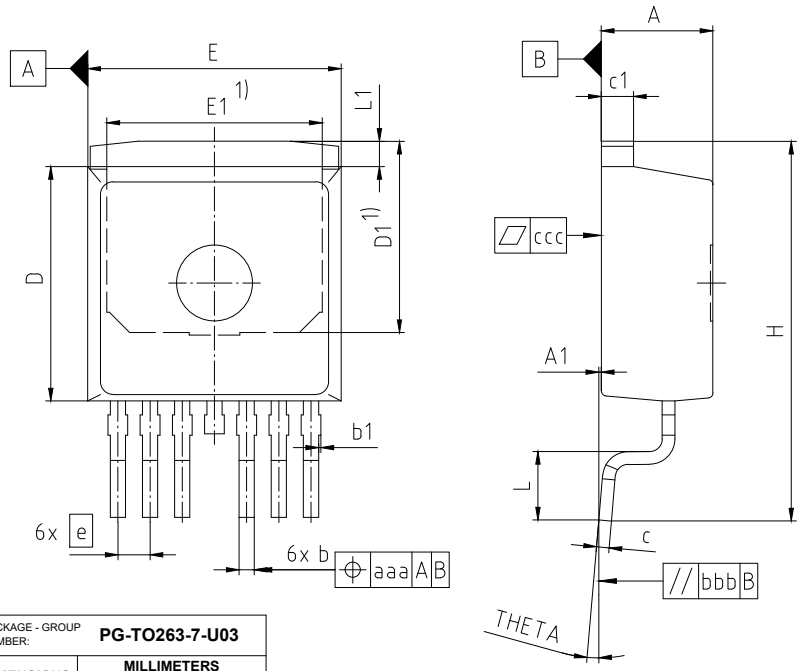
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TO263-7-U03	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.20
b	0.50	0.70
b1	0.00	0.15
c	0.40	0.60
c1	1.17	1.37
D	9.05	9.45
D1	7.45	7.65
E	9.80	10.20
E1	8.40	8.60
e	1.27	
N	7	
H	14.90	15.10
L	2.40	3.00
L1	0.70	1.30
THETA	---	8.00°
aaa	0.25	
bbb	0.10	
ccc	0.05	

NOTES:
1) TYPICAL METAL SURFACE. MIN. X=7.25 MM / Y= 6.9 MM
ALL METAL SURFACES: TIN PLATED, EXPECT AREA OF CUT

Figure 1 Outline PG-TO263-7, dimensions in mm

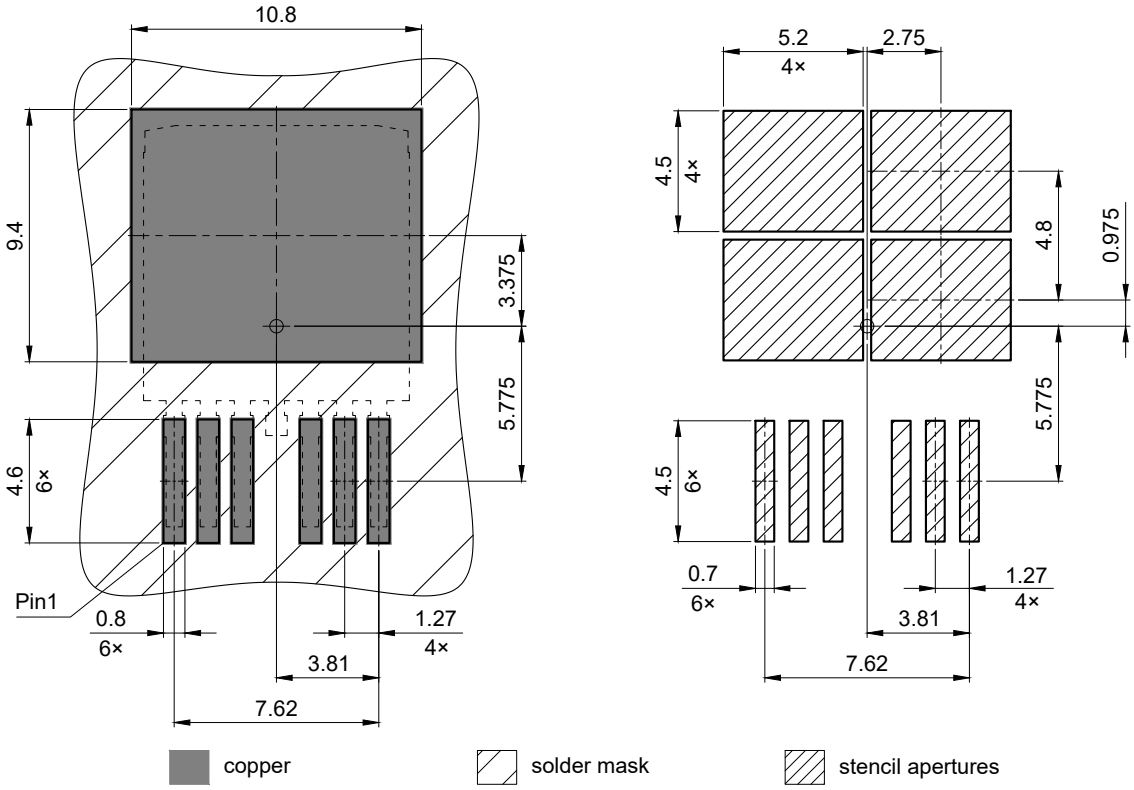


Figure 2 Outline PG-TO263-7, dimensions in mm

Revision History

IPF026N15NM6

Revision 2024-04-22, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-03-15	Release of preliminary version
2.0	2024-04-22	Release of final

Published by
Infineon Technologies AG
81726 München, Germany