

MOSFET

600V CoolMOS™ G7 SJ Power Device

The C7 GOLD series (G7) for the first time brings together the benefits of the C7 GOLD CoolMOS™ technology, 4 pin Kelvin Source capability and the improved thermal properties of the TOLL package to enable a possible SMD solution for high current topologies such as PFC up to 3kW

Features

- C7 Gold gives best in class FOM $R_{DS(on)} * E_{oss}$ and $R_{DS(on)} * Q_g$.
- Suitable for hard and soft switching (PFC and high performance LLC)
- C7 Gold technology enables best in class $R_{DS(on)}$ in smallest footprint.
- TOLL package has inbuilt 4th pin Kelvin Source configuration and low parasitic source inductance (~1nH).
- TOLL package is MSL1 compliant, total Pb-free and has easy visual inspection grooved leads.
- TOLL SMD package combined with lead free die attach process enables improved thermal performance R_{th} .

Benefits

- C7 Gold FOM $R_{DS(on)} * Q_g$ is 15% better than previous C7 600V enabling faster switching leading to higher efficiency.
- Increased economies of scale by use in PFC and PWM topologies in the application
- C7 Gold can reach 28mΩ in in TOLL 115mm² footprint, whereas previous BIC C7 600V was 40mΩ in 150mm² D²PAK footprint.
- Reducing parasitic source inductance by Kelvin Source improves efficiency by faster switching and ease of use due to less ringing.
- TOLL package is easy to use and has the highest quality standards.
- Improved thermals enable SMD TOLL package to be used in higher current designs than has been previously possible.

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Product validation

Fully qualified according to JEDEC for Industrial Applications

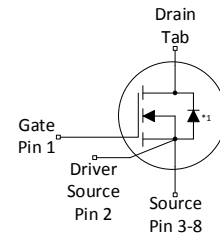
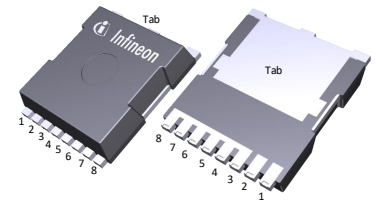
Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	80	mΩ
$Q_{g,typ}$	42	nC
$I_{D,pulse}$	83	A
$I_{D,continuous} @ T_j < 150^{\circ}C$	40	A
$E_{oss}@400V$	5	μJ
Body diode di/dt	820	A/μs

Part number	Package	Marking	Related links
IPT60R080G7	PG-HSOF-8	60R080G7	see Appendix A

TOLL



*1: Internal body diode

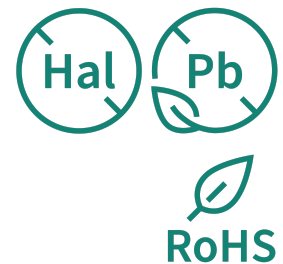




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1 Maximum ratings

at $T_{\hat{I}} = 25^{\circ}\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	29	A	$T_C=25^{\circ}\text{C}$
				18		$T_C=100^{\circ}\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	83	A	$T_C=25^{\circ}\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	97	mJ	$I_D=5\text{A}; V_{DD}=50\text{V};$ see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.49		
Avalanche current, single pulse	I_{AS}	-	-	5.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	167	W	$T_C=25^{\circ}\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^{\circ}\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^{\circ}\text{C}$	
Mounting torque	-	-	-	n.a.	Ncm	
Continuous diode forward current	I_S	-	-	29	A	$T_C=25^{\circ}\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	83		
Reverse diode dv/dt ³⁾	dv/dt	-	-	25	V/ns	$V_{DS}=0\dots400\text{V}, I_{SD}\leq 7.7\text{A}, T_j=25^{\circ}\text{C}$ see table 8
Maximum diode commutation speed	di_t/dt	-	-	820	A/ μs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	$V_{rms}, T_C=25^{\circ}\text{C}, t=1\text{min}$

1) Limited by $T_{j,max}$.

2) Pulse width t_p limited by $T_{j,max}$.

3) Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.75	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.49\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$
			10	-		$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.069	0.080	Ω	$V_{GS}=10\text{V}$, $I_D=9.7\text{A}$, $T_j=25^\circ\text{C}$
			0.172	-		$V_{GS}=10\text{V}$, $I_D=9.7\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.8	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1640	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	34	-		
Effective output capacitance, energy related ⁴⁾	$C_{o(er)}$	-	63	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related ⁵⁾	$C_{o(tr)}$	-	643	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	19	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=9.7\text{A}$, $R_G=5.3\Omega$; see table 9
Rise time	t_r		5			
Turn-off delay time	$t_{d(off)}$		61			
Fall time	t_f		3.5			

⁴⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	$V_{DD}=400V, I_D=9.7A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	Q_{gd}	-	15	-	nC	
Gate charge total	Q_g	-	42	-	nC	
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.8	-	V	$V_{GS}=0V, I_F=9.7A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	310	-	ns	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	3.7	-	μC	
Peak reverse recovery current	I_{rrm}	-	26	-	A	

4 Electrical characteristics diagrams

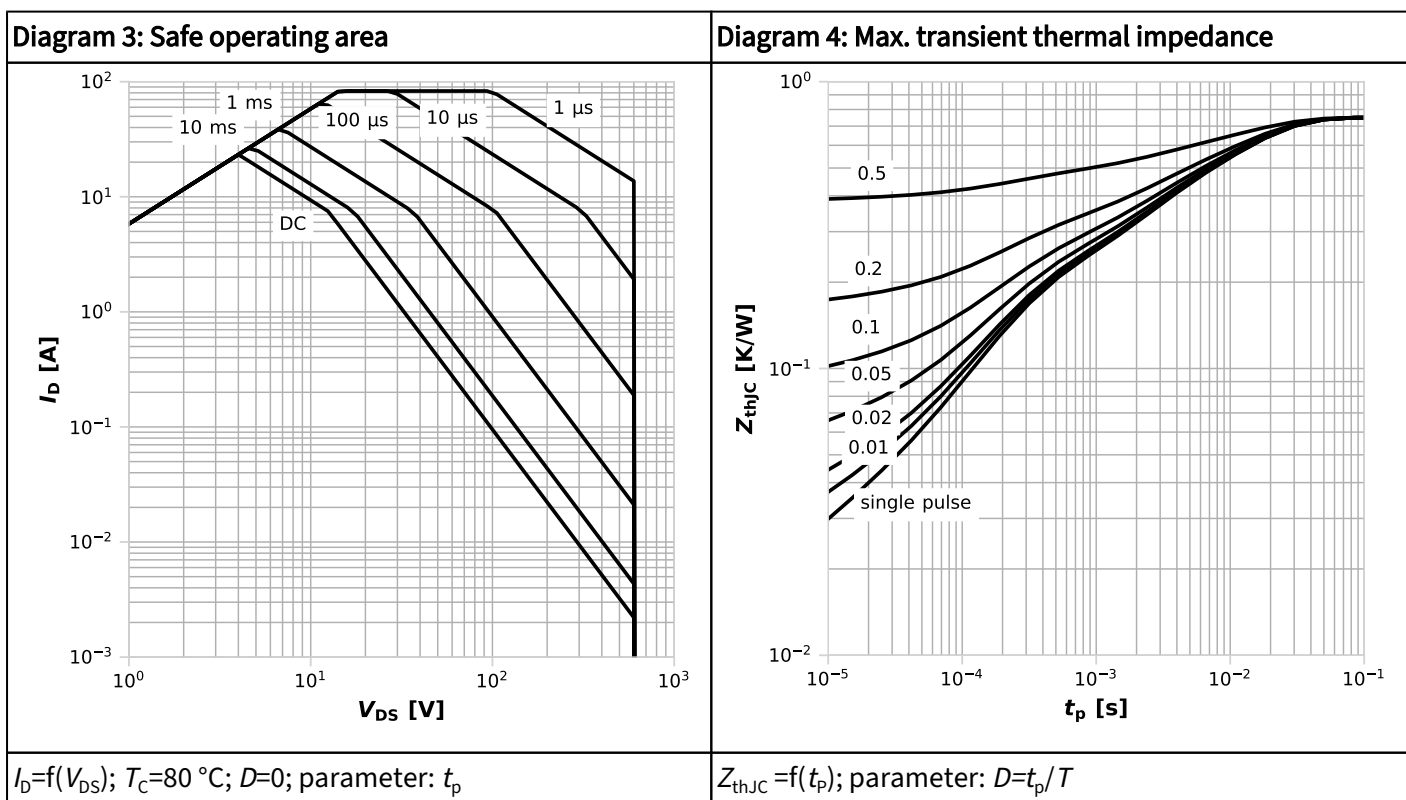
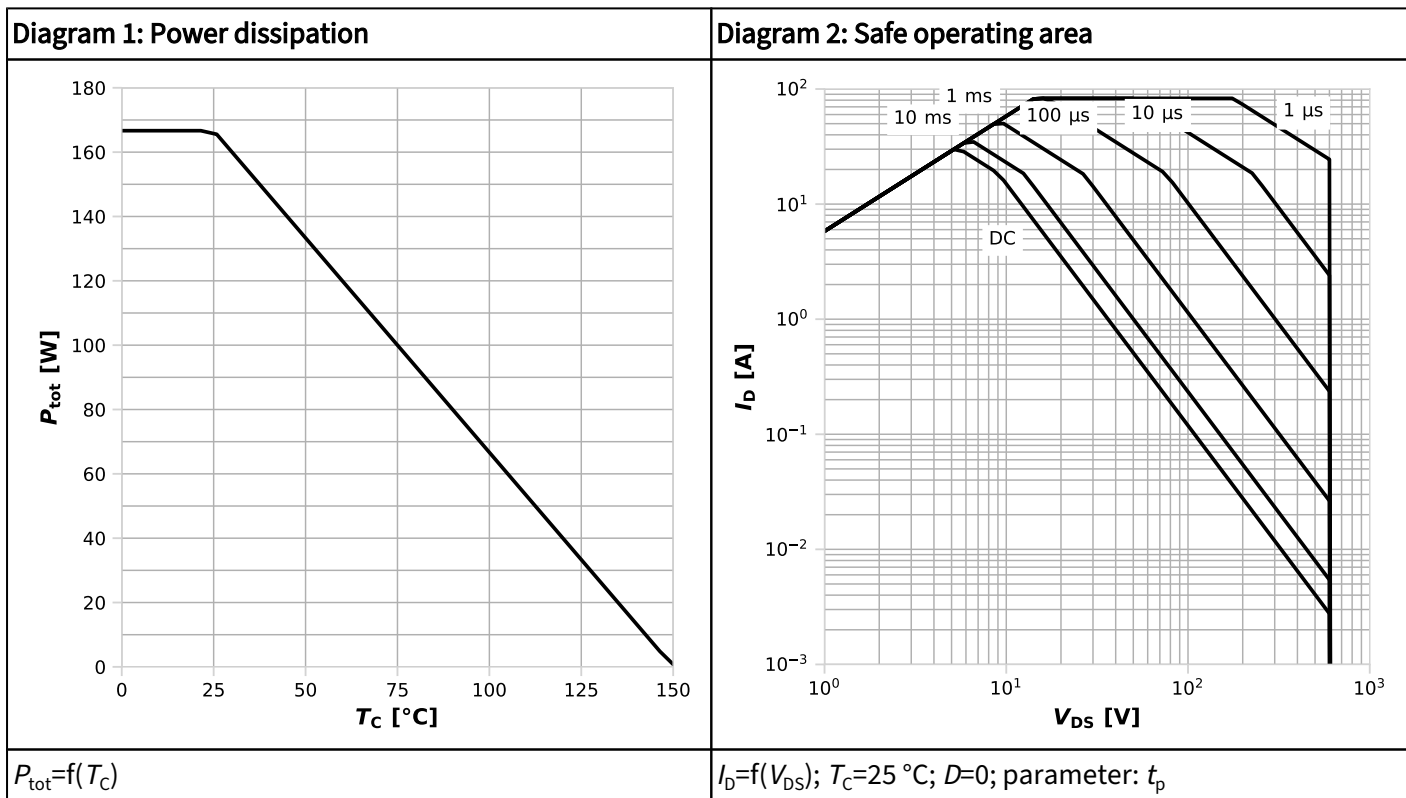
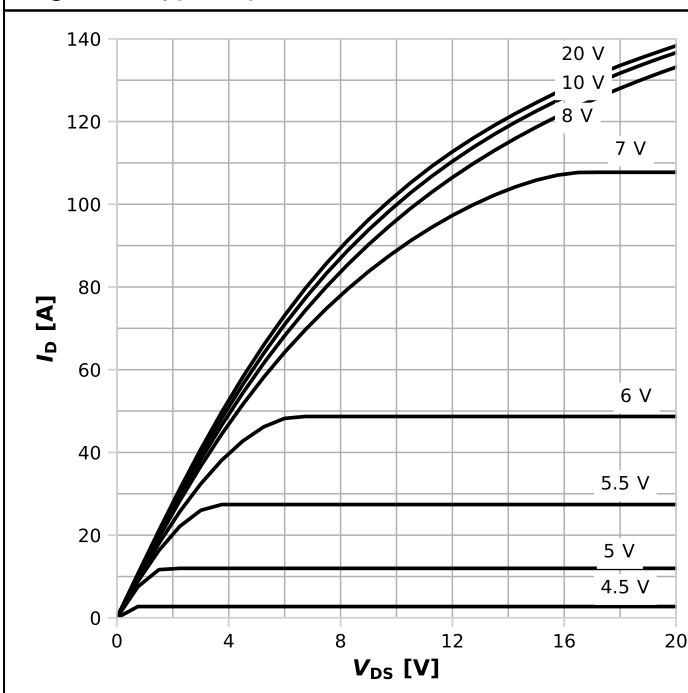
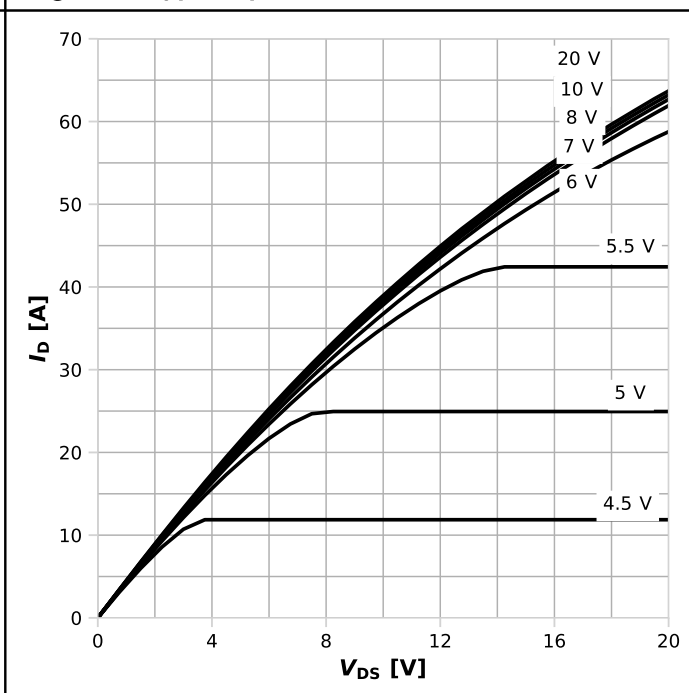


Diagram 5: Typ. output characteristics



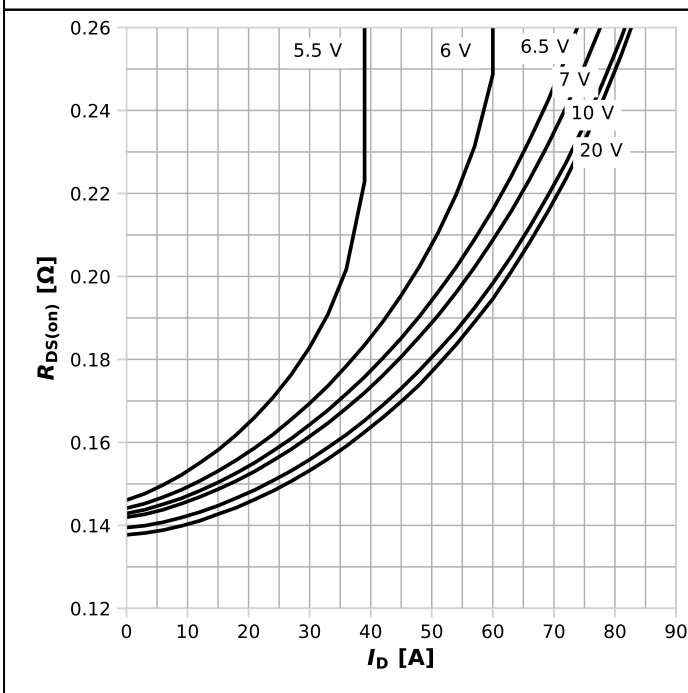
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics



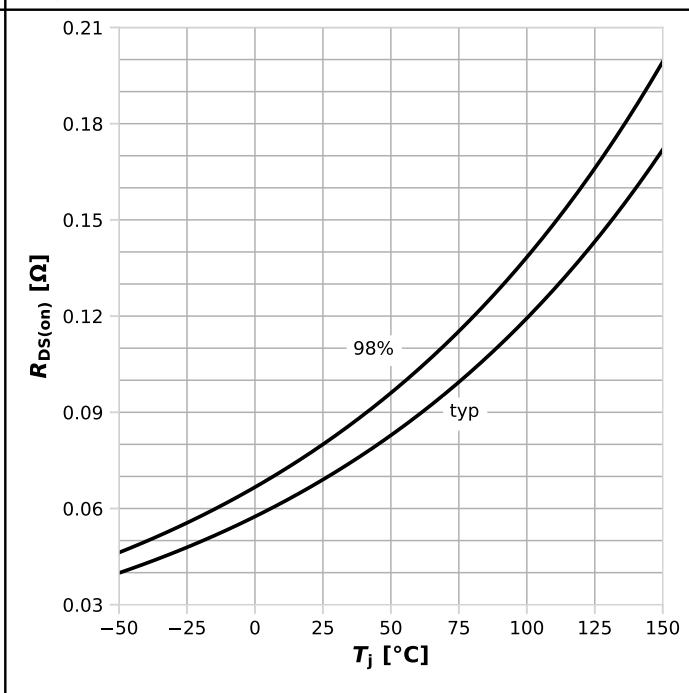
$I_D = f(V_{DS}); T_j = 125\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D); T_j = 125\text{ °C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance



$R_{DS(on)} = f(T_j); I_D = 9.7\text{ A}; V_{GS} = 10\text{ V}$

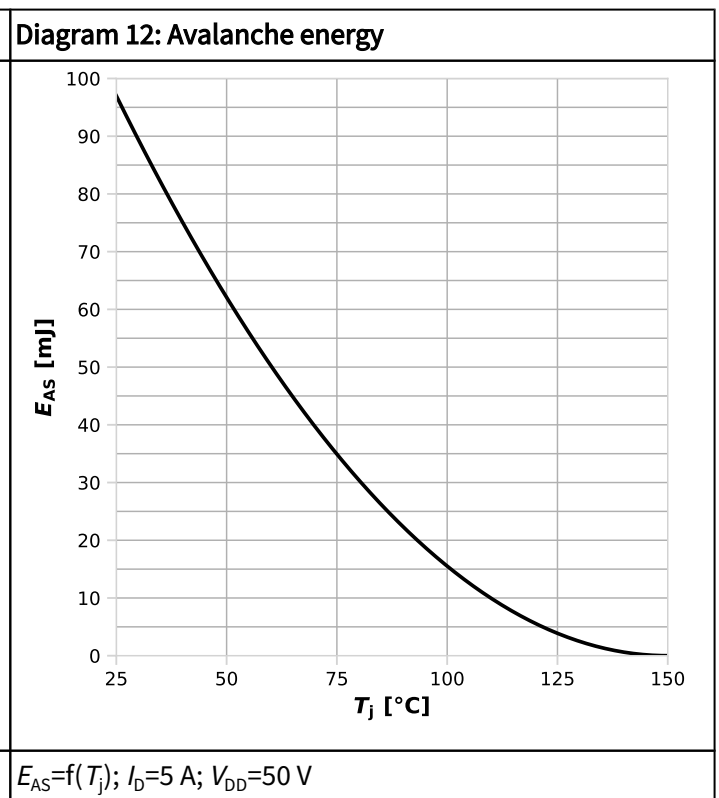
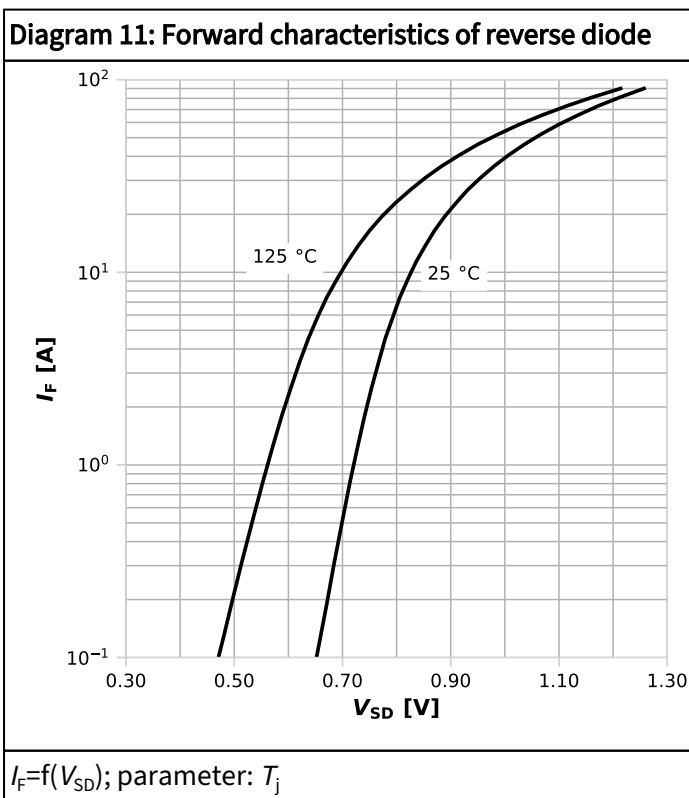
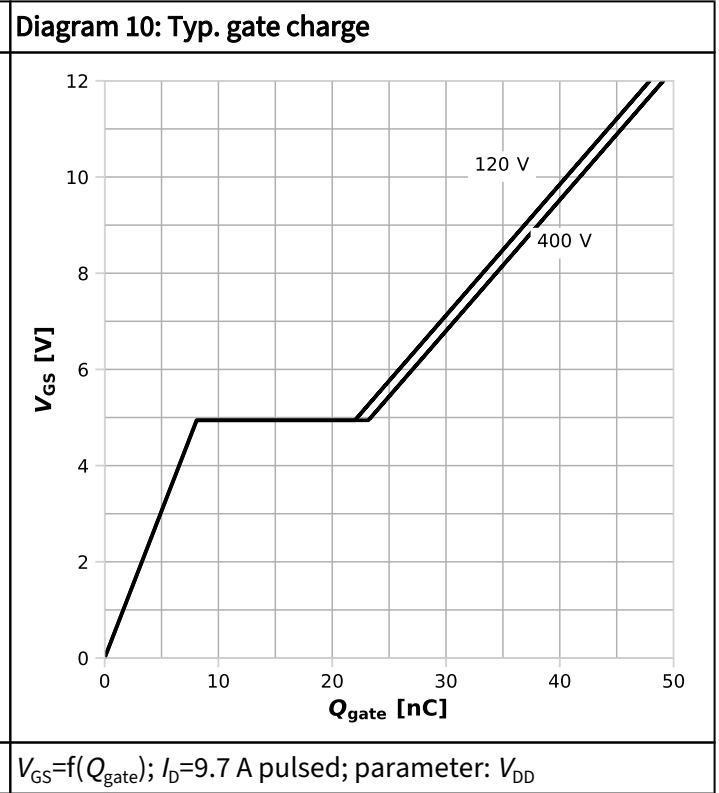
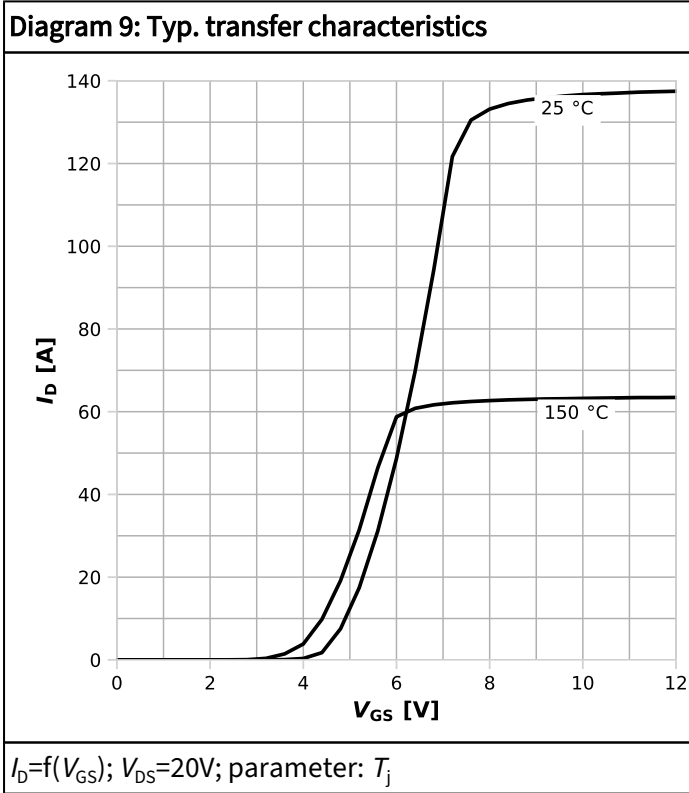
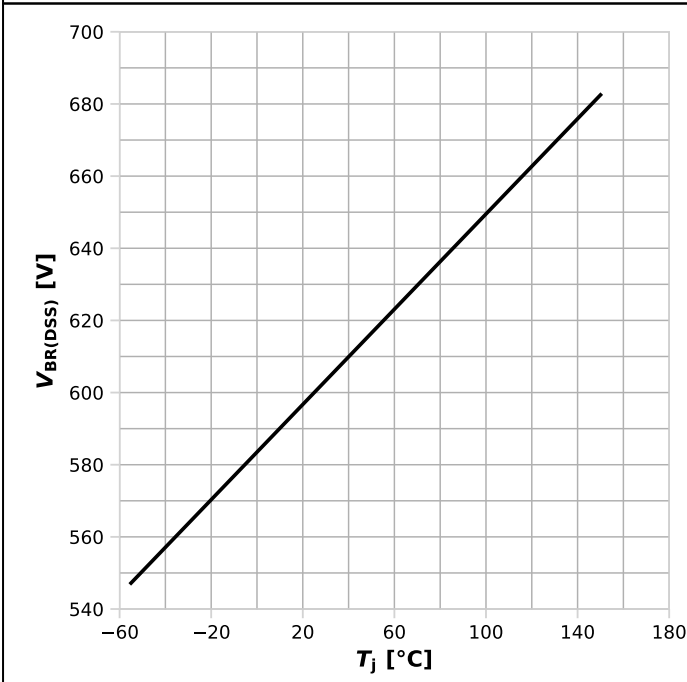
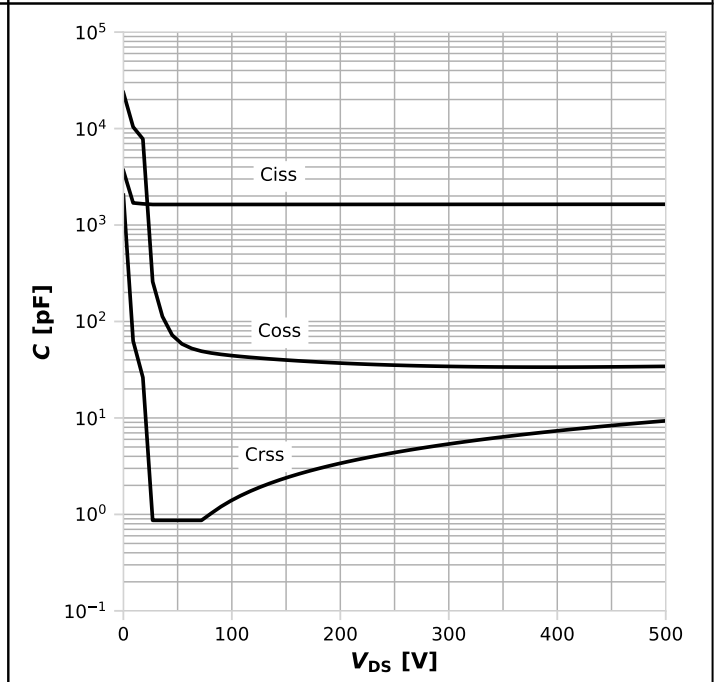


Diagram 13: Drain-source breakdown voltage



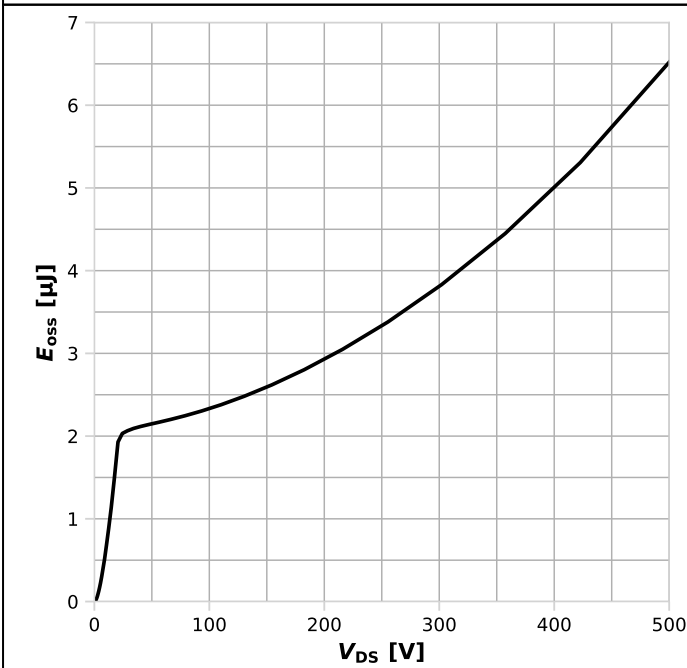
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform

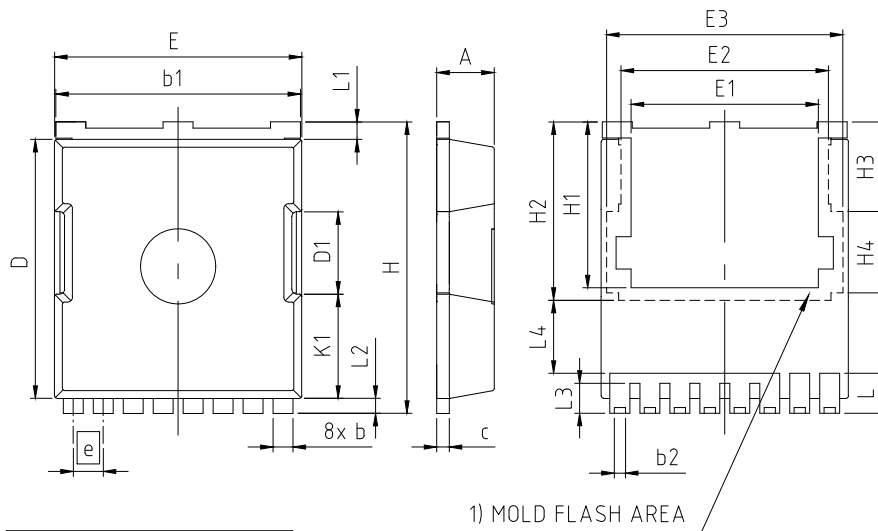
Table 9 Switching times (ss)

Switching times test circuit for inductive load	Switching times waveform

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform

6 Package outlines



PACKAGE - GROUP NUMBER: PG-HSOF-8-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

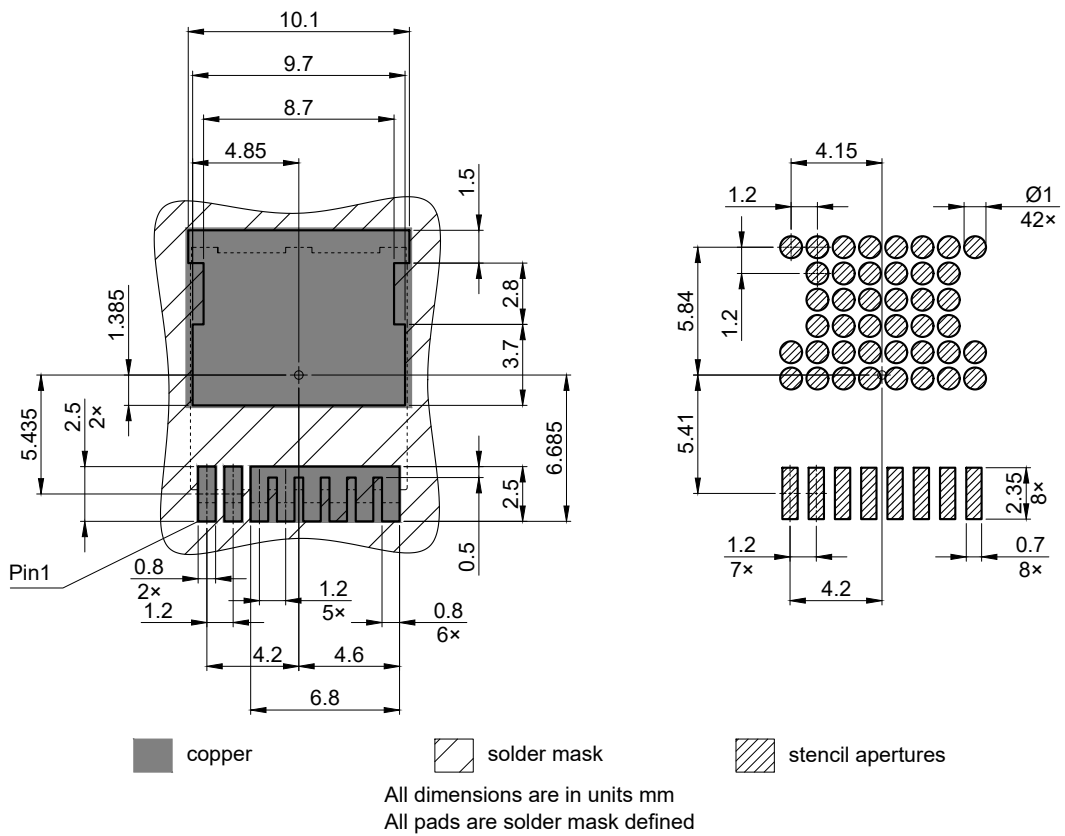
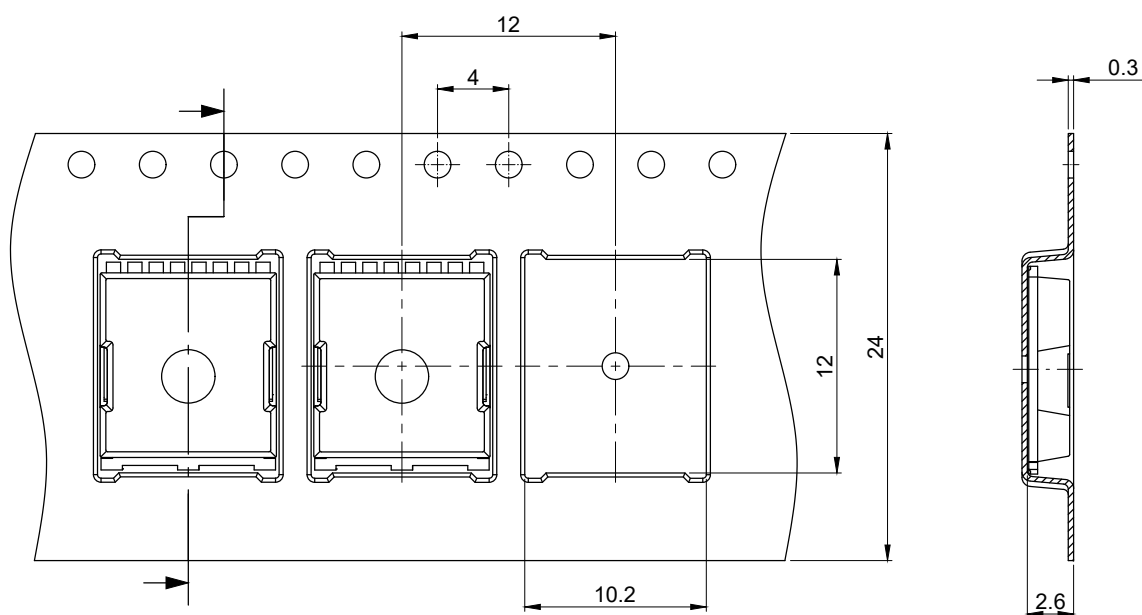


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm


The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 Related links

- [IFX CoolMOS™ G7 Webpage](#)
- [IFX CoolMOS™ G7 application note](#)
- [IFX CoolMOS™ G7 simulation model](#)
- [IFX Design tools](#)

Revision history

IPT60R080G7

Revision 2025-02-03, Rev. 2.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2017-01-27	Release of final version
2.1	2020-10-27	Content update diagram 2,3,4,7,8 and format update
2.2	2025-02-03	Implementation of standardized Infineon Umbrella-Templates for package drawings. H1 Extension from 6.75 to 6.95 MAX

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Published by

Infineon Technologies AG

81726 München, Germany

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