

# IRFM250 (JANTX2N7225)

PD-90554G

## Power MOSFET Thru-Hole (TO-254AA) 200V, 27.4A, N-channel, HEXFET™ MOSFET Technology

### Features

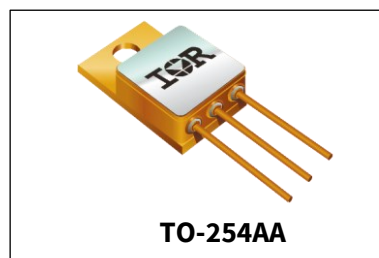
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Dynamic dv/dt rating
- Light weight
- Ceramic eyelets

### Potential Applications

- DC-DC converter
- Motor drives

### Product Summary

- **$BV_{DSS}$** : 200V
- **$I_D$** : 27.4A
- **$R_{DS(on),max}$** : 100m $\Omega$
- **$Q_G, max$** : 115nC
- **REF**: MIL-PRF-19500/592



### Product Validation

Qualified to JANTXV screening flow according to MIL-PRF-19500 for high-reliability applications

### Description

IR HiRel HEXFET™ technology is advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET™ transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, fast switching and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET™ transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

### Ordering Information

**Table 1**      **Ordering options**

Part number	Package	Screening Level
IRFM250	TO-254AA	COTS
JANTX2N7225	TO-254AA	JANTX
JANTXV2N7225	TO-254AA	JANTXV

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**Absolute Maximum Ratings**

**1 Absolute Maximum Ratings**

**Table 2 Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 10V, T_C = 25^\circ C$	Continuous Drain Current	27.4	A
$I_{D2} @ V_{GS} = 10V, T_C = 100^\circ C$	Continuous Drain Current	17	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current <sup>1</sup>	110	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>	500	mJ
$I_{AR}$	Avalanche Current <sup>1</sup>	27.4	A
$E_{AR}$	Repetitive Avalanche Energy <sup>1</sup>	15	mJ
dv/dt	Peak Diode Reverse Recovery <sup>3</sup>	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup>  $V_{DD} = 50V$ , starting  $T_J = 25^\circ C$ ,  $L = 1.3mH$ , Peak  $I_L = 27.4A$ ,  $V_{GS} = 10V$

<sup>3</sup>  $I_{SD} \leq 27.4A$ ,  $di/dt \leq 190A/\mu s$ ,  $V_{DD} \leq 200V$ ,  $T_J \leq 150^\circ C$

**Device Characteristics**

**2 Device Characteristics**

**2.1 Electrical Characteristics**

**Table 3 Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.28	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	100	mΩ	V <sub>GS</sub> = 10V, I <sub>D2</sub> = 17A <sup>1</sup>
		—	—	105		V <sub>GS</sub> = 10V, I <sub>D1</sub> = 27.4A <sup>1</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
G <sub>fs</sub>	Forward Transconductance	9.0	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 17A
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	25	μA	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	115	nC	I <sub>D1</sub> = 27.4A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	22		V <sub>DS</sub> = 100V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	60		V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	35	ns	I <sub>D1</sub> = 27.4A ** V <sub>DD</sub> = 100V R <sub>G</sub> = 2.35Ω V <sub>GS</sub> = 10V
t <sub>r</sub>	Rise Time	—	—	190		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	170		
t <sub>f</sub>	Fall Time	—	—	130		
L <sub>s</sub> + L <sub>D</sub>	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C <sub>iss</sub>	Input Capacitance	—	3500	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	700	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	110	—		
C <sub>DC</sub>	Drain-to-Case Capacitance	—	12	—		

\*\* Switching speed maximum limits are based on manufacturing test equipment and capability.

<sup>1</sup> Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

**Device Characteristics**

**2.2 Source-Drain Diode Ratings and Characteristics**

**Table 4 Source-Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	27.4	A	
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>1</sup>	—	—	110	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.9	V	$T_J = 25^\circ\text{C}$ , $I_S = 27.4\text{A}$ , $V_{GS} = 0\text{V}$ <sup>2</sup>
$t_{rr}$	Reverse Recovery Time	—	—	950	ns	$T_J = 25^\circ\text{C}$ , $I_F = 27.4\text{A}$ , $V_{DD} \leq 50\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$
$Q_{rr}$	Reverse Recovery Charge	—	6.0	—	$\mu\text{C}$	
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

**2.3 Thermal Characteristics**

**Table 5 Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.83	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	48	

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup> Pulse width  $\leq 300 \mu\text{s}$ ; Duty Cycle  $\leq 2\%$

Electrical Characteristics Curves

3 Electrical Characteristics Curves

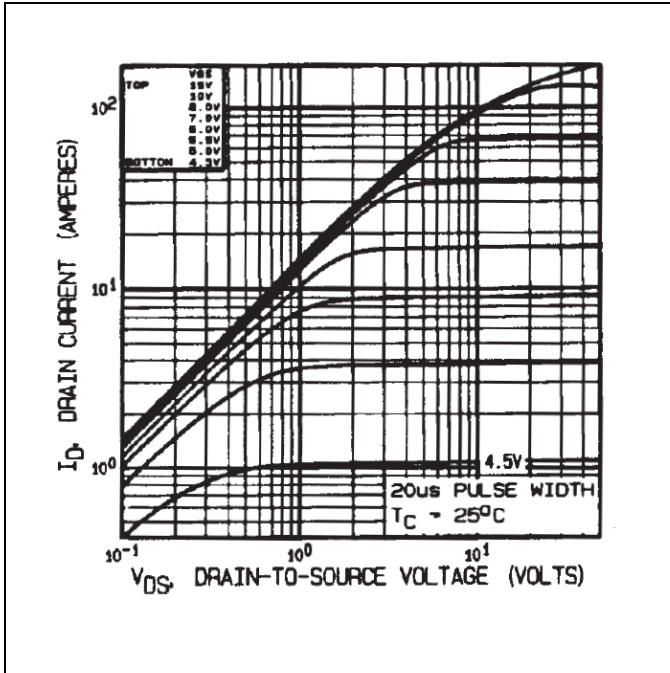


Figure 1 Typical Output Characteristics

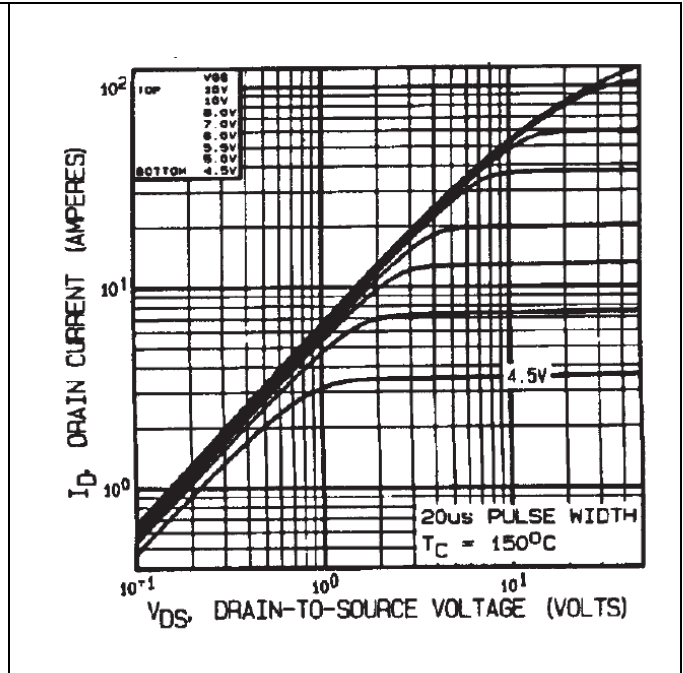


Figure 2 Typical Output Characteristics

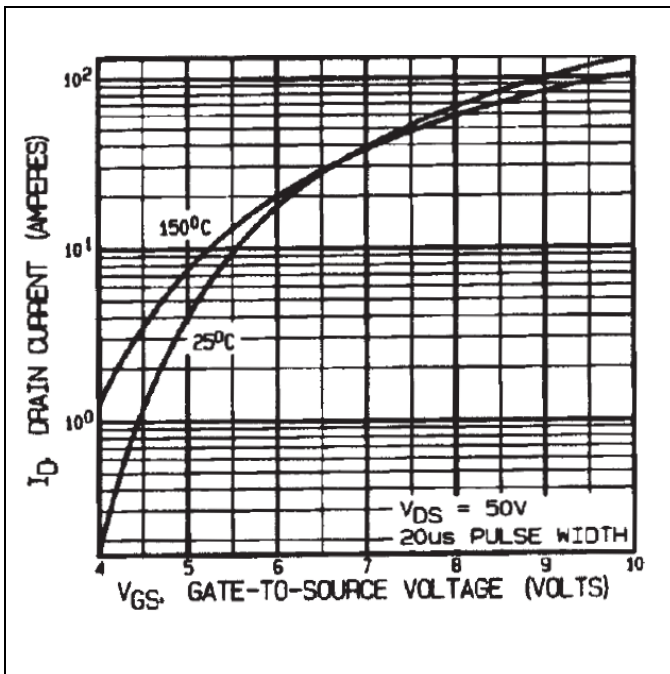


Figure 3 Typical Transfer Characteristics

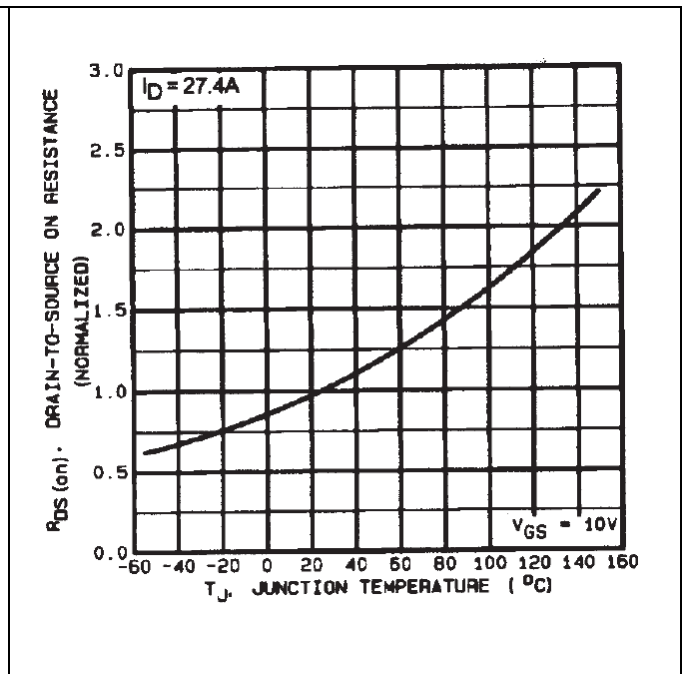
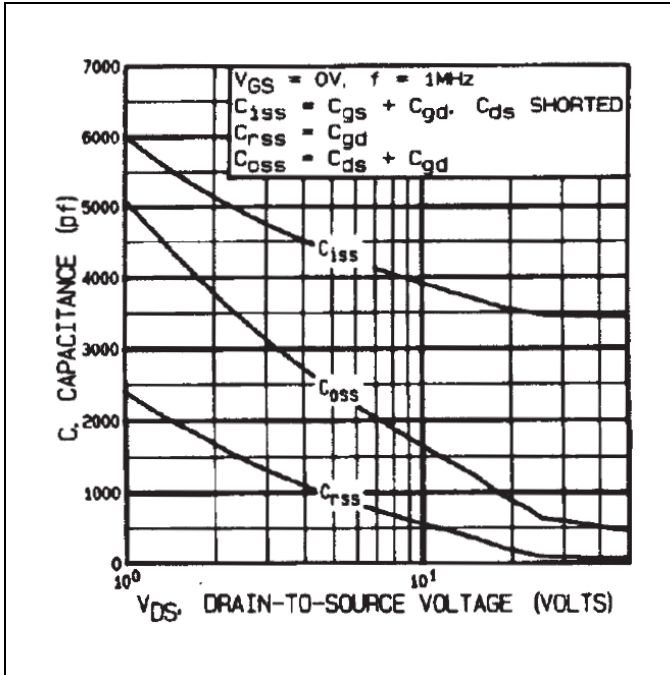
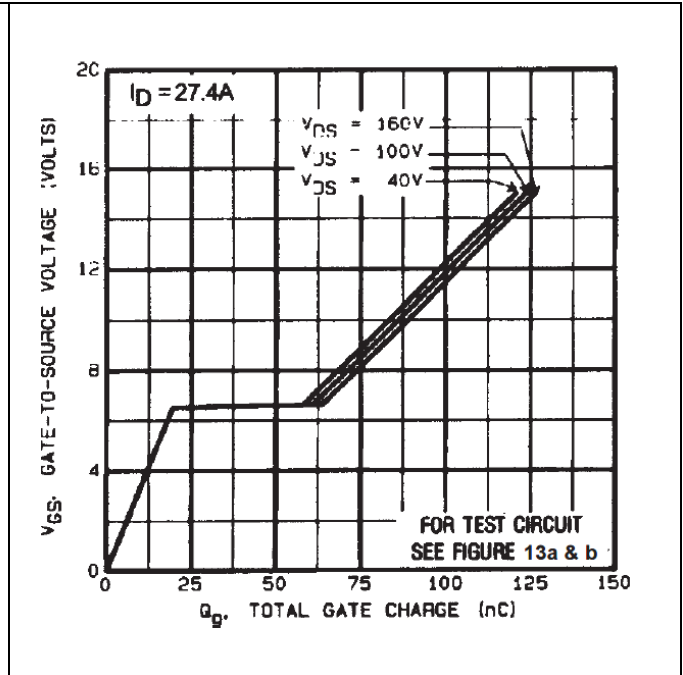


Figure 4 Normalized On-Resistance Vs. Temperature

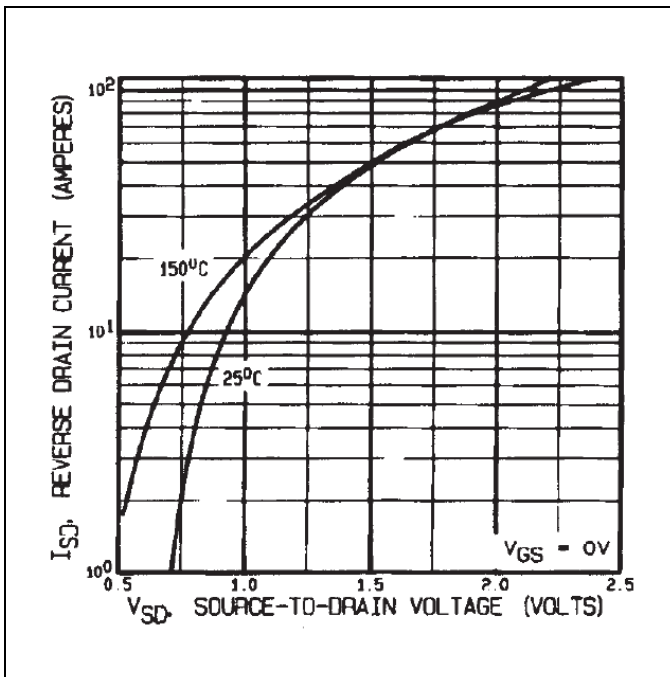
**IRFM250 (JANTX2N7225)**  
**Power MOSFET Thru - Hole (TO-254AA)**  
**Electrical Characteristics Curves**



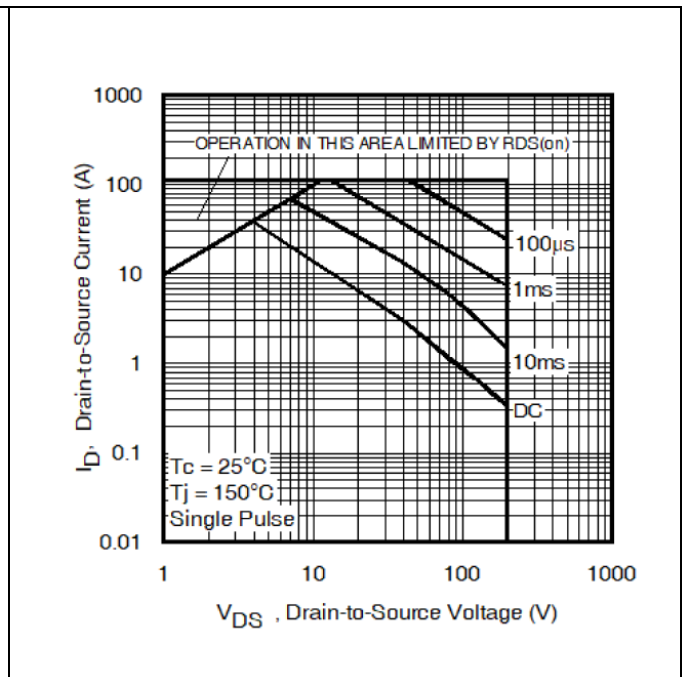
**Figure 5** Typical Capacitance Vs. Drain-to-Source Voltage



**Figure 6** Typical Gate Charge Vs. Gate-to-Source Voltage



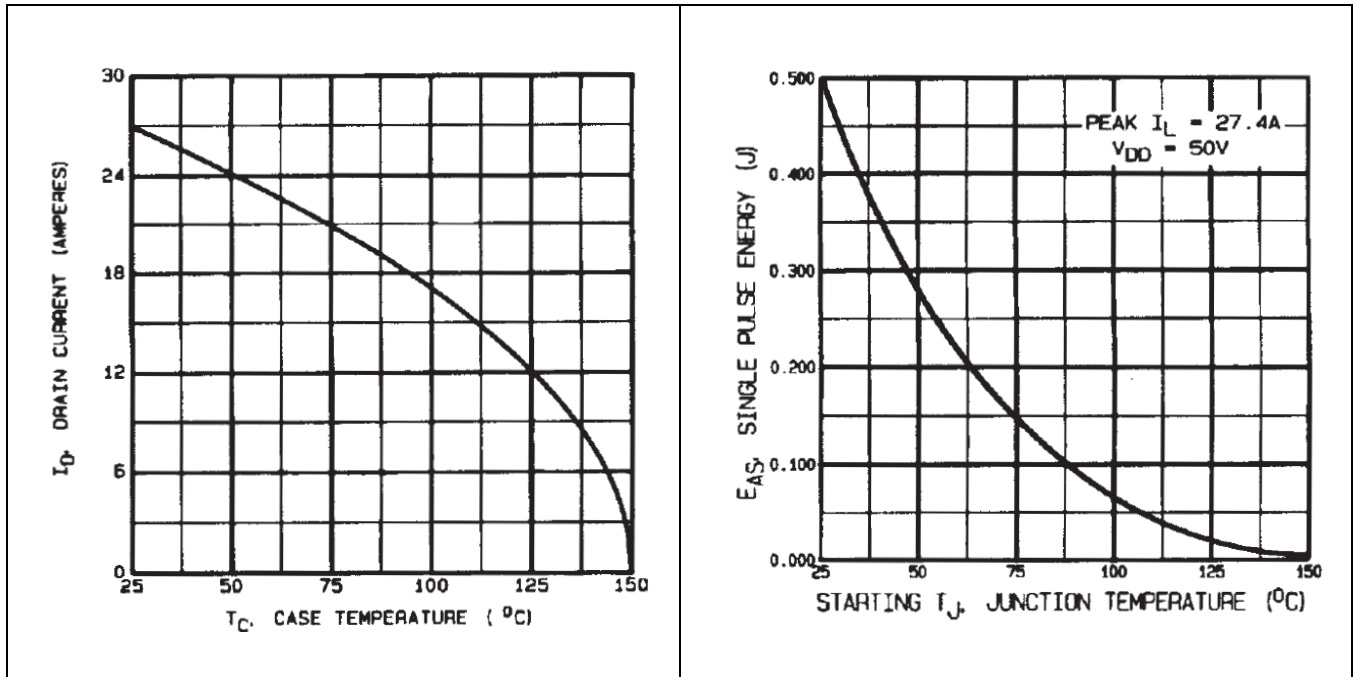
**Figure 7** Typical Source-Drain Current Vs. Diode Forward Voltage



**Figure 8** Maximum Safe Operating Area

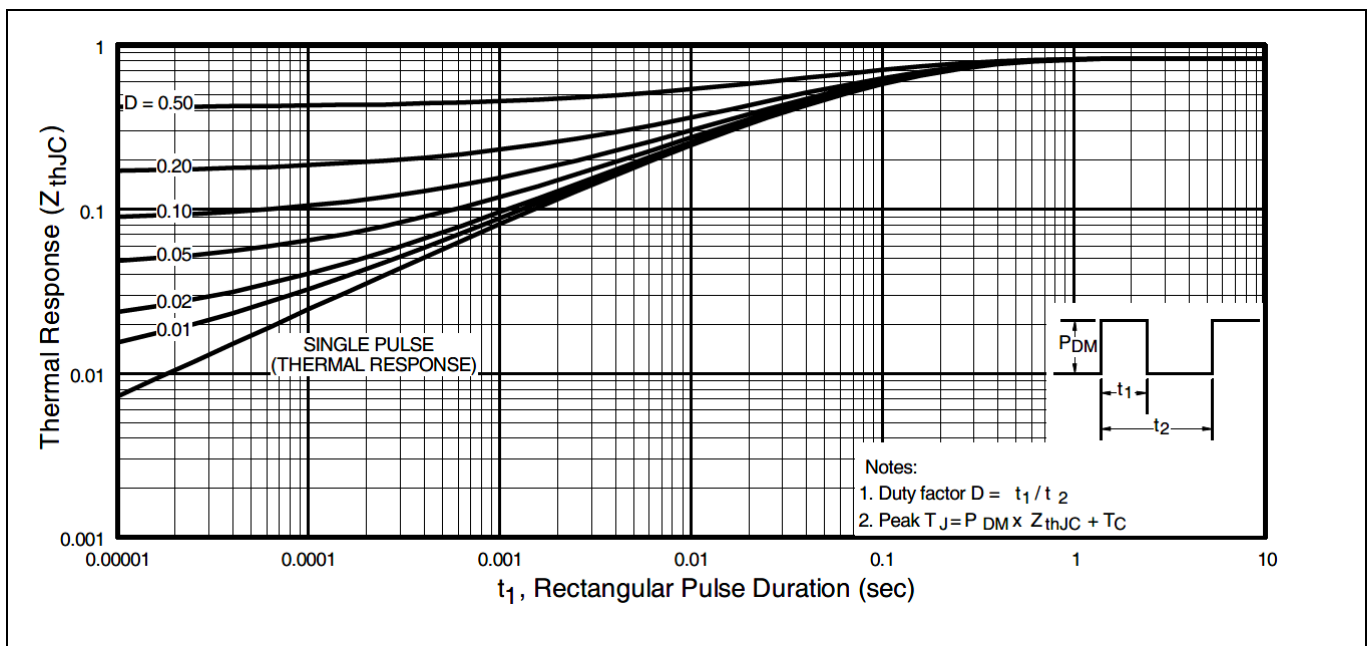
**IRFM250 (JANTX2N7225)**  
**Power MOSFET Thru - Hole (TO-254AA)**

**Electrical Characteristics Curves**



**Figure 9 Maximum Drain Current Vs. Case Temperature**

**Figure 10 Maximum Avalanche Energy Vs. Junction Temperature**



**Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case**



# IRFM250 (JANTX2N7225)

## Power MOSFET Thru - Hole (TO-254AA)

### Test Circuits

## 4 Test Circuits

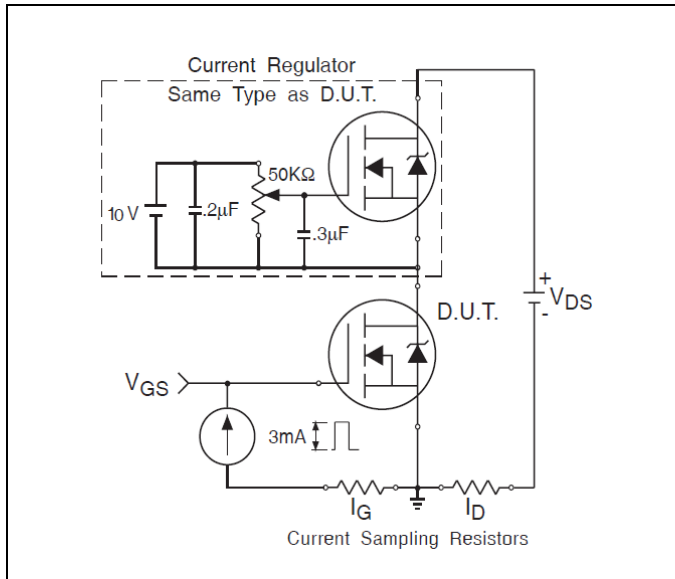


Figure 12 Gate Charge Test Circuit

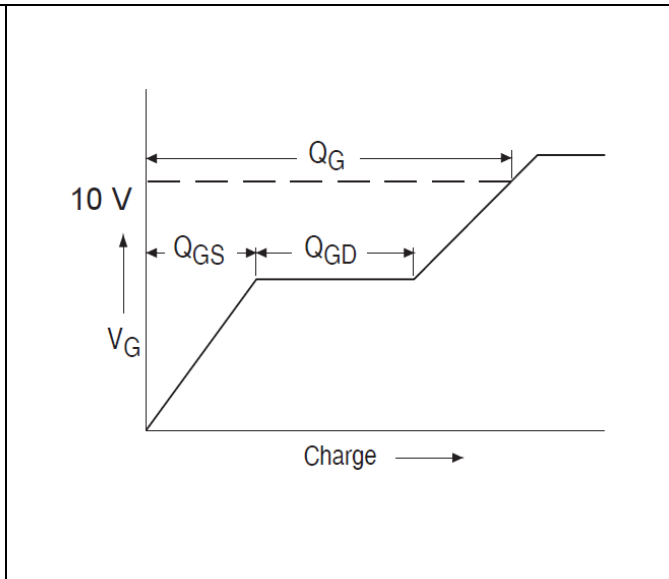


Figure 13 Gate Charge Waveform

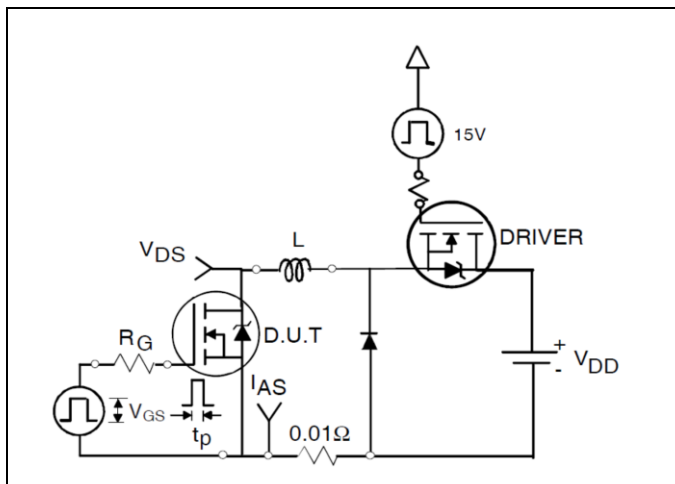


Figure 14 Unclamped Inductive Test Circuit

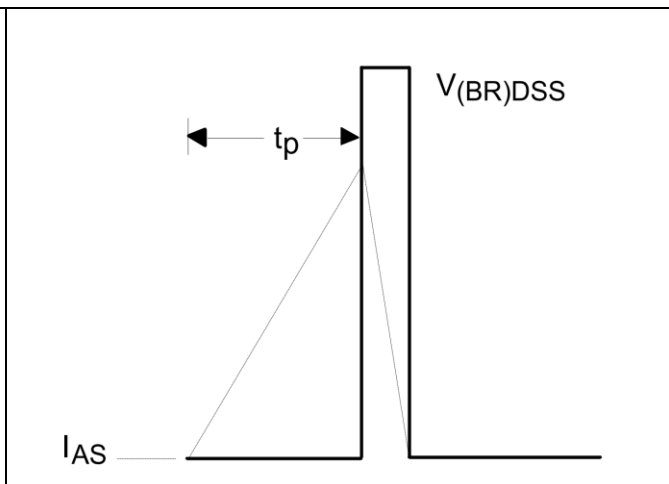


Figure 15 Unclamped Inductive Waveform

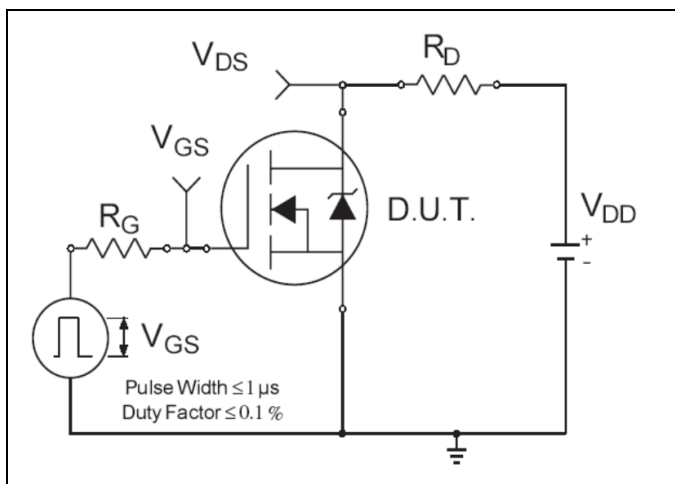


Figure 16 Switching Time Test Circuit

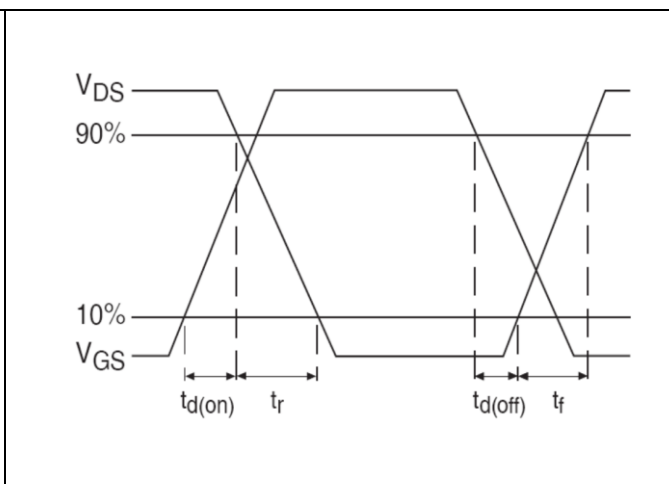


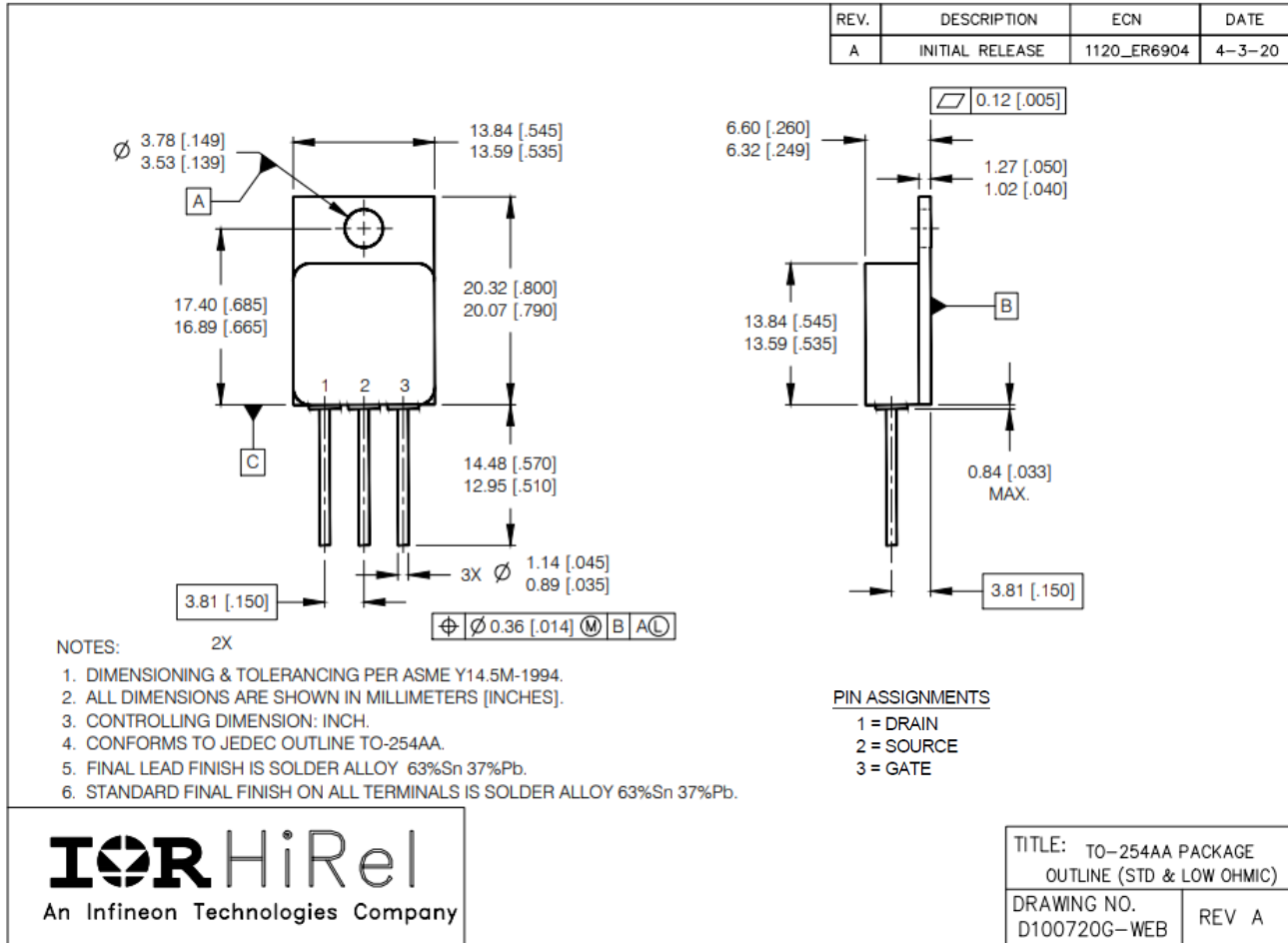
Figure 17 Switching Time Waveforms

**IRFM250 (JANTX2N7225)**  
**Power MOSFET Thru - Hole (TO-254AA)**

**Package Outline**

**5 Package Outline**

**Note:** For the most updated package outline, please see the website: [TO-254AA](http://www.infineon.com/toc-254aa)



**BERYLLIA WARNING PER MIL-PRF-19500**

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

**Revision history**

**Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
Rev E	01/14/2002	Datasheet (PD-90554)
Rev F	07/19/2024	Updated based on ECN-1120_00003
Rev G	08/06/2024	Updated based on ECN-1120_10008

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