

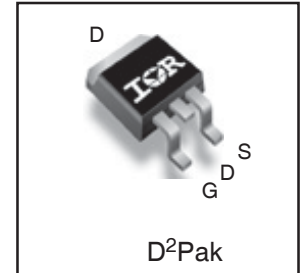
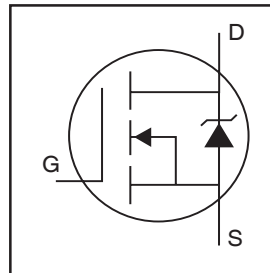
PDP SWITCH

IRFS4229PbF

Features

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low E_{PULSE} Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low Q_G for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
V_{DS} min	250	V
V_{DS} (Avalanche) typ.	300	V
$R_{DS(ON)}$ typ. @ 10V	42	mΩ
I_{RP} max @ $T_C = 100^\circ\text{C}$	91	A
T_J max	175	°C



G	D	S
Gate	Drain	Source

Description

This HEXFET® Power MOSFET is specifically designed for Sustain; Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low E_{PULSE} rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	±30	V
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	45	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	32	
I_{DM}	Pulsed Drain Current ①	180	
I_{RP} @ $T_C = 100^\circ\text{C}$	Repetitive Peak Current ⑤	91	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	W
P_D @ $T_C = 100^\circ\text{C}$	Power Dissipation	190	
	Linear Derating Factor	2.2	W/°C
T_J	Operating Junction and Storage Temperature Range	-40 to + 175	°C
T_{STG}			
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lb·in (1.1N·m)	N

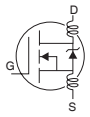
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.45*	
$R_{\theta JA}$	Junction-to-Ambient ④	—	62	

* $R_{\theta JC}$ (end of life) for D²Pak and TO-262 = 0.65°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium.

Notes ① through ⑤ are on page 9

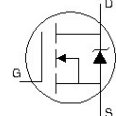
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	210	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	42	48	mΩ	$V_{GS} = 10V, I_D = 26A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-14	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 250V, V_{GS} = 0V$
		—	—	200		$V_{DS} = 250V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	83	—	—	S	$V_{DS} = 25V, I_D = 26A$
Q_g	Total Gate Charge	—	72	110	nC	$V_{DD} = 125V, I_D = 26A, V_{GS} = 10V$ ③
Q_{gd}	Gate-to-Drain Charge	—	26	—		
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 125V, V_{GS} = 10V$ ③ $I_D = 26A$ $R_G = 2.4\Omega$ See Fig. 22
t_r	Rise Time	—	31	—		
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		
t_f	Fall Time	—	21	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 200V, V_{GS} = 15V, R_G = 4.7\Omega$
E_{PULSE}	Energy per Pulse	—	790	—	μJ	$L = 220\text{nH}, C = 0.3\mu F, V_{GS} = 15V$ $V_{DS} = 200V, R_G = 4.7\Omega, T_J = 25^\circ\text{C}$
		—	1390	—		$L = 220\text{nH}, C = 0.3\mu F, V_{GS} = 15V$ $V_{DS} = 200V, R_G = 4.7\Omega, T_J = 100^\circ\text{C}$
C_{iss}	Input Capacitance	—	4560	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz},$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 200V$
C_{oss}	Output Capacitance	—	390	—		
C_{rss}	Reverse Transfer Capacitance	—	100	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	290	—		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	130	mJ
E_{AR}	Repetitive Avalanche Energy ①	—	33	mJ
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	300	—	V
I_{AS}	Avalanche Current ②	—	26	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	45	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 26A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	190	290	ns	$T_J = 25^\circ\text{C}, I_F = 26A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	840	1260	nC	$di/dt = 100A/\mu s$ ③

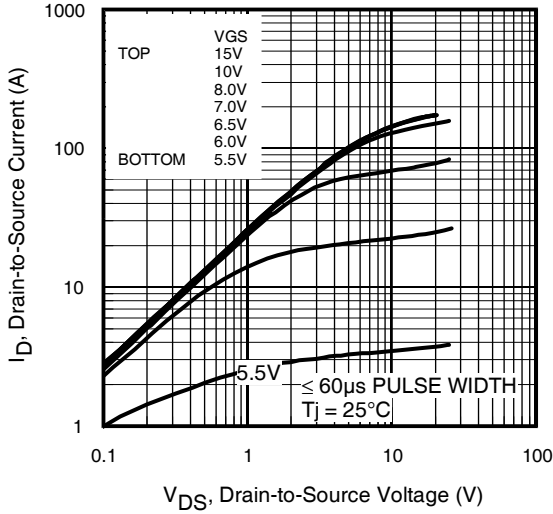


Fig 1. Typical Output Characteristics

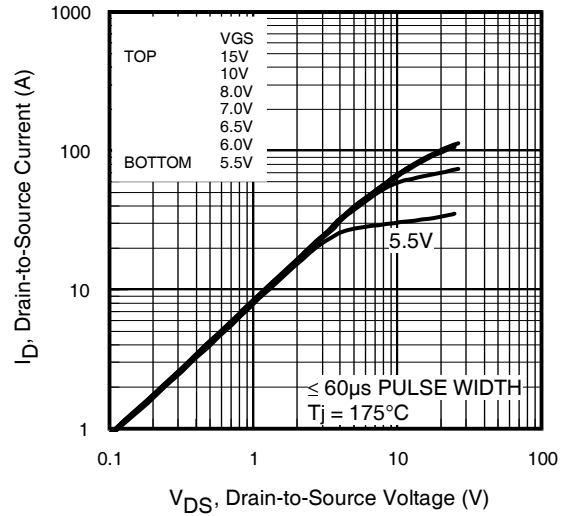


Fig 2. Typical Output Characteristics

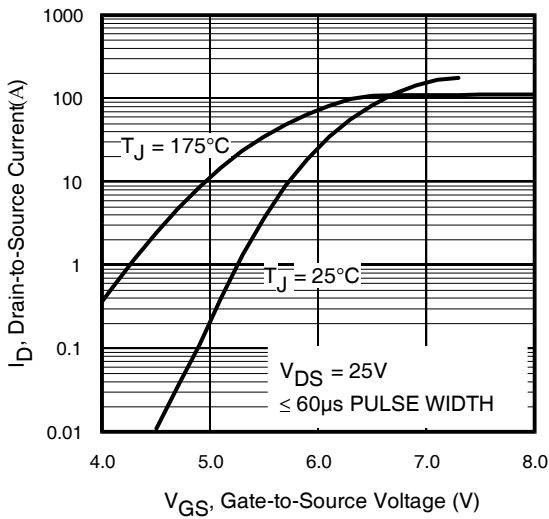


Fig 3. Typical Transfer Characteristics

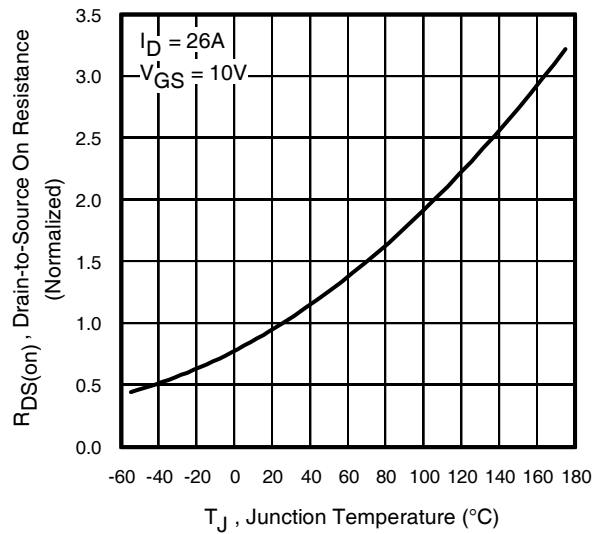


Fig 4. Normalized On-Resistance vs. Temperature

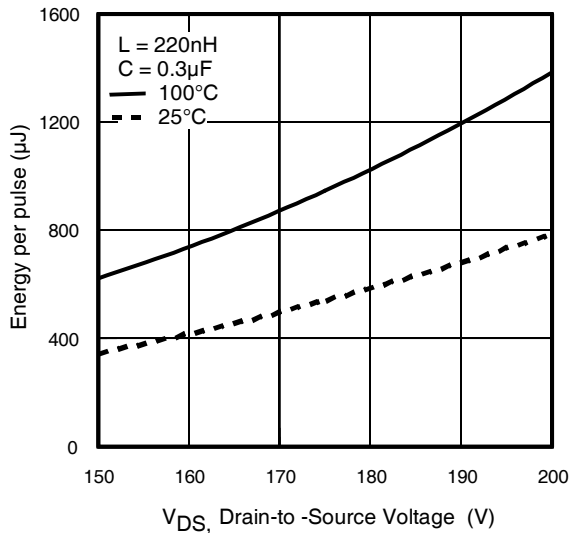


Fig 5. Typical E_{PULSE} vs. Drain-to-Source Voltage

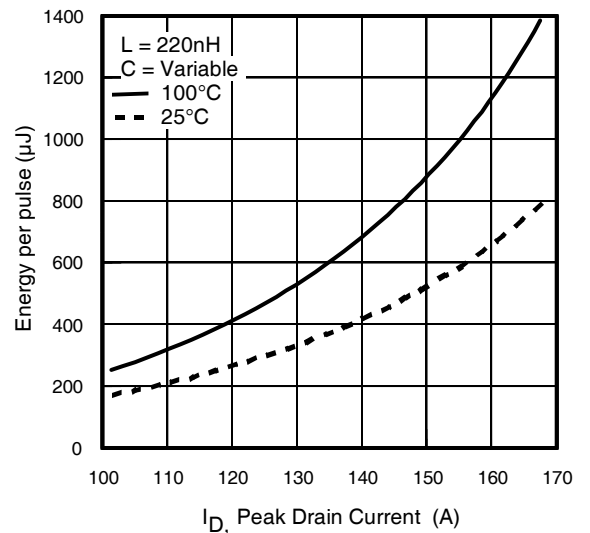


Fig 6. Typical E_{PULSE} vs. Drain Current

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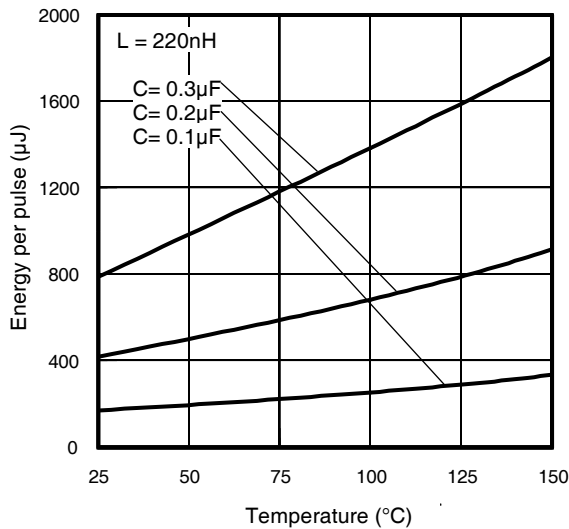


Fig 7. Typical E_{PULSE} vs. Temperature

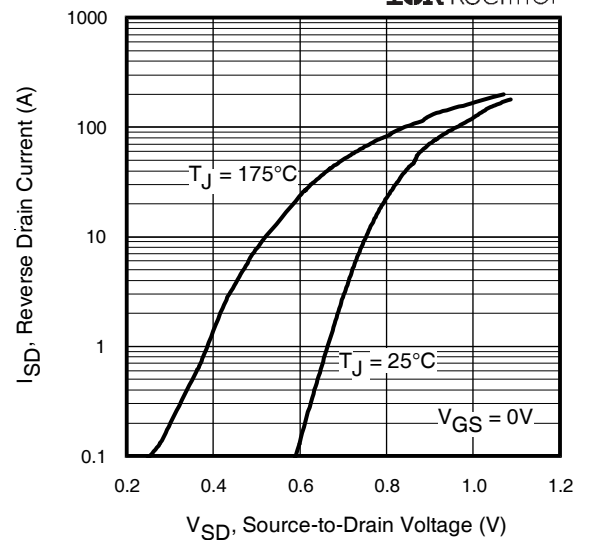


Fig 8. Typical Source-Drain Diode Forward Voltage

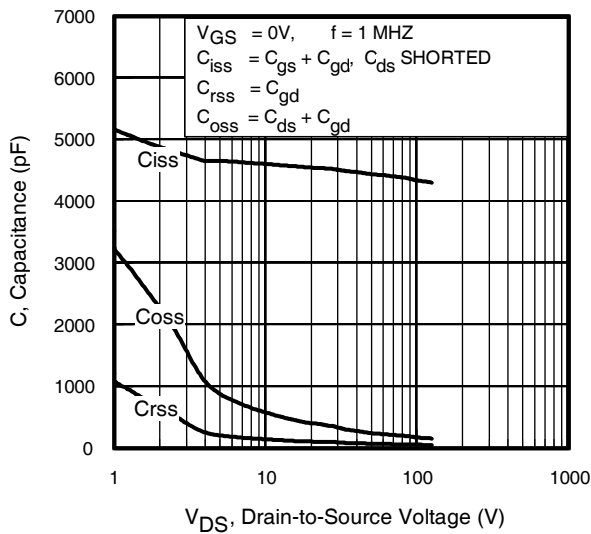


Fig 9. Typical Capacitance vs. Drain-to-Source Voltage

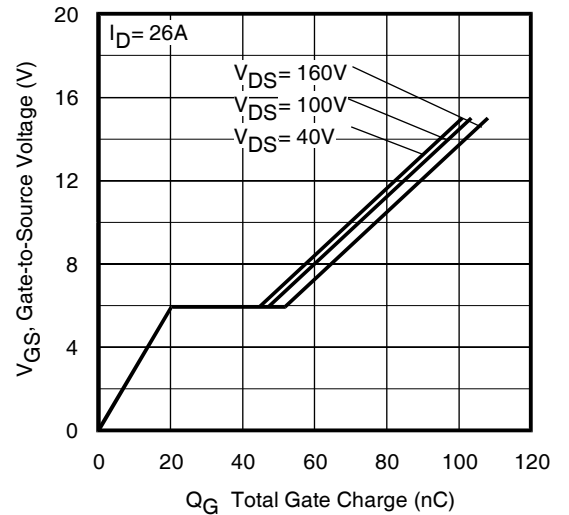


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

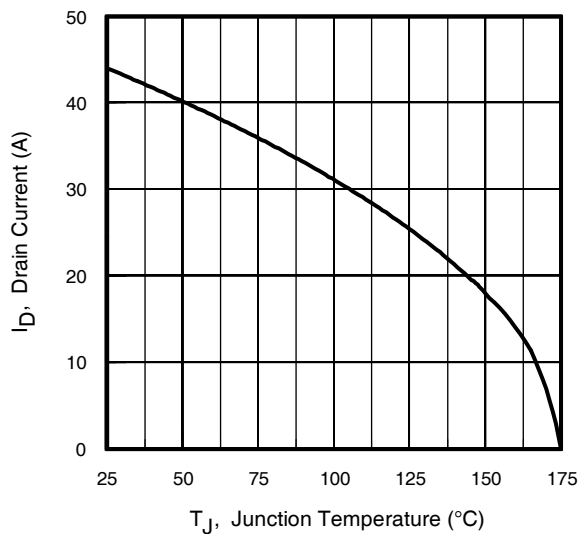


Fig 11. Maximum Drain Current vs. Case Temperature

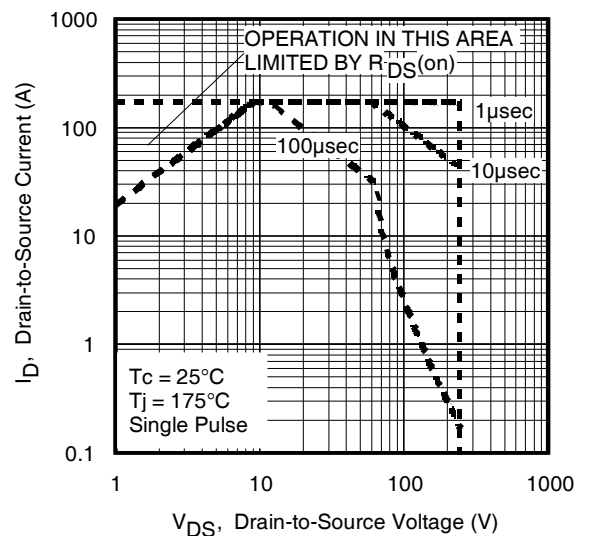


Fig 12. Maximum Safe Operating Area

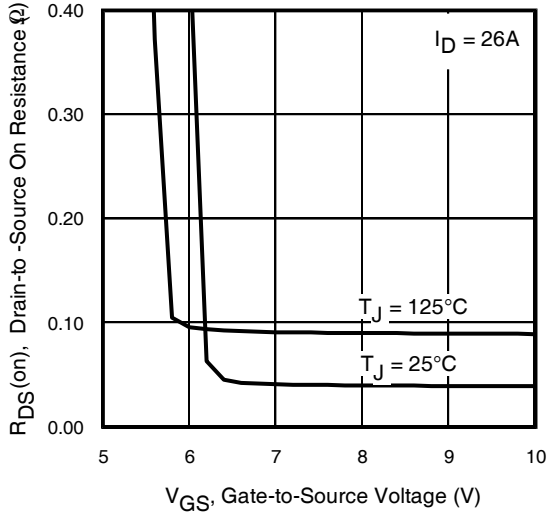


Fig 13. On-Resistance Vs. Gate Voltage

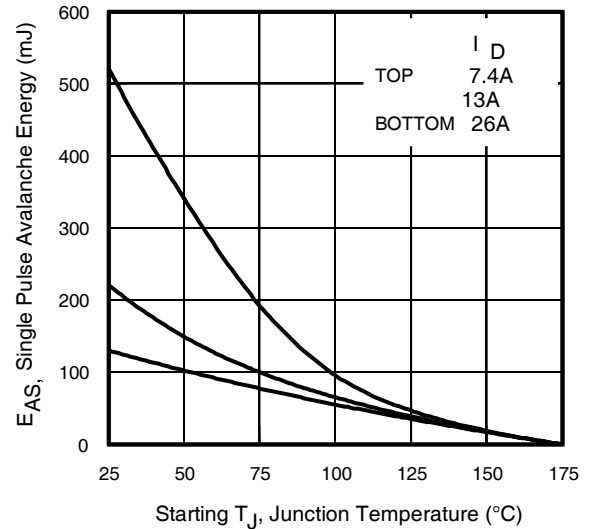


Fig 14. Maximum Avalanche Energy Vs. Temperature

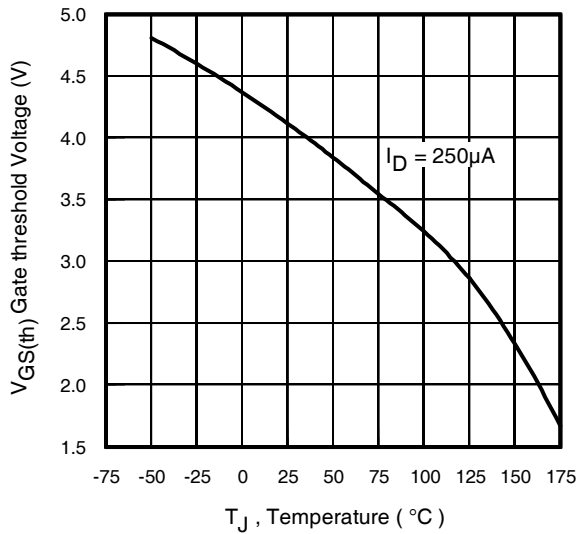


Fig 15. Threshold Voltage vs. Temperature

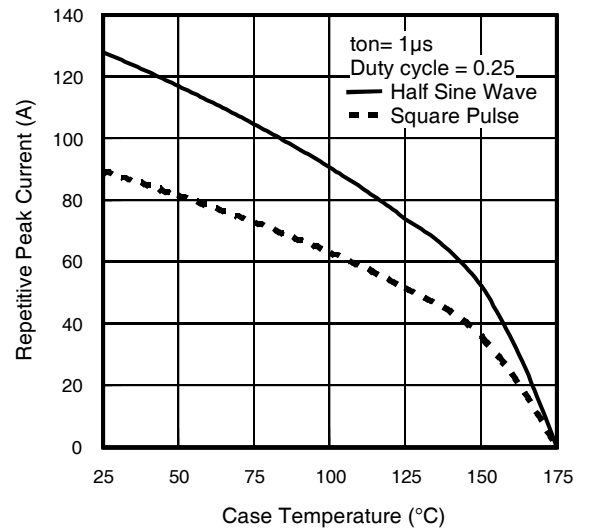


Fig 16. Typical Repetitive peak Current vs. Case temperature

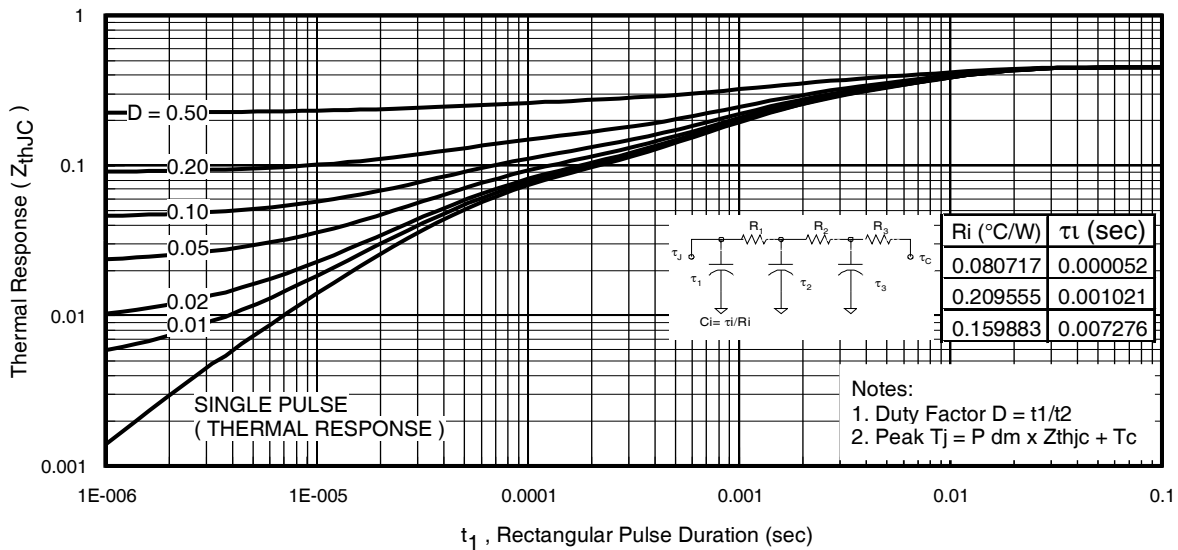


Fig 17. Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs



Fig 19a. Unclamped Inductive Test Circuit

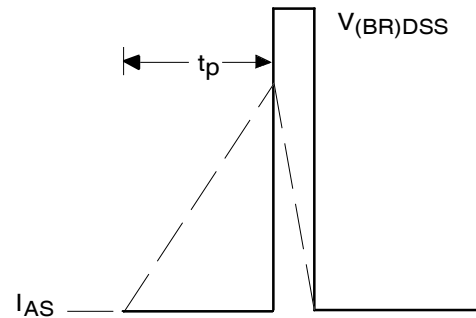


Fig 19b. Unclamped Inductive Waveforms

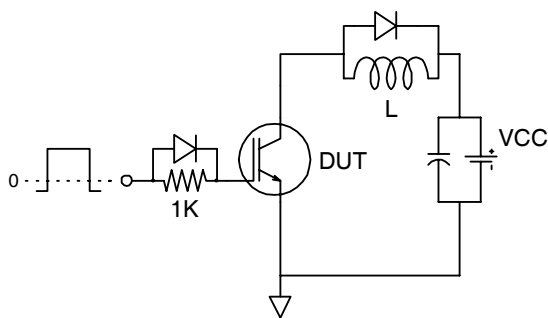


Fig 20a. Gate Charge Test Circuit



Fig 20b. Gate Charge Waveform

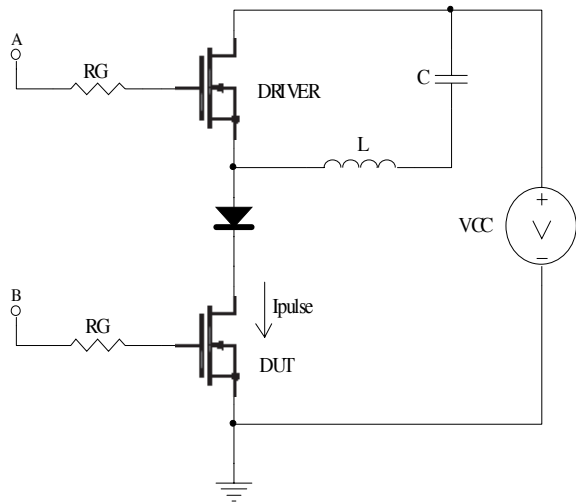


Fig 21a. t_{st} and E_{PULSE} Test Circuit

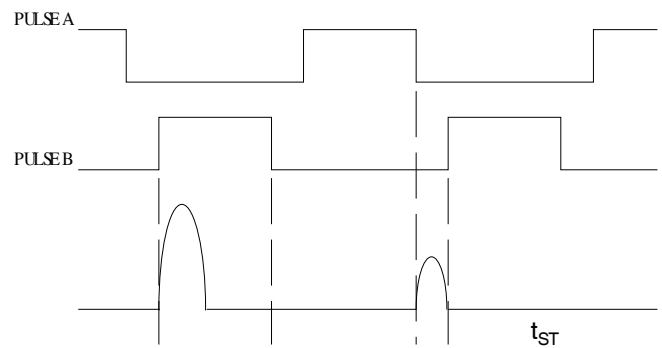


Fig 21b. t_{st} Test Waveforms

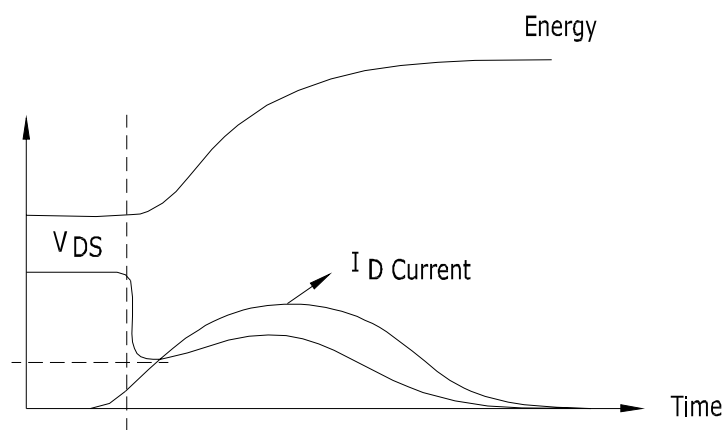


Fig 21c. E_{PULSE} Test Waveforms

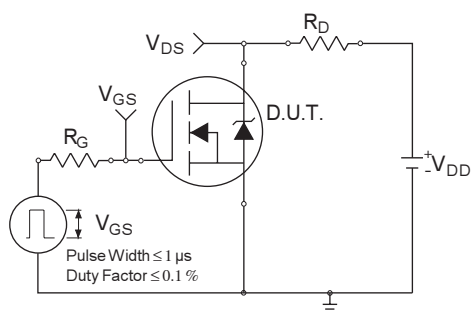


Fig 22a. Switching Time Test Circuit

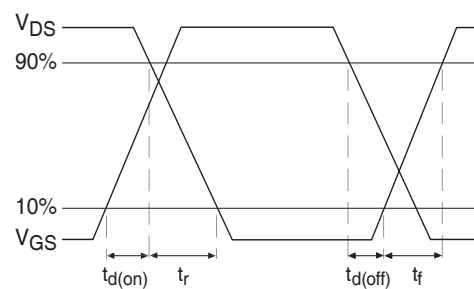
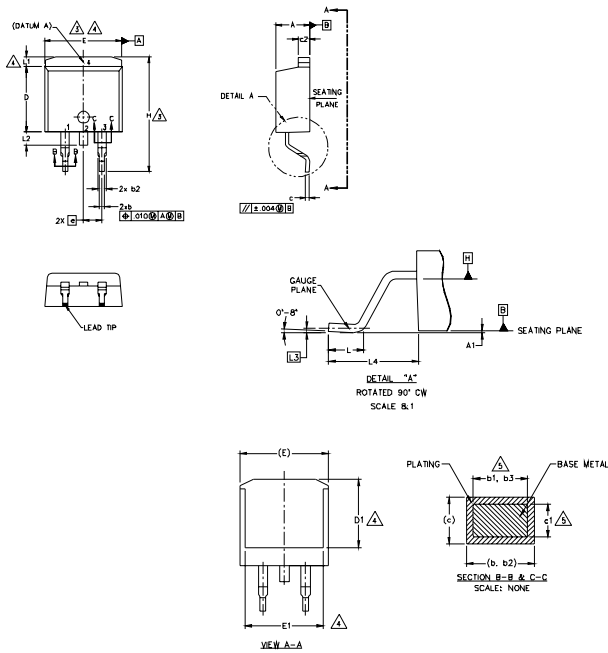


Fig 22b. Switching Time Waveforms

IRFS4229PbF

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54	BSC	.100	BSC	
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	4
L2	—	1.78	—	.070	
L3	0.25	BSC	.010	BSC	
L4	4.78	5.28	.188	.208	

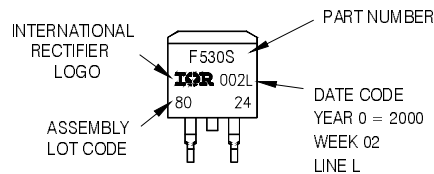
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

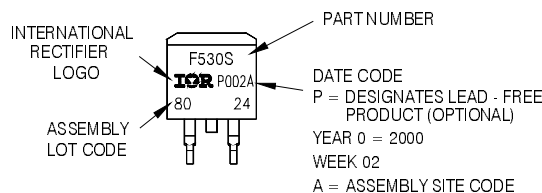
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE 'L'

Note: "P" in assembly line position
indicates "Lead - Free"

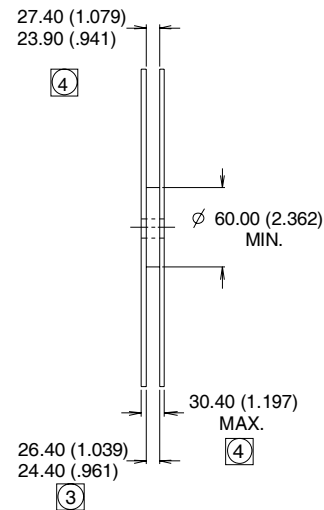
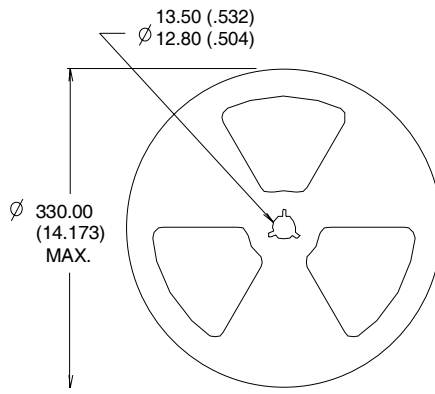
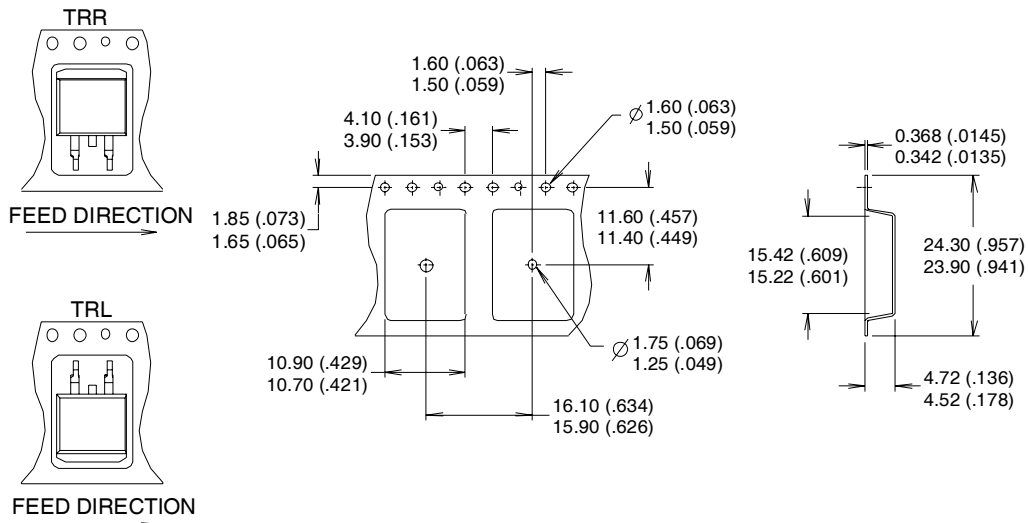


OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

D²Pak Tape & Reel Information



- NOTES :
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.37\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 26\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ Half sine wave with duty cycle = 0.25, $t_{on} = 1\mu\text{sec}$.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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 TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 09/2008

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