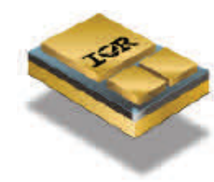
IRL5NJ7404

LOGIC LEVEL POWER MOSFET SURFACE MOUNT (SMD-0.5)

20V, P-CHANNEL



SMD-0.5

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRL5NJ7404	-20V	0.04Ω	-11A

Description

IRL5NJ7404 is part of the International Rectifier HiRel family of products. IR HiRel Fifth Generation Power MOSFETs utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provide the designer with an extremely efficient device for use in a wide variety of applications. These devices are well-suitable for applications such as switching power supplies, motor established advantages of MOSFETs such as voltage controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

Features

- Logic Level Gate Drive
- Low RDS(on)
- Avalanche Energy Ratings
- Dynamic dv/dt Ratings
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Package
- Light Weight
- Surface Mount

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-11	A
I_D @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-7.0	
I_{DM}	Pulsed Drain Current ①	-44	
P_D @ T_C = 25°C	Maximum Power Dissipation	50	W
	Linear Derating Factor	0.4	W/°C
V_{GS}	Gate-to-Source Voltage	±12	V
E_{AS}	Single Pulse Avalanche Energy ②	157	mJ
I_{AR}	Avalanche Current ①	-11	A
E_{AR}	Repetitive Avalanche Energy ①	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-0.7	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-20	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.14	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.04	Ω	V_{GS} = -4.5V, I_D = -11A ④
		—	—	0.07		V_{GS} = -2.7V, I_D = -7.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	-0.7	—	—	V	V_{DS} = V_{GS}, I_D = -250μA
Gfs	Forward Transconductance	9.0	—	—	S	V_{DS} = -15V, I_D = -3.2A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V_{DS} = -16V, V_{GS} = 0V
		—	—	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -12V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 12V
Q_G	Total Gate Charge	—	—	50	nC	I_D = -3.2A
Q_{GS}	Gate-to-Source Charge	—	—	5.5		V_{DS} = -16V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	21		V_{GS} = -4.5V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = -10V
tr	Rise Time	—	—	150		I_D = -3.2A
$t_{d(off)}$	Turn-Off Delay Time	—	—	72		R_G = 6.0Ω
t_f	Fall Time	—	—	90		V_{GS} = -4.5V
Ls +L_D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	1450	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	830	—		V_{DS} = -15V
C_{rss}	Reverse Transfer Capacitance	—	430	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-11	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-1.0	V	T_J=25°C, I_S=-3.2A, V_{GS}=0V④
t_{rr}	Reverse Recovery Time	—	—	80	ns	T_J=25°C, I_F= -3.2A, $V_{DD} \leq$ -20V
Q_{rr}	Reverse Recovery Charge	—	—	100	nC	di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.5	°C/W

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -15V, starting T_J = 25°C, L = 2.6mH, Peak I_L = -11A, V_{GS} = -10V

③ $I_{SD} \leq$ -11A, di/dt $\leq$ -84A/μs, V_{DD} $\leq$ -20V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 μs; Duty Cycle $\leq$ 2%

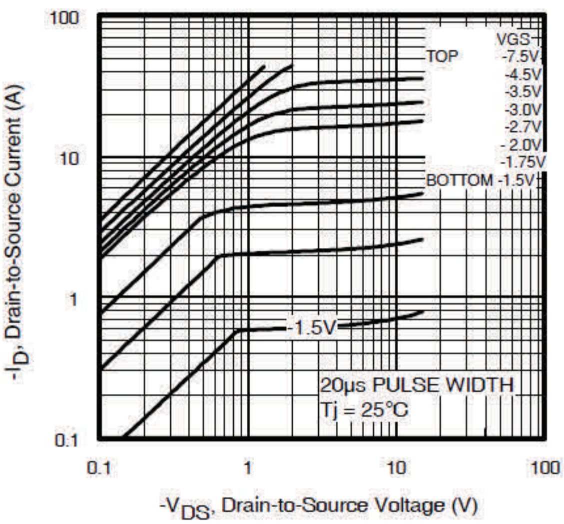


Fig 1. Typical Output Characteristics

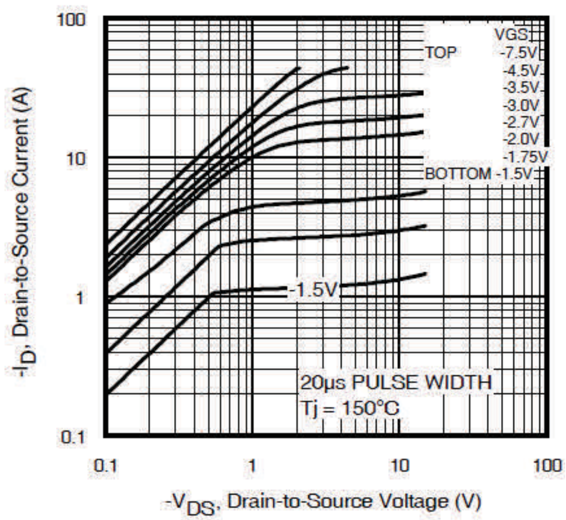


Fig 2. Typical Output Characteristics

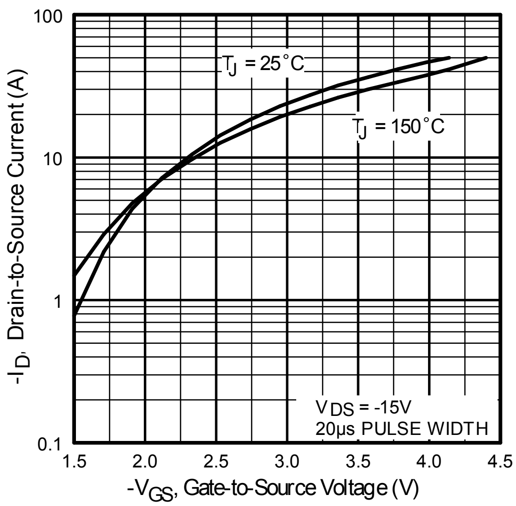


Fig 3. Typical Transfer Characteristics

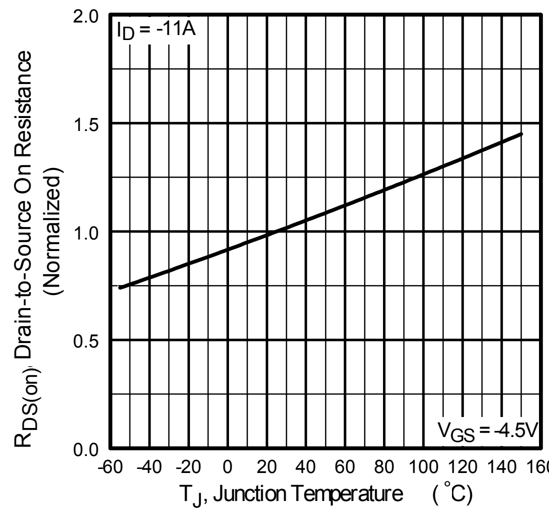


Fig 4. Normalized On-Resistance Vs. Temperature

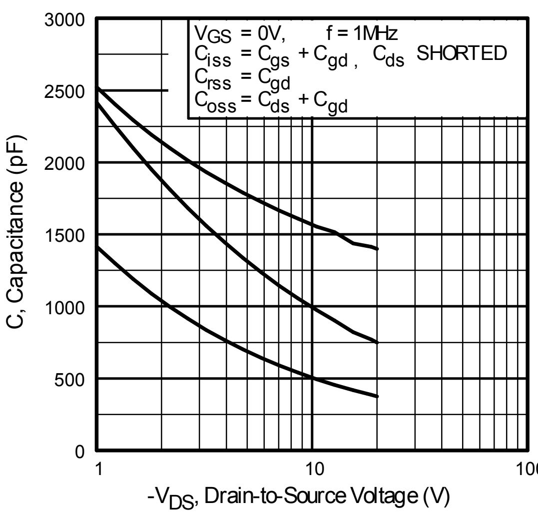


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

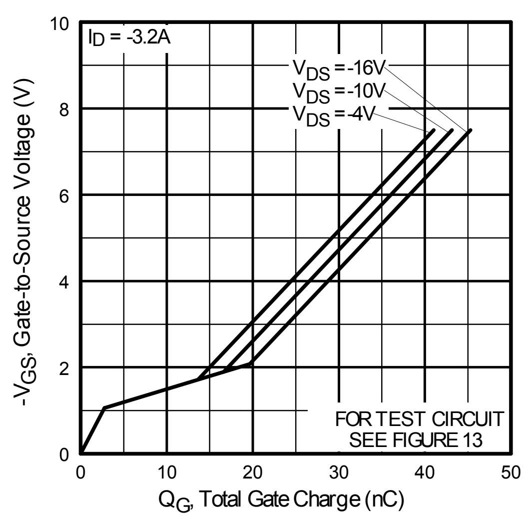


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

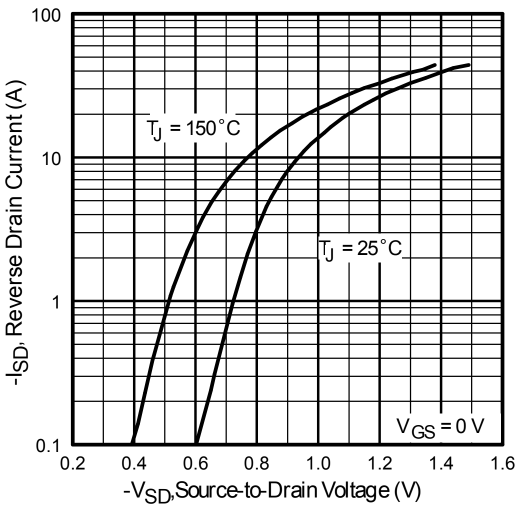


Fig 7. Typical Source-Drain Diode Forward Voltage

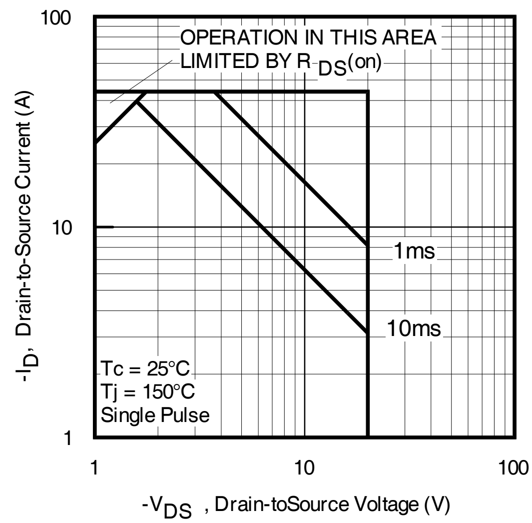


Fig 8. Maximum Safe Operating Area

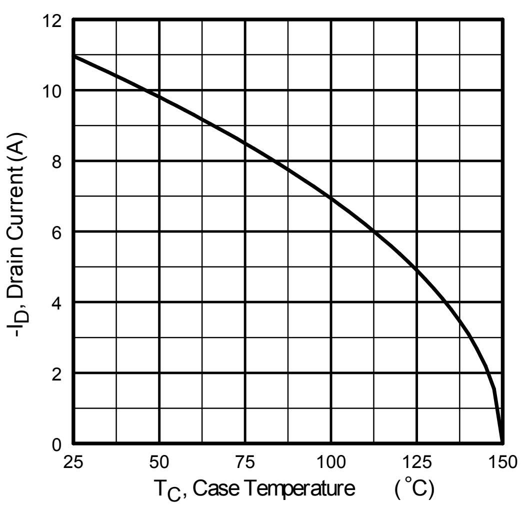


Fig 9. Maximum Drain Current Vs. Case Temperature

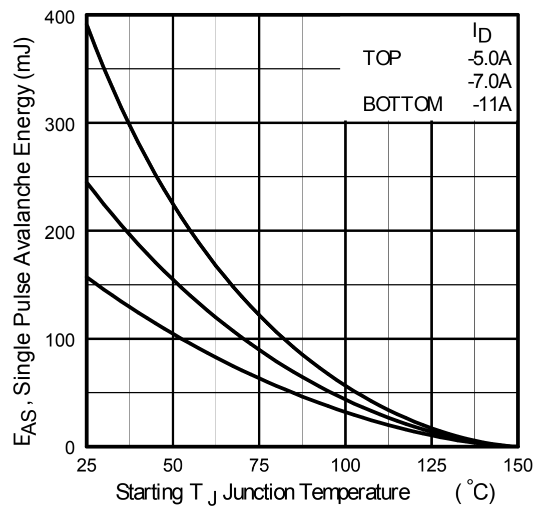


Fig 10. Maximum Avalanche Energy Vs. Drain Current

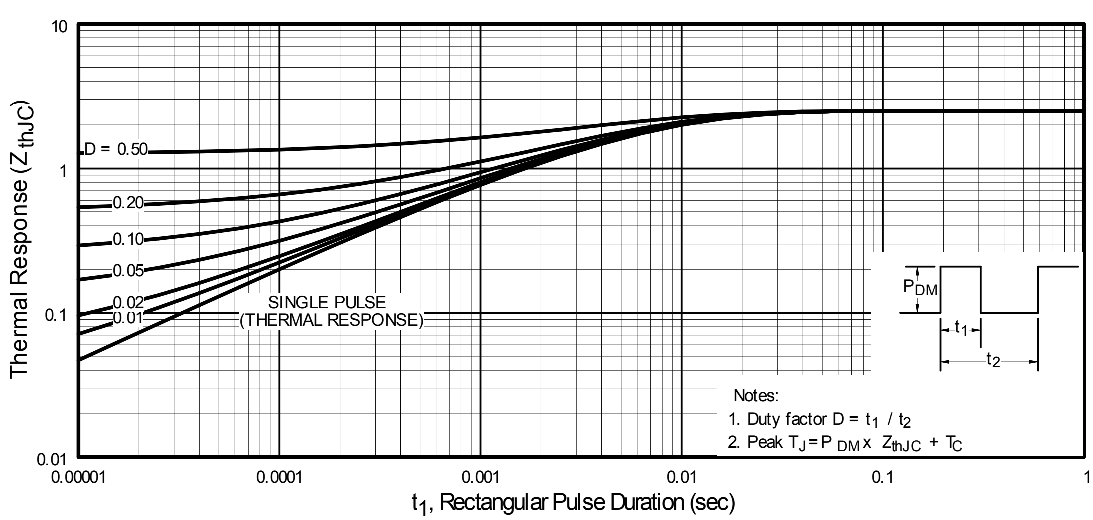


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

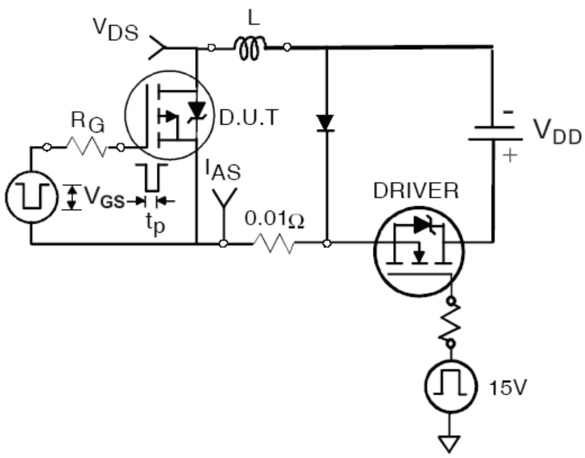


Fig 12a. Unclamped Inductive Test Circuit

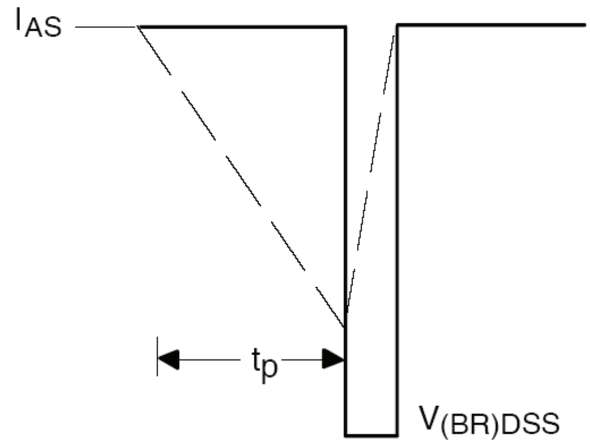


Fig 12b. Unclamped Inductive Waveforms

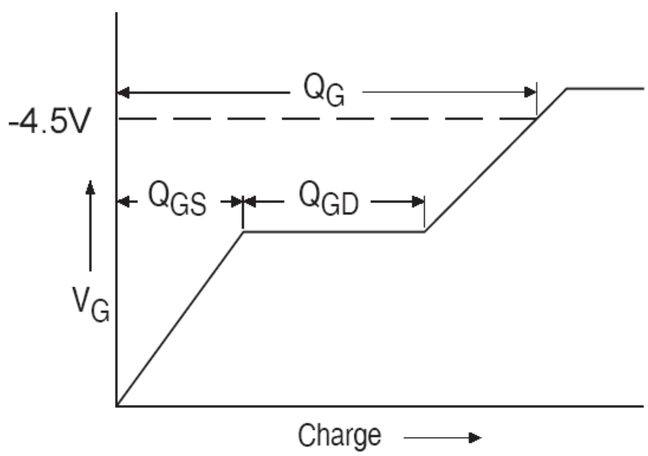


Fig 13a. Basic Gate Charge Waveform

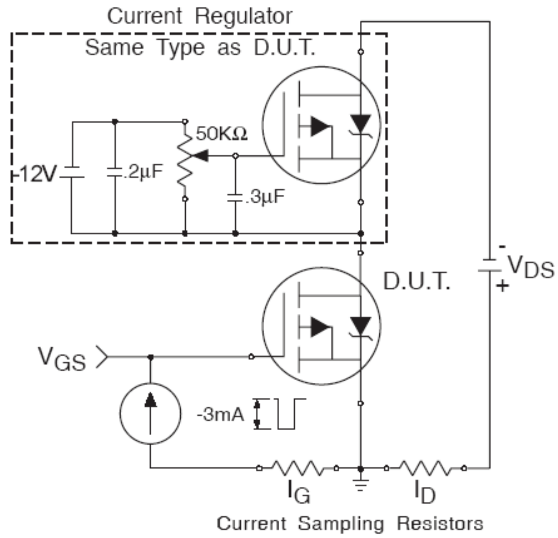


Fig 13b. Gate Charge Test Circuit

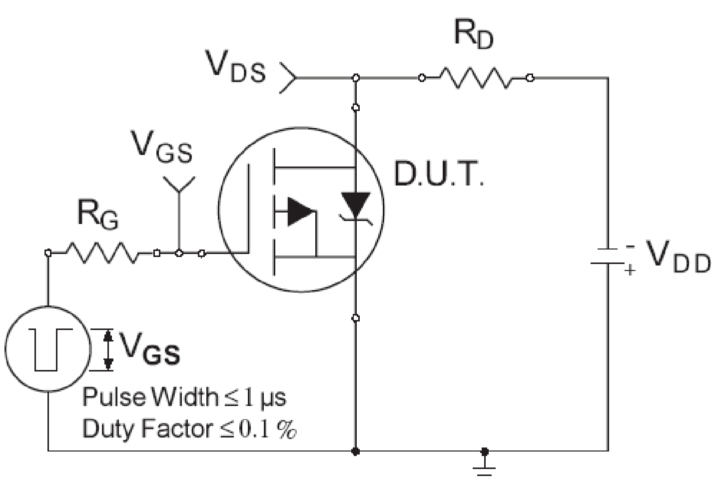


Fig 14a. Switching Time Test Circuit

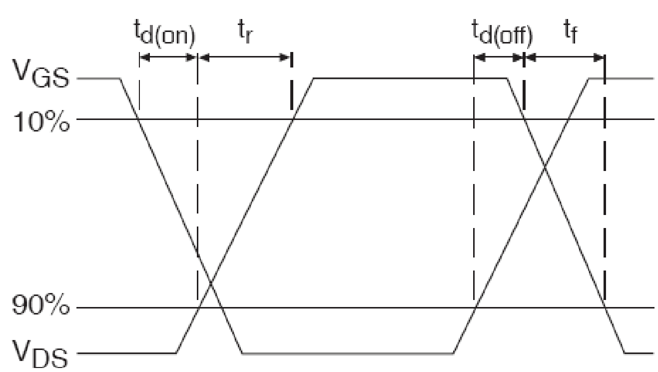
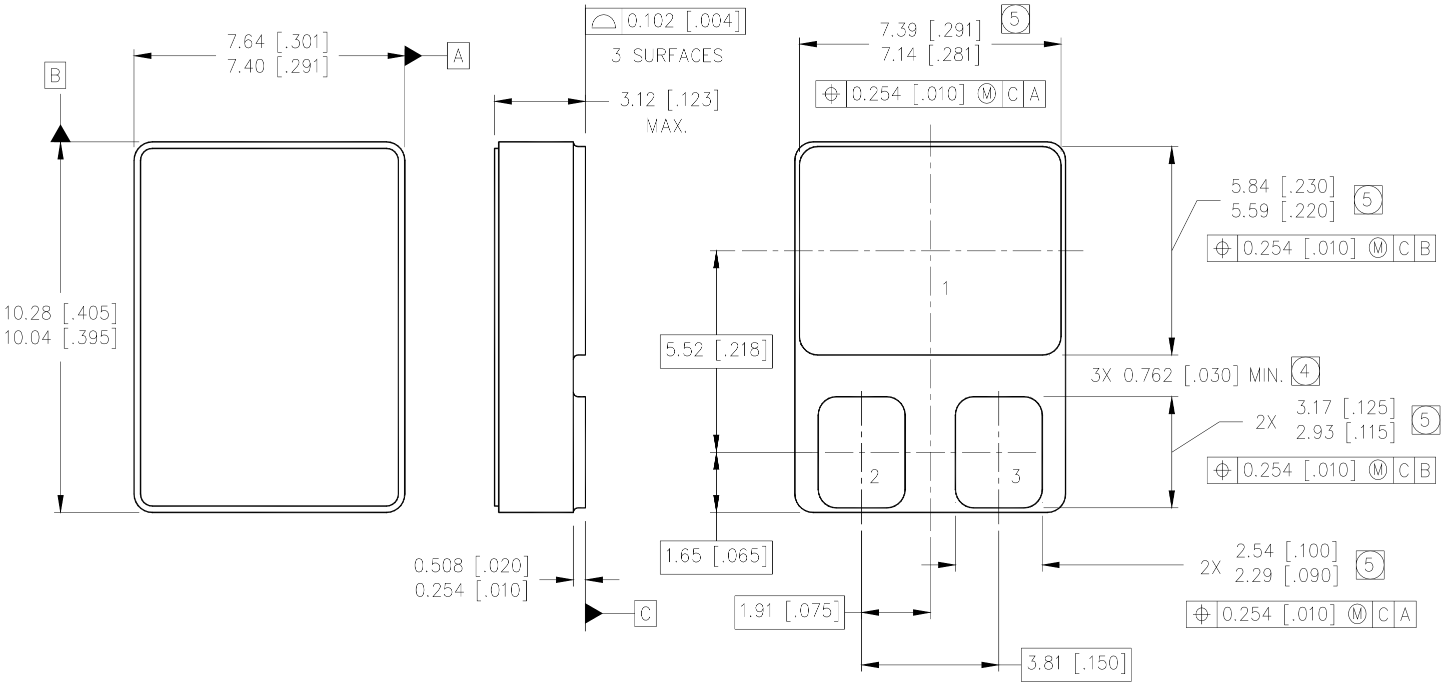


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — SMD-0.5



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

MOSFET

1 = DRAIN
2 = GATE
3 = SOURCE

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