

## MOSFET

### OptiMOS™ 6 Power-Transistor, 150 V

#### Features

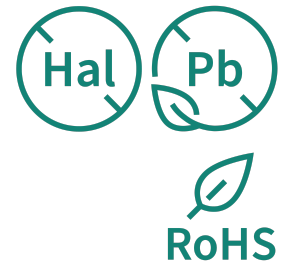
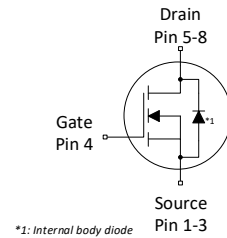
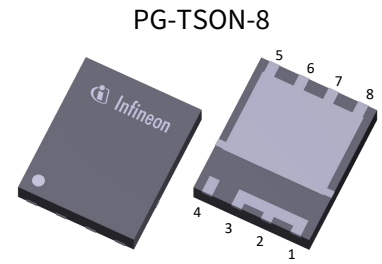
- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- MSL 1 classified according to J-STD-020

#### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	4.4	m $\Omega$
$I_D$	156	A
$Q_{oss}$	163	nC
$Q_G$	55	nC
$Q_{rr}$ (500 A/ $\mu$ s)	137	nC



Type/Ordering Code	Package	Marking	Related Links
ISC044N15NM6	PG-TSON-8	04415N6	-



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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	156 111 103 17.1	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=8\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	624	A	$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	-	-	50	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	1050	mJ	$I_D=15\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	250 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ °C/W}$ <sup>2)</sup>
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	0.59	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>5)</sup>	$R_{thJA}$	-	-	50	°C/W	-

<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.5	4.0	V	$V_{DS}=V_{GS}$ , $I_D=140\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.5 3.8 4.3	4.2 4.4 5.1	m $\Omega$	$V_{GS}=15\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=8\text{ V}$ , $I_D=25\text{ A}$
Gate resistance	$R_G$	-	0.86	1.29	$\Omega$	-
Transconductance	$g_{fs}$	48	97	-	S	$ V_{DS}  \geq 2 I_D  R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>6)</sup>	$C_{iss}$	-	3900	5100	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>6)</sup>	$C_{oss}$	-	1200	1600	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>6)</sup>	$C_{riss}$	-	16	24	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	7	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	20	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	10	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

<sup>6)</sup> Defined by design. Not subject to production test.

**Table 6 Gate charge characteristics** <sup>7)</sup>

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge <sup>8)</sup>	$Q_{gs}$	-	21	27	nC	$V_{DD}=75\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	13.6	-	nC	$V_{DD}=75\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>8)</sup>	$Q_{gd}$	-	12.5	18.8	nC	$V_{DD}=75\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	19.5	-	nC	$V_{DD}=75\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>8)</sup>	$Q_g$	-	55	72	nC	$V_{DD}=75\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=75\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	46	-	nC	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>8)</sup>	$Q_{oss}$	-	163	212	nC	$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}$

<sup>7)</sup> See "Gate charge waveforms" for parameter definition

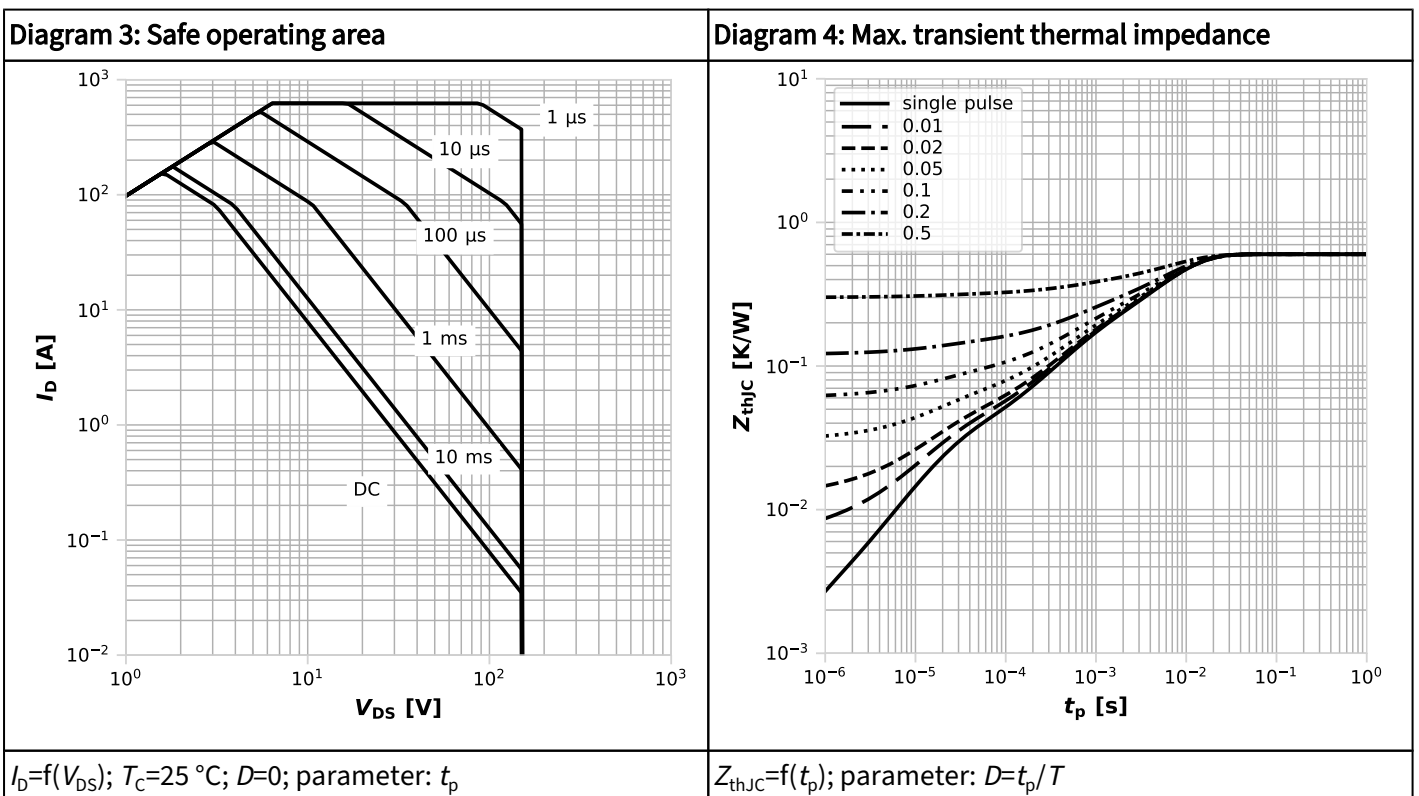
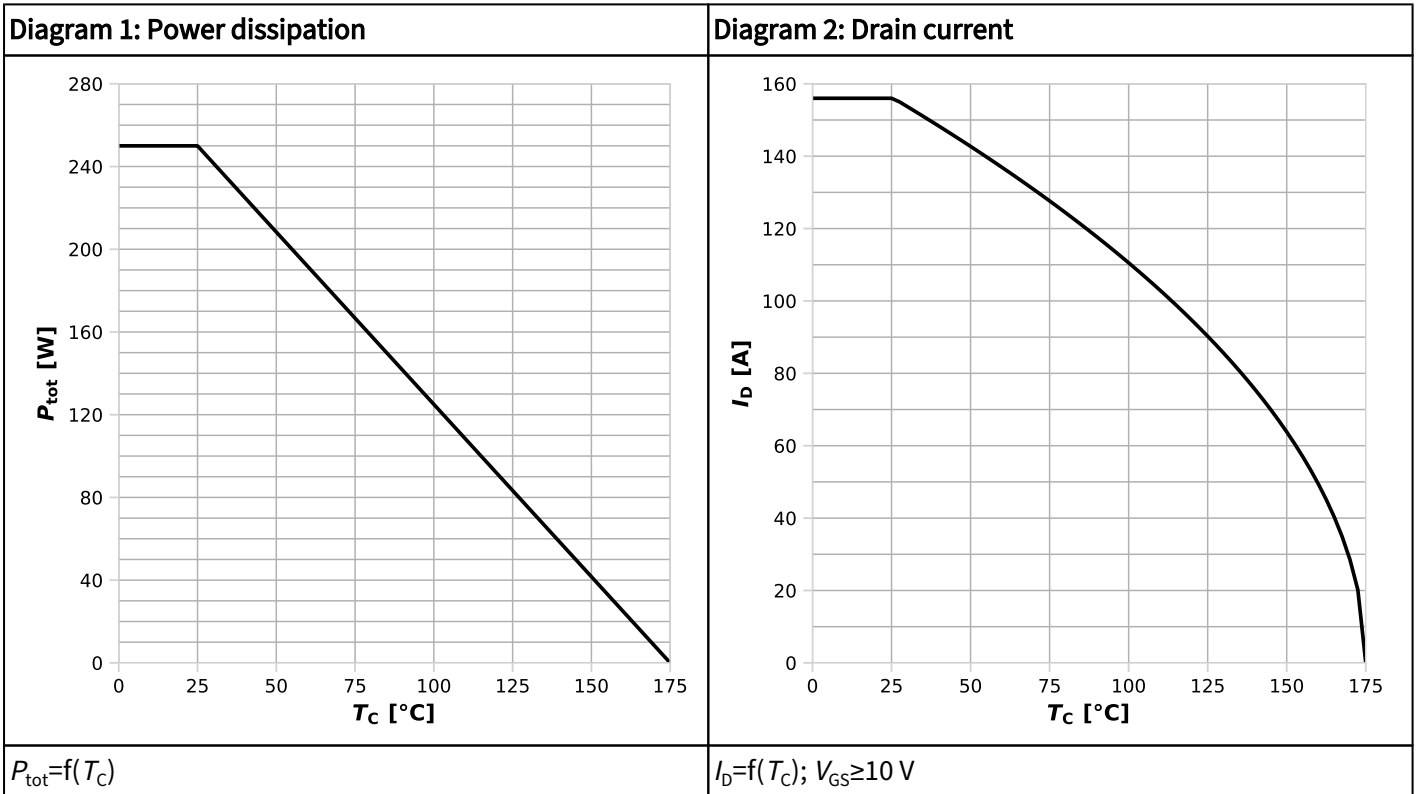
<sup>8)</sup> Defined by design. Not subject to production test.

**Table 7 Reverse diode**

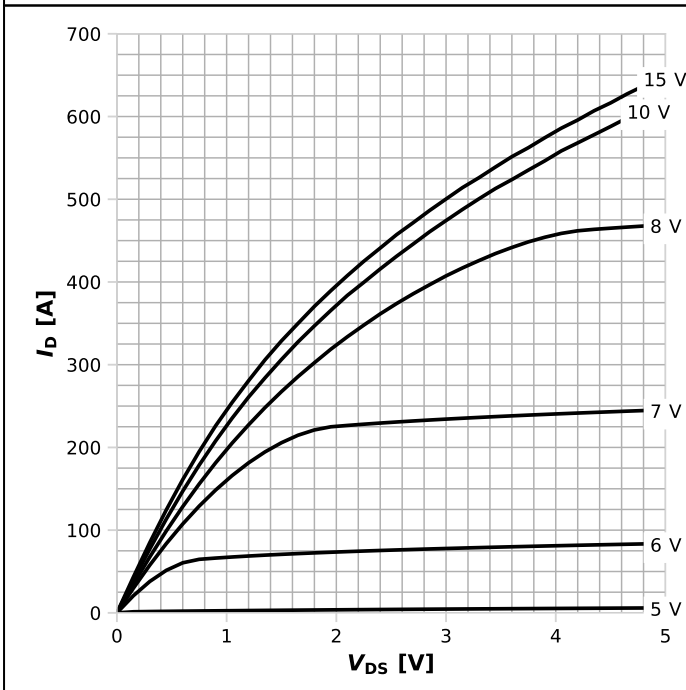
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	156	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	624	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.83	1.0	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>9)</sup>	$t_{rr}$	-	33	66	ns	$V_R=75\text{ V}, I_F=25\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	-	137	274	nC	$V_R=75\text{ V}, I_F=25\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery time <sup>9)</sup>	$t_{rr}$	-	29	58	ns	$V_R=75\text{ V}, I_F=25\text{ A}, di_F/dt=1000\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>9)</sup>	$Q_{rr}$	-	274	548	nC	$V_R=75\text{ V}, I_F=25\text{ A}, di_F/dt=1000\text{ A}/\mu\text{s}$

<sup>9)</sup> Defined by design. Not subject to production test.

## 4 Electrical characteristics diagrams

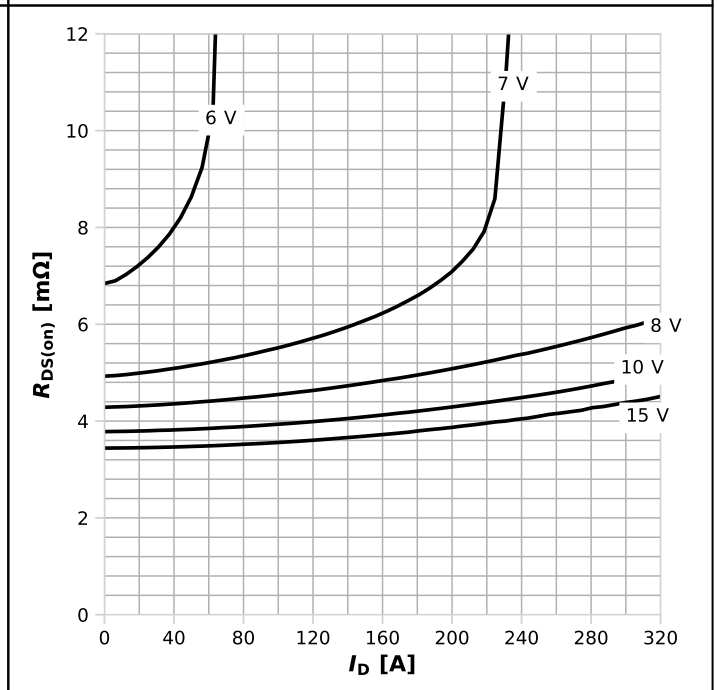


**Diagram 5: Typ. output characteristics**



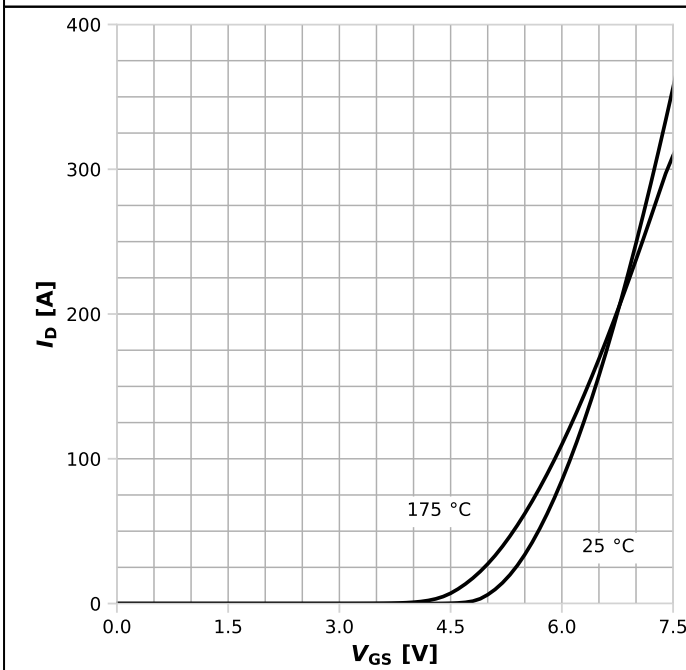
$I_D = f(V_{DS}), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



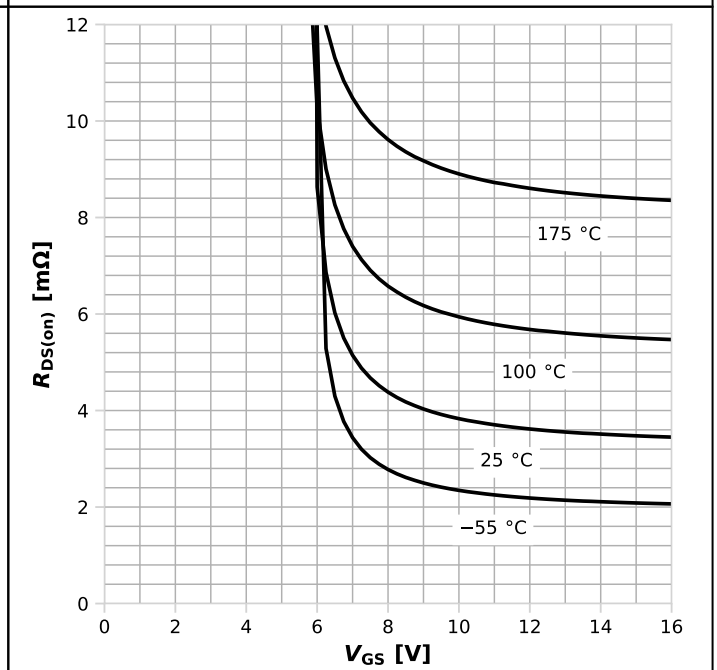
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



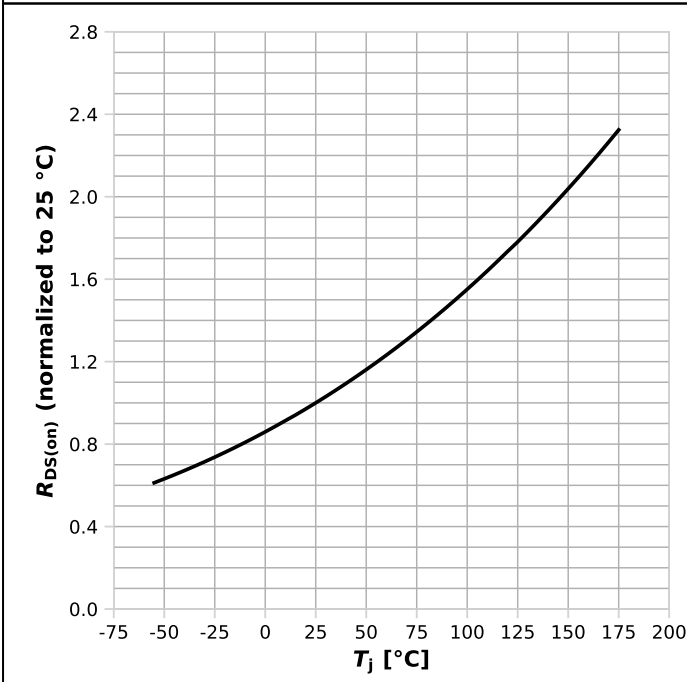
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



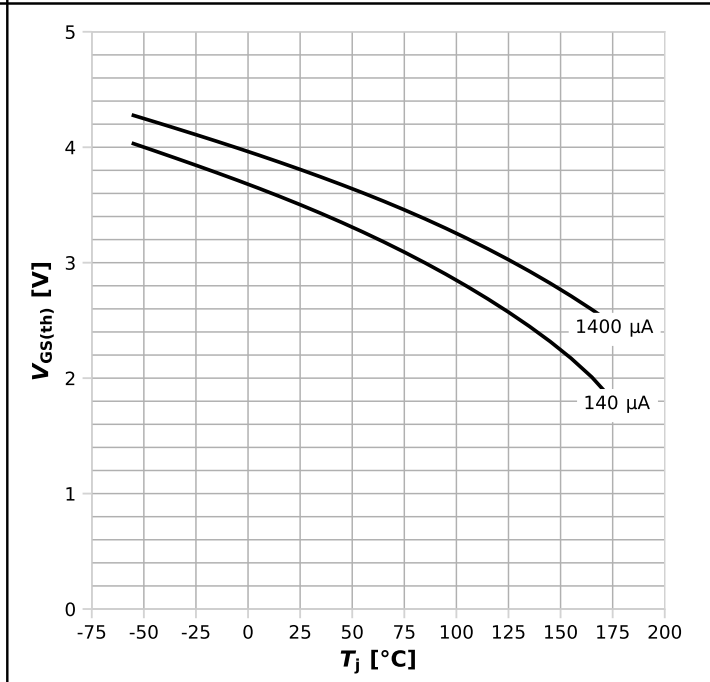
$R_{DS(on)} = f(V_{GS}), I_D = 50\text{ A};$  parameter:  $T_j$

**Diagram 9: Normalized drain-source on resistance**



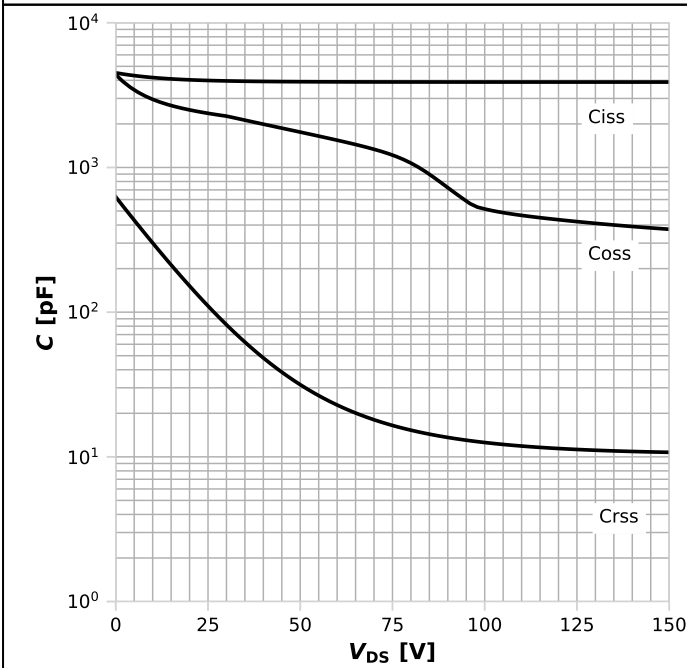
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

**Diagram 10: Typ. gate threshold voltage**



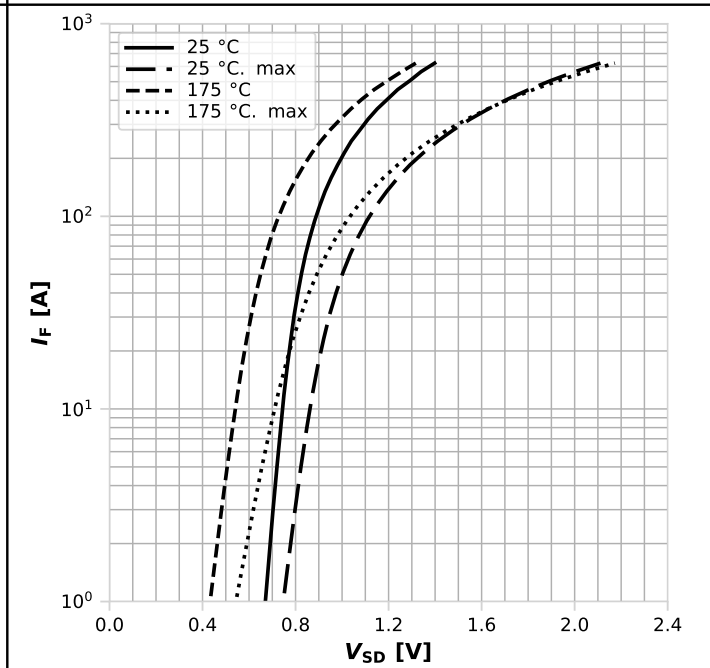
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS}; \text{parameter: } I_D$

**Diagram 11: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

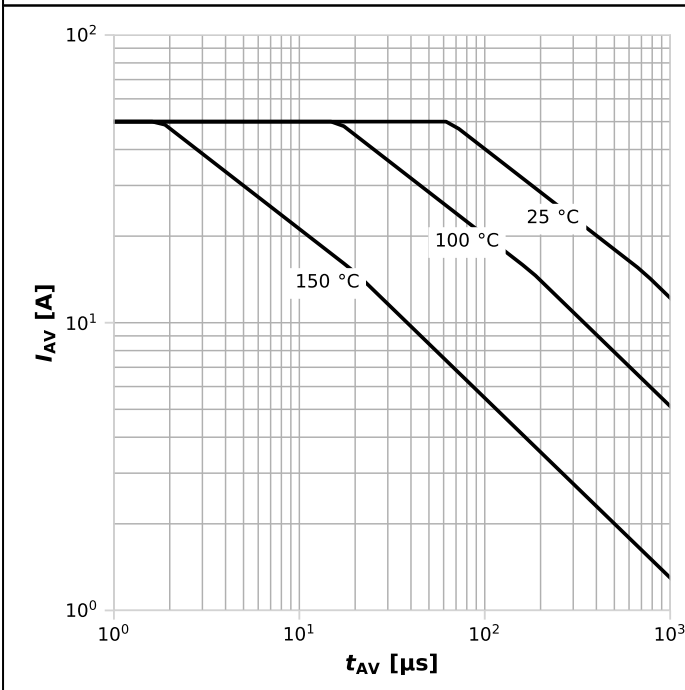
**Diagram 12: Forward characteristics of reverse diode**



$I_F=f(V_{SD}); \text{parameter: } T_j$

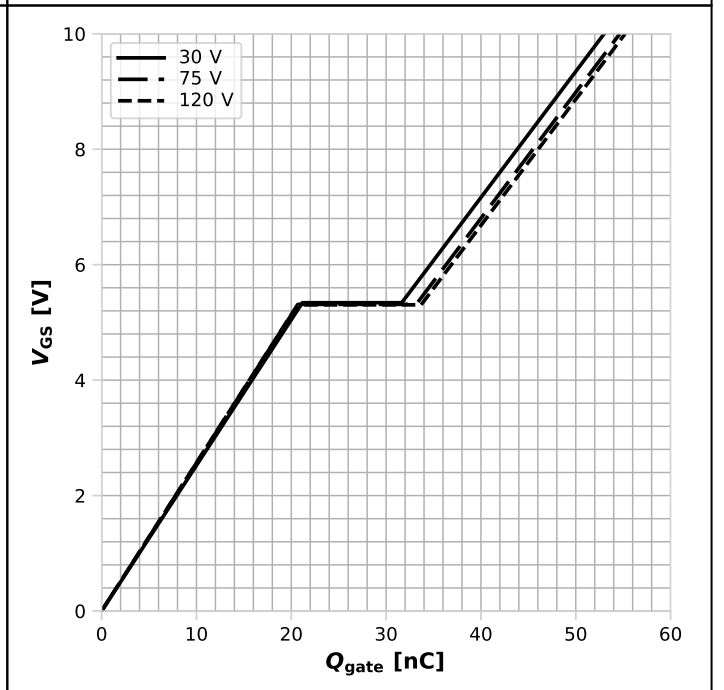


**Diagram 13: Avalanche characteristics**



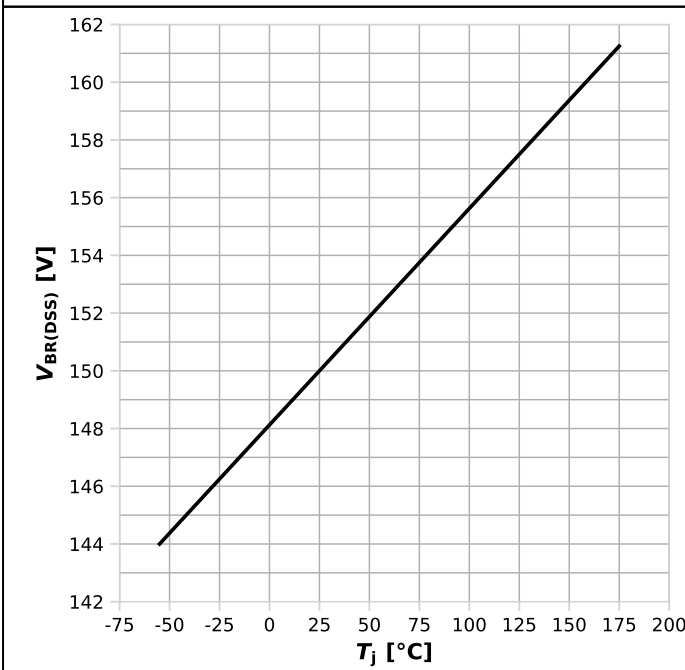
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



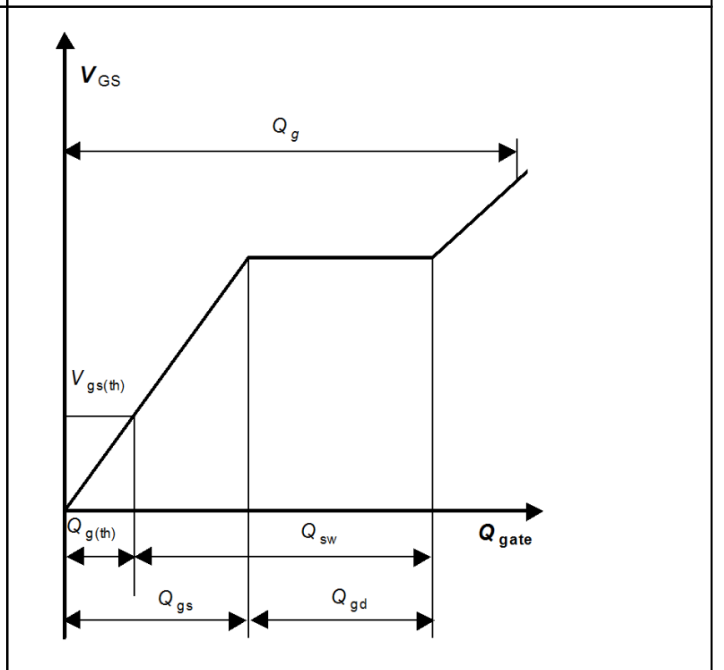
$V_{GS}=f(Q_{gate}), I_D=25 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

**Diagram 15: Min. drain-source breakdown voltage**



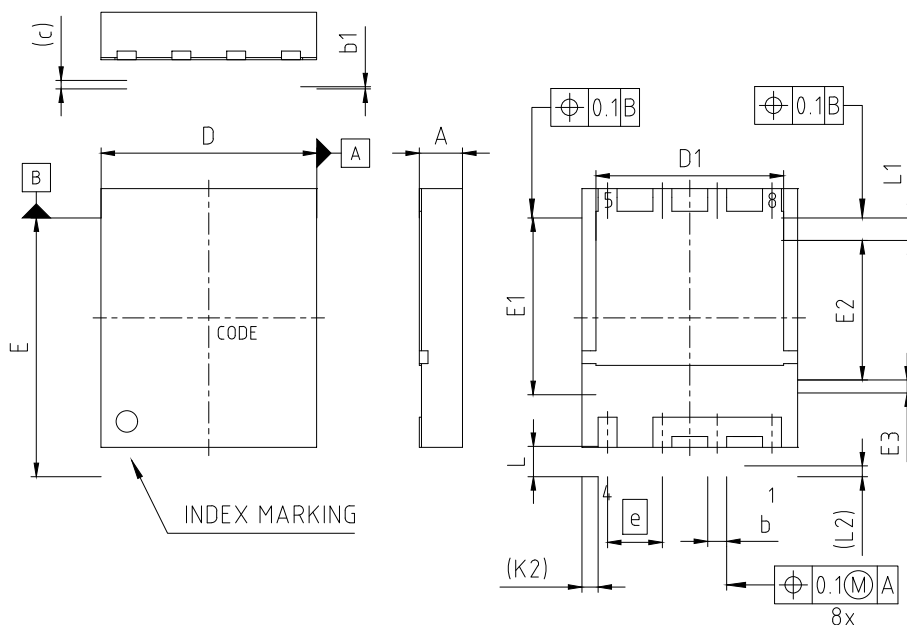
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Gate charge waveforms**



-

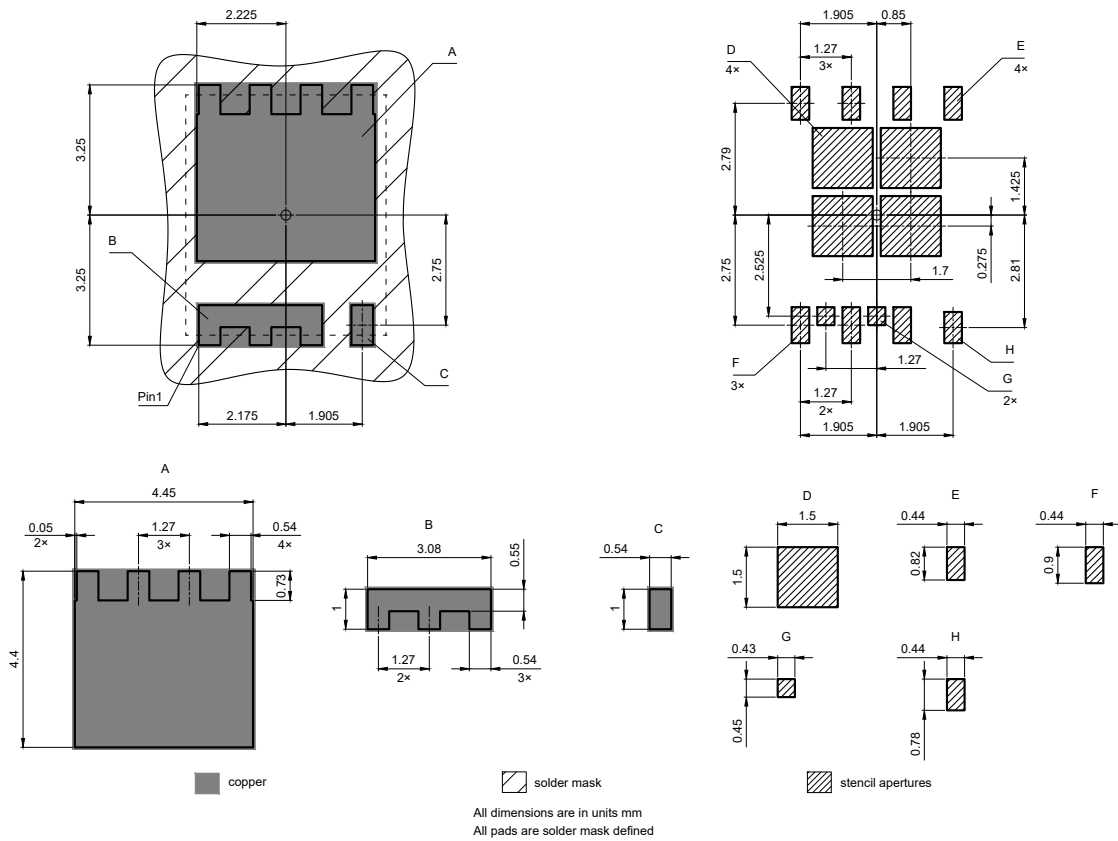
## 5 Package Outlines



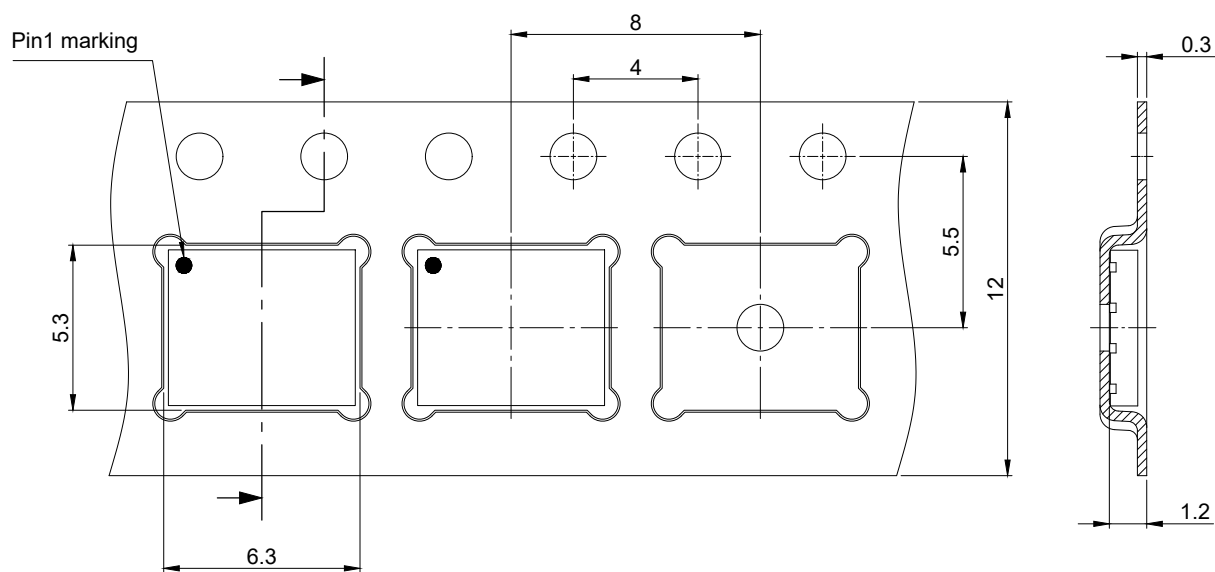
PACKAGE - GROUP NUMBER:		PG-TSON-8-U05	
DIMENSION	MILLIMETERS		
	MIN.	MAX.	
A	0.90	1.10	
b	0.34	0.54	
b1	0.00	0.05	
c	0.20		
D	4.90	5.10	
D1	4.25	4.45	
E	5.90	6.10	
E1	4.00	4.20	
E2	3.14	3.34	
E3	0.20	0.40	
e	1.27		
K2	0.38		
L	0.60	0.80	
L1	0.43	0.63	
L2	0.25		

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

**Figure 1** Outline PG-TSON-8, dimensions in mm



**Figure 2 Outline PG-TSON-8, dimensions in mm**



All dimensions are in units mm  
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

**Figure 3** Outline PG-TSON-8, dimensions in mm

## Revision History

ISC044N15NM6

### Revision 2024-04-24, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-03-15	Release of preliminary version
2.0	2024-04-24	Release of final

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