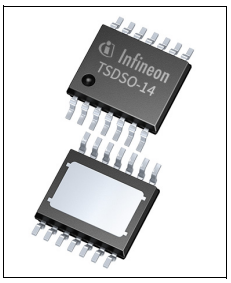
Industrial PROFET™

ITS4035S-EP-D
35 mΩ single channel smart high-side power switch

RoHS



1 Overview

Features

- Single channel smart high-side power switch with integrated protection and diagnosis
- Maximum $R_{DS(ON)}$ 35 mΩ at T_j = 25°C
- Supply voltage tolerance up to 45 V
- User adjustable current limitation ranging from: 3 A to 13.2 A
- Wide output current range
- Open load diagnosis
- 24 V control inputs compatible to 3.3 V and 5 V logic levels
- 4 kV electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Very small, thermally enhanced TSDSO-14 package
- Product validation according to JEDEC standard “JESD47J”
- Green product (RoHS compliant)

Potential applications

- Digital output modules (PLC applications, factory automation)
- Industrial peripheral switches and power distribution
- Switching resistive, inductive and capacitive loads in industrial environments
- Replacement for electromechanical relays, fuses and discrete circuits
- Most suitable for loads that require a flexible but precise current limit

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47J.

Description

The ITS4035S-EP-D is a single channel smart high side switch providing diagnosis capabilities and enhanced protection functions. The device offers an adjustable current limitation to offer higher reliability for protecting the system. It provides enhanced diagnostic features including a separated status pin for sensing fault conditions. The ITS4035S-EP-D is designed to switch resistive, inductive or capacitive loads in the industrial application. The high voltage IN and DEN pins, can directly be interfaced with an optocoupler.

Diagnostic functions

- Short circuit to ground (overload) indication
- Open load detection in OFF
- Overtemperature switch off indication
- Stable diagnostic signal during short circuit and overtemperature shutdown

Protection Functions

- Overvoltage protection
- User adjustable overload- and short circuit protection
- Stable behavior during undervoltage
- Overtemperature protection with restart after cooling down phase
- Reverse polarity / inverse current protection with external components
- Loss of ground protection

The qualification of this product is based on JEDEC JESD47J and may reference to existing qualification results of similar products. Such referring is justified by the structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive and/or transportation applications. Infineon Technologies administrates a comprehensive quality management system according to the latest version of the ISO9001 and IATF 16949.

The most updated certificates of the ISO9001 and IATF 16949 are available at **www.infineon.com/cms/en/product/technology/quality/**

Type	Package	Marking
ITS4035S-EP-D	PG-TSDSO-14	IT4035SD

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2 Block diagram

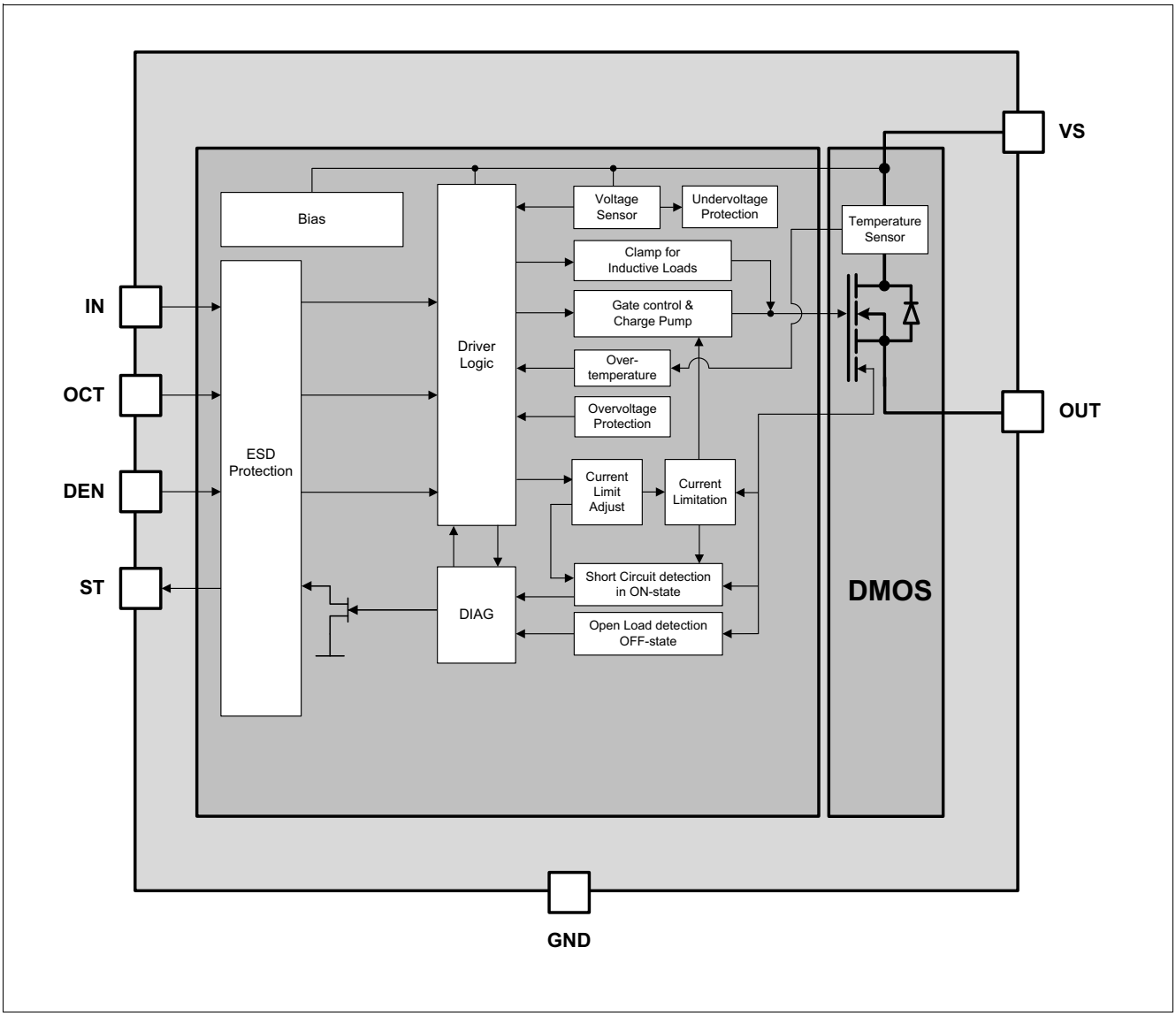


Figure 1 Block diagram ITS4035S-EP-D

3 Pin configuration

3.1 Pin assignment ITS4035S-EP-D (PG-TSDSO-14)

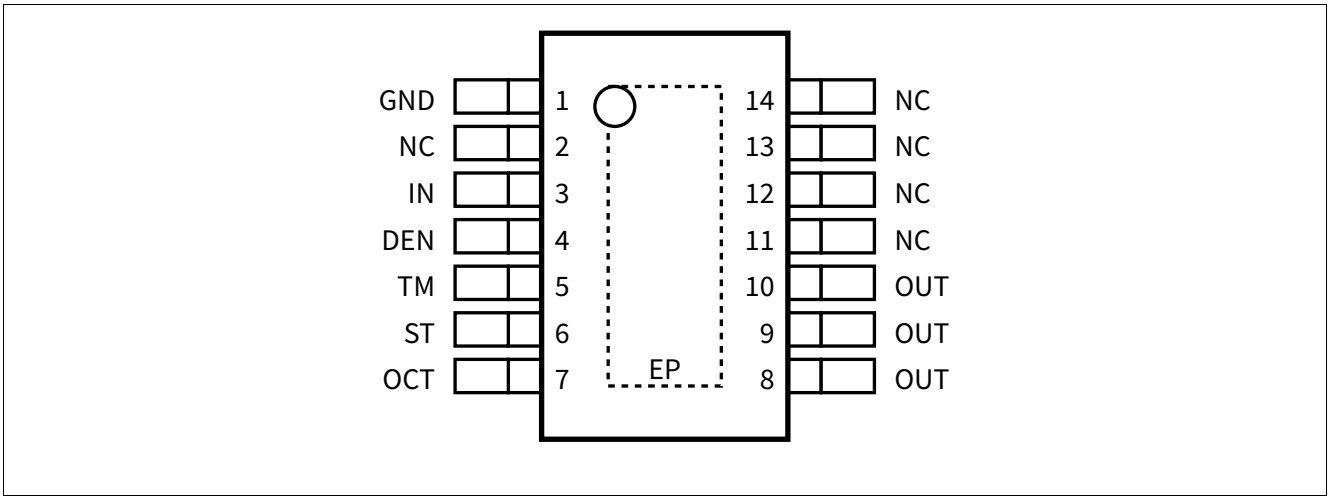


Figure 2 Pin configuration PG-TSDSO-14

3.2 Pin definitions and functions ITS4035S-EP-D (PG-TSDSO-14)

Pin	Symbol	Function
1	GND	Ground pin
3	IN	**Input Channel Control;** digital input signal for channel activation, active high
4	DEN	**Diagnosis Enable;** digital input signal to enable/disable the extended diagnosis features, active high
5	TM	**Test Mode Entry;** must be connected with a serial resistor to device GND (pin 1) [1]
6	ST	**Status pin;** open drain output to provide digital diagnosis information. Connect ST-pin with external pull-up resistor to high (logic level or V_S)
7	OCT	**Over Current Threshold;** connect pin with an appropriate external resistor to device GND in order to adjust the current limitation threshold to the desired value
8, 9, 10	OUT	**Output;** Protected high side power output channel [2]
2, 11, 12, 13, 14	NC	**Not Connected**
Exposed Pad	VS	**Voltage Supply**

1) The recommended value for this resistor is 2.2 kΩ

2) All three output pins should be connected to each other on the PCB as close as possible to the corresponding pads in order to avoid non-homogeneous current densities on separated traces

3.3 Voltage and current definitions

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

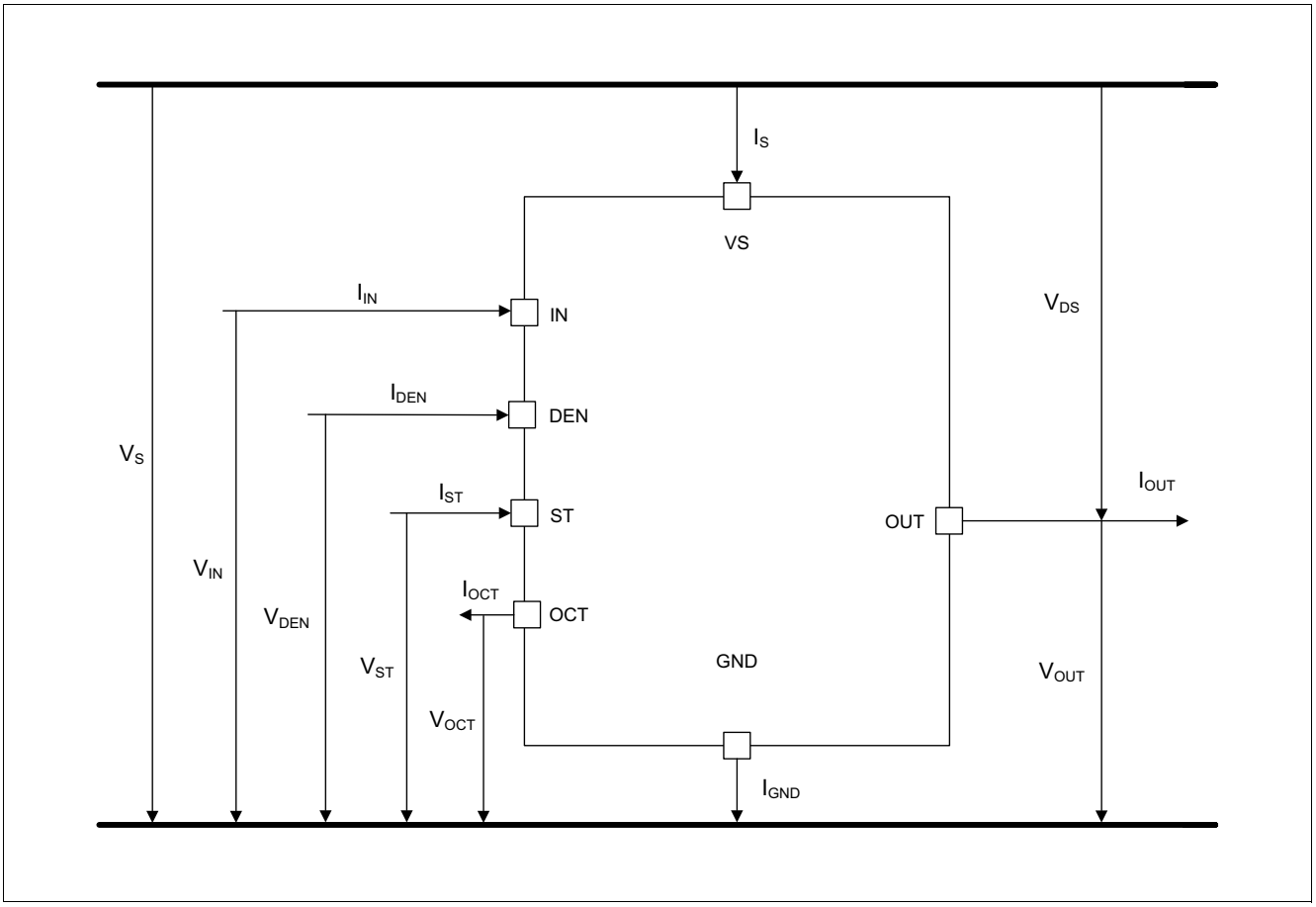


Figure 3 Voltage and current definitions

4 General product characteristics

4.1 Absolute maximum ratings

Table 1 Absolute maximum ratings [1)]

T_j = -40°C to 150°C, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Supply voltage	V_S	-0.3	–	45	V	[2)]	**P_4.1.2**
Reverse polarity voltage	$-V_{S(REV)}$	0	–	28	V	[3)] t < 2 minutes; T_A = 25°C; R_L ≥ 25 Ω; a sufficiently dimensioned ground path protection D_{GND} needs to be foreseen externally	**P_4.1.3**
Supply voltage for short circuit protection	$V_{S(SC)}$	0	–	36	V	–	**P_4.1.4**
Control input pins (IN, DEN)							
Voltage at control input pins	V_{IN}, V_{DEN}	-0.3	–	V_S	V	$V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	**P_4.1.5**
Current through control input pins	I_{IN}, I_{DEN}	-2	–	2	mA	–	**P_4.1.6**
OCT-pin							
Voltage at OCT-pin	V_{OCT}	-0.3	–	V_S	V	$V_S \geq V_{OCT}$	**P_4.1.7**
Current through OCT-pin	I_{OCT}	-2	–	2	mA	–	**P_4.1.8**
ST-pin							
Voltage at ST-pin	V_{ST}	-0.3	–	V_S	V	$V_S \geq V_{ST}$	**P_4.1.12**
Current through ST-pin	I_{ST}	-2	–	2	mA	–	**P_4.1.13**
Power stage							
Power dissipation (DC)	P_{TOT}	–	–	2	W	[4)] T_A = 85°C T_j < 150°C	**P_4.1.16**
Maximum energy dissipation Single pulse	E_{AS}	–	–	350	mJ	I_L = 2 A T_j = 150°C V_S = 28 V	**P_4.1.17**
Voltage at power transistor	V_{DS}	–	–	65	V	–	**P_4.1.19**
Ground current							
Current through ground pin	I_{GND}	-20	–	20	mA	–	**P_4.1.20**
Temporary current through ground pin	I_{GND}	-250	–	250	mA	[5)] t < 2 minutes	**P_4.1.21**

Table 1 Absolute maximum ratings [1)] (cont'd)

T_j = -40°C to 150°C, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.22
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.23
ESD susceptibility							
ESD susceptibility (all pins)	V_{ESD_HBM}	-2	–	2	kV	[6)] HBM	P_4.1.24
ESD susceptibility OUT-pin vs. GND and VS connected	V_{ESD_HBM}	-4	–	4	kV	[6)] HBM	P_4.1.25
ESD susceptibility	V_{ESD_CDM}	-500	–	500	V	[7)] CDM	P_4.1.26
ESD susceptibility pin (corner pins)	V_{ESD_CDM}	-750	–	750	V	[7)] CDM	P_4.1.27

1) Not subject to production test; specified by design
2) Please note that in case of transient voltage spikes exceeding $V_{S(AZ)}$ the resulting GND current must be limited by an external resistor in the ground path in order to ensure I_{GND} remains inside the allowed maximum ratings
3) Reverse polarity protection can only be achieved in combination with external components. For more details please refer to the corresponding chapters **"Overvoltage protection" on Page 30** and **"Reverse polarity protection" on Page 30**.
4) This parameter serves as reference for the thermal budget: it illustrates the power dissipation that can be handled by the device in an application under the given boundary conditions before exceeding the maximum rating of T_j when assuming a R_{thJA} value for a thermally well dimensioned PCB connection like given in the JEDEC case **$R_{thJA\_2s2pvia}$** listed in **Table 3** in **Chapter 4.3**. As R_{thJA} depends strongly on the applied PCB and layout of any individual application the actual achievable values of P_{TOT} can either be lower or higher depending on the given application
5) During Discharge pin operation or during reverse current situations
6) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001(1.5 kΩ, 100 pF)
7) ESD susceptibility, Charged Device Model "CDM" JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 2 Functional range

T_j = -40°C to 150°C; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	$V_{S(NOM)}$	8	24	36	V	$V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_4.2.1
Extended operating voltage	$V_{S(NOM)}$	5	–	45	V	1) $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$ (parameter deviations possible)	P_4.2.2
Minimum functional supply voltage during power-up	$V_{S(OP)\_MIN}$	–	4.3	5	V	V_S increasing IN = high From $V_{DS} = V_S$ to $V_{DS} \leq 0.5$ V	P_4.2.4
Undervoltage shutdown	$V_{S(UV)}$	3	3.5	4.1	V	V_S decreasing IN = high From $V_{DS} \leq 1$ V to $V_{DS} = V_S$	P_4.2.5
Undervoltage shutdown hysteresis	$V_{S(UV)\_HYS}$	–	850	–	mV	1) –	P_4.2.6
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.11

1) Not subject to production test; specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal resistance

Table 3 Thermal resistance [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to exposed pad soldering point	R_{thJC}	–	2	–	K/W	–	P_4.3.1
Junction to ambient All channels active	$R_{thJA\_2s2pvia}$	–	36	–	K/W	[2)] –	P_4.3.2
Junction to ambient All channels active	R_{thJA_1s0p}	–	124	–	K/W	[3)] –	P_4.3.3
Junction to ambient All channels active	$R_{thJA\_1s0p\_300mm}$	–	58	–	K/W	[4)] –	P_4.3.4
Junction to ambient All channels active	$R_{thJA\_1s0p\_600mm}$	–	47	–	K/W	[5)] –	P_4.3.5

1) Not subject to production test; specified by design

2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer

3) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, footprint; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 × 70 µm Cu

4) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, 300 mm; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 × 70 µm Cu

5) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board, 600 mm; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 1 × 70 µm Cu

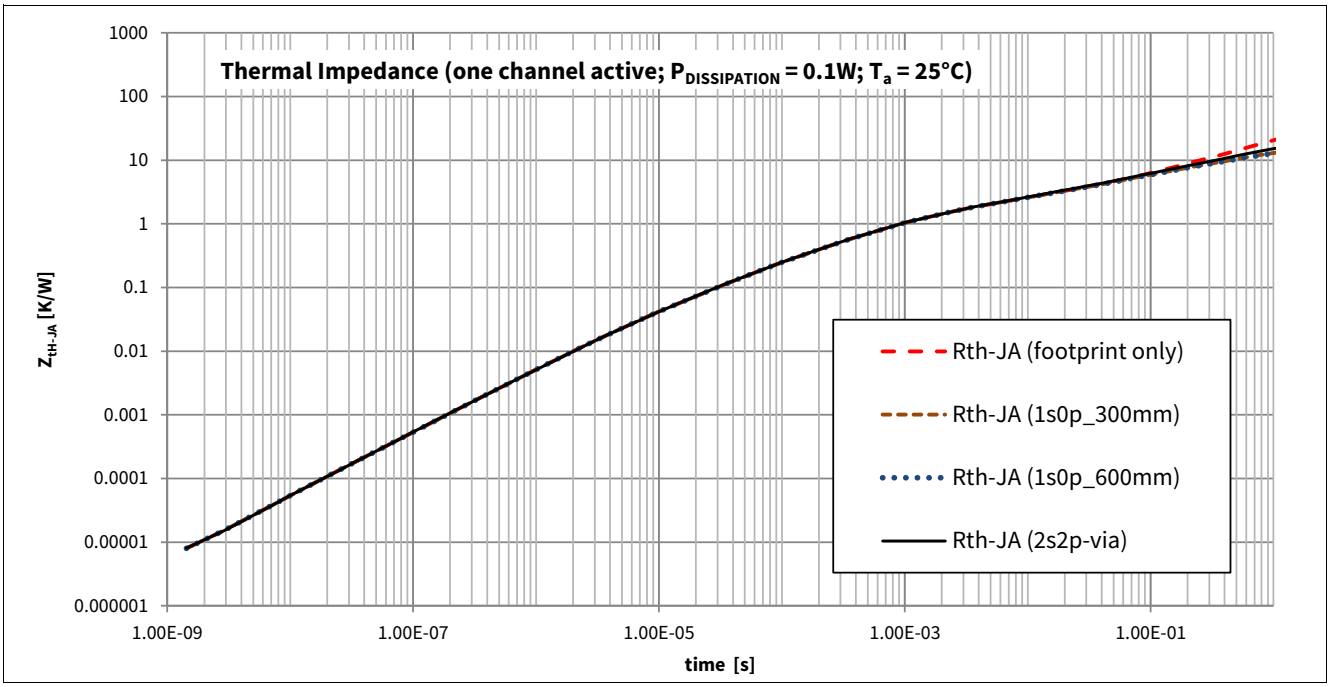


Figure 4 Thermal impedance (short time scale)

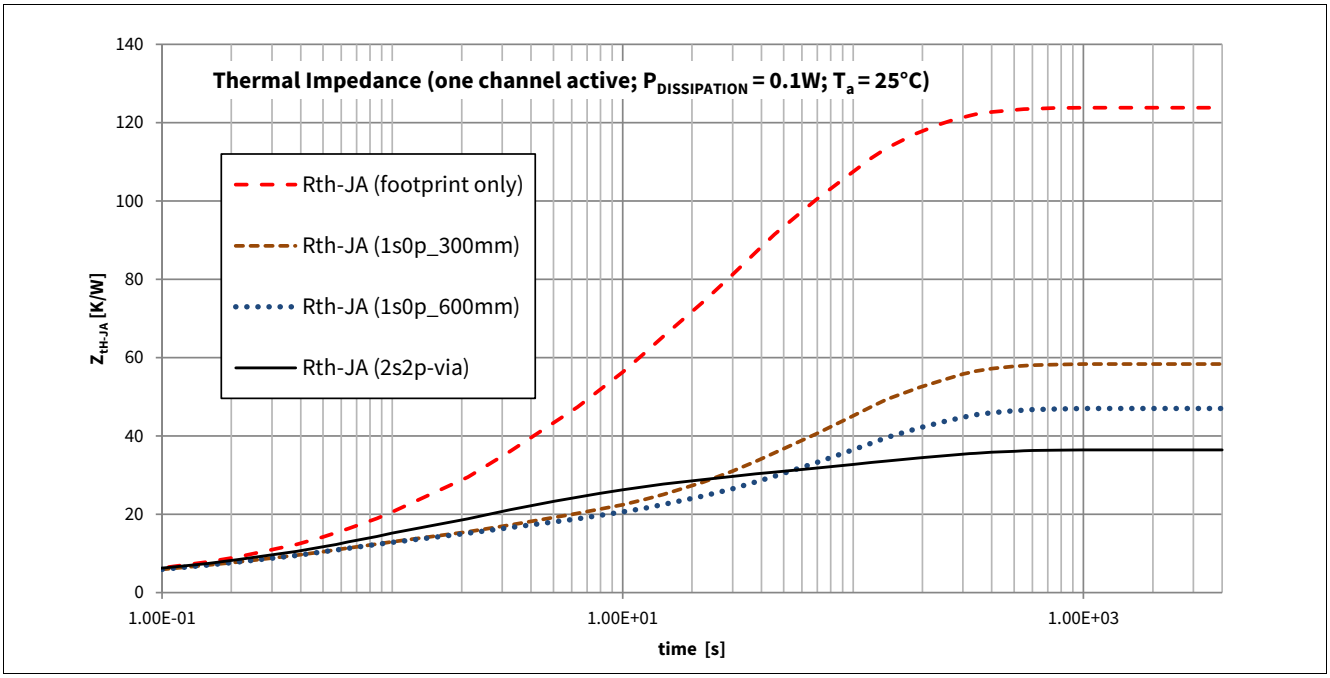


Figure 5 Thermal impedance (long time scale; one channel active)

5 Operation and diagnostic modes

5.1 State diagram

Depending on supply voltage V_S, input signals and usage of diagnosis the ITS4035S-EP-D can be in different operation modes. **Figure 6** provides an overview of the operation modes and their corresponding operation currents.

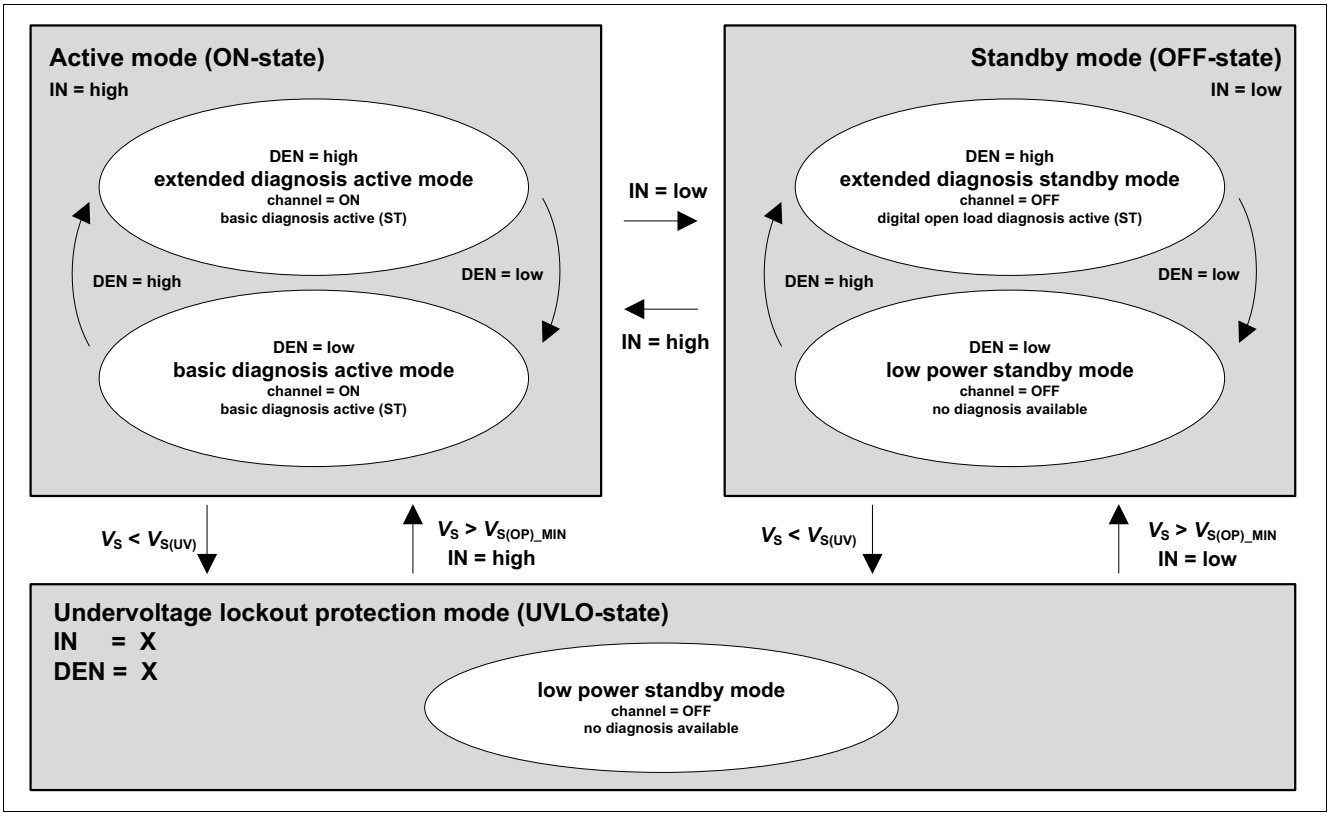


Figure 6 State diagram ITS4035S-EP-D

5.2 Electrical characteristics: current consumption

Table 4 Electrical characteristics: current consumption

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

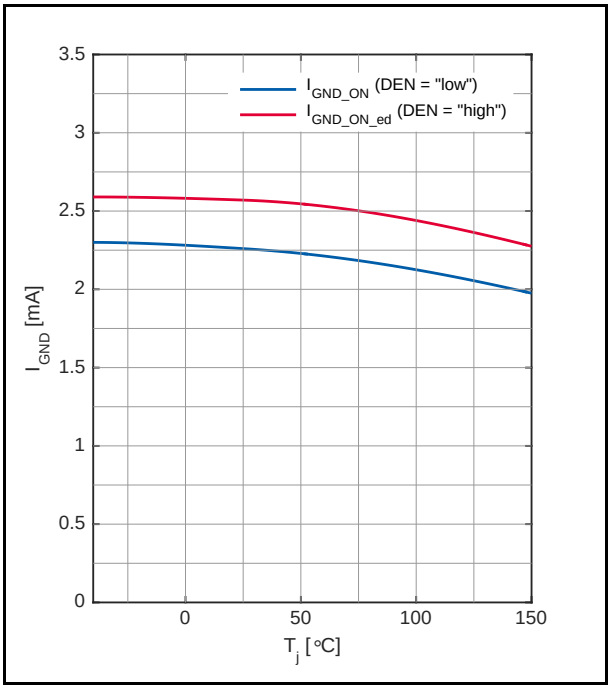
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Operation currents							
ON - state current;	I_{GND_ON}	–	2.3	2.9	mA	1) $T_j \leq 25°C$; V_S = 24 V; V_{IN} = high; V_{DEN} = low; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.6
ON - state current;	I_{GND_ON}	–	2	2.5	mA	1) T_j = 150°C; V_S = 24 V; V_{IN} = high; V_{DEN} = low; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.1
ON - state current; (extended diagnosis active mode)	$I_{GND\_ON\_ed}$	–	2.6	3.2	mA	1) $T_j \leq 25°C$; V_S = 24 V; V_{IN} = high; V_{DEN} = high; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.7
ON - state current; (extended diagnosis active mode)	$I_{GND\_ON\_ed}$	–	2.3	2.8	mA	1) T_j = 150°C; V_S = 24 V; V_{IN} = high; V_{DEN} = high; I_{OCT} = 50 µA; Device in $R_{DS(ON)}$	P_5.2.2
Standby currents (to device GND)							
OFF - state current; (low power standby mode)	I_{GND_OFF}	–	0.1	1	µA	V_S = 24 V; V_{IN} floating; V_{DEN} floating	P_5.2.3
OFF - state current; (extended diagnosis standby mode)	$I_{GND\_OFF\_ed}$	–	1.3	1.6	mA	2) V_S = 24 V; V_{IN} = low; V_{DEN} = high	P_5.2.4

1) The current flowing out of the OCT-pin I_{OCT} depends on the adjusted current limitation value (R_{OCT}) and is not included in this parameter. In case of fault conditions also an additional current may be drawn from the ST-pin to device GND if applied. The ST-pin current - if applicable - is also not included in this parameter
2) The ST-pin current drawn by the ST-pin to device GND if applied is not included in this parameter. The ST-pin current during fault conditions will depend on the external pull-up circuit

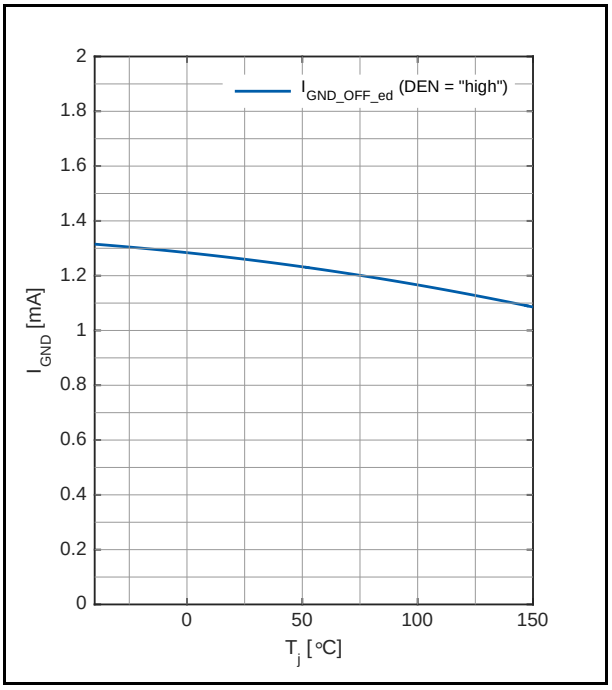
5.3 Typical performance characteristics current consumption

Typical performance characteristics

Operating current I_{GND_ON} versus junction temperature T_j (IN = high)



Extended diagnosis standby current $I_{GND\_OFF\_ed}$ versus junction temperatureT_j (IN = high)



6 Power stage

The power stage is built using an N-channel vertical power MOSFET (DMOS) with charge pump.

6.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ of the power stage depends on supply voltage as well as on junction temperature T_j. **Figure 7** shows the influence of temperature on the typical ON-state resistance. The behavior of the power stage in reverse polarity condition is described in **Chapter 7.4**.

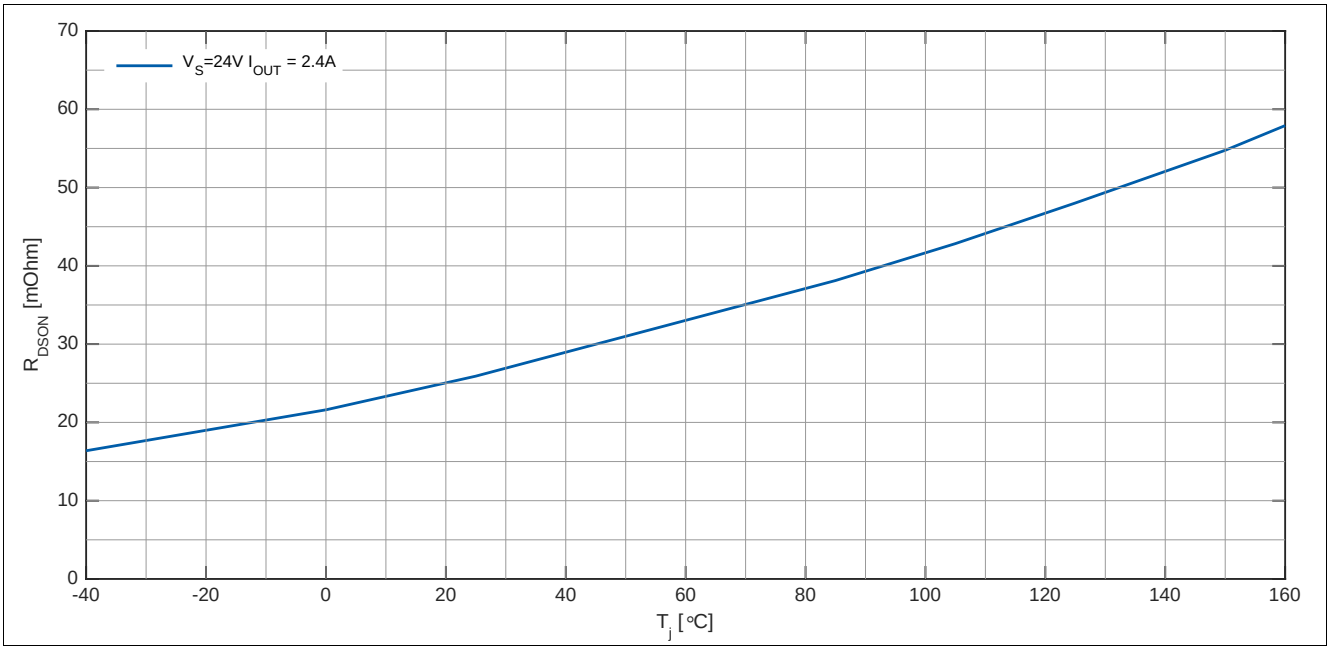


Figure 7 Typical ON-state resistance

6.2 Turn on/off characteristics with resistive load

A high signal at the input pin (see **Chapter 9**) causes the power DMOS to switch on with a dedicated slope, which is optimized in terms of EMC emission.

Figure 8 shows the typical timing when switching a resistive load.

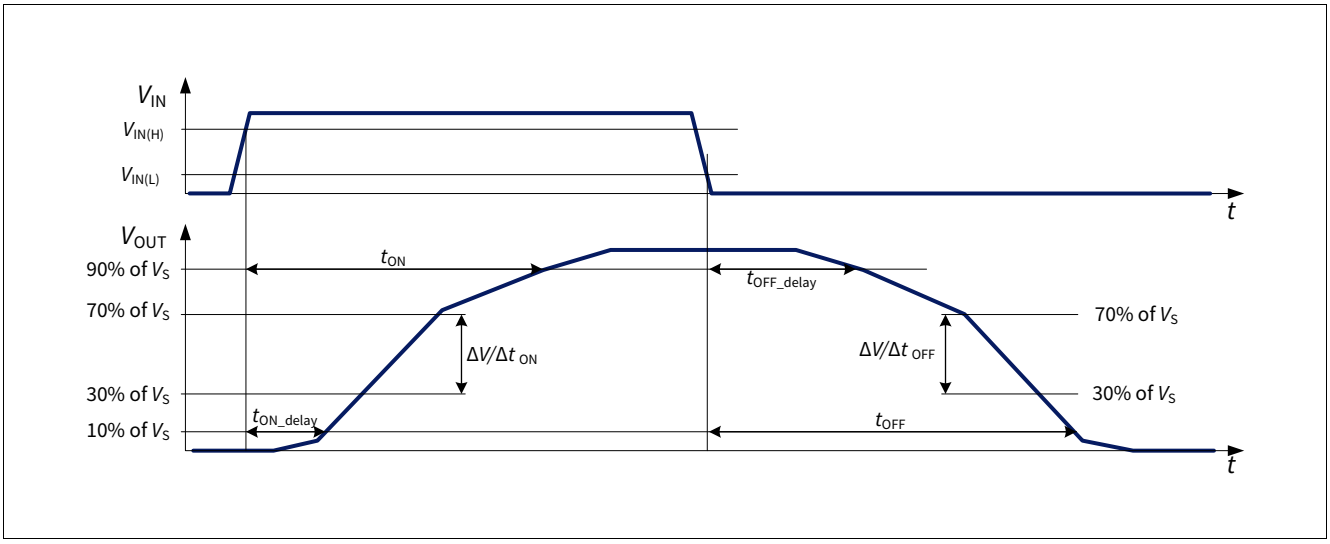


Figure 8 Switching a resistive load timing

6.3 Inductive load

6.3.1 Output clamping

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltage drop over the power stage a voltage clamp mechanism $Z_{DS(AZ)}$ is implemented that limits negative output voltage to a certain level (V_S - $V_{DS(AZ)}$). The clamping mechanism allows in addition a fast demagnetization of inductive loads because during the phase of active clamping the power is dissipated to a great extent rapidly inside the switch. On the other hand, the power dissipated inside the switch while switching off inductive loads can cause considerable stress to the device. Therefore the maximum allowed energy at a given current (and by this also the inductance) is limited. In **Figure 9** and **Figure 10** the basic principle of active clamping is illustrated as well as simplified waveforms when switching off inductive loads.

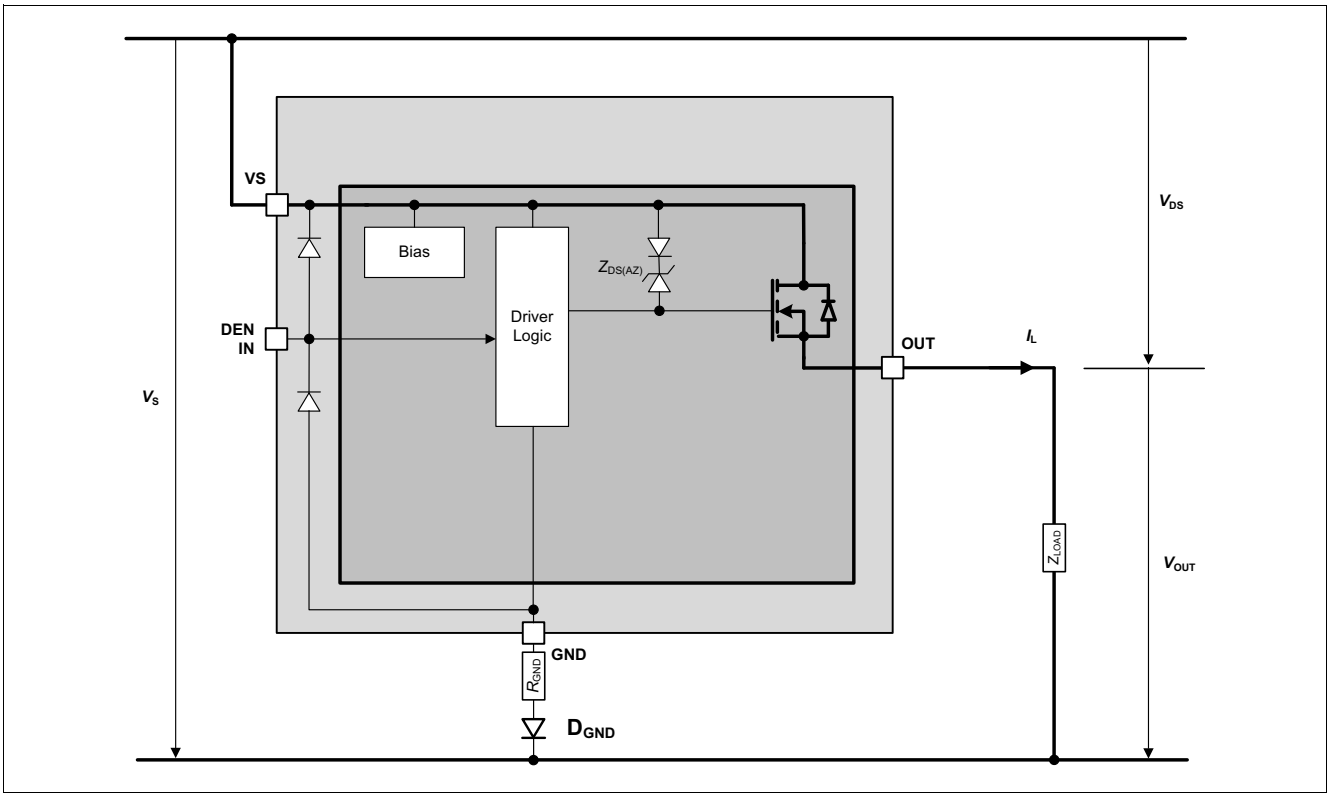


Figure 9 Output clamp ITS4035S-EP-D

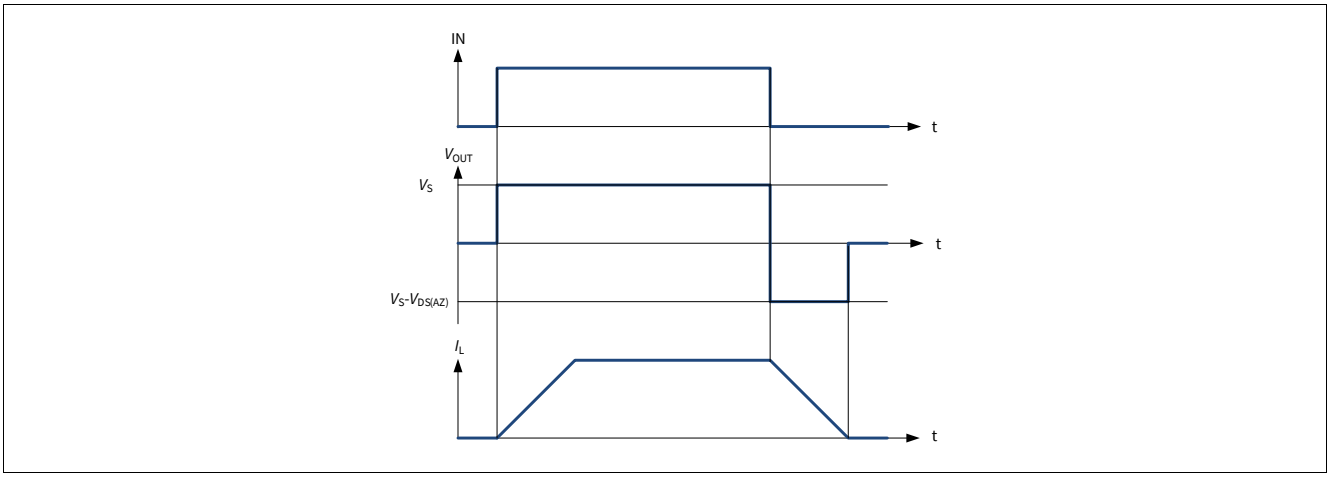


Figure 10 Switching an Inductive load timing

6.3.2 Maximum load inductance

During demagnetization of inductive loads, the following energy must be dissipated by the ITS4035S-EP-D. This energy can be calculated by help of the following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(AZ)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right] \quad (6.1)$$

Following equation gets simplified under the assumption of $R_L = 0\ \Omega$:

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \quad (6.2)$$

The energy, which may be converted into heat, is limited by the thermal design of the component. See **Figure 11** for the maximum allowed energy dissipation as a function of the load current for a singular pulse event on the channel.

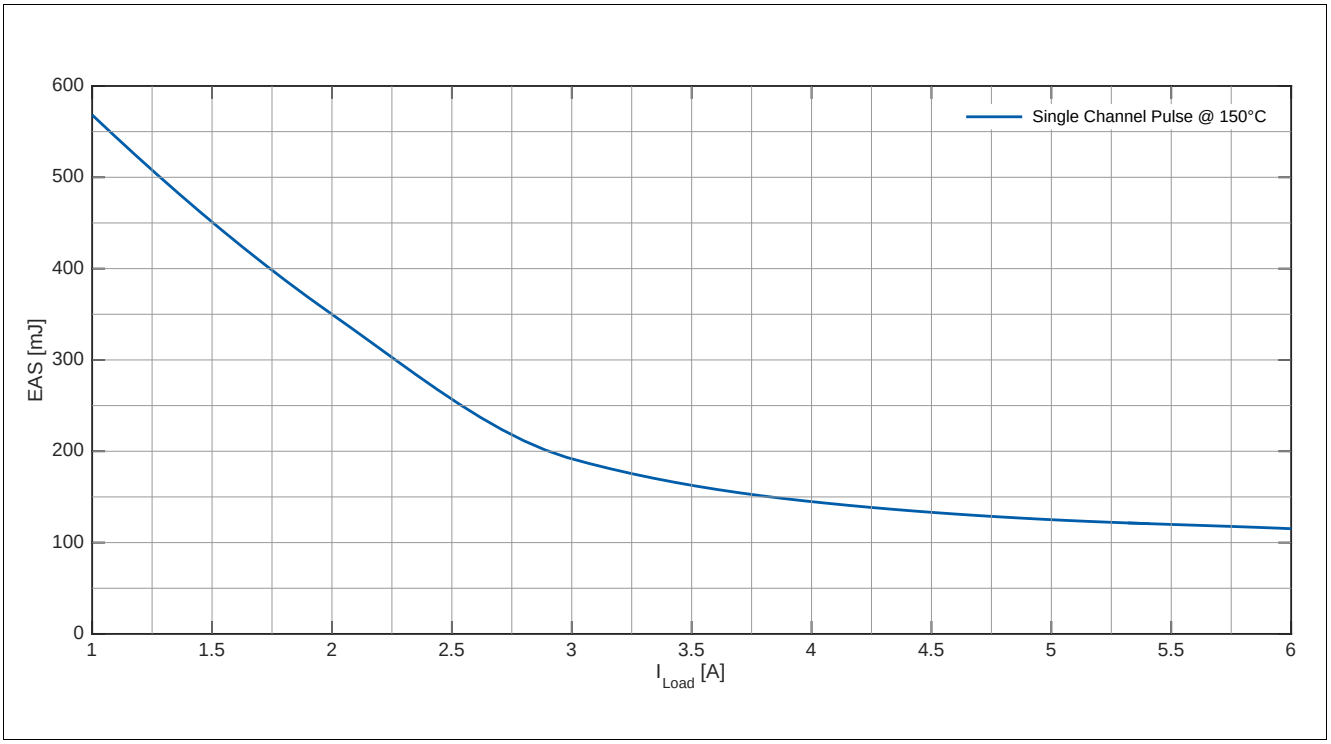


Figure 11 Maximum energy dissipation single pulse; V_S = 28 V

6.4 Inverse current capability

In case of inverse current, meaning a voltage V_{INV} at the output higher than the supply voltage V_S, a current I_{INV} will flow from output to VS-pin via the body diode of the power transistor (please refer to **Figure 12**). If the channel is active (ON-state) by the time when the inverse current condition appears it will remain active and its output stage will follow the state of the corresponding IN-pin, which means that the channel can be switched off during inverse current condition. If the channel is inactive (OFF-state) by the time when the inverse current condition appears it will remain inactive regardless of the state of the IN-pin. If during an inverse current condition the IN-pin is set from low to high in order to activate the channel, the output stage of the channel is kept OFF until the inverse current disappears. For all cases the current I_{INV} should not be higher than $I_{L(INV)}$. Please note that during inverse current condition the protection functions are not available.

Power stage

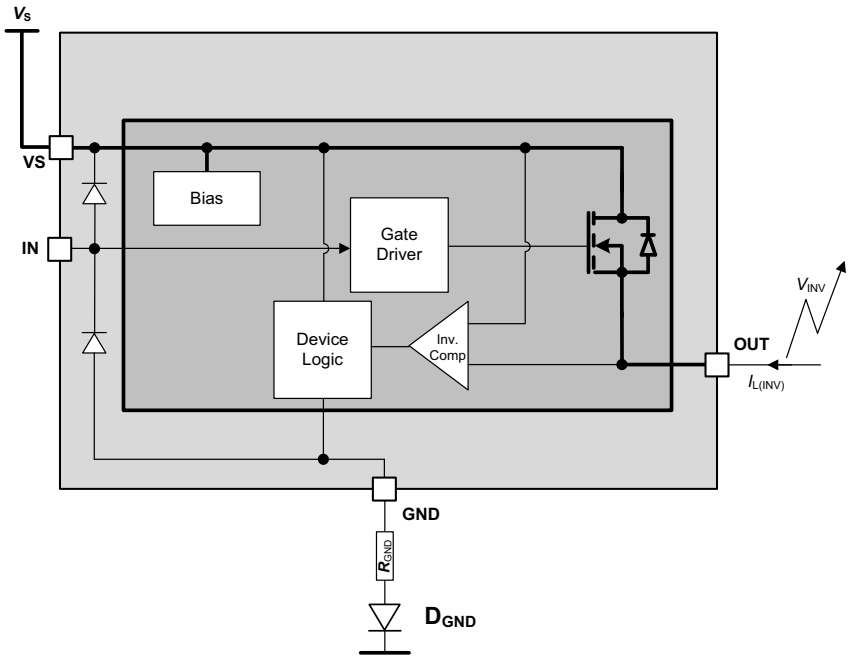


Figure 12 Inverse current circuitry ITS4035S-EP-D

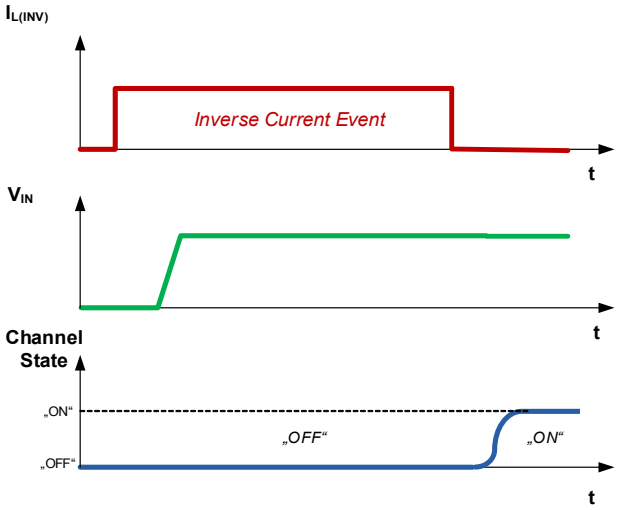


Figure 13 Inverse current event: channel in OFF-state (channel remains off for duration of inverse current event)

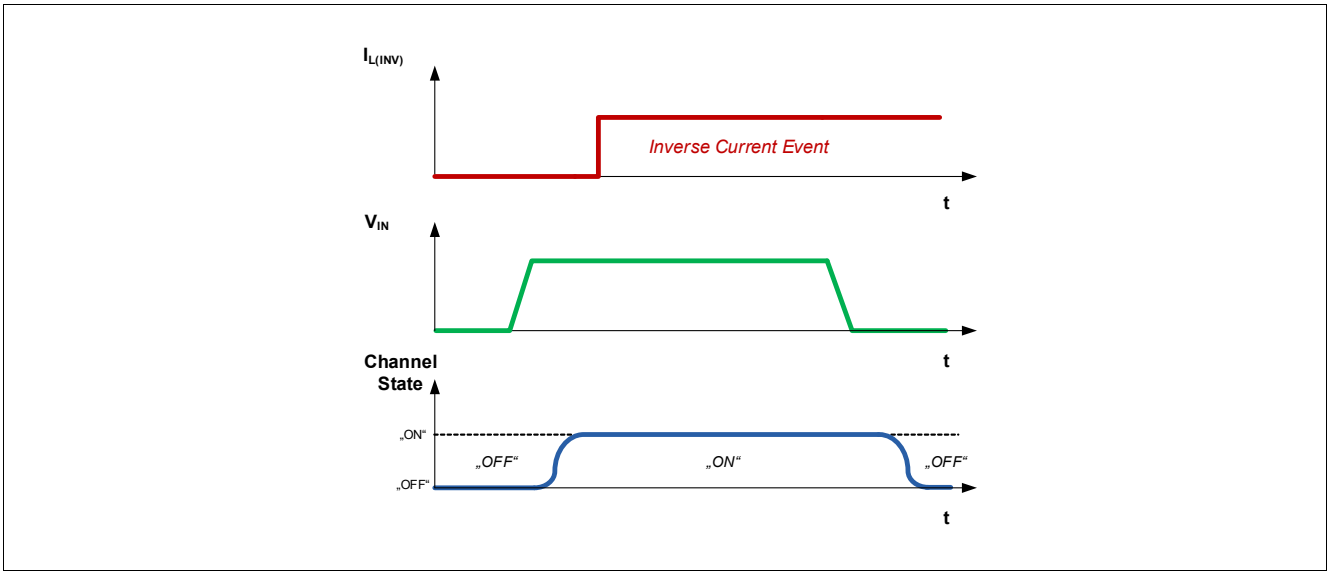


Figure 14 Inverse current event: channel in ON-state (output not influenced and can be switched off)

6.5 Electrical characteristics: Power stage

Table 5 Electrical characteristics: Power stage

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance (T_j = 25°C)	$R_{DS(ON)}$	–	27	35	mΩ	[1] I_L = 2.0 A; V_{IN} = high; T_j = 25°C	P_6.5.1
ON-state resistance (T_j = 125°C)	$R_{DS(ON)\_125}$	–	48	–	mΩ	[1] I_L = 2.0 A; V_{IN} = high; T_j = 125°C	P_6.5.2
ON-state resistance (T_j = 150°C)	$R_{DS(ON)\_150}$	–	55	70	mΩ	I_L= 2.0 A; V_{IN} = high; T_j = 150°C	P_6.5.3
Allowable nominal load current range in conjunction with a selected current limit setting or based on thermal constraints	$I_{L(NOM)}$	–	5.0		A	[1] [2] T_A = 85°C, T_J < 150°C	P_6.5.4
Drain to source clamping voltage $V_{DS(AZ)} = [V_S - V_{OUT}]$	$V_{DS(AZ)}$	65	70	75	V	I_{DS} = 5 mA	P_6.5.6

Table 5 Electrical characteristics: Power stage (cont'd)

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current (OFF-state)	$I_{L(OFF)}$	–	0.1	0.5	µA	1) V_{IN} = low; V_{OUT} = 0 V; $T_j \leq 85°C$	P_6.5.7
Output leakage current (OFF-state)	$I_{L(OFF)\_150}$	–	2.5	5	µA	V_{IN} = low; V_{OUT} = 0 V; T_j = 150°C	P_6.5.8
Inverse current capability	$I_{L(INV)}$	–	2.2	–	A	1) 3) $V_S < V_{OUT}$; t < 2 minutes	P_6.5.9
Slew rate (switch on) 30% to 70% of V_S	$\Delta V/\Delta t_{ON}$	–	0.7	–	V/µs	R_L = 12 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.10
Slew rate (switch off) 70% to 30% of V_S	$-\Delta V/\Delta t_{OFF}$	–	0.7	–	V/µs	R_L = 12 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.11
Turn on time to V_{OUT} = 90% of V_S	t_{ON}	–	60	85	µs	4) R_L = 12 Ω; V_S = 24 V; I_{OCT} = 50 µA; V_{DEN} = low	P_6.5.13
Turn off time to V_{OUT} = 10% of V_S	t_{OFF}	–	55	85	µs	R_L = 12 Ω; V_S = 24 V; I_{OCT} =50 µA	P_6.5.14
Turn on/off matching t_{OFF} - t_{ON}	Δt_{SW}	-35	0	35	µs	R_L = 12 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.15
Turn on time to V_{OUT} = 10% of V_S	t_{ON_delay}	–	25	40	µs	4) R_L = 12 Ω; V_S = 24 V; I_{OCT} = 50 µA; V_{DEN} = low	P_6.5.16
Turn off time to V_{OUT} = 90% of V_S	t_{OFF_delay}	–	25	40	µs	R_L = 12 Ω; V_S = 24 V; I_{OCT} = 50 µA	P_6.5.17

1) Not subject to production test; specified by design

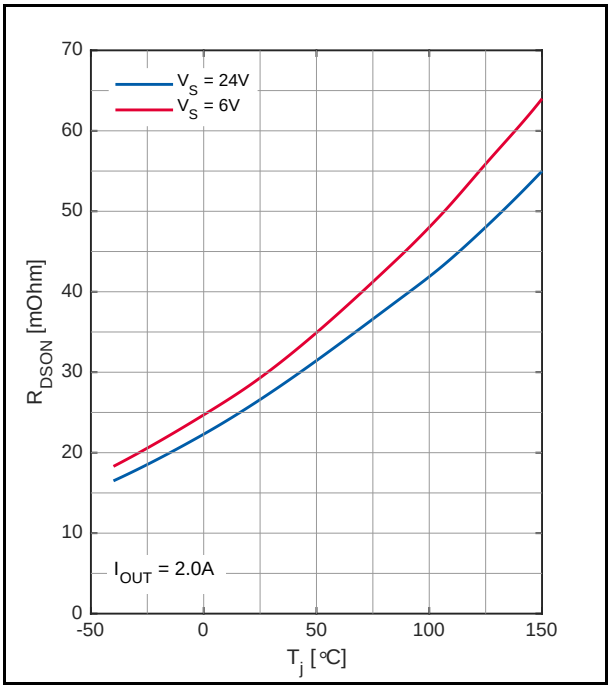
2) The allowable nominal load current can be restricted by two different factors - the magnitude of the adjusted current limitation but as well by thermal constraints. The minimum limit given here corresponds to the limitation by the current limitation when adjusted to its minimum value (I_{OCT} = 6.67 µA) while the maximum limit corresponds to the thermal limitation where the maximum T_j of 150°C is reached assuming T_{AMB} =85°C and $R_{thJA\_2s2pvia}$. In normal operation the minimum required distance of $I_{L(NOM)}$ to the adjusted current limitation has to be maintained. For further details and numbers please refer to **Table 11**

3) Please note that during inverse current condition the protection features are not operational
4) This timing will be faster if device is in extended diagnosis standby mode (DEN = high). For further details see typical performance graphs **“Turn on time t_{ON} to V_{OUT} = 90% versus current limit adjust current I_{OCT} (DEN = low & high)” on Page 27** and **“Turn on delay time t_{ON_delay} to V_{OUT} = 10% versus current limit adjust current I_{OCT} (DEN = low & high)” on Page 27**

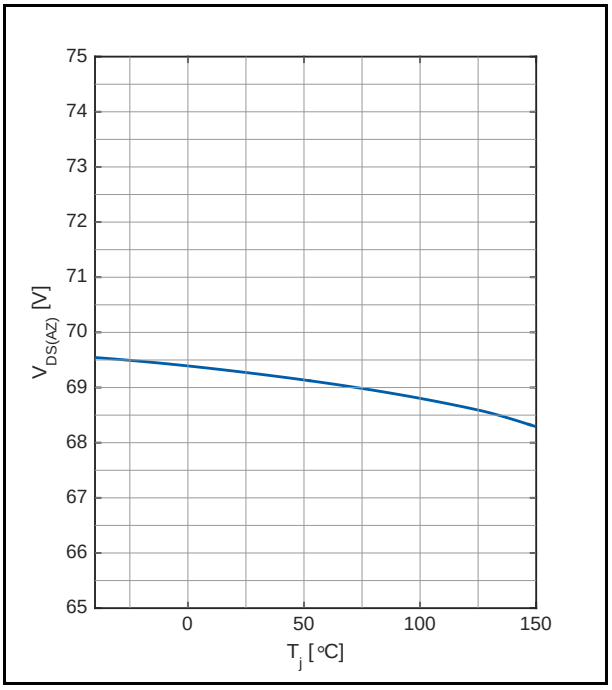
6.6 Typical performance characteristics power stage ITS4035S-EP-D

Typical performance characteristics

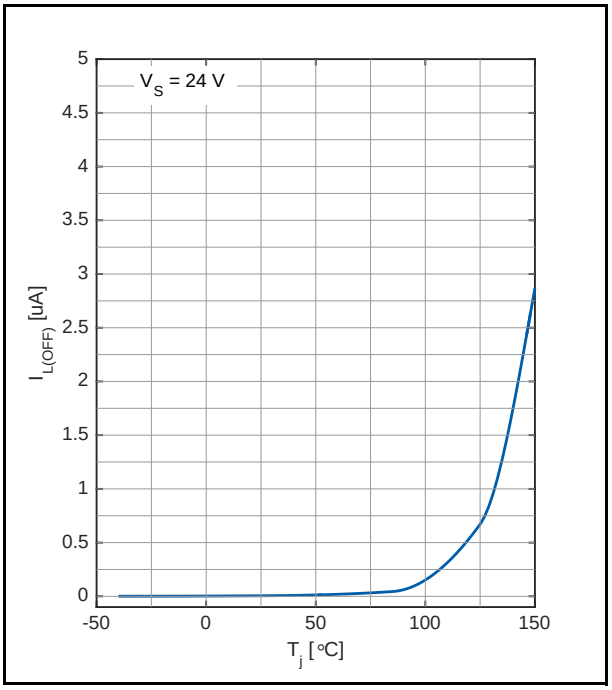
ON-state resistance R_{DSON} versus junction temperature T_j



Output clamp voltage $V_{DS(AZ)}$ versus junction temperature T_j

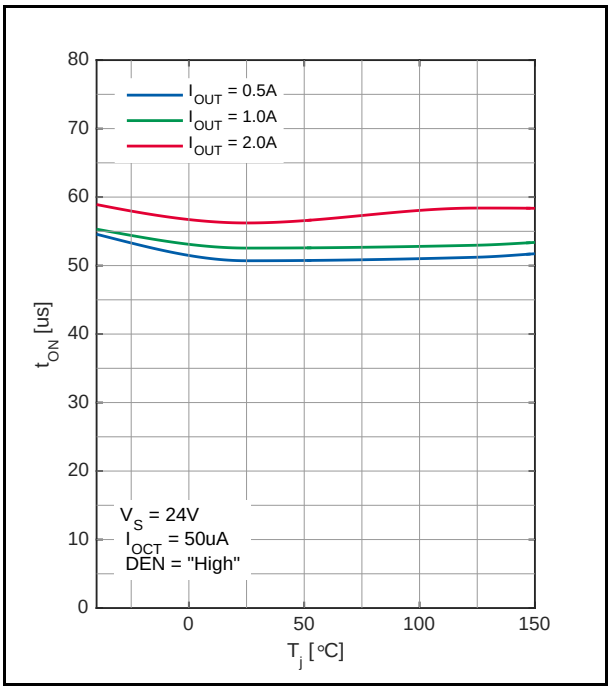


Output leakage current $I_{L(OFF)}$ versus junction temperature T_j

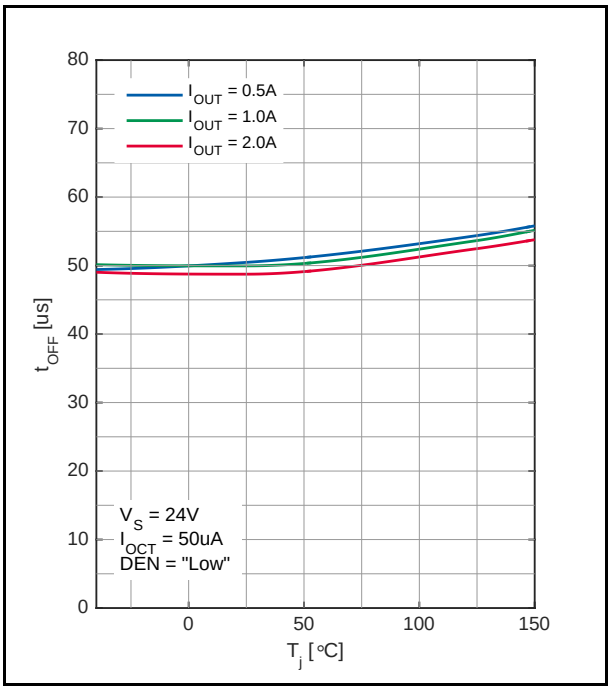


Power stage

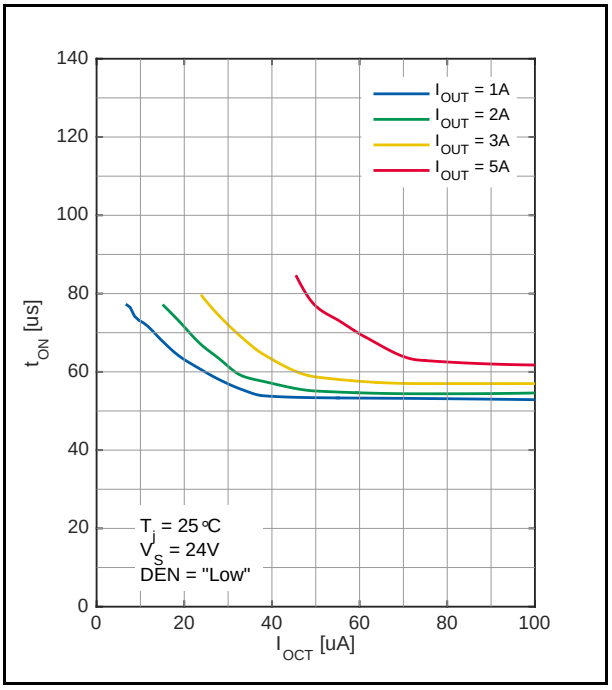
Turn on time t_{ON} to V_{OUT} = 90% versus junction temperature T_j



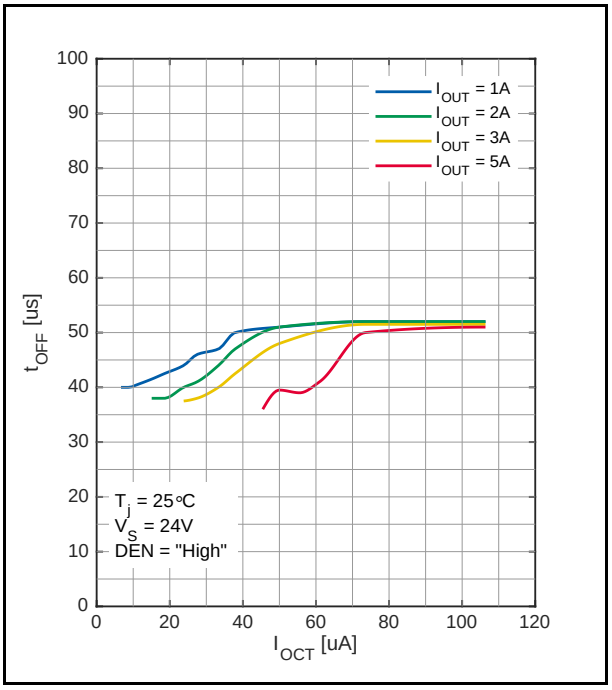
Turn off time t_{OFF} to V_{OUT} = 90% versus junction temperature T_j



Turn on time t_{ON} to V_{OUT} = 90% versus current limit adjust current I_{OCT}

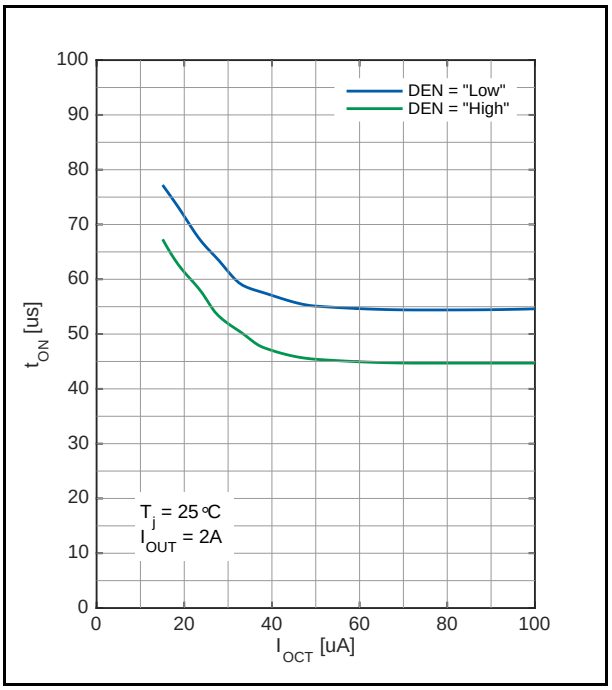


Turn off time t_{OFF} to V_{OUT} = 10% versus current limit adjust current I_{OCT}

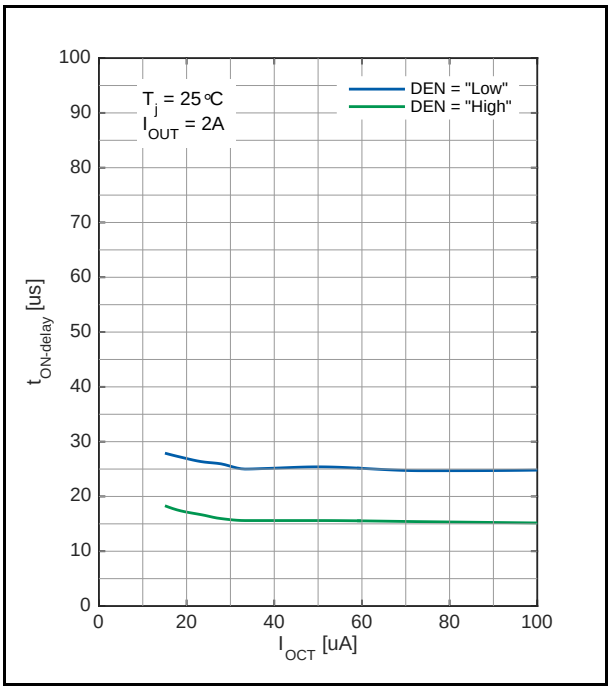


Power stage

Turn on time t_{ON} to V_{OUT} = 90% versus current limit adjust current I_{OCT} (DEN = low & high)



Turn on delay time t_{ON_delay} to V_{OUT} = 10% versus current limit adjust current I_{OCT} (DEN = low & high)



7 Protection functions

The device provides integrated protection functions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Protection functions are designed to prevent the destruction of the ITS4035S-EP-D due to fault conditions described in the data sheet. Please note that fault conditions are not considered as normal operation conditions and the protection functions are neither designed for continuous operation nor for repetitive operation.

7.1 Loss of ground protection

In case of loss of module ground when the load remains connected to ground, the device protects itself by automatically turning off (when it was previously on) or remaining off, regardless of the voltage applied at the input pin, IN.

In an application where the input IN is directly controlled by logic levels < V_S (e.g. by a microcontroller without galvanic isolation), it is recommended to use input resistors [1)] between the external control circuit (microcontroller) and the ITS4035S-EP-D to protect also the external control circuit in case of loss of ground.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS as is illustrated in **Figure 15**, below.

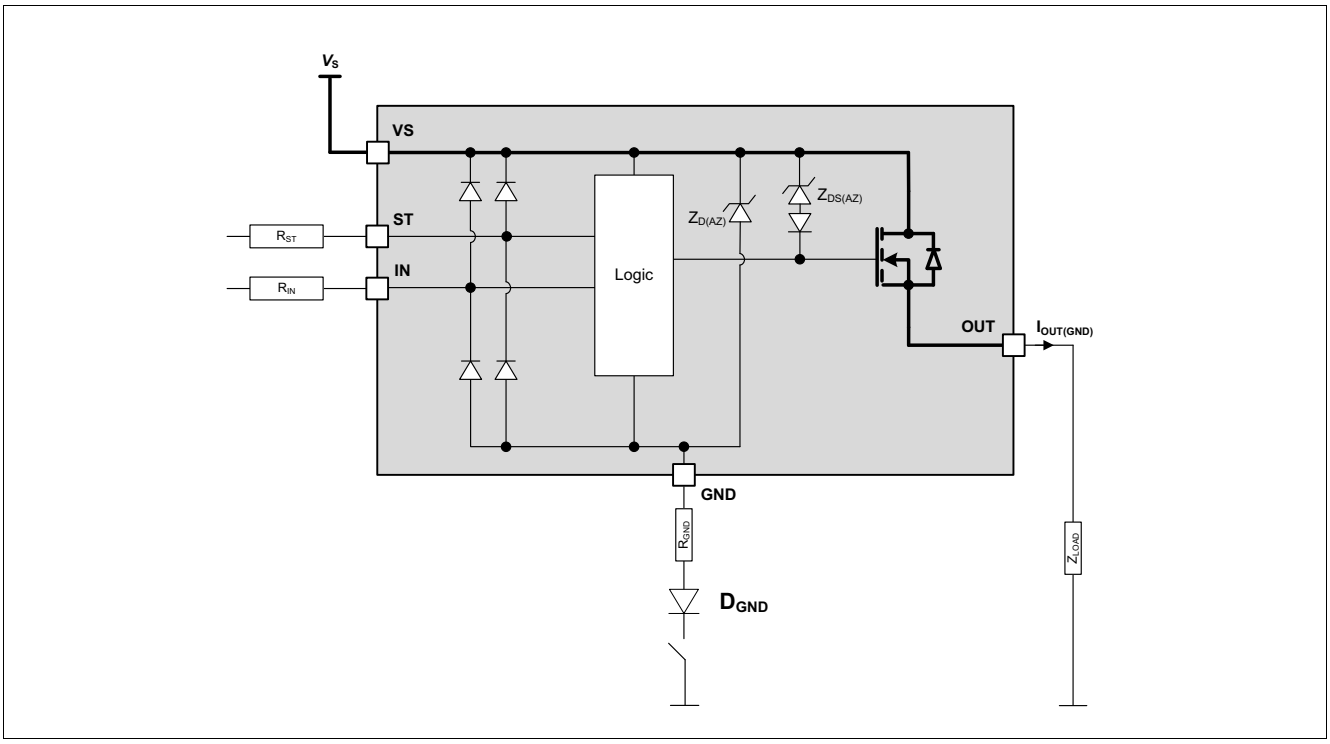


Figure 15 Loss of ground protection with external components

1) Recommended value is 10 kΩ

7.2 Undervoltage protection

If the supply voltage falls below $V_{S(UV)}$ the undervoltage protection of the device is triggered. $V_{S(UV)}$ represents hence the minimum voltage for which the switch still can hold ON. Once the device is off $V_{S(OP)\_MIN}$ represents the lowest voltage where the device is turning on again (and thus the channel can be switched again). If the supply voltage is below the undervoltage threshold $V_{S(UV)}$, the channel of the device is off (or turning off). As soon as the supply voltage is recovering and exceeding the threshold of the functional supply voltage $V_{S(OP)\_MIN}$, the device is re-powering and its channel can be switched again. In addition the protection functions as well as diagnosis becomes operational once $V_{S(OP)\_MIN}$ is reached. **Figure 16** illustrates the undervoltage mechanism.

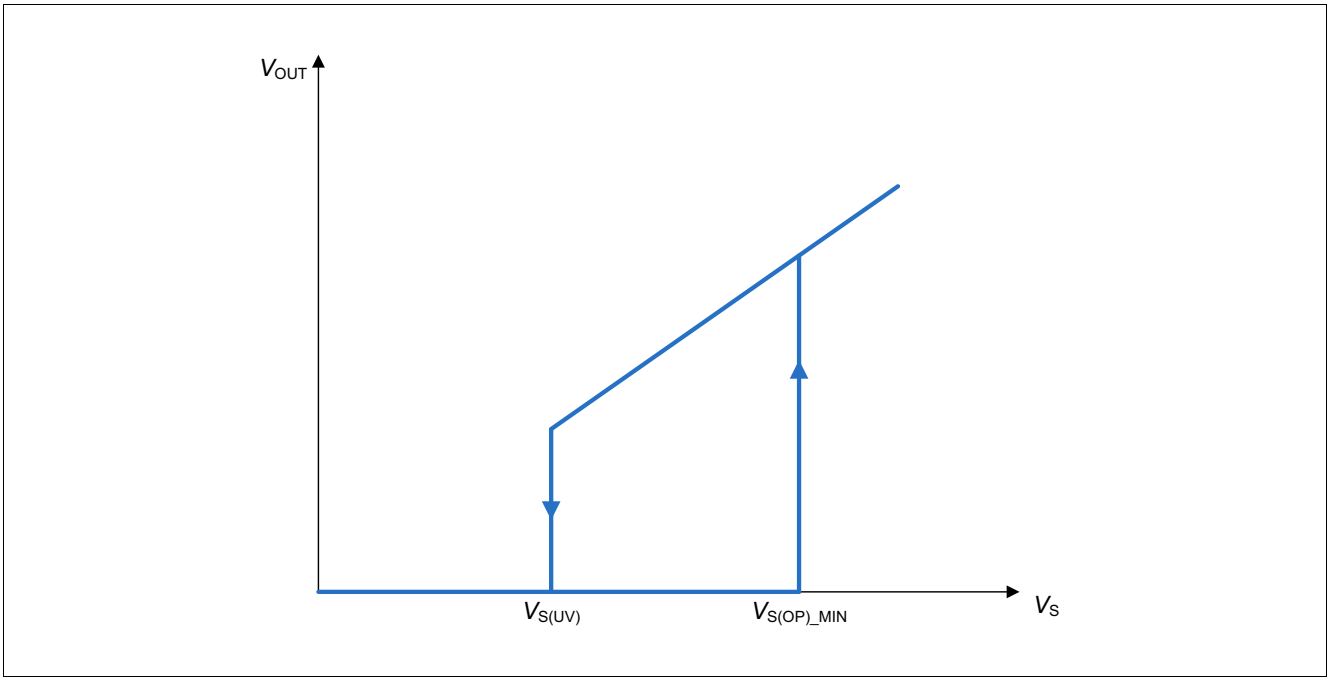


Figure 16 Undervoltage behavior

7.3 Overvoltage protection

The ITS4035S-EP-D provides a protection against transient overvoltage spikes by an integrated overvoltage clamp.

7.3.1 Overvoltage clamp

There is an integrated clamping mechanism for overvoltage protection ($Z_{D(AZ)}$) against transient overvoltage spikes. To ensure this mechanism operates properly within the application, the current in the Zener diode $Z_{D(AZ)}$ must be limited by an external GND protection R_{GND}. **Figure 17** shows a typical application to withstand overvoltage events. In case of supply voltage transients higher than $V_{S(AZ)}$, the voltage from supply to device ground is clamped. As a result, the device ground potential rises to V_S - $V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at IN-pin rises almost to that potential, depending on the impedance of the connected circuitry. As a consequence, in case of transient overvoltage events > $V_{S(AZ)}$, external resistors have to be placed at the control pins that limit the current that can flow out of these pins while the device GND potential becomes higher than the voltage level at the control pins. Next to these protection resistors at the control pins also the GND path itself has to be protected against excessive current flow during such pulses by placing a resistor in the GND path. For a more detailed description of external devices for protection under fault conditions please refer to **Chapter 10.2**.

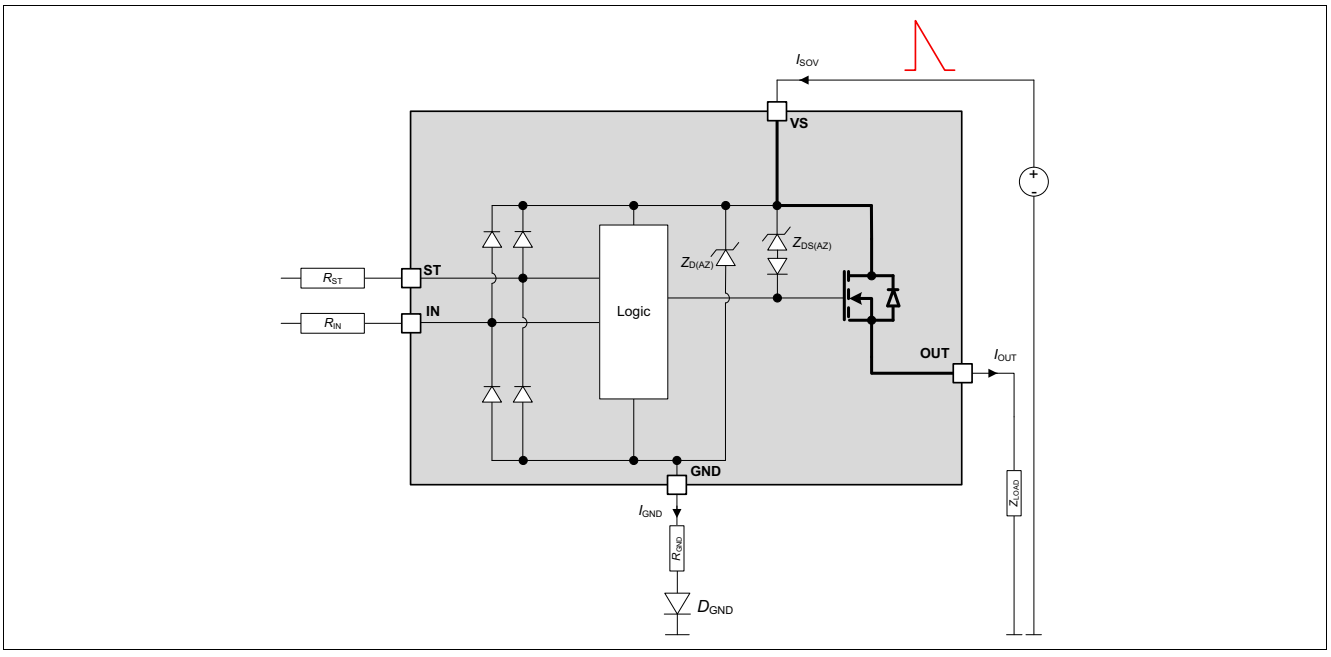


Figure 17 Overvoltage clamp protection with external components

7.4 Reverse polarity protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS will dissipate power. The current flowing through the intrinsic body diode is limited externally by the load itself. But in addition also the current into the ground path and the logic pins must be limited by external components to the maximum allowed current described in **Chapter 4.1**. shows a typical application. As external protection of the ground path the usage of a diode in the GND-path is recommended. For a more detailed description of external devices for protection please refer to **Chapter 10.2**

During reverse polarity no protection functions are available.

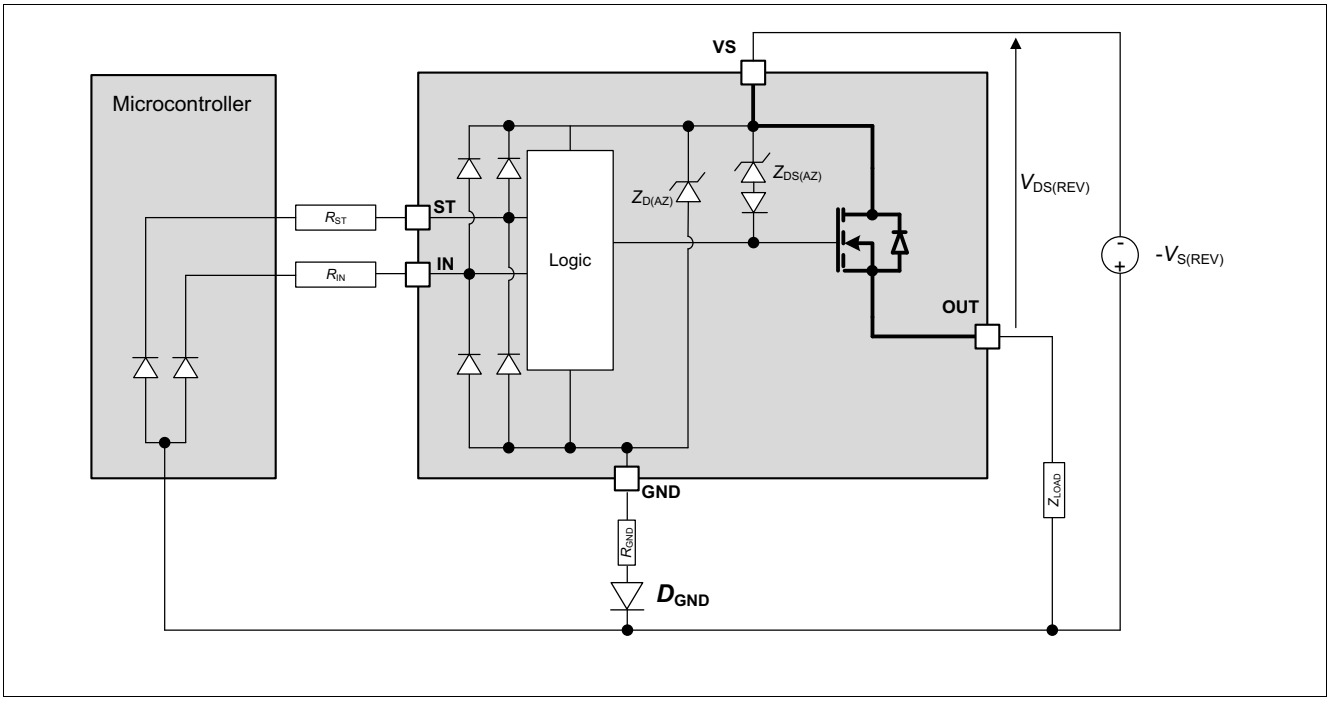


Figure 18 Reverse polarity protection with external components

7.5 Overload protection

In case of overload, such as high inrush currents or short circuit to ground, the ITS4035S-EP-D offers a set of protection mechanisms. As a first step, it comprises an accurate adjustable current limitation. This feature offers protection against overstress for the load as well as for the power output stage. In case of DMOS temperature increase exceeding the device safe operating environment, overtemperature and dynamic temperature protection mechanism will be triggered.

7.5.1 Current limitation

The ITS4035S-EP-D provides a very versatile and user friendly current limitation functionality that can be adjusted externally by the user in a broad range. The adjustment of the current limitation threshold $I_{LIM(th,adj)}$ to the desired value is controlled by the I_{OCT} current that is driven by the overcurrent threshold pin (OCT-pin) out of the device. The OCT-pin thereby is acting as a voltage source providing V_{OCT}. In the most simple and straight forward way the current limit adjustment can hence be achieved by connecting the OCT-pin with an appropriately dimensioned resistor to device ground. **Figure 20** is illustrating the usage of the adjustable current limitation. Please note that the values for the current limitation threshold $I_{LIM(th,adj)}$ are defined in such a way that they coincide with the typical values of the resulting current limitation at 25°C. The typical values of the current limitation at different temperatures may hence differ from $I_{LIM(th,adj)}$ to a certain degree. Typical values of the current limitation for different temperatures as a function of I_{OCT} are shown in **Figure 19**.

The adjusted current limit threshold $I_{LIM(th,adj)}$ is a function of the current I_{OCT} driven by the OCT-pin.

The appropriate resistor, R_{OCT} can be derived by the equation [1]:

$$R_{OCT} = (V_{OCT})/(I_{OCT}) \quad (7.1)$$

The specified range of I_{OCT} that can be used to adjust $I_{LIM(th,adj)}$ allows to vary the current limitation over a wide area. If the upper specified I_{OCT} range is exceeded resulting in higher I_{OCT} currents the current limitation will

1) A look-up table with values can be found in **Chapter 10.3**

not change anymore and saturates at its maximum current limit $I_{LIM\_int(MAX)}$. This means that from this point onwards any further increase of I_{OCT} will not result in increased current limitation values anymore. This is useful in case the OCT-pin unintentionally is shorted to GND to provide also in this case a basic protection for the device and the application. Despite this additional protection feature the device must not be operated with I_{OCT} currents above the allowed range as the R_{OCT} resistor also has additional functions. On the one hand R_{OCT} has always to be in place to protect the pin in case of reverse polarity situations while on the other hand R_{OCT} will also reduce potential EMC disturbances at the OCT-pin [1]. If I_{OCT} exceeds the threshold $I_{OCT(short2GND)}$ it will be reported as a fault flag on the ST-pin. Please note that this fault flag will be set only during ON-state when DEN = low. For more details about diagnosis upon being outside the specified I_{OCT} range please refer to **Chapter 8.1**.

R_{OCT} values causing the I_{OCT} currents below the specified OCT adjust range are not recommended for usage as the resulting current limitation suffers from limited accuracy and hence is not specified.

The adjustable current limitation feature of the ITS4035S-EP-D offers several advantages and flexibility to the user. When adjusting the device to a specific current limitation threshold LIM(th,adj), ensure that between the adjusted current limitation threshold $I_{LIM(th,ad)}$ and the expected nominal current of the application there is a certain distance in order to avoid unwanted activation of the current limitation circuit during normal operation. **Table 10** defines the maximum allowable load current for a certain OCT resistor setting.

Please note that when the load current of the device gets close(r) to the adjusted current limitation threshold, the turn on slew rate gets slower, resulting in longer t_{ON} timing, while at the same time corresponding turn off slew rate may become faster leading to shorter t_{OFF} timings.

Keeping the above mentioned distance will ensure that the influence of the current limitation threshold on switching timings is moderate and is illustrated in the graph **"Turn on time t_{ON} to V_{OUT} = 90% versus current limit adjust current I_{OCT} (DEN = low & high)" on Page 27**.

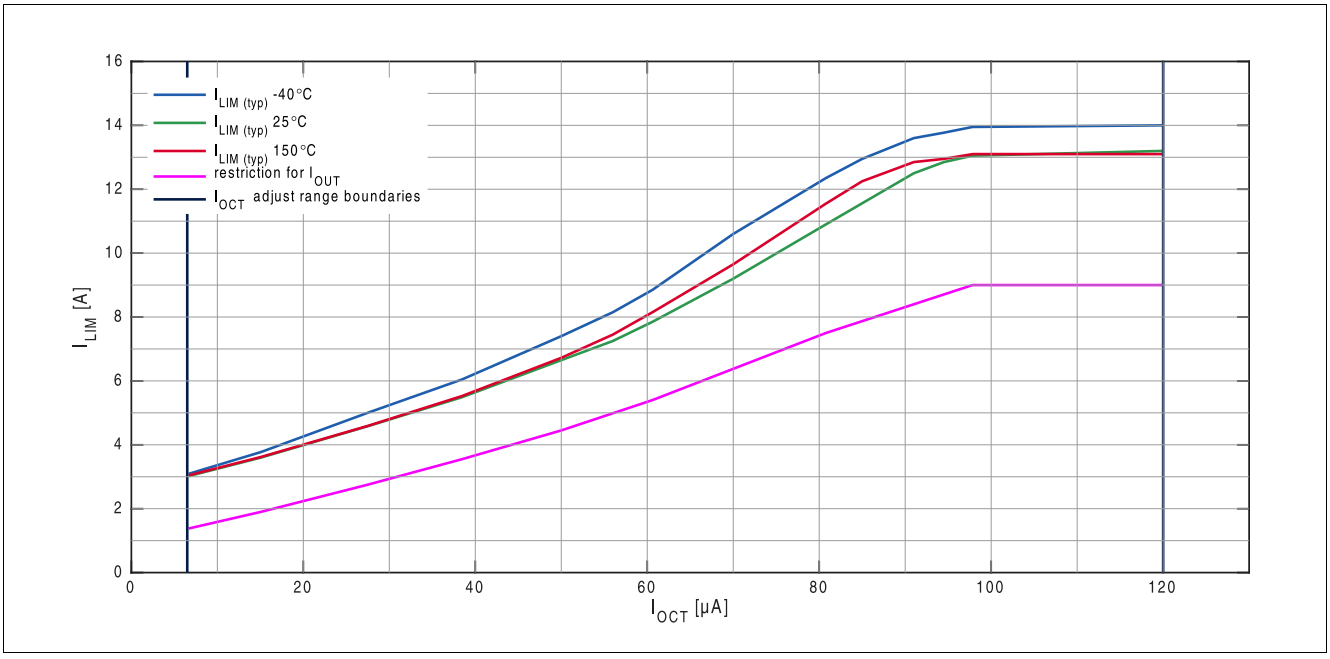


Figure 19 Typical values of the current limitation as function of the adjusted I_{OCT} current

1) For this reason R_{OCT} should always be placed as close as possible to the OCT-pin

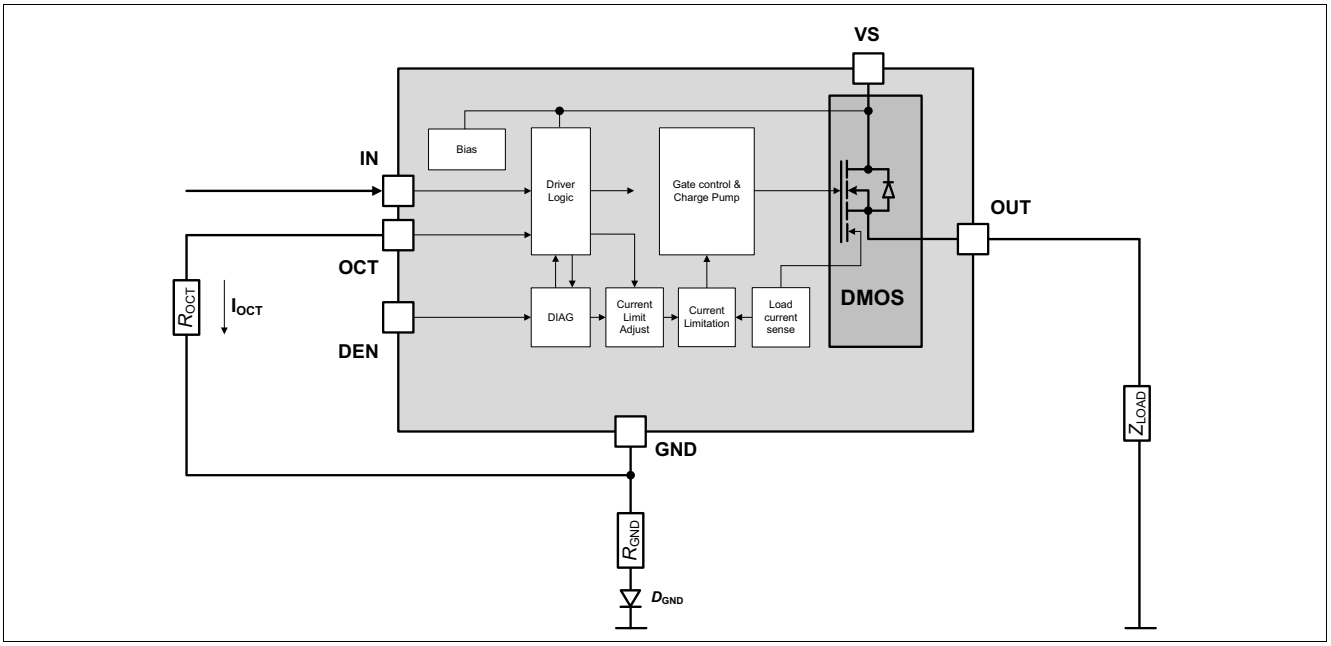


Figure 20 Adjustment of Current Limit threshold with external resistor R_{OCT}

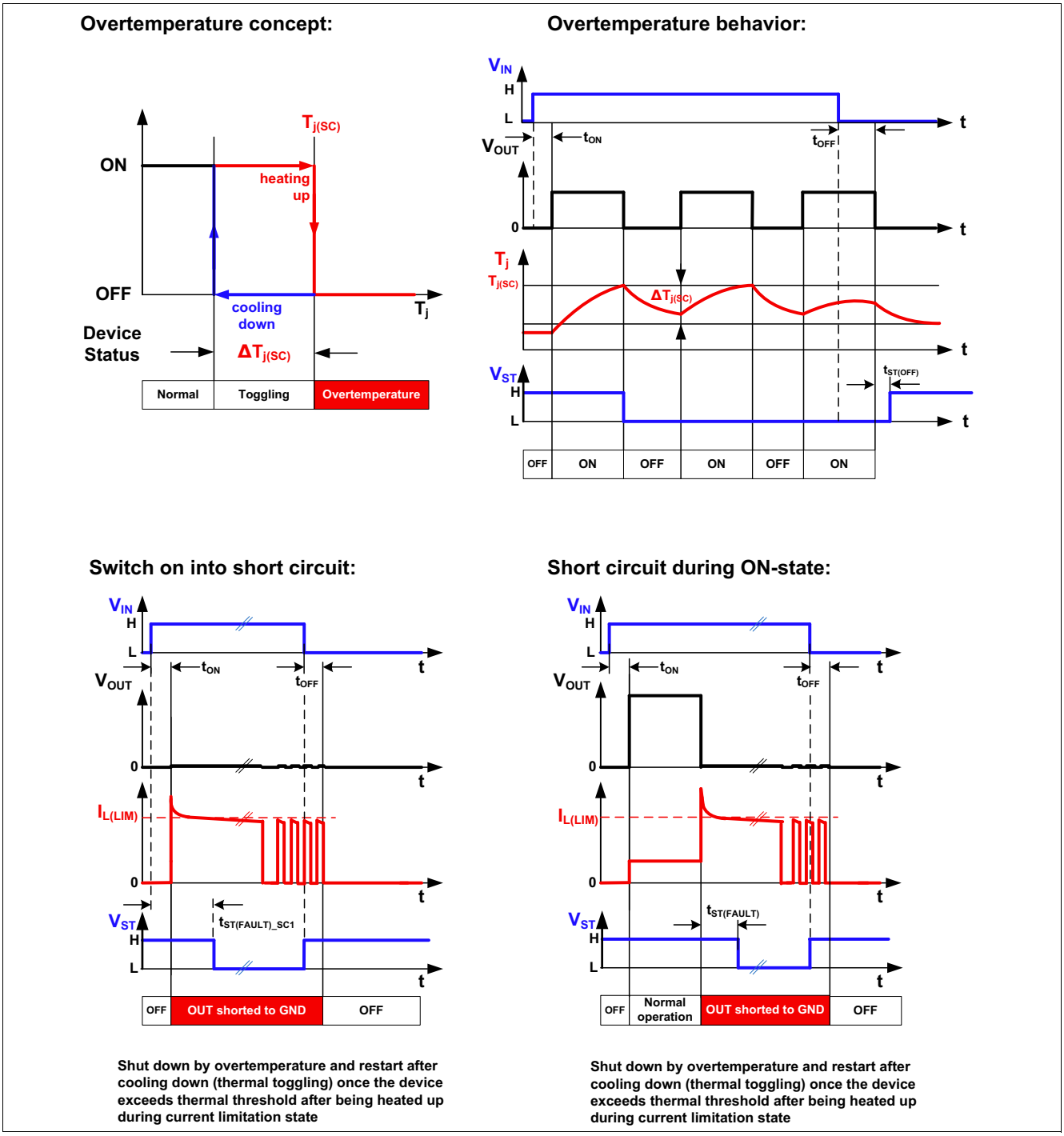


Figure 21 Protection behavior of the ITS4035S-EP-D

7.5.2 Temperature limitation in the power DMOS

The DMOS channel incorporates a temperature sensor concept that allows to detect the absolute junction temperature T_j as well as a temperature gradient resulting of a power stage that heats up too fast. Activation of any of the temperature sensors will cause an overheated channel to switch off to prevent destruction. Any protective overtemperature shutdown event triggered by an overheated channel switches off the output until the temperature reaches an acceptable value again.

A restart functionality is implemented that switches the channel on again after the DMOS temperature has sufficiently cooled down.

7.6 Electrical characteristics: Protection functions

Table 6 Electrical Characteristics: Protection Functions [1)]

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{OUT(GND)}$	–	0.1	–	mA	[2)] V_S = 24 V	P_7.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{DS(REV)}$	–	650	700	mV	I_L = -2 A; T_j = 150°C;	P_7.6.2
Overvoltage							
Overvoltage protection	$V_{S(AZ)}$	65	70	75	V	[3)] I_{SOV} = 5 mA	P_7.6.3
Current limitation							
Allowed I_{OCT} range for adjusting current limit threshold $I_{LIM(th,adj)}$	I_{OCT_range}	6.67	–	120	µA	[2)] –	P_7.6.4
OCT-pin voltage V_{OCT} (in ON- state)	V_{OCT}	–	0.5	–	V	V_{IN} = high; 6.67 µA ≤ I_{OCT} ≤ 120 µA	P_7.6.16
Current limitation with setting I_{OCT} < 6.67 µA (corresponds to R_{OCT} > 75 kΩ)							
Current limit when OCT-pin is detected open	$I_{LIM\_int(MIN)}$	–	2.63	–	A	[2) 5)]	P_7.6.46
Current limitation with setting I_{OCT} = 6.67 µA (corresponds to R_{OCT} = 75 kΩ)							
Current limitation I_{LIM} = I_{LIM}(I_{OCT}= 6.67 µA)	I_{LIM}	2.00	3.02	4.06	A	[4)] I_{OCT} = 6.67 µA (R_{OCT} = 75 kΩ); 25°C ≤T_j ≤ 150°C	P_7.6.19
Current limitation I_{LIM} = I_{LIM}(I_{OCT}= 6.67 µA)	I_{LIM}	1.78	3.09	4.37	A	I_{OCT} = 6.67 µA (R_{OCT} = 75 kΩ); T_j = -40°C	P_7.6.35
Current limitation with setting I_{OCT} = 27.47 µA (corresponds to R_{OCT} = 18.2 kΩ)							
Current limitation I_{LIM} = I_{LIM}(I_{OCT}= 27.47 µA)	I_{LIM}	3.28	4.58	5.85	A	[4)] I_{OCT}= 27.47 µA (R_{OCT} = 18.2 kΩ); 25°C ≤ T_j ≤ 150°C	P_7.6.37
Current limitation I_{LIM} = I_{LIM}(I_{OCT}= 27.47 µA)	I_{LIM}	3.32	5.00	6.58	A	I_{OCT}= 27.47 µA (R_{OCT} = 18.2 kΩ); T_j = -40°C	P_7.6.38

Table 6 Electrical Characteristics: Protection Functions [1)] (cont'd)

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

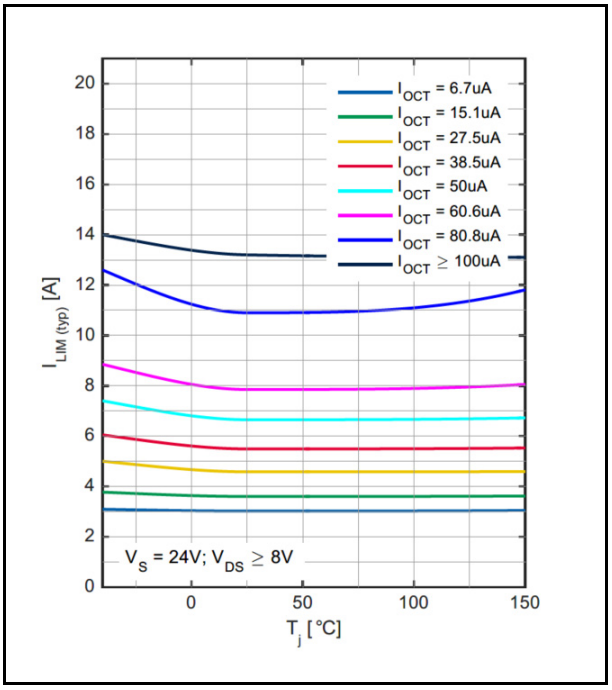
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current limitation with setting I_{OCT} = 50 µA (corresponds to R_{OCT} = 10 kΩ)							
Current limitation $I_{LIM} = I_{LIM}(I_{OCT}= 50.0\ µA)$	I_{LIM}	4.97	6.65	8.32	A	[4)] I_{OCT} = 50.0 µA (R_{OCT} = 10 kΩ); 25°C ≤T_j ≤ 150°C	P_7.6.22
Current limitation $I_{LIM} = I_{LIM}(I_{OCT}= 50.0\ µA)$	I_{LIM}	5.25	7.40	9.47	A	I_{OCT} = 50.0 µA (R_{OCT} = 10 kΩ); T_j = -40°C	P_7.6.41
Current limitation with setting I_{OCT} ≥ 97.85 µA (corresponds to R_{OCT} ≤ 5.11 kΩ)							
Current limit when OCT-pin is shorted to GND-pin or I_{OCT} exceeding upper specified range	$I_{LIM\_int(MAX)}$	10.00	13.20	15.85	A	[2) 5) 6)] I_{OCT} ≥ 97.85 µA; (R_{OCT} ≤ 5.11 kΩ) 25°C ≤T_j ≤ 150°C	P_7.6.6
Current limit when OCT-pin is shorted to GND-pin or I_{OCT} exceeds upper specified range	$I_{LIM\_int(MAX)}$	10.50	14.00	16.30	A	[2) 5) 6)] I_{OCT} ≥ 97.85 µA; (R_{OCT} ≤ 5.11 kΩ) T_j = -40°C	P_7.6.45
Thermal Protection							
Dynamic thermal shutdown protection threshold (temperature gradient within IC)	$T_{j(SW)}$	–	80	–	K	[2)] –	P_7.6.8
Thermal shutdown temperature (absolute T_J)	$T_{j(SC)}$	150	175	200	°C	[2)] –	P_7.6.10
Thermal shutdown hysteresis	$\Delta T_{j(SC)}$	–	30	–	K	[2)] –	P_7.6.11

1) Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC from destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are designed neither for continuous nor repetitive operation
2) Not subject to production test; specified by design
3) During transient overvoltage events the current through the GND path needs to be limited. It is recommended to place a resistor in the range of ≥ 27 Ω into the GND path if transient overvoltage events have to be considered in the application
4) Test at T_j = 150°C
5) Please note that operation above allowed I_{OCT} range is considered as fault condition and will be flagged on the ST-pin. For further details please refer to **Chapter 8.1** and **Chapter 8.2**
6) Without a properly dimensioned R_{OCT} the device can be damaged under reverse polarity condition

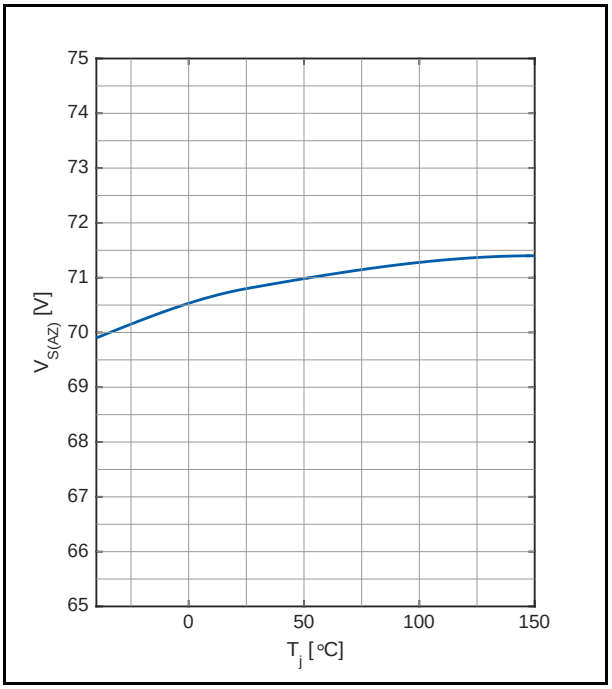
7.7 Typical performance characteristics protection functions

Typical performance characteristics

Current limit $I_{LIM(th,adj)}$ versus junction temperature T_j (as f(R_{OCT}, I_{OCT})



Clamping voltage $V_{S(AZ)}$ versus junction temperature T_j



8 Diagnostic functions

The ITS4035S-EP-D is able to provide detailed diagnosis information during operation. The diagnosis information can be split into basic diagnosis and extended diagnosis. The basic diagnosis is continuously monitored during the ON-state of the device and given as digital signal to the user via the ST-pin.

The ITS4035S-EP-D offers a diagnosis capability that comprise:

The basic diagnosis comprises:

- Overload/short circuit to GND
- Overtemperature
- Open load diagnosis (during OFF-state)[1)]
- Violation of minimum allowed R_{OCT} (e.g. OCT-pin shorted to GND)

In addition to the basic diagnosis there is also an extended diagnosis that needs to be requested by the DEN-pin.

The extended diagnosis comprises:

- Digital open load detection during OFF-state (in combination with external pull-up resistor)
- Digital feedback on Short to V_S during OFF-state (in combination with external pull-down resistor)
- Overtemperature during OFF-state
- I_{OCT} is monitored continuously in ON-state. If $I_{OCT} > I_{OCT(short2GND)}$, a fault state is flagged on ST during ON-state as long as DEN = low. In order to be able to distinguish this specific fault condition from overtemperature and overload or overvoltage faults, this flag is blanked if DEN is set to high but re-flagged if DEN is set to low again in case the fault condition persists, as shown in **Table 7**.

Figure 22 and **Figure 23** illustrate the timings of basic and extended diagnosis functionality while **Figure 24** shows a simplified application example.

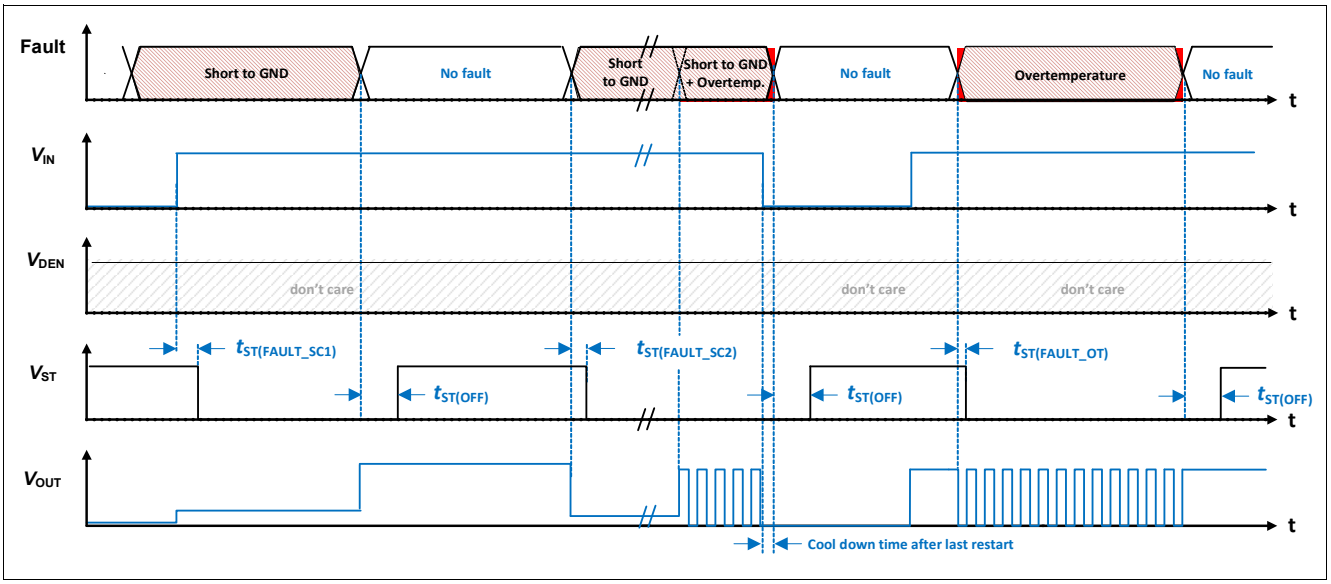


Figure 22 Behavior and timings of diagnostic features

1) Open load in OFF - diagnosis needs to be requested by DEN = high

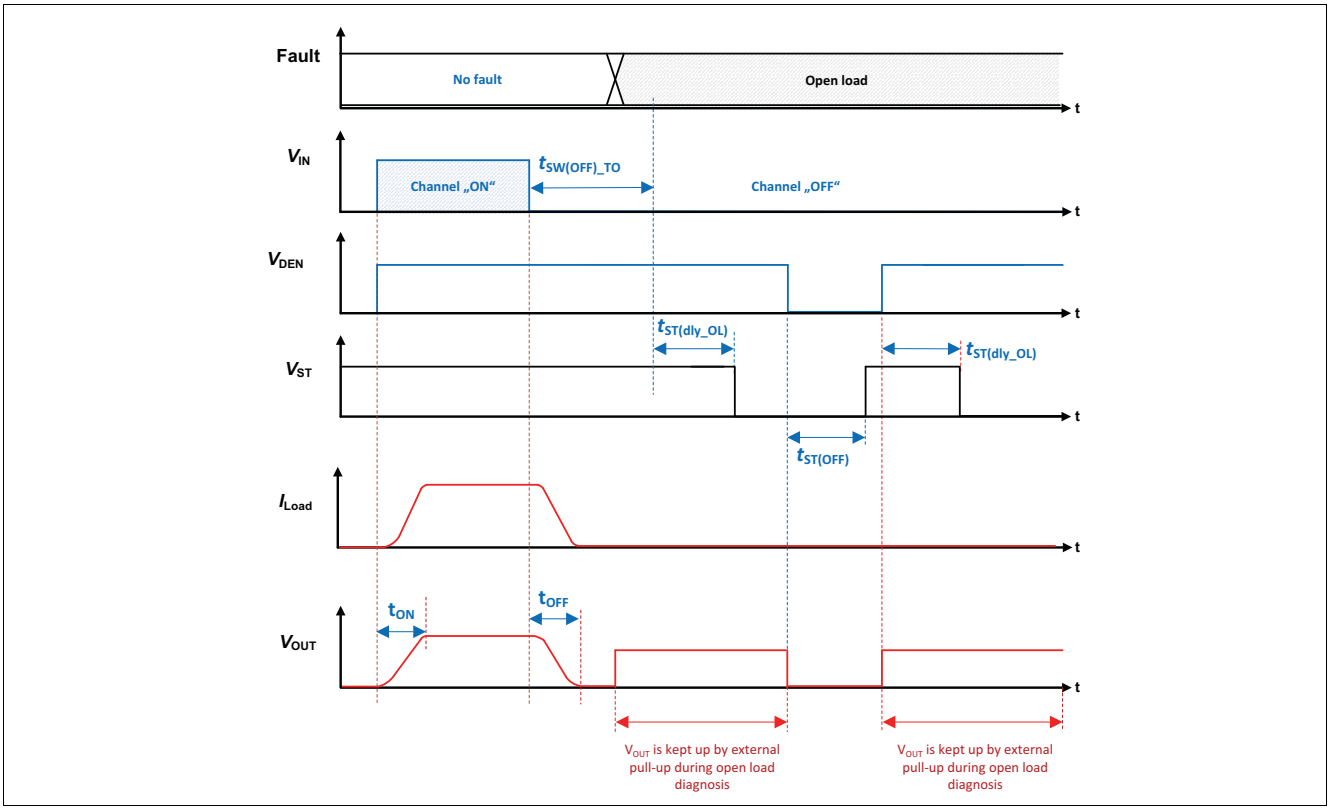


Figure 23 Behavior and timings of the extended diagnostic capabilities (the usage of a DEN - controlled switchable pull-up resistor from OUT to V_S in OFF-state is assumed)

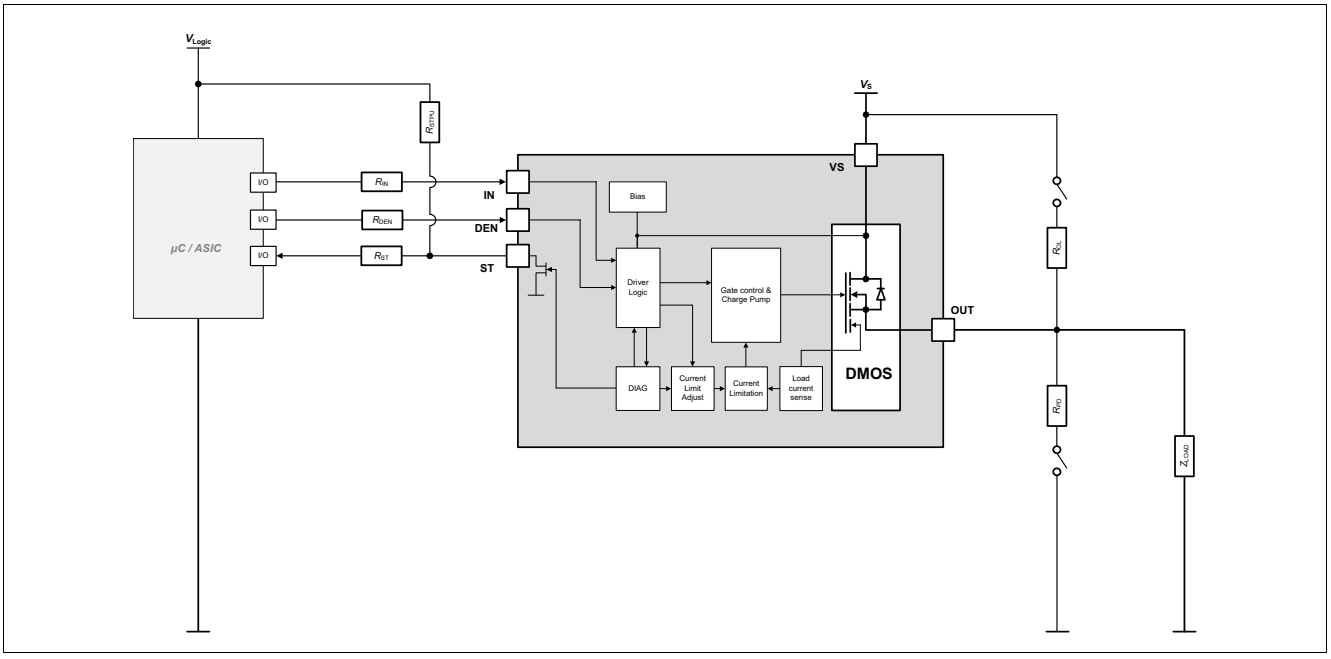


Figure 24 Overview: usage of diagnosis

8.1 Digital status flag ST (STATUS)

The ITS4035S-EP-D provides a digital signal for diagnostic information on the ST-pin. This signal is called STATUS. The ST-pin is realized as open drain output and must be connected to an external pull-up resistor to either logic supply or to V_S. During normal operation the STATUS signal is logic high (H). When the device is in

Diagnostic functions

ON-state the presence of the fault conditions short circuit to ground, overtemperature or a violation of the allowed minimum resistance of R_{OCT} is flagged by a logic low (L) level on the ST-pin. **Table 7** shows the truth table of the ST-pin output. In addition, the extended diagnosis information for detection of open load is also flagged on the ST-pin during OFF-state indicating the presence of an open load condition (OL) in OFF. Open load in OFF-state will be flagged on the ST only after the blanking time $t_{ST(dly\_OL)}$ has elapsed which means after the device has been monitored in this fault condition continuously throughout the blanking time. The blanking time counter for $t_{ST(dly\_OL)}$ is always started with the rising DEN edge except directly after switching off the channel. After switching off the channel the open load blanking time counter is started earliest after the switch off time-out delay $t_{SW\_OFF\_TO}$. This means that an open load fault in OFF-state can be detected earliest after $t_{SW\_OFF\_TO}$ + $t_{ST(dly\_OL)}$ referenced to the falling IN edge. The open load detection in OFF-state is realized by a voltage comparator at the output. If the output voltage stays or gets closer to V_S than a threshold (V_S - $V_{OUT(OL)}$) for a duration of t > $t_{ST(dly\_OL)}$ the flag is set. This means that for open load detection in OFF-state an external pull-up resistor to V_S must be applied. Adjusting the resistance of the pull-up resistor allows to adjust the desired open load criteria. [1)]

Open load diagnosis in OFF-state must be requested via the DEN signal. Without setting the DEN-pin to high no open load diagnosis is flagged on ST.

Table 7 Diagnostic Truth Table ST-pin

Condition	IN	DEN [1)]	OUT	ST [2)]	Comment
ON-state					
Normal Operation	H	X	ON	H	–
Short circuit to GND	H	X	ON	L	–
Overtemperature in ON-state [3)]	H	X	OFF [4)]	L	–
I_{OCT} exceeding the specified range (e.g. if OCT-pin is shorted to GND)	H	L	ON	L	[5)] I_{OCT} is monitored continuously in ON-state. If I_{OCT} > $I_{OCT(short2GND)}$ a fault state is flagged on ST during ON-state as long as DEN = low. In order to be able to distinguish this specific fault condition from overtemperature and overload faults, this flag is blanked if DEN is set to high but re-flagged if DEN is set to low again in case the fault condition persists
	H	H	ON	H	
OFF-state					
Open load condition while device is in OFF-state	L	L	OFF	H	Open load in OFF not diagnosed unless extended diagnosis requested by DEN = high
Open load condition while device is in OFF-state [6)]	L	H	OFF	L	[7) 8)] Requires external pull-up attached from OUT to V_S
Any fault condition	L	L	OFF	H	–

1) In the same manner also short circuit to V_S can be realized with a pull-down resistor. In both cases it is recommended to use pull-up or pull-down circuits that can be switched off while not being used to minimize power dissipation

Table 7 Diagnostic Truth Table ST-pin (cont'd)

Condition	IN	DEN [1]	OUT	ST [2]	Comment
OUT shorted to V_S while device is in OFF-state [6]	L	H	OFF	L	[7] [8] Requires external pull-down attached from OUT to GND
Overtemperature in OFF-state	L	H	OFF	L	–

1) X denotes that logic level of DEN is irrelevant (don't care)
2) External pull-up resistor needs to be placed at ST-pin
3) This fault condition can be caused by both - a violation of the maximum allowed T_j but as well by exceeding the maximum allowed temperature gradient $T_{j(SW)}$ within the IC
4) Automatic restart after T_j has sufficiently cooled down
5) Please note that $t_{ST(OFF)}$ will apply when DEN is set from low to high until ST-flag for indicating I_{OCT} outside the limits is cleared
6) Diagnosis of open load in OFF-state and diagnosis OUT shorted to V_S cannot be evaluated simultaneously. If both diagnosis features are applied in the same application the corresponding required external pull-up or pull-down circuits must be controlled with external switches
7) Flag will be set after blanking time $t_{ST(dly\_OL)}$ has elapsed
8) Please note that for this fault condition the ST flag is reset directly after the fault situation has cleared. $t_{ST(OFF)}$ does not apply

8.2 Electrical characteristics: Diagnostic functions

Table 8 Electrical characteristics: Diagnostic functions

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Basic diagnostics (ST-pin)							
Status settling time for channel start-up into existing overload [1] (from IN slope to ST low)	$t_{ST(FAULT\_SC1)}$	–	50	–	µs	$V_{DS} \geq$ 5 V	P_9.4.1
Status settling time for channel entering short circuit condition during ON-state (from point where SC is reached to ST low)	$t_{ST(FAULT\_SC2)}$	–	25	–	µs	[2] $V_{DS} \geq$ 5 V	P_9.4.2
Status settling time for over-temperature indication on ST-pin	$t_{ST(FAULT\_OT)}$	–	5	–	µs	[2] –	P_9.4.3
Status blanking time for open load detection (device in stable OFF-state)	$t_{ST(dly\_OL)}$	–	130	–	µs	–	P_9.4.4
Time-out before status blanking delay timer for open load diagnostics can be started after entering OFF-state	$t_{SW(OFF)\_TO}$	–	195	260	µs	–	P_9.4.34
Status reset blanking time	$t_{ST(OFF)}$	–	120	–	µs	[2] –	P_9.4.26
Low level status voltage	$V_{ST(L)}$	–	–	0.5	V	[3] I_{ST} = 1.6 mA	P_9.4.5
Open load detection voltage threshold in OFF-state	V_S - $V_{OUT(OL)}$	4	4.45	6	V	[4] V_{IN} = low; V_{DEN} = high	P_9.4.10

Table 8 Electrical characteristics: Diagnostic functions (cont'd)

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

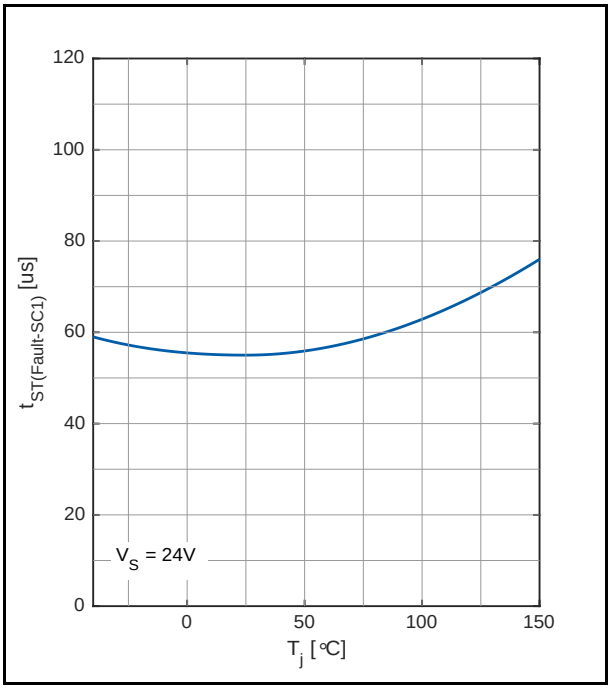
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
OCT-pin short to ground detection threshold in ON-state	$I_{OCT(short2GND)}$	150		240	µA	5) V_{IN} = high; V_{DEN} = low; I_{OCT} exceeding allowed range to higher values (ST will go from high to low	P_9.4.30
OCT-pin short to ground reset threshold in ON-state (hysteresis)	$I_{OCT(S2G\_reset)}$	–	175	–	µA	5) V_{IN} = high; V_{DEN} = low; I_{OCT} going from fault range to pass range (ST will go from low to high	P_9.4.37

1) This parameter describes the status settling time when a channel is switched on into an already existing overload condition. This parameter is referenced to the edge of the input pin, IN that switches the channel into overload
2) Not subject to production test, specified by design
3) Levels referenced to device ground
4) Level for open load detection in OFF referenced to V_S
5) This fault is only reported as long as DEN = low

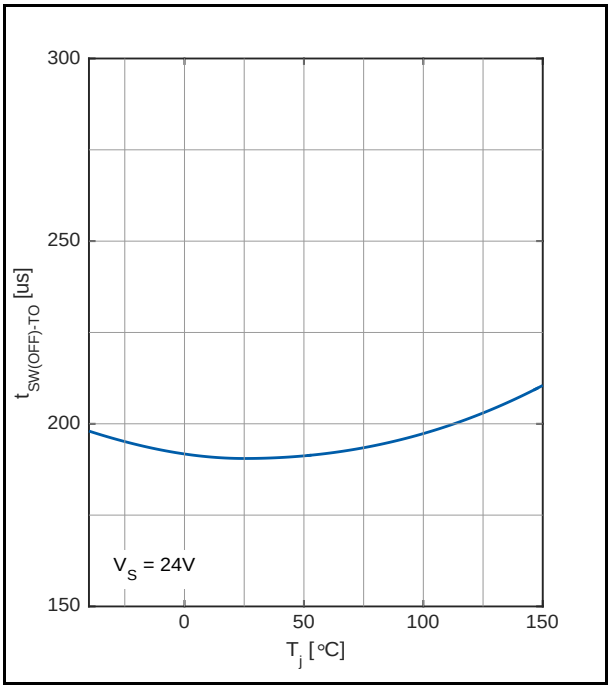
8.3 Typical performance characteristics: Diagnostic functions

Typical performance characteristics

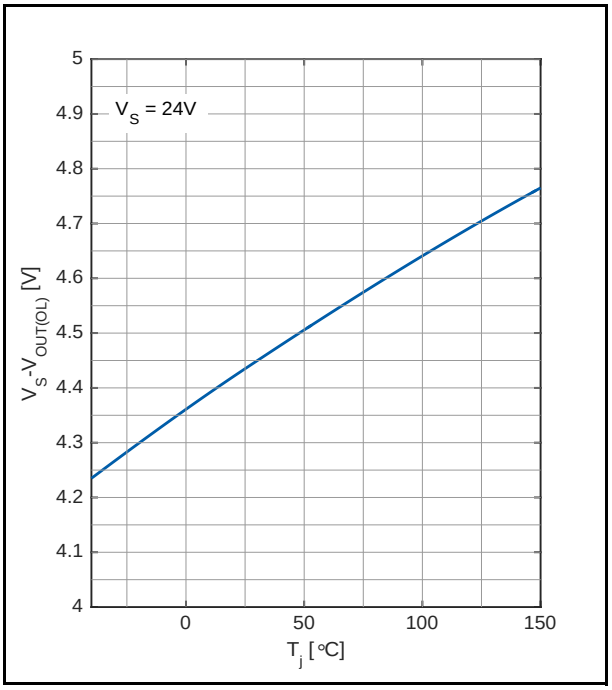
Status settling Time $t_{ST(FAULT\_SC1)}$ versus Junction temperature T_j (switch on into overload)



Time-out delay $t_{SW(OFF)\_TO}$ versus Junction temperature T_j



Open load threshold V_S - $V_{OUT(OL)}$ versus Junction temperature T_j



9 Control input pins

9.1 Input pin circuitry of control pins (IN and DEN)

The IN-pin and DEN-pin circuitry are compatible with 3.3 V and 5 V microcontrollers as well as input levels up to V_S [1]. The concept of the input pin is to react to voltage thresholds which are referenced to device ground. An implemented Schmitt trigger avoids an undefined state if the voltage on the control pin is slowly increasing or decreasing. The output is either OFF or ON but cannot be in a linear or undefined state. The input circuitry of the control pins is compatible with PWM applications. **Figure 25** shows the electrical equivalent input pin circuitry.

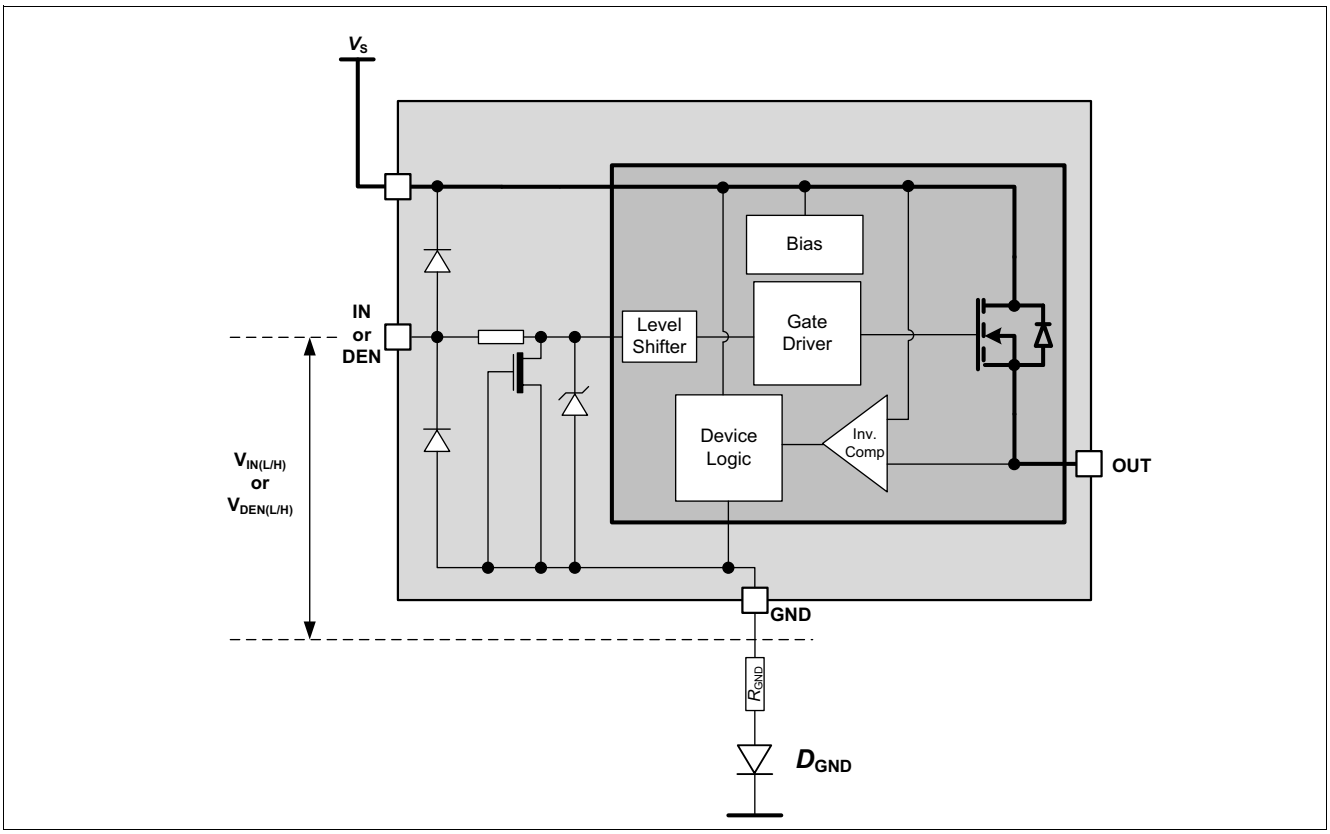


Figure 25 Input pin circuitry

9.2 Input pin voltage (IN and DEN)

The control pins IN and DEN use a comparator with hysteresis which is implemented in order to improve immunity to noise. Switching on/off of the channel takes place in a defined region, set by the thresholds $V_{IN(L),MAX}$ and $V_{IN(H),MIN}$.

1) V_{IN} must not exceed V_S. The relation $V_{IN} \leq V_S$ must always be fulfilled

9.3 Electrical characteristics: Control input pins

Table 9 Electrical characteristics: Input pins

V_S = 8 V to 36 V, T_j = -40°C to 150°C (unless otherwise specified)
Typical values are given at V_S = 24 V, T_j = 25°C

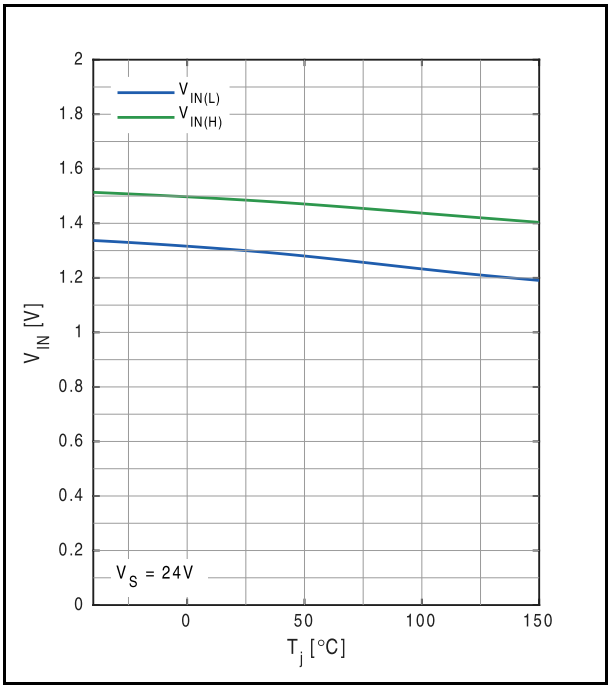
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input pins characteristics							
Low level input voltage range	$V_{IN(L)}$ $V_{DEN(L)}$	-0.3	–	0.8	V	1) –	P_10.3.1
High level input voltage range	$V_{IN(H)}$ $V_{DEN(H)}$	2	–	V_S	V	1) $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_10.3.2
Input voltage hysteresis	$V_{IN(HYS)}$ $V_{DEN(HYS)}$	–	250	–	mV	2) –	P_10.3.3
Low level input current	$I_{IN(L)}$ $I_{DEN(L)}$	–	35	70	µA	V_{IN} = 0.8 V V_{DEN} = 0.8V	P_10.3.4
High level input current	$I_{IN(H)}$ $I_{DEN(H)}$	–	35	70	µA	V_{IN} = 24 V V_{DEN} = 24 V $V_S \geq V_{IN}$; $V_S \geq V_{DEN}$	P_10.3.5

1) Levels referenced to device ground
2) Not subject to production test; specified by design

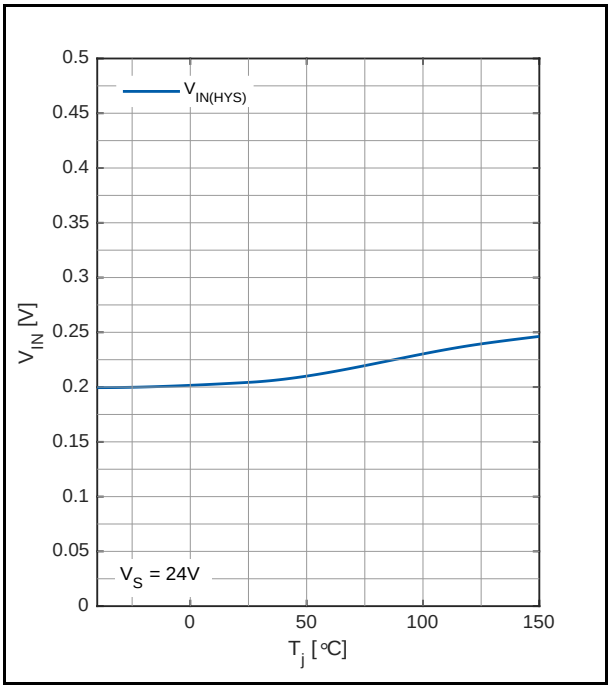
9.4 Typical performance characteristics: Input pins

Typical performance characteristics

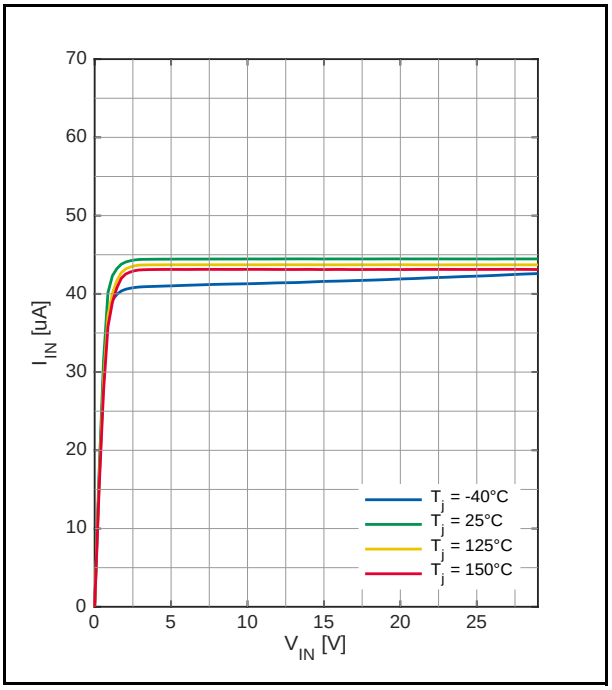
Input voltage thresholds $V_{IN(L)}$ $V_{IN(H)}$ versus Junction temperature T_j



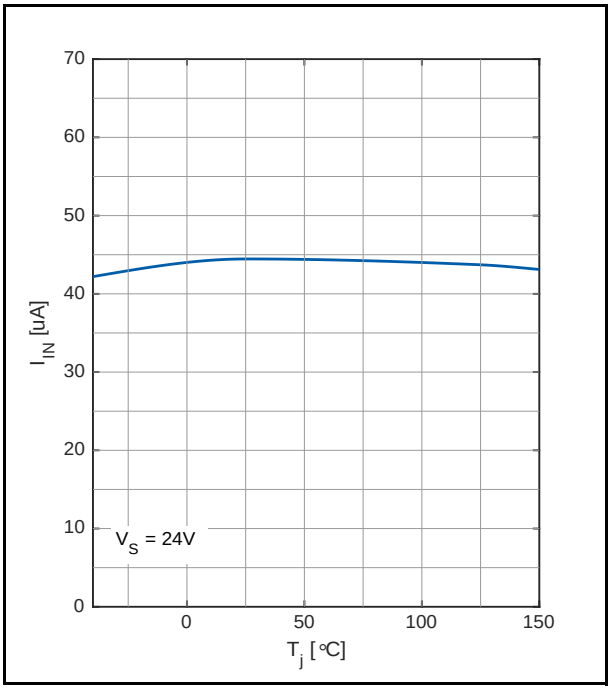
Input voltage hysteresis $V_{IN(HYS)}$ versus Junction temperature T_j



Input pin current $I_{IN(H)}$ versus Supply voltage V_S

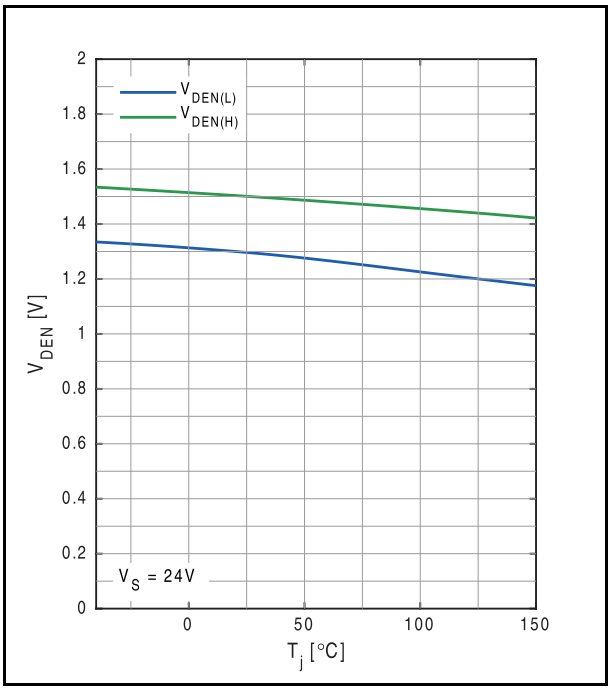


Input pin current $I_{IN(H)}$ versus Junction temperature T_j

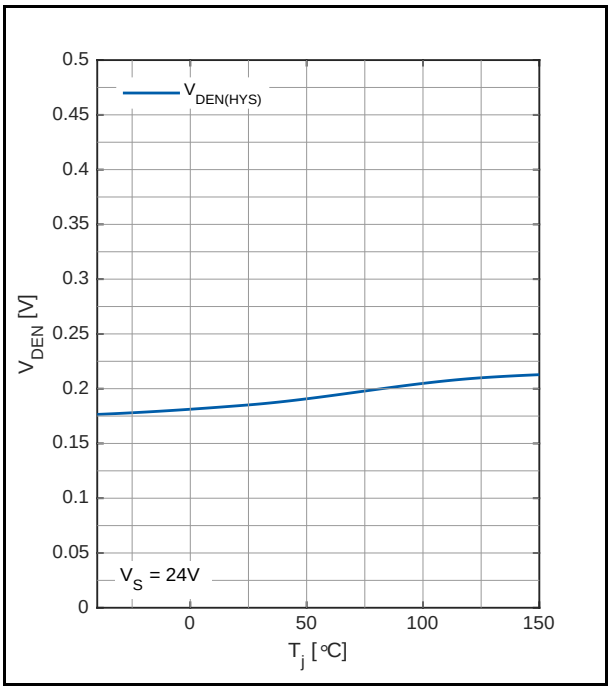


Control input pins

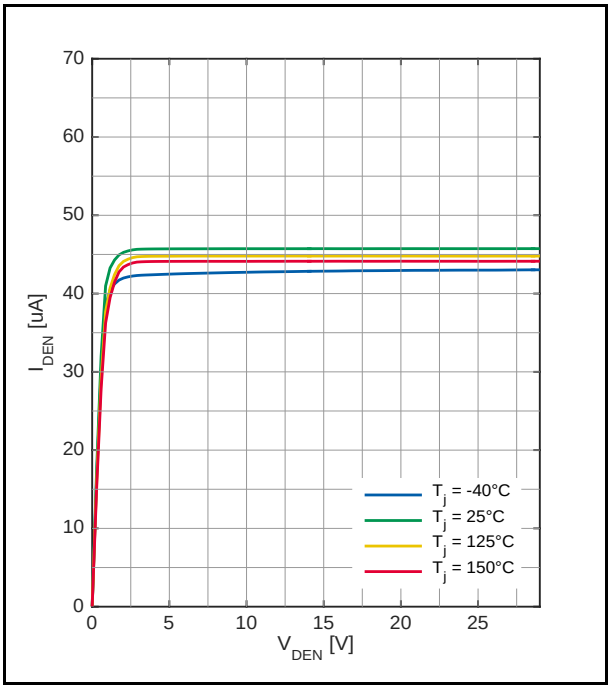
Input voltage thresholds $V_{DEN(L)}$ $V_{DEN(H)}$ versus Junction temperature T_j



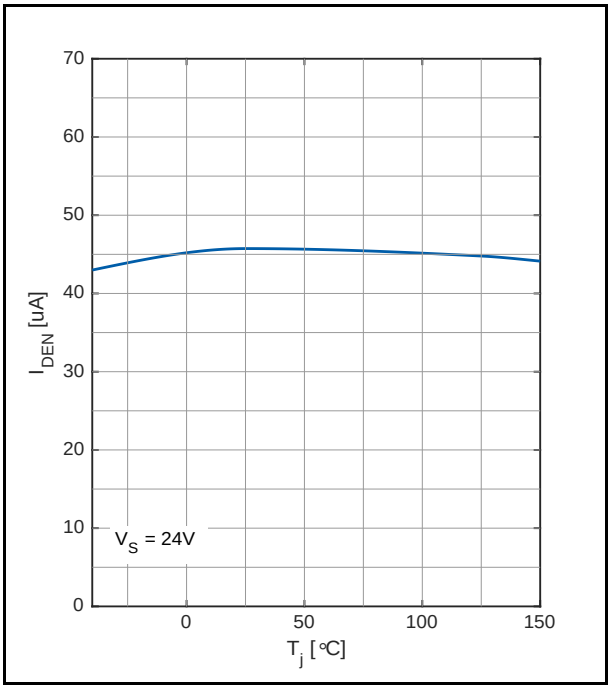
Input voltage hysteresis $V_{DEN(HYS)}$ versus Junction temperature T_j



Input pin current $I_{DEN(H)}$ versus Supply voltage V_S



Input pin current $I_{DEN(H)}$ versus Junction temperature T_j



10 Application information

10.1 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Figure 26 and **Figure 27** show two simplified application examples where the ITS4035S-EP-D is directly controlled by logic levels of a microcontroller. In **Figure 27** the current limitation can be controlled by a microcontroller pin. It is furthermore recommended to place serial input resistors at the interface pins to the microcontroller (IN/DEN) in order to protect the external control circuitry and the input structures of the ITS4035S-EP-D under fault conditions (e.g. reverse polarity, loss of ground or overvoltage).

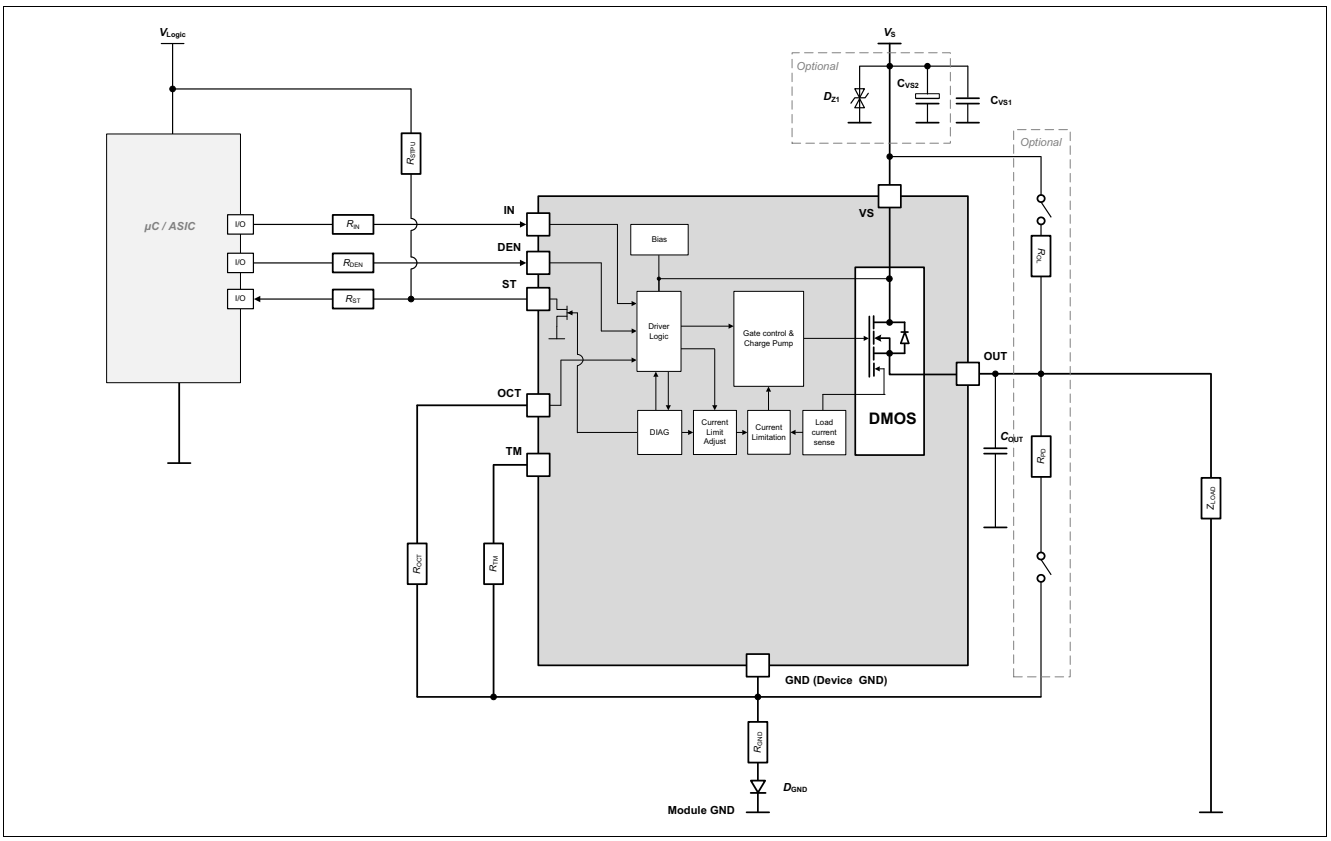


Figure 26 Application diagram with ITS4035S-EP-D

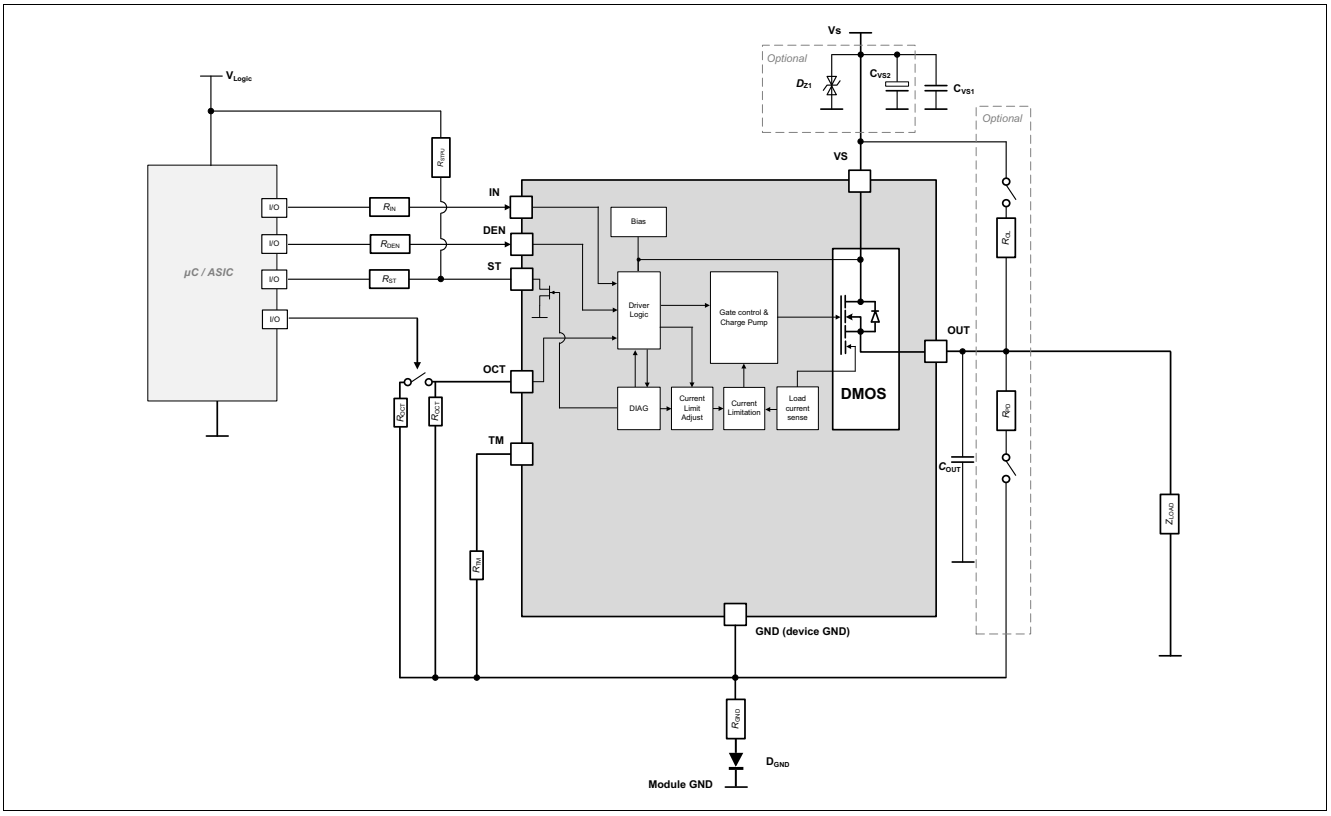


Figure 27 Application diagram with ITS4035S-EP-D controlled by logic levels (µC] with dynamic inrush current control

10.2 External components for protection

Some of the features of the ITS4035S-EP-D require external components in order to work properly inside the application.

Table 10 Suggested component values

Reference	Value	Purpose
R_{IN}	10 kΩ	Protection of the external control circuitry and the input structures under fault conditions (e.g. reverse polarity, loss of ground or overvoltage)
R_{DEN}	10 kΩ	Protection of the external control circuitry and the input structures under fault conditions (e.g. reverse polarity, loss of ground or overvoltage)
R_{ST}	10 kΩ	Protection of the external control circuitry and the input structures under fault conditions (e.g. reverse polarity, loss of ground or overvoltage)
R_{TM}	2.2 kΩ	Must be connected with a serial resistor to device GND for proper functionality
R_{STPU}	10 kΩ	Pull up resistor for open drain status output
R_{OCT}	–	Adjustable overcurrent limitation resistor connected to device ground. Protection of the device during overvoltage and reverse polarity. Please refer to **Table 11**
R_{GND}	27 Ω	To limit the GND current at a safe value during ISO pulse
D_{GND}	BAS21	Protection of the ITS4035S-EP-D during reverse polarity

Table 10 Suggested component values (cont'd)

Reference	Value	Purpose
D_{Z1}	54 V TVS Diode	Transient voltage suppressor diode. Protection during overvoltage and in case of loss of supply while driving an inductive load
C_{VS1}	100 nF	Filtering of voltage spikes on the supply line
C_{VS2}	10 µF	Supply voltage buffer capacitor at supply
R_{OL}	1.5 kΩ	Output polarization (pull-up). Ensure polarization of the output during open load in OFF diagnosis
R_{PD}	47 kΩ	Output polarization (pull-down). Ensures polarization of the outputs to distinguish between open load and short to VS in OFF diagnosis
C_{OUT}	10 nF	Protection of the output during ESD and BCI

10.2.1 Protection of GND path during fault conditions

During specific fault conditions the GND path of the device needs to be protected in order to avoid excessive stress to the device or potential destruction. The most important fault conditions are reverse polarity, transient overvoltage spikes or pulses that are exceeding the absolute maximum ratings of the device. The recommended GND protection in case of reverse polarity is to place a diode into the GND path. This solution is also depicted in the application diagrams. Reverse polarity cannot only be an issue in case of unintended wrong wiring of V_S and GND but may occur as well transiently in combination with pulses at VS or OUT.

If surge pulses (e.g. according IEC61000-4-5) have to be considered the usage of a TVS-protection diode at VS or a comparable protection device is mandatory because the energy content of such pulses is by far higher than what the ITS4035S-EP-D can absorb within the duration of the pulse. The chosen TVS diode for this purpose must provide a clamp voltage that is safely lower than the internal overvoltage clamp $V_{S(AZ)}$ of the ITS4035S-EP-D and should be fast enough to clamp fast transient overvoltage spikes. If by the choice of the TVS-diode or by the nature of the application transient overvoltage spikes > $V_{S(AZ)}$ can be safely excluded the above mentioned blocking diode is sufficient for protecting the GND path. However, in cases where overvoltage spikes > $V_{S(AZ)}$ at VS still need to be considered a resistor in series to the diode needs to be placed in the GND path that limits the current through the GND path during such transient overvoltage events (see also **Chapter 7.3.1**). In such cases where a resistor in series to the external diode needs to be placed in the GND path also the resulting GND-shifts need to be considered.

10.2.2 Input resistors for I/O pins

During fault conditions (e.g. reverse polarity, loss of GND, transient pulses at V_S or OUT, etc.) where the potential of I/O pins may become lower than the potential of device GND or where it may rise above the voltage being present at the VS-pin the ESD protection diodes of the corresponding I/O pins have to be protected by limiting the current through the pin by an external resistor. For the control pins IN and DEN a value of 10 kΩ for an input resistor will be fitting for a broad range of applications.

To use the status functionality, an external pull-up resistor needs to be placed at the ST-pin. This pull-up resistor must be dimensioned in a way that the ST-pin current during fault conditions is not exceeding the maximum ratings given in **Table 1 "Absolute maximum ratings" on Page 8**. Therefore the dimensioning of the pull-up resistor will depend on whether it is connected to V_S or to the logic supply rail of the microcontroller. In addition, an input resistor R_{ST} to the microcontroller interface needs to be placed in the same manner and for the same reasons as mentioned above for the control pins IN and DEN.

The OCT-pin will be protected by R_{OCT} in case of reverse polarity. This is also one reason that the OCT-pin must not be directly tied to device GND even if the highest possible current limitation threshold should be used. A corresponding fault flag will be set, if I_{OCT} exceeds the current threshold $I_{OCT(short2GND)}$ [1].

10.3 Current limitation adjustment

Table 11 below indicates which resistor value R_{OCT} needs to be soldered between OCT-pin and device GND to obtain a desired current limitation threshold $I_{LIM(th,adj)}$. The adjusted current limitation threshold is defined for ambient temperature (T_j = 25°C) and hence, these values coincide with the typical values of the current limit at 25°C. **Table 11** provides an overview about the related minimum and maximum values of the current limit. The column "Typical of maximum allowable I_{OUT} [A]" provides information about the required distance of the output current to the adjusted current limit setting in order to avoid unwanted activation of the current limitation circuit during normal operation.

This clearance needs to be respected for the nominal load current of a given application and represents an upper limit for the allowable nominal load current [2]. As the typical values of a selected current limit do not vary significantly from T_j = 25°C up to T_j = 150°C for most of the I_{OCT} - settings the given maximum and minimum values of the current limit listed in **Table 11** hold true for the temperature range 25°C ≤ T_j ≤ 150°C. Deviations that have to be expected for the typical values of the current limit at 150°C can be seen in **Figure 28**.

Figure 28 moreover illustrates how the current limitation values will shift for low temperatures. **Table 12** provides typical values for the current limitation for the extreme case of T_j = -40°C and an overview of corresponding minimum and maximum values for the current limitations.

Using R_{OCT} resistor values ≤ 5 kΩ will always result in the current limitation value of the device which represents the maximum current limit value. In this way the application is still protected with the current limitation if the OCT-pin is accidently shorted to GND. Nevertheless R_{OCT} < 5.11 kΩ must not be used in applications as the susceptibility to EMC influences may increase. For the same reason the R_{OCT} resistor always has to be placed as close as possible to the OCT-pin and avoiding long traces with high inductances. Please note that for excessive I_{OCT} currents also a diagnosis flag will be set when reaching the corresponding threshold $I_{OCT(short2GND)}$ [3].

Using R_{OCT} values above 75 kΩ will bring the current limitation outside the allowed lower boundary of the current limit adjust range. It is not recommended to operate the device outside the allowed current limitation adjust range because the accuracy will decrease and stability of the regulation may suffer.

Table 11 R_{OCT} resistor value selection guide for adjusting current limitation threshold $I_{LIM(th,adj)}$ and overview of resulting current limitation data (typical values & expected range) for temperature range 25°C ≤ T_j ≤ 150°C

R_{OCT} [kΩ]	I_{OCT} [µA]	$I_{LIM(th,adj)}$ [A] (T_j = 25°C) [1]	$I_{LIM,MIN}$ [A] (25°C≤T_j≤150°C)	$I_{LIM,MAX}$ [A] (25°C≤ T_j ≤150°C)	Typical of max allowable I_{OUT} [A] [2]	Comment
< 5.11 [3]	> 97.85	13.20	10.0	15.85	9.00	[4]
5.11	97.85	13.20	10.0	15.85	9.00	[5]
5.36	93.28	12.58	9.48	15.76	8.60	[6]

1) The corresponding flag is set in ON-state conditionally if DEN = low. See for further details

2) Independent of this electrical restriction possibly additional restrictions due to thermal constraints may apply depending on the load current and thermal properties of the PCB

3) This fault flag will be set only in ON-state and will depend on the logic state of the DEN-pin so that it can be distinguished from other fault situations by changing the logic state of DEN to high. For further information please refer to **Chapter 8.1**

Table 11 R_{OCT} **resistor value selection guide for adjusting current limitation threshold** $I_{LIM(th,adj)}$ **and overview of resulting current limitation data (typical values & expected range) for temperature range 25°C ≤** T_j **≤ 150°C**

R_{OCT} [kΩ]	I_{OCT} [µA]	$I_{LIM(th,adj)}$ [A] (T_j = 25°C) [1]	$I_{LIM,MIN}$ [A] (25°C≤T_j≤150°C)	$I_{LIM,MAX}$ [A] (25°C≤ T_j ≤150°C)	Typical of max allowable I_{OUT} [A] [2]	Comment
5.62	88.97	12.00	8.99	15.67	8.22	[6]
5.90	84.75	11.43	8.51	15.58	7.85	[6]
6.19	80.78	10.90	8.06	15.50	7.50	[5]
6.65	75.19	10.05	7.48	14.00	6.92	[6]
7.15	69.93	9.26	6.93	12.58	6.37	[6]
7.68	65.10	8.53	6.43	11.28	5.87	[6]
8.25	60.61	7.85	5.96	10.06	5.40	[5]
9.09	55.01	7.22	5.44	9.14	4.90	[6]
10.0	50.00	6.65	4.97	8.32	4.45	[7]
11.0	45.45	6.19	4.61	7.76	4.10	[6]
12.1	41.23	5.77	4.29	7.24	3.77	[6]
13.0	38.46	5.49	4.08	6.90	3.55	[5]
15.0	33.33	5.07	3.70	6.41	3.18	[6]
18.2	27.47	4.58	3.28	5.85	2.75	[8]
21.5	23.26	4.25	3.02	5.45	2.46	[6]
26.7	18.73	3.89	2.74	5.03	2.15	[6]
33.2	15.06	3.60	2.51	4.68	1.90	[5]
39.2	12.76	3.44	2.37	4.51	1.76	[6]
56.2	8.90	3.17	2.14	4.22	1.52	[6]
75.0	6.67	3.02	2.00	4.06	1.25	[9]
> 75.0	< 6.67	–	–	–	–	outside specified range [10]

1) $I_{LIM(th,\ adj)}$ values coincide with typical values of the current limit I_{LIM} @ 25°C. Typical values for I_{LIM} @ 150°C may show deviation from $I_{LINM(th,\ adj)}$; see **Figure 28** for further details

2) The listed values for I_{OUT} indicate the required clearance of the output current from the adjusted current limit without being at risk to interact. These values can be used as a maximum nominal current if there is no constraint from a thermal point of view

3) R_{OCT} value must be selected in a way, that I_{OCT} current does not exceed $I_{OCT(short2GND)}$. Please be aware that if the OCT-pin is connected with a too low R_{OCT} resistor to device GND the device will not be protected appropriately against reverse polarity. The device must not be operated with OCT-pin shorted to device GND

4) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} ≥ 97.85 µA (corresponds to R_{OCT} ≤ 5.11 kΩ)**

5) Not subject to production test, values specified by design

6) Values given in this line are based on interpolation of corresponding neighboring specified values

7) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} = 50 µA (corresponds to R_{OCT} = 10 kΩ)**

8) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} = 27.47 µA (corresponds to R_{OCT} = 18.2 kΩ)**
9) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} = 6.67 µA (corresponds to R_{OCT} = 75 kΩ)**
10) R_{OCT} values > 75k are not allowed for usage as the accuracy of the current limit will degrade

Table 12 R_{OCT} resistor value selection guide for adjusting current limitation threshold $I_{LIM(th,adj)}$ and an overview of resulting current limitation data (typical values & expected range) for low temperatures T_j = -40°C

R_{OCT} [kΩ]	I_{OCT} [µA]	$I_{LIM,TYP}$ [A] (T_j = -40°C)	$I_{LIM,MIN}$ [A] (T_j = -40°)	$I_{LIM,MAX}$ [A] (T_j= -40°C)	Typical of max allowable I_{OUT} [A] [1]	Comment
≤ 5.11 [2]	≥ 97.85	14.00	10.50	16.30	9.00	[3]
5.11	97.85	14.00	10.50	16.30	9.00	[4]
5.36	93.28	13.63	9.99	16.30	8.60	[5]
5.62	88.97	13.28	9.51	16.30	8.22	[5]
5.90	84.75	12.93	9.05	16.30	7.85	[5]
6.19	80.78	12.60	8.60	16.30	7.50	[4]
6.65	75.19	11.56	7.94	14.92	6.92	[5]
7.15	69.93	10.58	7.32	13.62	6.37	[5]
7.68	65.10	9.68	6.75	12.43	5.87	[5]
8.25	60.61	8.85	6.22	11.32	5.40	[4]
9.09	55.01	8.08	5.71	10.34	4.90	[5]
10.0	50.00	7.40	5.25	9.47	4.45	[6]
11.0	45.45	6.87	4.86	8.82	4.10	[5]
12.1	41.23	6.37	4.50	8.22	3.77	[5]
13.0	38.46	6.05	4.26	7.83	3.55	[4]
15.0	33.33	5.56	3.82	7.24	3.18	[5]
18.2	27.47	5.00	3.32	6.58	2.75	[7]
21.5	23.26	4.58	2.98	6.11	2.46	[5]
26.7	18.73	4.14	2.62	5.60	2.15	[5]
33.2	15.06	3.77	2.33	5.20	1.90	[4]
39.2	12.76	3.59	2.18	4.97	1.76	[5]
56.2	8.90	3.27	1.92	4.59	1.52	[5]
75.0	6.67	3.09	1.78	4.37	1.25	[8]
> 75.0	< 6.67	–	–		–	outside specified range [9]

1) The listed values for I_{OUT} indicate the required clearance of the output current from the adjusted current limit without being at risk to interact. These values can be used as a maximum nominal current if there is no constraint from a thermal point of view

2) R_{OCT} value must be selected in a way, that I_{OCT} current does not exceed $I_{OCT(short2GND)}$. Please be aware that if the OCT-pin is connected with an too low R_{OCT} resistor to device GND the device will not be protected appropriately against reverse polarity. The device must not be operated with OCT-pin shorted to device GND
3) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} ≥ 97.85 µA (corresponds to R_{OCT} ≤ 5.11 kΩ)**
4) Not subject to production test, values specified by design
5) Values given in this line are based on interpolation of corresponding neighboring specified values
6) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} = 50 µA (corresponds to R_{OCT} = 10 kΩ)**
7) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} = 27.47 µA (corresponds to R_{OCT} = 18.2 kΩ)**
8) See **Electrical Characteristics: Protection Functions**; **Current limitation with setting I_{OCT} = 6.67 µA (corresponds to R_{OCT} = 75 kΩ)**
9) R_{OCT} values > 75k are not recommended for usage as the accuracy of the current limit will degrade

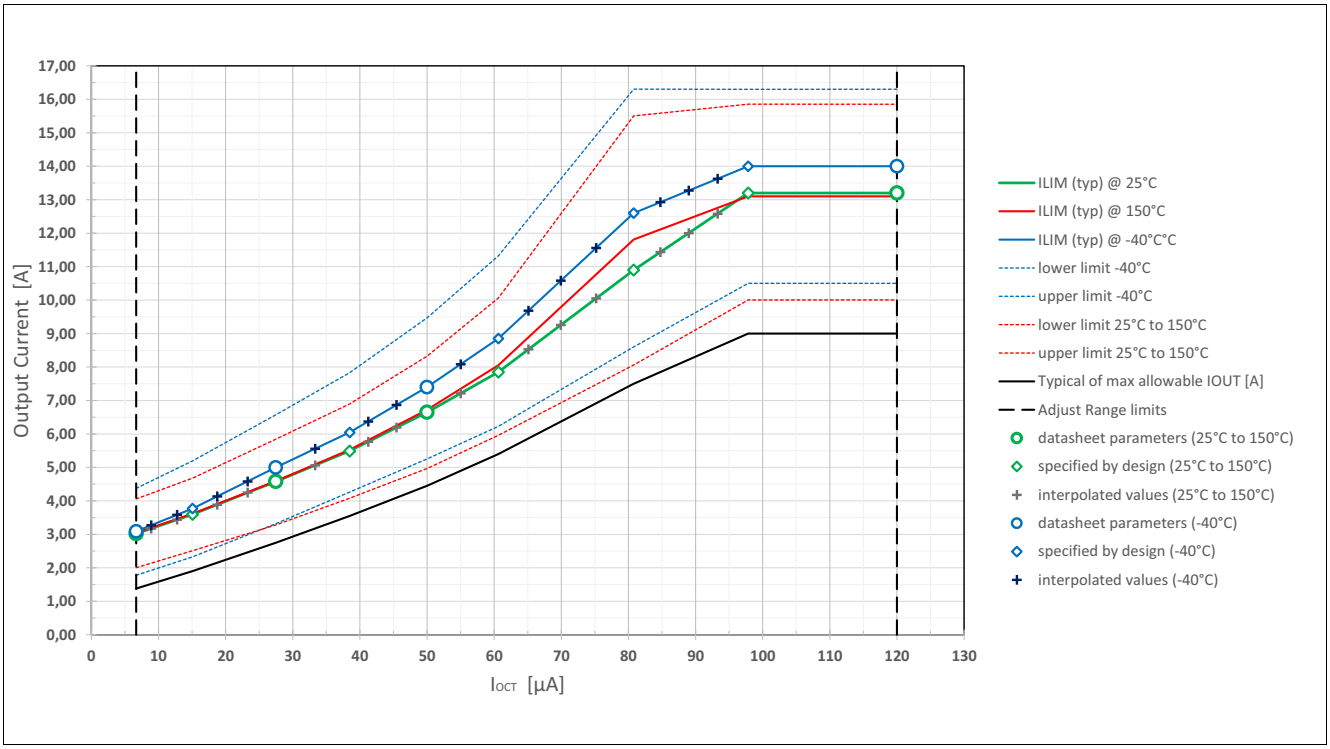


Figure 28 Current limitation threshold $I_{LIM(th,adj)}$ as function of I_{OCT} and related limitation values for different temperatures

11 Package outlines

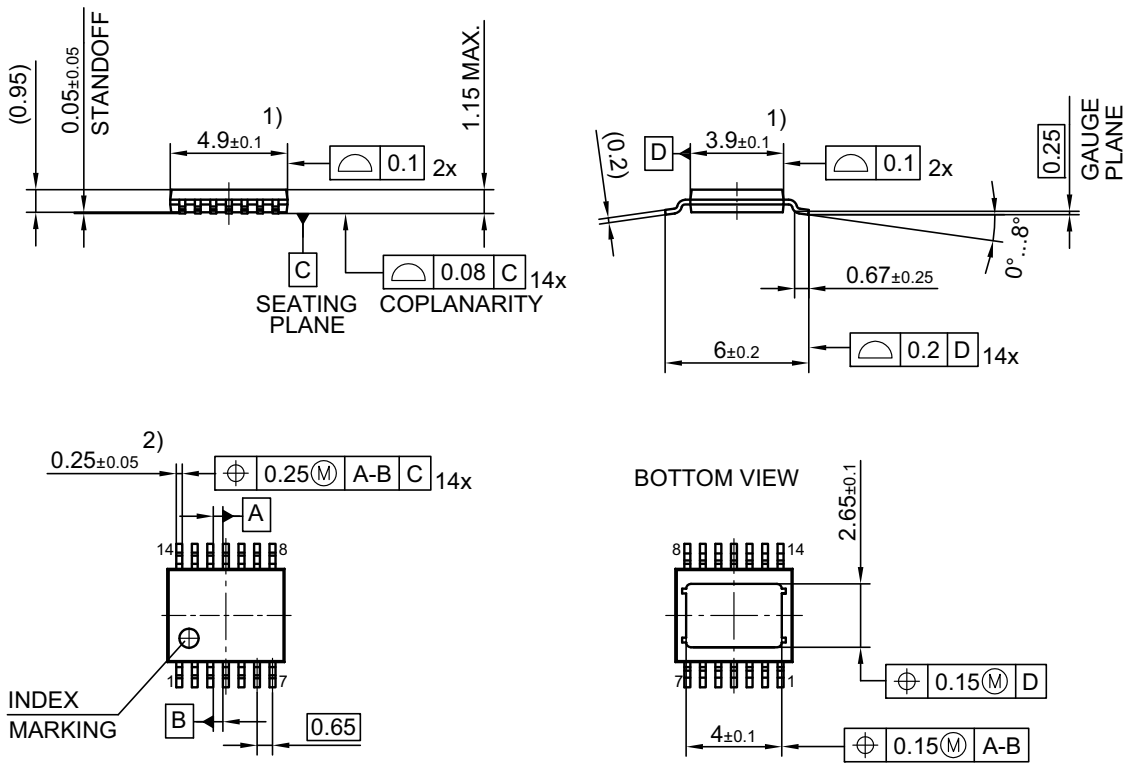


Figure 29 PG-TSDSO-14 (Plastic Dual Small Outline Package) (RoHS-Compliant)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

12 Revision history

Revision	Date	Changes
1.00	2023-11-09	Datasheet release

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