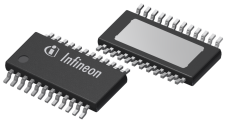
LITIX™ Power TLD6098-2ES

Multitopology dual-channel DC-DC controller

Features

- Dual channel device
- Wide input voltage (up to 58 V) and output voltage range (up to 70 V)
- Switching frequency range from 100 kHz to 500 kHz and synchronization at 2.2 MHz with an external clock source
- EMC optimized device
- Analog adjust input
- Overvoltage, Short to ground, overcurrent, open feedback and overtemperature diagnostic output
- PMOS gate driver for dimming and protection with enhanced dimming features
- LED current accuracy ±3.5%



Product type	Package	Marking
TLD6098-2ES	PG-TSDSO-24	TLD6098-2

Potential applications

- LED driver for: front light module, rear light module, interior light
- Voltage regulator

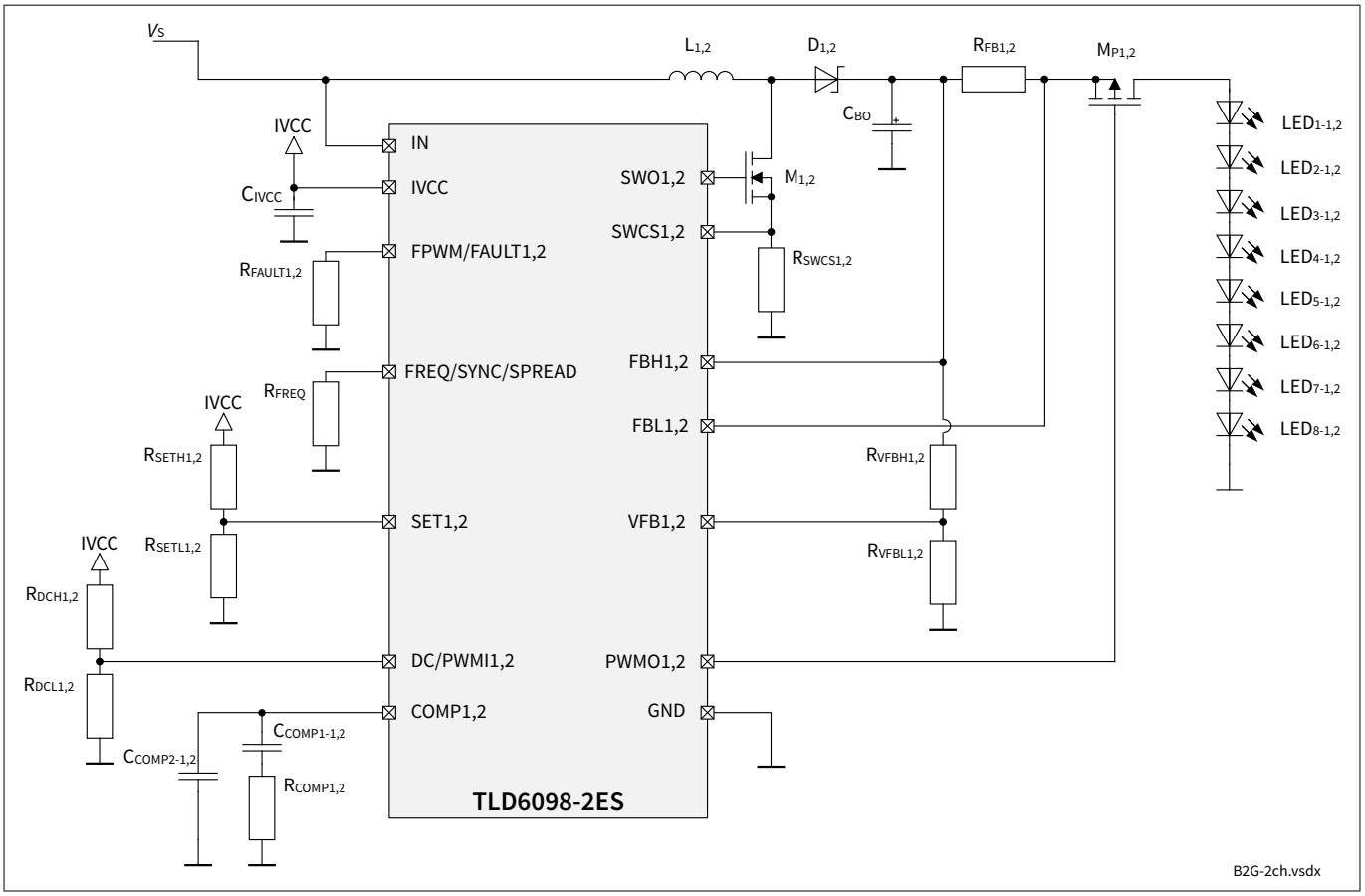


Figure 1 Application diagram

Description of TLD6098-2ES

TLD6098-2ES is a dual channel multi-topology DC-DC controller designed for LED applications with built-in protection features to implement a compact LED driver.

The output current generated by the two channels are independent and they are regulated by means of a peak current control loop. An internal slope compensation is used to avoid sub-harmonic oscillation at high duty cycle (e.g. higher than 50%).

The current accuracy is better than 3.5% (with no analog adjustment applied) over the operating temperature range. A rail to rail current sense amplifiers provide flexibility on the topology choice needed to supply LED string with more than 20 white LED (up to 70 V at output).

The switching frequency can be adjusted from 100 kHz to 500 kHz using an external resistor. A synchronization with an external clock is also possible. The device incorporates even a spread spectrum modulator to achieve easy fulfilment of electromagnetic emission standards.

Each channel of TLD6098-2ES can drive an external PMOS for dimming and protection.

For this purpose each channel of TLD6098-2ES incorporates even a PWM generator controlled by an analog voltage on DC/PWM1,2 pin. The generated PWM signal has the duty cycle adjustable from 0 to 100% with 10 bits of resolution and the frequency range programmable from 150 Hz to 750 Hz. On the same DC/PWMI1,2 pin the digital PWM signal can also be used.

Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100.

Table of contents

Table of contents . . . 3
1 Block diagram . . . 5
2 Pin configuration . . . 6
3 General product characteristics . . . 9
3.1 Absolute maximum ratings . . . 9
3.2 Functional range . . . 11
3.3 Thermal resistance . . . 11
4 Switching regulator . . . 13
4.1 Soft start . . . 13
4.2 Electrical characteristics . . . 16
5 Linear regulator . . . 19
5.1 Undervoltage protection for the external switching MOSFET . . . 19
5.2 Electrical characteristics . . . 20
6 Switching frequency setup and synchronization . . . 22
6.1 Switching frequency setup with external resistor . . . 22
6.1.1 Electrical characteristics . . . 23
6.1.2 Spread Spectrum . . . 23
6.1.2.1 Electrical characteristics . . . 24
6.2 Synchronization with external clock (low frequency mode) . . . 24
6.2.1 Electrical characteristics . . . 25
6.3 Synchronization with external clock (high frequency range) . . . 25
7 Analog output adjustment . . . 26
7.1 Electrical characteristics . . . 26
8 Dimming functions . . . 28
8.1 Electrical characteristics . . . 28
8.2 Digital PWM dimming . . . 29
8.2.1 Electrical characteristics . . . 30
8.3 Embedded PWM engine . . . 30
8.3.1 Electrical characteristics . . . 33
9 Protections and fault management . . . 34
9.1 Electrical characteristics . . . 34
9.2 Short to ground . . . 34
9.2.1 Electrical characteristics . . . 35
9.3 Output overvoltage and voltage regulation . . . 36
9.3.1 Electrical characteristics . . . 37
9.4 Overvoltage on FBH pin . . . 37
9.4.1 Electrical characteristics . . . 39

Table of contents

9.5 Output overcurrent 40
9.5.1 Electrical characteristics 43
9.6 Overtemperature 43
9.6.1 Electrical characteristics 44
10 Application information 45
11 Package 49
12 Revision history 50
Disclaimer 51

1 Block diagram

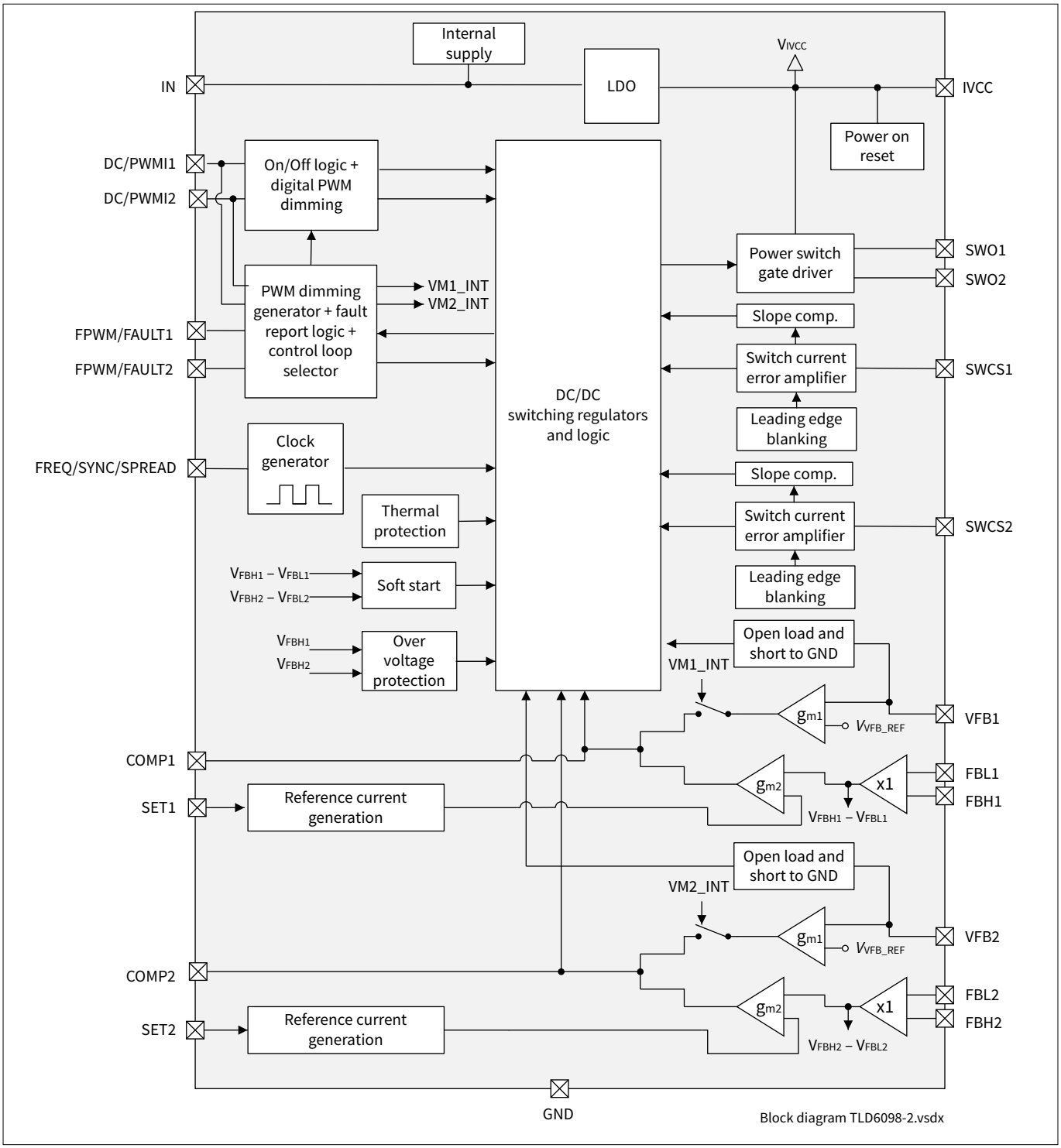


Figure 2 Block diagram

2 Pin configuration

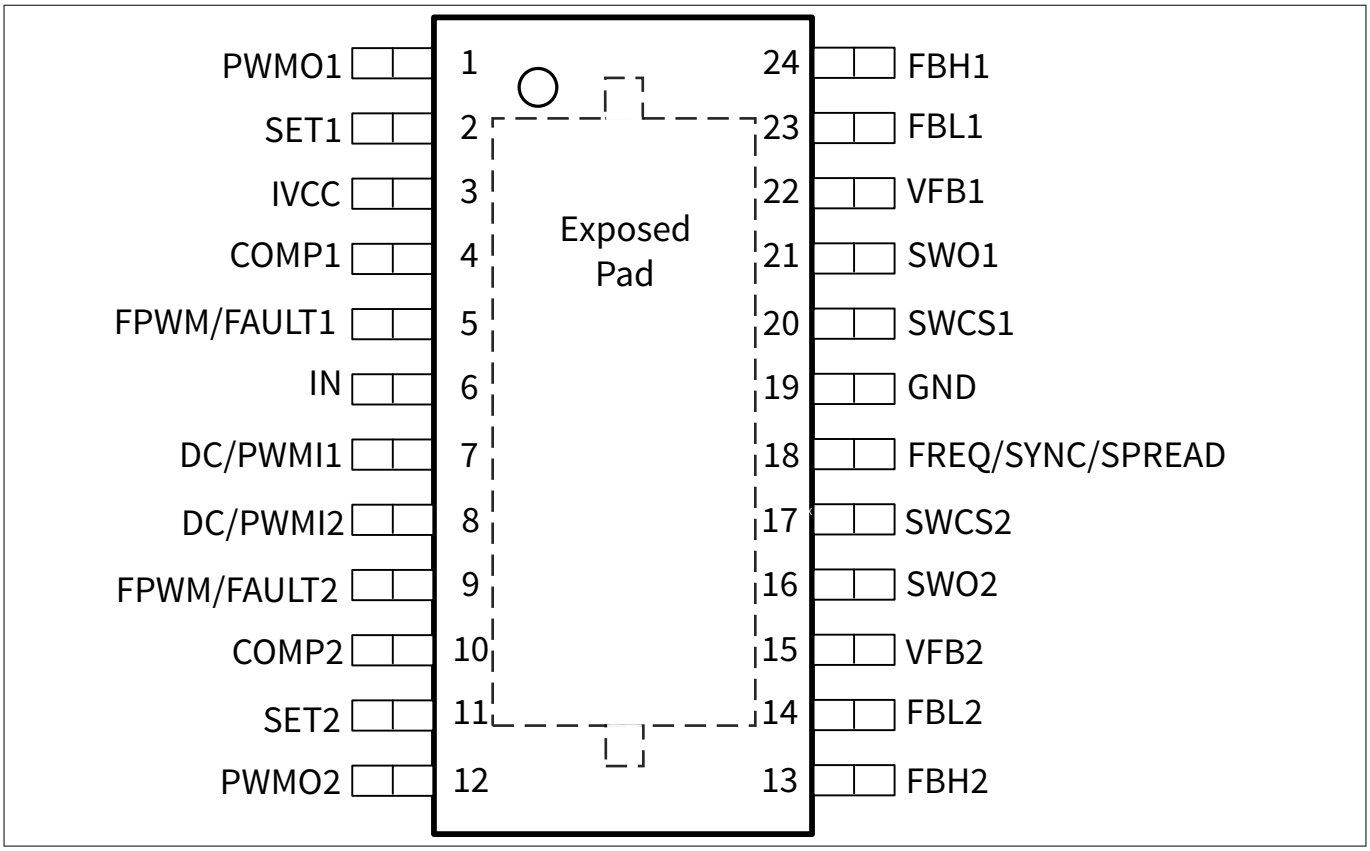


Figure 3 Pin configuration - PG-TSDSO-24

Table 1 Pin configuration of PG-TSDSO-24

Name	Pos.	Description	Direction
PWMO1	1	**PMOS driver for dimming and protection** *Channel 1* Connect to gate of external MOSFET Pin must be left open if external MOSFET is not used	Output
SET1	2	**Analog adjust input** *Channel 1* Load current adjustment pin Pin must not be left open If analog adjustment is not used, connect to IVCC pin	Input
IVCC	3	**Internal linear voltage regulator** Used for internal biasing and gate drive Bypass with external capacitor Pin must not be left open	Output
COMP1	4	**Compensation** *Channel 1* Connect R and C network for stability	Input

(table continues...)

2 Pin configuration

Table 1 (continued) Pin configuration of PG-TSDSO-24

Name	Pos.	Description	Direction
FPWM/FAULT1	5	**PWM frequency selector/Fault** *Channel 1* Connect external R to set PWM frequency Faults are reported by raising the voltage on this pin	Input/Output
IN	6	**Supply** Supply for internal biasing	Input
DC/PWMI1	7	**PWM adjustment** *Channel 1* Set Duty cycle of PWM engine or digital input for PWM dimming	Input
DC/PWMI2	8	**PWM adjustment** *Channel 2* Set Duty cycle of PWM engine or digital input for PWM dimming	Input
FPWM/FAULT2	9	**PWM frequency selector / Fault** *Channel 2* Connect external R to set PWM frequency Faults are reported by raising the voltage on this pin	Input/Output
COMP2	10	**Compensation** *Channel 2* Connect R and C network for stability	Input
SET2	11	**Analog adjust input** *Channel 2* Load current adjustment pin Pin must not be left open If analog adjustment is not used, connect to IVCC pin	Input
PWMO2	12	**PMOS driver for dimming and protection** *Channel 2* Connect to gate of external MOSFET Pin must be left open if external MOSFET is not used	Output
FBH2	13	**Voltage feedback positive** *Channel 2* Non inverting input (+)	Input
FBL2	14	**Voltage feedback negative** *Channel 2* Inverting input (-)	Input

(table continues...)

Table 1 (continued) Pin configuration of PG-TSDSO-24

Name	Pos.	Description	Direction
VFB2	15	**Overvoltage/Voltage loop reference** *Channel 2* Connect to resistive voltage divider to set the maximum voltage at output and the short to ground threshold	Input
SWO2	16	**Switch gate driver** *Channel 2* Connect to gate of external switching power n-channel MOSFET	Output
SWCS2	17	**Current sense/Power ground** *Channel 2* Detects peak current through power switch Power ground for gate driver of SWO2	Input
FREQ/SYNC/SPREAD	18	**Frequency select or synchronization** Connect external resistor to GND to set switching frequency Apply square waveform for synchronization	Input
GND	19	**Ground**	–
SWCS1	20	**Current sense/Power ground** *Channel 1* Detects peak current through power switch Power ground for gate driver of SWO1	Input
SWO1	21	**Switch gate driver** *Channel 1* Connect to gate of external switching power n-channel MOSFET	Output
VFB1	22	**Overvoltage/Voltage loop reference** *Channel 1* Connect to resistive voltage divider to set the maximum voltage at output and the short to ground threshold	Input
FBL1	23	**Voltage feedback negative** *Channel 1* Inverting input (-)	Input
FBH1	24	**Voltage feedback positive** *Channel 1* Non inverting input (+)	Input
Exposed pad	EP	**Exposed pad** Used only for heat dissipation Connect to pin 19 (GND)	–

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Not subject to production test, specified by design

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply input voltage	V_{IN}	-0.3	–	60	V	–	PRQ-31
Voltage at pin SET1, SET2	$V_{SET1,2}$	-0.3	–	5.5	V	–	PRQ-182
Voltage at pin DC/PWMI1, DC/PWMI2	$V_{DC/PWMI1,2}$	-0.3	–	60	V	–	PRQ-286
Voltage at pin FBH1, FBH2	$V_{FBH1,2}$	-1	–	75	V	–	PRQ-171
Voltage at pin FBL1, FBL2	$V_{FBL1,2}$	-1	–	75	V	–	PRQ-172
Differential input voltage	$V_{REF1,2(MAX)}$	-75	–	75	V	$V_{REF1,2(MAX)} = V_{FBH1,2} - V_{FBL1,2}$ Differential signal (not referred to ground)	PRQ-173
Current at pin FBH1, FBH2, FBL1, FBL2	$I_{FBH1,2}$ $I_{FBL1,2}$	-7.5	–	7.5	mA	$V_{REF1,2}$ =150 mV	PRQ-288
Voltage at pin VFB1, VFB2	$V_{FB1,2}$	-0.3	–	5.5	V	–	PRQ-174
Voltage at pin SWCS1, SWCS2	$V_{SWCS1,2}$	-0.3	–	0.3	V	–	PRQ-175
Voltage at pin SWO1, SWO2	$V_{SWO1,2}$	-0.3	–	5.5	V	–	PRQ-176
Voltage at pin FPWM/FAULT1	$V_{FPWM/FAULT1}$	-0.3	–	5.5	V	–	PRQ-179
Voltage at pin FPWM/FAULT2	$V_{FPWM/FAULT2}$	-0.3	–	5.5	V	–	PRQ-177
Voltage at pin COMP1, COMP2	$V_{COMP1,2}$	-0.3	–	5.5	V	–	PRQ-180
Voltage at pin FREQ/SYNC/SPREAD	$V_{FREQ/SYNC}$	-0.3	–	5.5	V	–	PRQ-42

(table continues...)

Table 2 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Not subject to production test, specified by design

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage at pin PWMO1, PWMO2	$V_{PWMO1,2}$	-0.3	–	75	V	–	PRQ-181
PMOS output voltage	$V_{PMOS1,2}$	-1	–	10	V	$V_{PMOS1,2}$= $V_{FBH1,2}$ - $V_{PWMO1,2}$ Differential signal (Not referred to ground)	PRQ-580
Voltage at pin IVCC	V_{IVCC}	-0.3	–	5.5	V	–	PRQ-45
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-46
Storage temperature	T_{stg}	-40	–	150	°C	–	PRQ-47
ESD susceptibility							
ESD susceptibility	V_{ESD_HBM}	-2	–	2	kV	HBM: ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002	PRQ-48
ESD susceptibility inner pins	V_{ESD_CDM}	-0.5	–	0.5	kV	CDM: ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011	PRQ-49
ESD susceptibility corner pins	$V_{ESD\_CDM\_CR}$	-0.75	–	0.75	kV	CDM: ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011	PRQ-50

***Attention**:*

1. ***Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability***
2. ***Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for repetitive operation.***

3.2 Functional range

Table 3 Functional range

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Extended power supply input voltage range	V_{IN_EXT}	4.5	–	58	V	1) Parameter deviations possible	PRQ-51
Power supply input voltage operating range	V_{IN_OP}	8	–	36	V	–	PRQ-52
Operating voltage at pin FBH1, FBH2	$V_{FBH1,2\_OP}$	0	-	70	V	–	PRQ-303
Operating voltage at pin FBL1, FBL2	$V_{FBL1,2\_OP}$	-0.3	–	70	V	–	PRQ-582
Switching frequency adjustment range	f_{SWO}	100	–	500	kHz	–	PRQ-85
Synchronization low frequency capture range	$f_{FREQ/SYNC/SPREAD(LF)}$	100	–	500	kHz	–	PRQ-90
Synchronization high frequency capture range	$f_{FREQ/SYNC/SPREAD(HF)}$	2	–	2.4	MHz	–	PRQ-132
PWM1, PWMO2 frequency range	$f_{PWMO1,2}$	150	–	750	Hz	–	PRQ-213

1) Not subject to production test, specified by design

Attention: ***Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.***

3.3 Thermal resistance

Table 4 Thermal resistance

Not subject to production test, specified by design

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	22.3	–	K/W	1)	PRQ-362
Junction to ambient	R_{thJA}	–	52.7	–	K/W	2) 2s2p	PRQ-363
Junction to ambient	R_{thJA}	–	71.2	–	K/W	2) 1s0p + 600 mm^2	PRQ-364

(table continues...)

Table 4 (continued) Thermal resistance

Not subject to production test, specified by design

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to ambient	R_{thJA}	–	80.4	–	K/W	2) 1s0p + 300 mm²	PRQ-365

1) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and exposed pads are fixed to ambient temperature) T_A = 25°C dissipates 1 W

2) Specified R_{thJA} value is according JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board. The device was simulated on 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layer (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the top layer and the inner layers to bottom layers of JEDEC PCB. T_A = 25°C; IC dissipates 1 W

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For further information visit* https://www.jedec.org

4 Switching regulator

The TLD6098-2ES implements a dual channel regulator suitable for Boost-to-ground, Boost-to-battery, Buck-to-battery, SEPIC, Flyback and Cuk configurations. The two channels work independently.

Each channel has two distinct control loops:

- A current control loop (always enabled)
- A voltage control loop (optional)

If the voltage loop is enabled the device regulates the output current as long as the feedback voltage on VFB1,2 pin is below the VFB1,2 voltage mode ON threshold ($V_{VFB1,2\_VM(ON)}$). The voltage control loop takes over and regulates the output voltage once the VFB1,2 reference voltage ($V_{VFB1,2\_REF}$) is reached.

The controller generates two independent PWM signals by sensing the inductor peak currents and the output of the internal error amplifiers. The control signals are applied to the internal gate drivers connected to SWO1,2 pin to drive the external n-channel MOSFETs.

4.1 Soft start

The soft start routine has 2 functionalities:

- Limiting the input current and output overshoot
- Guaranteeing that the system output reaches the target value in a reasonable time even when being operated in PWM dimming with low duty cycles

Each channel performs its own soft start routine independently.

The first rising edge on DC/PWMI1,2 pin or the first cycle of the embedded PWM engine enables the soft start routine.

It is then performed in the following cases:

- At start-up
- After an overvoltage on FBH1,2 pin
- After an overvoltage on VFB1,2 pin
- After an overtemperature fault
- After an undervoltage on IVCC pin

The soft start is applied after a short to ground fault and retriggered every t_{FAULT} in case of continuous presence of the fault.

The operation of the soft start is conditioned by the analog output adjustment.

During the soft start the switching regulator adjusts the PWM signal to make the voltage between FBH1,2 and FBL1,2 evolve from 0 to $V_{REF(100\%)}$in t_{SS} time. The evolution is performed in 15 steps if the analog adjustment is not applied, otherwise the intended steady-state is reached before the soft start ends.

An ON time extension of the PWM dimming pulses is applied to ensure a reasonable power-up time when a low duty cycle dimming is applied.

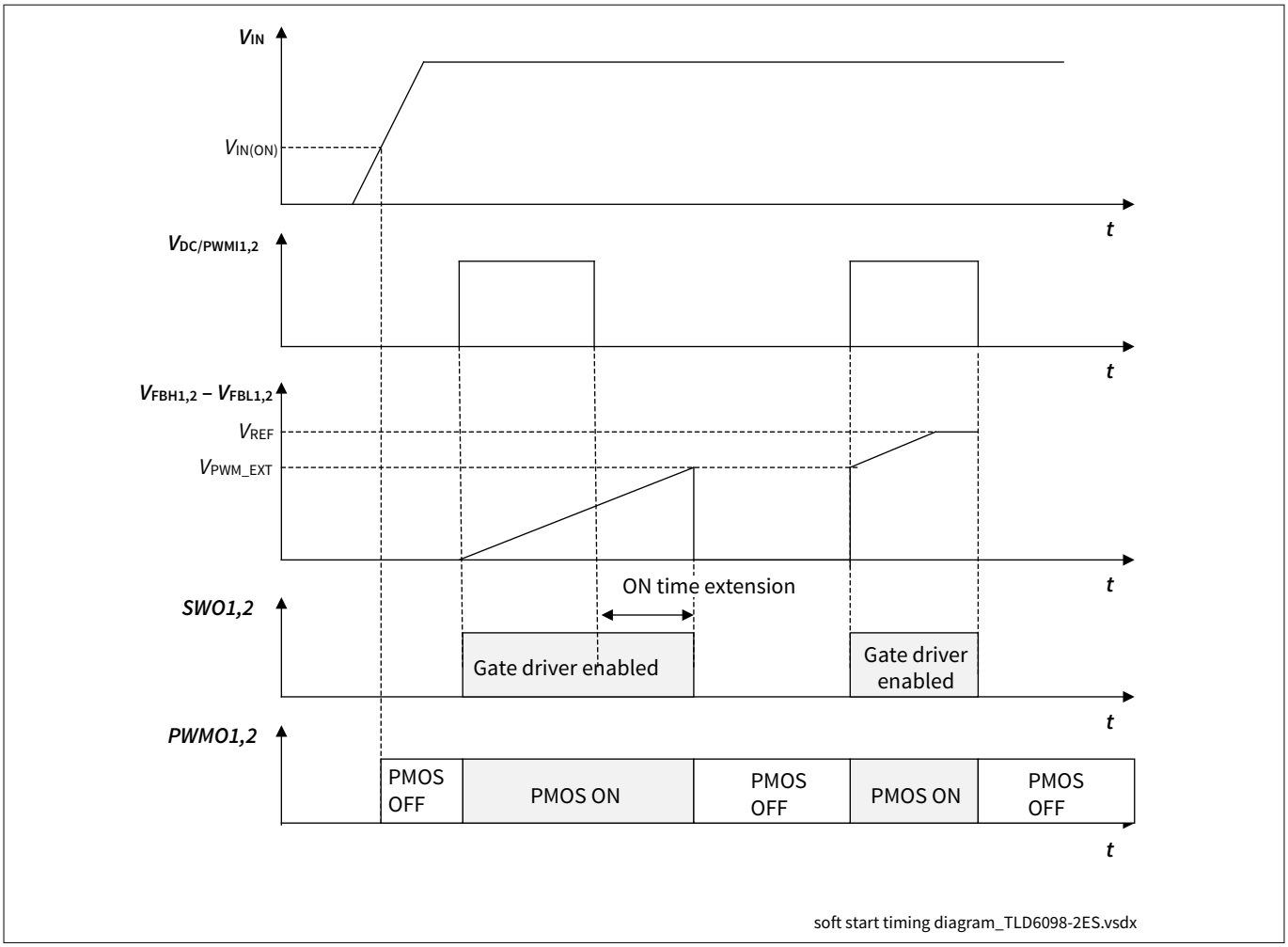


Figure 4 Soft start timing diagram (the linear waveform of V_{VFBH}-V_{VFBL} is an example of possible scenario)

The ON time extension is triggered if :

- The applied PWM dimming signal (or the signal generated by the PWM engine) has an ON time shorter than t_{SS} during the soft start

and

- The voltage across FBH1,2 and FBL1,2 is lower than the reference voltage during PWM extension V_{PWM_EXT} at the end of the ON time of the PWM signal

The ON time extension persists as long as the voltage across FBH1,2 and FBL1,2 reaches $V_{PWM\_EXT.}$

The V_{PWM_EXT} is limited by the analog output adjustment down to a minimum reference voltage during ON time extension V_{PWM_MIN}

For the first 3 steps of the V_{REF} signal, the V_{PWM_EXT} is higher than V_{REF}.

If the reference voltage across FBH1,2 and FBL1,2 adjusted by analog adjustment feature is lower than the V_{PWM_MIN} the ON time extension ends after t_{SS}.

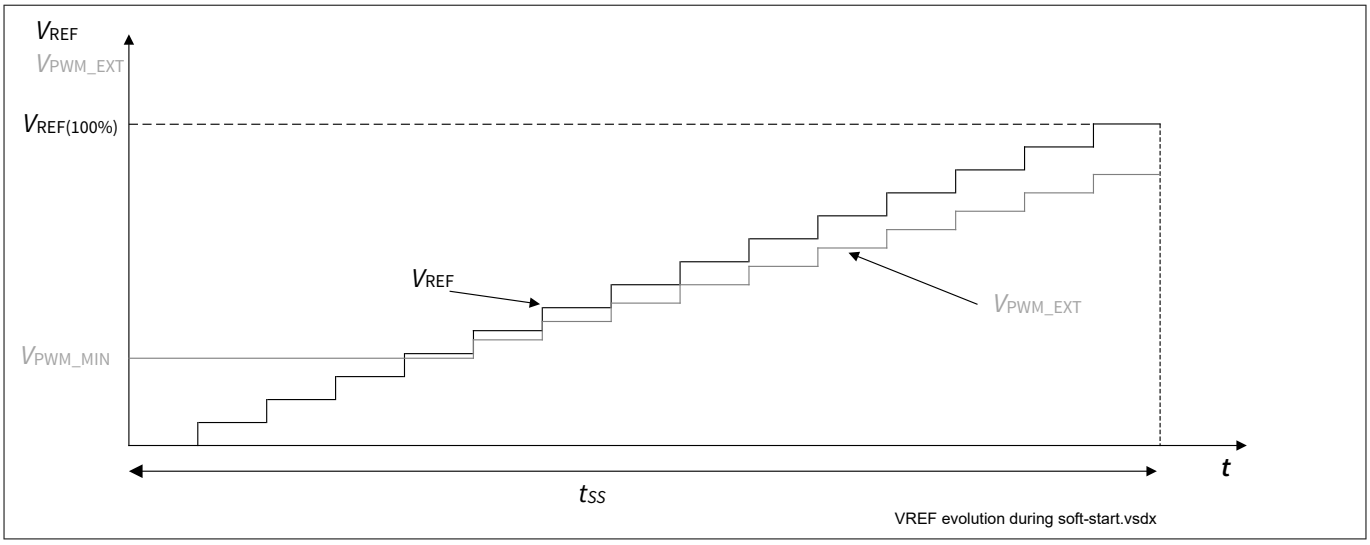


Figure 5 **V_{REF} and V_{PWM_EXT} waveforms during the soft start routine without analog output adjustment**

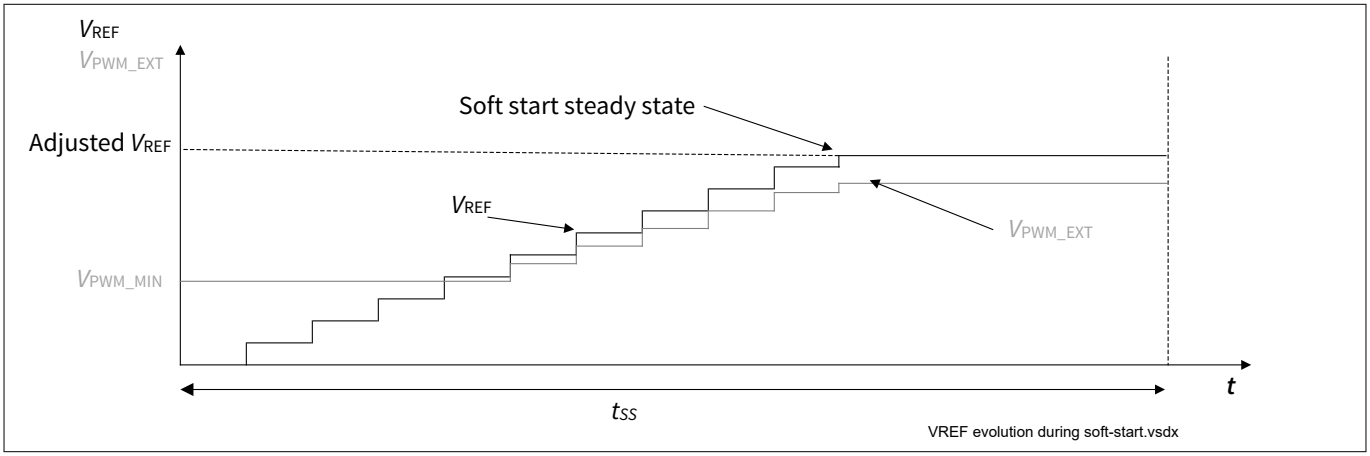


Figure 6 **V_{REF} and V_{PWM_EXT} waveforms during the soft start routine with analog output adjustment**

If the ON time extension ends before t_{SS} elapsed, the ON time extension is retriggered in the following PWM cycle, in case the voltage between FBH1,2 and FBL1,2 is once again lower than V_{PWM_EXT}

When the ON time extension ends, the remaining part of the soft start is allowed to evolve during the following ON time of the PWM dimming signal. In this case the actual duration of soft start could be longer than t_{SS}.

4.2 Electrical characteristics

Table 5 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Regulator							
VFB1,2 reference voltages (voltage loop)	$V_{VFB1,2\_REF}$	1.568	1.6	1.632	V	–	PRQ-183
Current loop reference voltages	$V_{REF1,2(100\%)}$	144.75	150	155.25	mV	Differential signal (not referred to ground) $V_{REF1,2} = V_{FBH1,2} - V_{FBL1,2}$; $V_{SET1,2}$ = 5V	PRQ-184
Current loop reference voltages	$V_{REF1,2(40\%)}$	54.6	60	65.4	mV	*1)* Differential signal (not referred to ground) $V_{SET1,2}$ = 940 mV	PRQ-185
Current loop reference voltages	$V_{REF1,2(0\%)}$	–	–	10	mV	Differential signal (not referred to ground) $V_{SET1,2}$ = 100 mV	PRQ-186
Transconductance error amplifier voltage loop	g_{m1}	–	0.95	–	mS	*1)* *2)*	PRQ-600
Transconductance error amplifier current loop	g_{m2}	–	1.6	–	mS	*2) 1)*	PRQ-463
Switch current limit thresholds	$V_{SWCS1,2\_TH}$	80	100	120	mV	–	PRQ-187
Maximum duty cycle in adjust. freq. mode	D_{MAX}	91	–	–	%	$R_{FREQ/SYNC/SPREAD}$ = 27 kΩ	PRQ-70
Maximum duty cycle in low frequency sync mode	$D_{MAX(LF)}$	88	–	–	%	f_{SW} = 500 kHz	PRQ-71
Maximum duty cycle in high frequency sync mode	$D_{MAX(HF)}$	80	–	–	%	f_{SW} = 2.2 MHz	PRQ-289
Soft start time	t_{SS}	1.8	2	2.2	ms	*2) 1)*	PRQ-72
Reference voltage during PWM extension	V_{PWM_EXT}	–	0.8*$V_{REF1,2}$	–	V	*1) 2)* $V_{PWM\_EXT} > V_{PWM\_MIN}$	PRQ-588

(table continues...)

Table 5 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Minimum reference voltage during PWM extension	V_{PWM_MIN}	–	31.5	–	mV	2) 1)	PRQ-589
Input current at pin FBH1, FBH2	$I_{FBH1,2}$	–	550	800	µA	$V_{FBH1,2}$ - $V_{FBL1,2}$ = 0.15 V $V_{FBH1,2}$ = 60 V	PRQ-188
Input current at pin FBL1, FBL2	$I_{FBL1,2}$	–	50	70	µA	$V_{FBH1,2}$ - $V_{FBL1,2}$ = 0.15V $V_{FBH1,2}$ = 60 V	PRQ-189
Input current at pin FBH1, FBH2	$I_{FBH1,2}$	–	50	70	µA	$V_{FBH1,2}$ - $V_{FBL1,2}$ = 0.15 V $V_{FBL1,2}$ = 0 V Current flows out of pin	PRQ-190
Input current at FBL1, FBL2	$I_{FBL1,2}$	–	50	70	µA	$V_{FBH1,2}$ - $V_{FBL1,2}$ = 0.15 V $V_{FBL1,2}$ = 0 V Current flows out of pin	PRQ-191
Threshold voltage high side sensing	$V_{FBH1,2\_HSS}$	–	2.55	2.8	V	1) $V_{FBH1,2}$ increasing	PRQ-265
Threshold voltage low side sensing	$V_{FBH1,2\_LSS}$	2.1	2.3	–	V	1) $V_{FBH1,2}$ decreasing	PRQ-266
Power supply undervoltage shutdown	$V_{IN(OFF)}$	2.5	–	4.5	V	V_{IN} decreasing	PRQ-77
Power supply minimum startup voltage	$V_{IN(ON)}$	–	–	5.5	V	V_{IN} increasing	PRQ-78
Power supply current consumption	I_{IN}	–	8	12	mA	$V_{DC/PWMI1,2}$ = 0 V $V_{SET1,2}$ = V_{IVCC} $R_{FREQ/SYNC/SPREAD}$ = 33 kΩ $R_{FPWM/FAULT1,2}$ = 57 kΩ no faults detected	PRQ-430

(table continues...)

Table 5 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate driver for external switch							
Gate drivers peak output current	$I_{SWO1,2}$	1	–	–	A	1) $V_{SWO1,2}$ increasing 1 V to 4 V Current flows out of pin	PRQ-192
Gate drivers peak output current	$I_{SWO1,2}$	1	–	–	A	1) $V_{SWO1,2}$ decreasing 4 V to 1 V	PRQ-193
Gate drivers output rise time	$t_{R\_SWO1,2}$	–	–	20	ns	1) $C_{L\_SWO1,2}$ = 3.3 nF $V_{SWO1,2}$ increasing 1 V to 4 V	PRQ-194
Gate drivers output fall time	$t_{F\_SWO1,2}$	–	–	20	ns	1) $C_{L\_SWO1,2}$ = 3.3 nF $V_{SWO1,2}$ decreasing 4 V to 1 V	PRQ-195
Gate driver high side resistance	R_{SWO_HS}	–	1	3	Ω	2) 1) I_{SWO} = -10 mA	PRQ-83
Gate driver low side resistance	R_{SWO_LS}	–	1	3	Ω	2) 1) I_{SWO} = 10 mA	PRQ-196

1) Not subject to production test, specified by design
2) Not subject to production test, specified by design

5 Linear regulator

The device incorporates a linear regulator to generate a 5 V output used to supply the internal gate drivers and, through IVCC pin, other auxiliary devices on the PCB (for example a microcontroller and resistor dividers).

The maximum output current of the linear regulator is limited to the IVCC output current limit I_{IVCC}.

If the load on IVCC (gate drivers plus connected devices on PCB) draws more than I_{IVCC} the linear regulator output voltage decreases.

The linear regulator starts to deliver current to IVCC pin when the input voltage V_{IN} goes above the power supply minimum start up voltage $V_{IN\ (ON)}$ for a time longer than IVCC start time t_{ST}

A low ESR capacitor has to be connected from IVCC to ground (C_{IVCC} in the figure) to stabilize the output voltage of the linear regulator.

The ESR of the capacitor C_{IVCC} has to be lower than IVCC buffer capacitor ESR $R_{IVCC(ESR)}$.

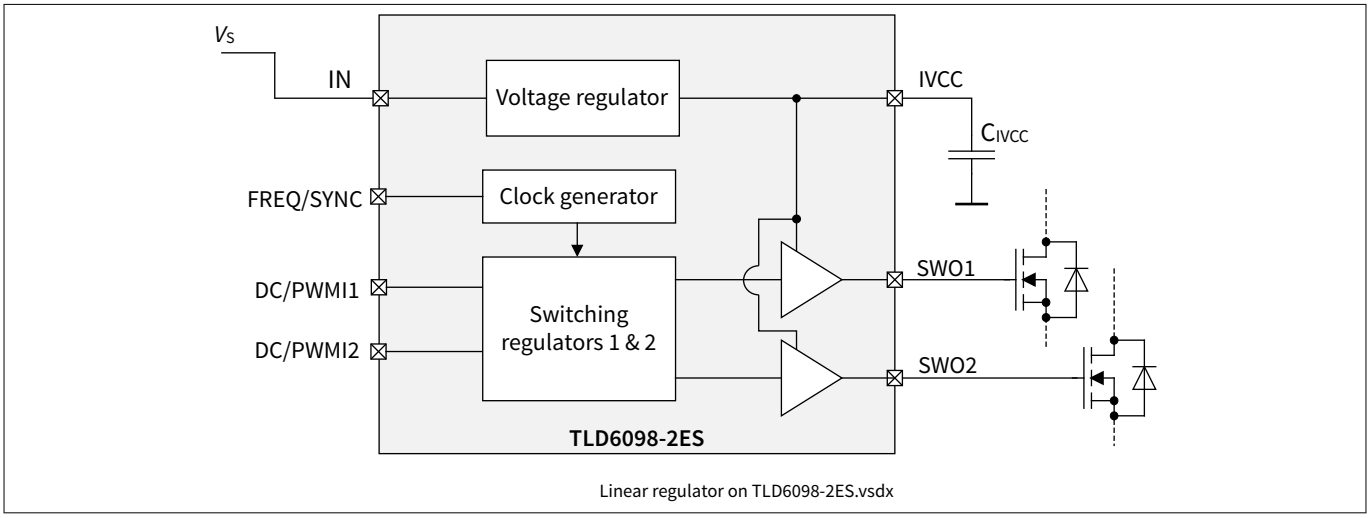


Figure 7 Block diagram of the linear regulator

5.1 Undervoltage protection for the external switching MOSFET

During the ON time of the switching PWM signal, the gate drivers have to bias the switching NMOS in deep ohmic region to avoid the overheating of the MOSFET themselves. This is ensured by choosing a logic level MOSFET with a maximum threshold voltage lower than IVCC undervoltage switch-off threshold $V_{IVCC\_TH\_D}$.

TLD6098-2ES has an integrated undervoltage reset threshold circuit to disable the gate driver if the V_{IVCC} drops below the $V_{IVCC\_TH\_D}$. The gate driver are then enabled again when the V_{IVCC} goes above the IVCC undervoltage switch-on threshold $V_{IVCC\_TH\_I}$.

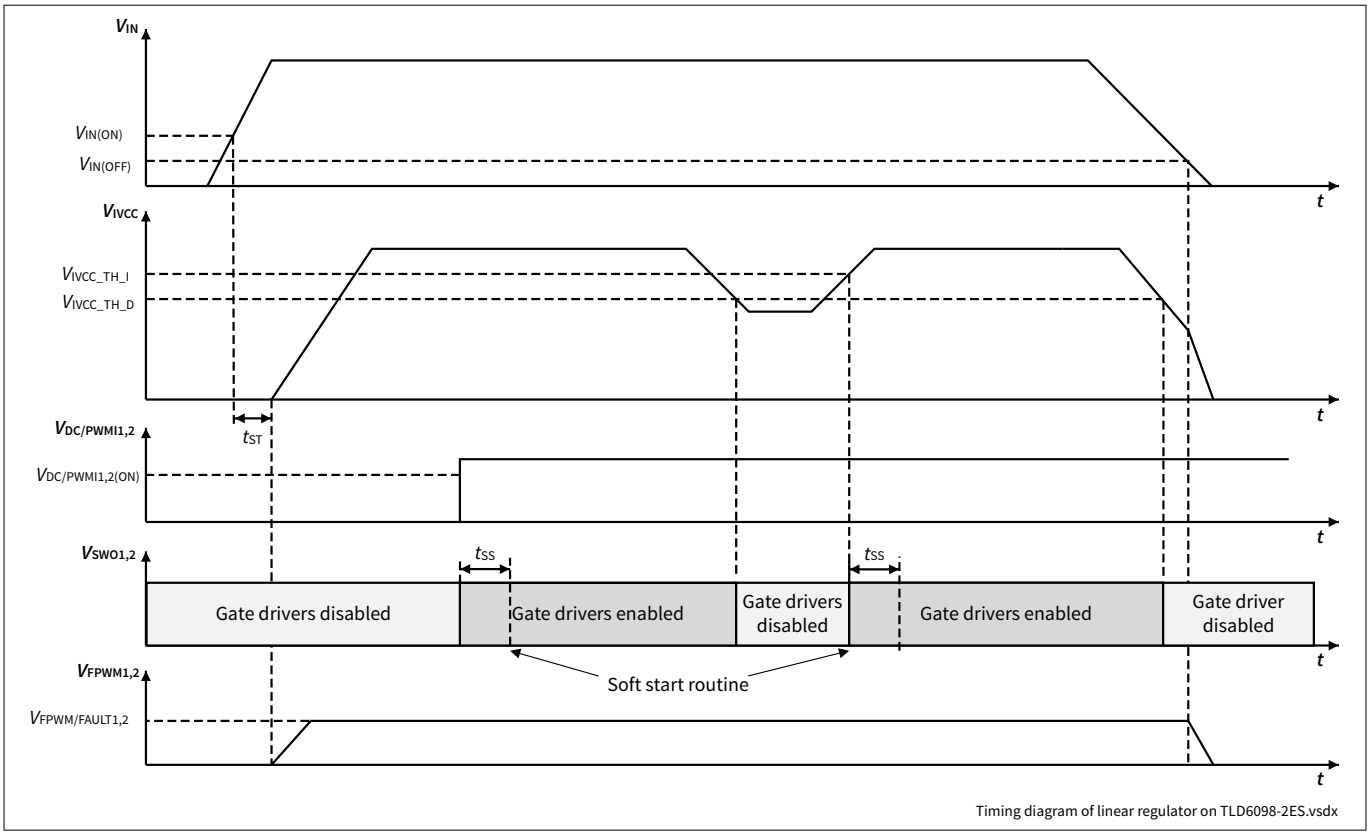


Figure 8 Thresholds and timing diagram related to the linear regulator

5.2 Electrical characteristics

Table 6 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IVCC output voltage	V_{IVCC}	4.85	5	5.15	V	8 V ≤ V_{IN} ≤ 36 V; 0.1 mA ≤ I_{IVCC} ≤ 40 mA	PRQ-58
IVCC output current limit	I_{IVCC}	51	–	100	mA	8 V < V_{IN} < 13.5 V; V_{IVCC} < 4.5 V; Current flows out of pin	PRQ-59
IVCC dropout voltage	V_{IVCC_DV}	–	–	0.5	V	V_{IN} = 5 V; I_{IVCC} < 20 mA	PRQ-60
IVCC start time	t_{ST}	–	–	300	µs	1) V_{IN} slew rate higher than 1 V/10 µs	PRQ-285
IVCC buffer capacitor	C_{IVCC}	1	4.7	10	µF	1) If embedded PWM engine is used, 4.7 µF has to be chosen as a minimum	PRQ-61

(table continues...)

Table 6 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IVCC buffer capacitor ESR	$R_{IVCC(ESR)}$	–	–	0.2	Ω	1) Maximum value given for regulator stability	PRQ-62
IVCC undervoltage switch-off threshold	$V_{IVCC\_TH\_D}$	3.6	–	4.0	V	V_{IVCC} decreasing	PRQ-64
IVCC undervoltage switch-on threshold	$V_{IVCC\_TH\_I}$	–	–	4.5	V	V_{IVCC} increasing	PRQ-65

1) Not subject to production test, specified by design

Attention: ***Select external switching MOSFET with worst case threshold voltage $V_{GS(th)}$ lower than minimum $V_{IVCC\_TH\_D}$***

6 Switching frequency setup and synchronization

The DC-DC switching frequency is adjusted by a resistor placed from FREQ/SYNC/SPREAD pin to ground or by providing to this pin a digital clock. The device incorporates also a spread spectrum modulator to reduce the design effort to fulfill the EMI compliance.

By using a resistor, the switching frequency of the regulator is adjusted in the switching frequency adjustment range f_{SWO}.

If an external clock is provided, the device accepts a digital clock in these two working windows:

- Synchronization low frequency capture range $f_{FREQ/SYNC/SPREAD(LF)}$ (low frequency synchronization mode)
- Synchronization high frequency capture range $f_{FREQ/SYNC/SPREAD(HF)}$ (high frequency synchronization mode)

Outside these ranges, the device does not recognize a valid clock and then the behavior of the regulator can be out of specification.

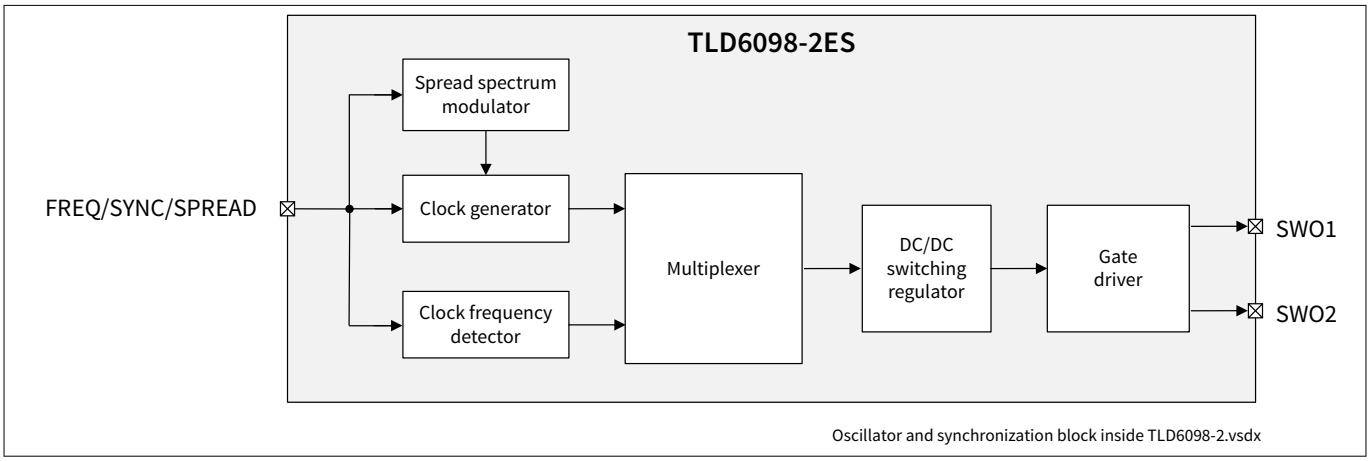


Figure 9 Diagram of switching frequency adjustment and synchronization blocks

To limit the input current spikes and then to relax the input filter requirements, SWO2 is in phase opposition to SWO1.

This means SWO2 is activated with a $1/(2*f_{SWO})$ delay respect to SWO1.

6.1 Switching frequency setup with external resistor

The resistor placed on FREQ/SYNC/SPREAD pin adjusts the frequency of the DC-DC and enables or disables the spread spectrum modulator.

The relationship between the biasing resistor and switching frequency with spread spectrum activated is

$$f_{SW} = \frac{1}{\left(1.11 \cdot 10^{-9} \cdot R_{FREQ/SYNC/SPREAD}\right)} \quad (1)$$

The relationship between the biasing resistor and the switching frequency with the spread spectrum not active is

$$f_{SW} = \frac{1}{\left(1.11 \cdot 10^{-10} \cdot R_{FREQ/SYNC/SPREAD}\right)} \quad (2)$$

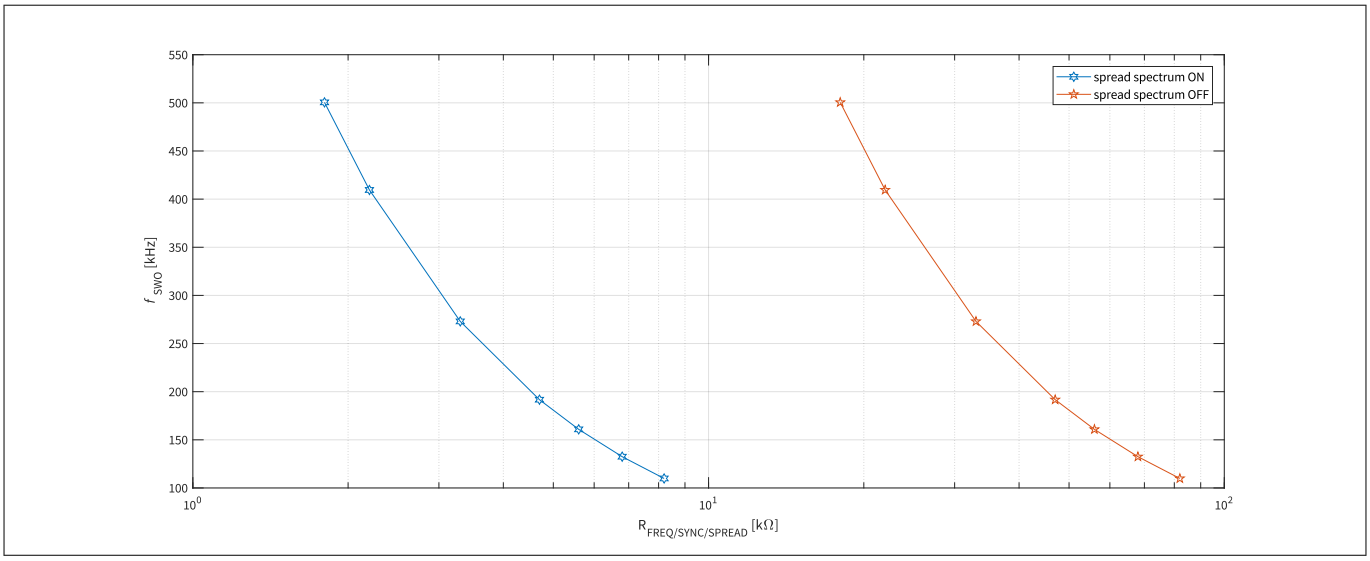


Figure 10 **Switching frequency versus $R_{FREQ/SYNC/SPREAD}$**

6.1.1 Electrical characteristics

Table 7 **Electrical characteristics**

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switching frequency	$f_{SWO\_SSM(OFF)}$	288	333	378	kHz	$R_{FREQ/SYNC/SPREAD}$ = 27 kΩ	PRQ-277
FREQ/SYNC/SPREAD output current	$I_{FREQ/SYNC/SPREAD}$	–	–	3	mA	$V_{FREQ/SYNC/SPREAD}$ = 0 V Current flowing out of pin	PRQ-86
FREQ/SYNC/SPREAD output voltage	$V_{FREQ/SYNC/SPREAD\_SSM(OFF)}$	0.72	0.8	0.88	V	$R_{FREQ/SYNC/SPREAD}$ = 27 kΩ	PRQ-87

6.1.2 Spread Spectrum

The spread spectrum modulation technique significantly reduces the electromagnetic harmonics emission at the lower frequency range of the spectrum (f < 30 MHz).

This technique is enabled by changing the switching frequency over the time. The final result is the movement over a broad band of the energy associated with the peaks of the electromagnetic harmonics emission.

The switching frequency is modulated with a triangular shape digitalized in 7 steps equally distributed over the entire frequency span (2 times the frequency deviation f_{DEV}).

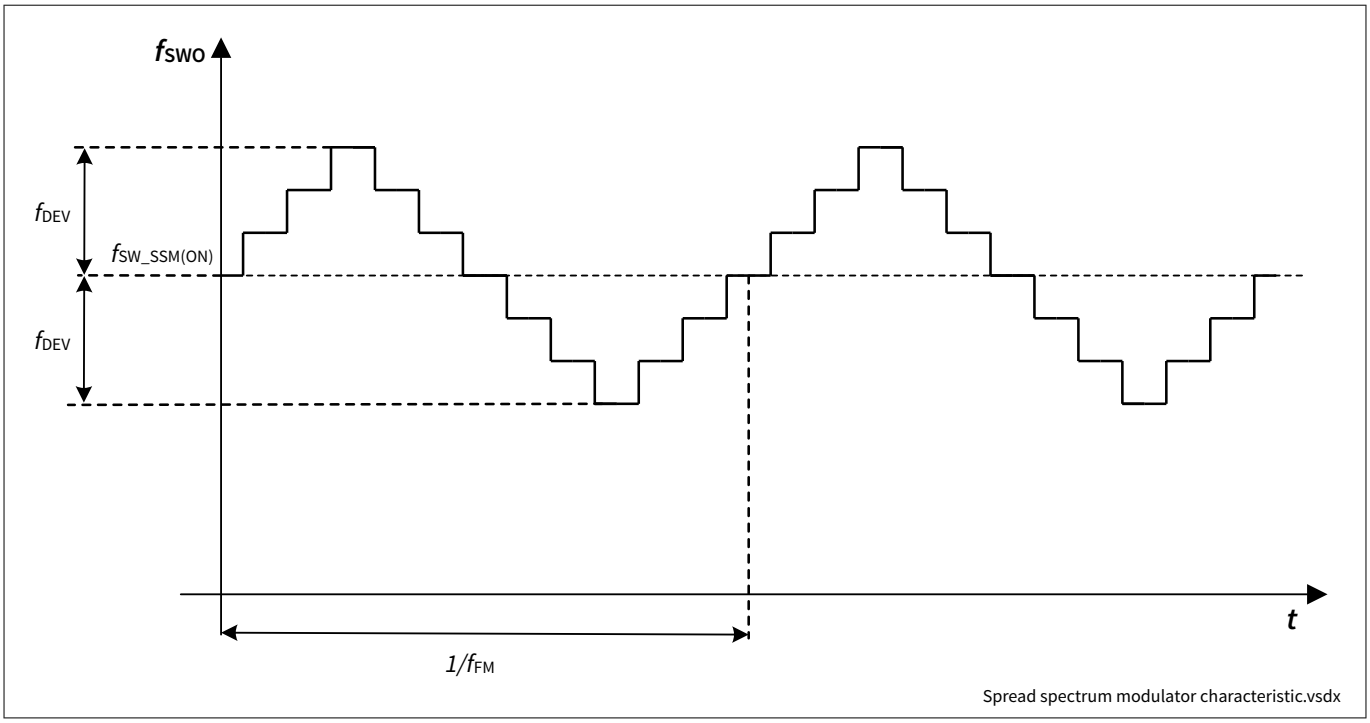


Figure 11 Spread spectrum modulator characteristic

6.1.2.1 Electrical characteristics

Table 8 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Average switching frequency	$f_{SWO\_SSM(ON)}$	288	333	378	kHz	1) $R_{FREQ/SYNC/SPREAD}$ = 2.7 kΩ	PRQ-84
Modulation frequency	f_{FM}	13.5	15	16.5	kHz	1) 1.8 kΩ ≤ $R_{FREQ/SYNC/SPREAD}$ ≤ 9 kΩ	PRQ-88
Frequency deviation	f_{DEV}	0.09*f_{SWO}	0.15*f_{SWO}	–	kHz	1) 1.8 kΩ ≤ $R_{FREQ/SYNC/SPREAD}$ ≤ 9 kΩ	PRQ-89
FREQ/SYNC/SPREAD output voltage	$V_{FREQ/SYNC/SPREAD\_SSM(ON)}$	0.72	0.8	0.88	V	$R_{FREQ/SYNC/SPREAD}$ = 2.7 kΩ	PRQ-385

1) Not subject to production test, specified by design

6.2 Synchronization with external clock (low frequency mode)

The switching frequency is synchronized with an external clock source applied on FREQ/SYNC/SPREAD pin if the frequency is in the synchronization low frequency capture range $f_{FREQ/SYNC/SPREAD(LF)}$ and the duty cycle is in the synchronization input duty cycle range $DC_{FREQ/SYNC/SPREAD}$.

The device detects the external clock source if the voltage on FREQ/SYNC/SPREAD exceeds the two thresholds:

- The synchronization input high voltage $V_{FREQ/SYNC/SPREAD(H)}$ during the positive pulse,
- The synchronization input low voltage $V_{FREQ/SYNC/SPREAD(L)}$ during the negative pulse.

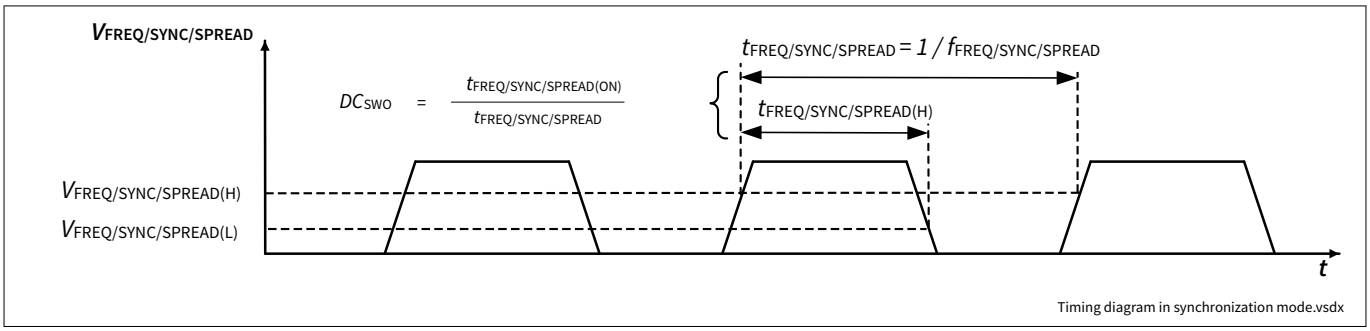


Figure 12 Timing diagram when synchronization mode is enabled

6.2.1 Electrical characteristics

Table 9 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Synchronization input high voltage	$V_{FREQ/SYNC/SPREAD(H)}$	3.0	–	–	V	–	PRQ-91
Synchronization input low voltage	$V_{FREQ/SYNC/SPREAD(L)}$	–	–	0.8	V	–	PRQ-92
Synchronization input duty cycle range	$DC_{FREQ/SYNC/SPREAD}$	40	–	60	%	1)	PRQ-94

1) Not subject to production test, specified by design

6.3 Synchronization with external clock (high frequency range)

High switching frequency enables a system cost down due to reduced value for the reactive components.

The high frequency synchronization is enabled if the input clock is in the synchronization high frequency capture range $f_{FREQ/SYNC/SPREAD(HF)}$.

Voltage threshold levels on FREQ/SYNC/SPREAD pin are the same as in the low frequency synchronization mode.

7 Analog output adjustment

Each channel can adjusts the reference voltage $V_{REF1,2}$ across FBH1,2 and FBL1,2 pins (thus adjusting the output currents) by monitoring the analog voltage on the respective SET1,2 pin ($V_{SET1,2}$).

The analog output adjustment acts independently channel by channel without any relations between the channels.

The SWO1,2 NMOS gate driver is disabled If the voltage applied on the SET1,2 pin is lower than SET input voltage no switching activity $V_{SET1,2(NOSW)}$.

The SET1,2 pin has to be connected to a voltage higher than $V_{SET1,2(100\%)}$ (e.g. connecting SET1,2 pin to IVCC pin) to exclude the output current adjustment feature.

The voltage on SET1,2 pins influences the voltage reference of the corresponding channel following the behavior of showed in the picture below.

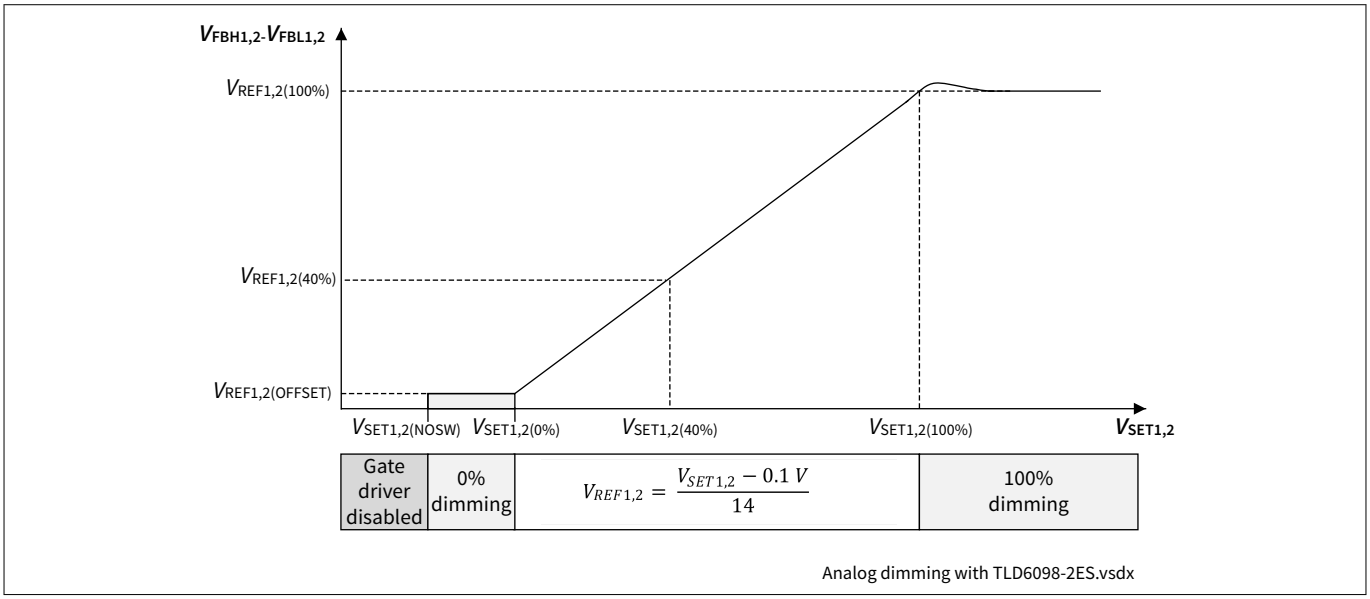


Figure 13 Relationship between $V_{SET1,2}$ and the respective voltage $V_{REF1,2}$

The SET pin can also be wired to an external thermistor (usually mounted on the LED module) to perform a thermal protection.

7.1 Electrical characteristics

Table 10 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SET1 SET2 input voltage 100%	$V_{SET1,2(100\%)}$	–	2.2	–	V	1)	PRQ-596
SET1 SET2 input voltage 40%	$V_{SET1,2(40\%)}$	–	940	–	mV	1)	PRQ-599
SET1 SET2 input voltage 0%	$V_{SET1,2(0\%)}$	–	100	–	mV	1)	PRQ-598

(table continues...)

Table 10 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SET1 SET2 input voltage no switching activity	$V_{SET1,2(NOSW)}$	–	–	50	mV	–	PRQ-597

1) Not subject to production test, specified by design

8 Dimming functions

The TLD6098-2ES offers two dimming inputs (one for each channel) for pulse width modulating (PWM) the output current.

This modulation is beneficial to reduce the average current at output (and then the brightness of the LEDs), without showing color shift on the light produced by the LEDs.

The output current modulation is operated by the channel as function of the signal on DC/PWMI1,2 pins:

- A digital clock signal imposes the duty cycle and the frequency
- An analog voltage is translated to a duty cycle and the frequency is adjusted with a resistor on FPWM/FAULT1,2 pin.

These features are present on both channels and they act independently channel by channel without any relations between channels.

For each channel, different voltage levels on DC/PWMI1,2 pins activates different functions on the respective channel, as described below:

- If the voltage is higher than DC/PWMI1,2 input voltage high threshold $V_{DC/PWMI(ON)}$ the dimming duty cycle is set to 100%
- If the voltage is in between the two digital thresholds ($V_{DC/PWMI(100\%)}$ and $V_{DC/PWMI(0\%)}$), the embedded PWM dimming function is activated
- If the voltage is lower than DC/PWMI1,2 input voltage low threshold $V_{DC/PWMI(OFF)}$ the dimming duty cycle is 0%

When a dimming function is activated, the PWM signal controls the switching regulator gate driver and the PMOS gate driver of the respective channel where the dimming function is applied.

To allow fast transitions of the dimming PMOS even at low output voltage, the positive power supply of the PWMO1,2 gate driver is connected to FBH1,2 pin if its voltage $V_{FBH1,2}$ is higher than V_{IVCC}, otherwise the gate driver is supplied by the IVCC pin.

During the ON state of the PWM dimming of each channel, the respective PMOS is biased with a PWMO output voltage ON state $V_{PWMO1,2,ON}$ (minimum $V_{PWMO1,2,ON}$ cannot go below 0 V).

8.1 Electrical characteristics

Table 11 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWMO1, PWMO2 peak output current	$I_{PWMO1,2}$	2	5	–	mA	1) $V_{FBH1,2}$ = 14 V $V_{PWMO1,2}$ increasing $V_{PWMO1,2(ON)}$ + 0.5 V to $V_{PWMO1,2(ON)}$ + 3.5 V $C_{L,PWMO1,2}$ = 3.3 nF Current flows out of pin	PRQ-199

(table continues...)

Table 11 (continued) Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWMO1 PWMO2 peak output current	$I_{PWMO1,2}$	2	5	–	mA	1) $V_{FBH1,2}$ = 14 V $V_{PWMO1,2}$ decreasing $V_{PWMO1,2(OFF)}$ - 0.5 V to $V_{PWMO1,2(OFF)}$ - 3.5 V $C_{L,PWMO1,2}$ = 3.3 nF	PRQ-200
PWMO1 PWMO2 gate drivers output rise time	$t_{R\_PWMO1,2}$	–	2	6	µs	1) $V_{FBH1,2}$ = 14 V $V_{PWMO1,2}$ increasing $V_{PWMO1,2(ON)}$ + 0.5 V to $V_{PWMO1,2(ON)}$ + 3.5 V $C_{L,PWMO1,2}$ = 3.3 nF	PRQ-201
PWMO1 PWMO2 gate drivers output fall time	$t_{F\_PWMO1,2}$	–	2	6	µs	1) $V_{FBH1,2}$ = 14 V $V_{PWMO1,2}$ decreasing $V_{PWMO1,2(OFF)}$ - 0.5 V to $V_{PWMO1,2(OFF)}$ - 3.5 V $C_{PWMO1,2}$ = 3.3 nF	PRQ-202
PWMO1 PWMO2 output voltage ON state	$V_{PWMO1,2(ON)}$	–	$V_{FBH1,2}$ - 6.5	V_{FBH} - 5	V	1) $V_{FBH1,2}$ > 7.5	PRQ-203
PWMO1 PWMO2 output voltage OFF state	$V_{PWMO1,2(OFF)}$	–	$V_{FBH1,2}$	–	V	1) $V_{FBH1,2}$ = 14 V	PRQ-204

1) Not subject to production test, specified by design

8.2 Digital PWM dimming

Each channel of the TLD6098-2ES has a dedicated input pin to modulate the average current in a LED string with a digital pattern.

Each channel recognizes a digital PWM dimming signal on DC/PWMI1,2 pin if:

- The minimum voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(OFF)}$
- The maximum voltage on DC/PWMI1,2 pin is higher than $V_{DC/PWMI1,2(ON)}$
- The maximum frequency on DC/PWMI1,2 is less than 1 kHz
- No faults are detected

If a valid pattern is recognized and the $V_{DC/PWMI}$ is higher than $V_{DC/PWMI(ON)}$ the NMOS gate driver is enabled and the voltage of PWMO pin is $V_{PWMO(ON)}$; else the NMOS gate driver is disabled and the voltage of PWMO pin is $V_{PWMO(OFF)}$

8.2.1 Electrical characteristics

Table 12 Electrical Characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DC/PWMI1, DC/PWMI2 input voltage high threshold	$V_{DC/PWMI1,2(ON)}$	4.0	–	–	V	–	PRQ-205
DC/PWMI1, DC/PWMI2 input voltage low threshold	$V_{DC/PWMI1,2(OFF)}$	–	–	0.8	V	–	PRQ-206
DC/PWMI1 DC/PWMI2 input current	$I_{DC/PWMI1,2}$	–	–	200	µA	$V_{DC/PWMI1,2} = V_{IN}$	PRQ-207
DC/PWMI1 DC/PWMI2 input current	$I_{DC/PWMI1,2}$	–	–	1	µA	$V_{DC/PWMI1,2}$ = 0.8 V	PRQ-208
DC/PWMI1 DC/PWMI2 minimum ON time	$t_{DC/PWMI1,2(ON)}$	6	–	–	µs	–	PRQ-209

8.3 Embedded PWM engine

The embedded PWM engine helps to reduce the color shift when a LED string is dimmed down without using timer or microcontroller. It generates a pulse width modulation (PWM) adjustable in frequency and duty cycle. A possible application is the daytime running light dimmed down to position light without using microcontroller or timer.

For each channel the embedded PWM dimming function is enabled if the voltage on DC/PWMI pin is in between DC/PWMI input voltage 0% dimming $V_{DC/PWM1,2(0\%)}$ and DC/PWMI input voltage 100% dimming $V_{DC/PWMI1,2(100\%)}$. This voltage is translated in the duty cycle of the PWM signal with DC/PWMI duty cycle resolution $n_{DC/PWMI}$.

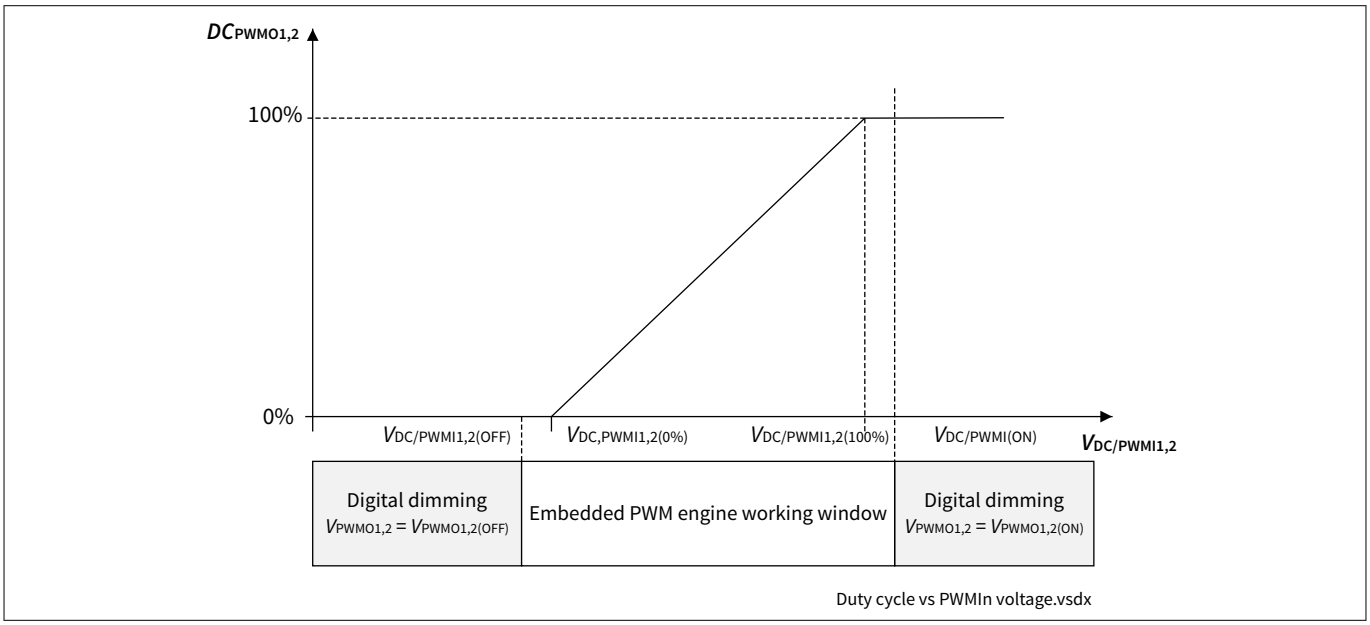


Figure 14 Relationship between $V_{DC/PWMI1,2}$ and dimming duty cycle

8 Dimming functions

If the embedded PWM dimming function is enabled the behavior of PWMO1,2 pin is the following:

- The PWMO1,2 voltage switches between PWMO1,2 output voltage ON state $V_{PWMO1,2(ON)}$ and PWMO1,2 output voltage OFF state $V_{PWMO1,2(OFF)}$
- The PWMO1,2 switching frequency depends on the resistor value placed on FPWM/FAULT1,2 pin
- The PWM duty cycle is linearly adjusted with the voltage on DC/PWMI1,2 pin

Any fault disables the embedded PWM engine and forces the voltage on PWMO1,2 pin to $V_{PWMO1,2(OFF)}$.

The resistor connected on FPWM/FAULT1,2 is used to:

- Adjust the frequency of the embedded PWM engine
- Enables two different reactions on FPWM/FAULT1,2 pin during the fault report
- Enable or disable the voltage control loop on the respective channel

If the resistor on FPWM/FAULT1,2 pin is in FPWM/FAULT high resistor range $R_{FPWM/FAULT(H)}$ the channel has the following behavior:

- The frequency of PWM engine is adjusted in f_{PWMO} range
- In case a fault is detected, it is reported on FPWM/FAULT1,2 pin with proper duty cycle
- The voltage loop is disabled and the overvoltage is detected with a comparator (detailed information are described in Protection and fault management section)

while, if resistor on FPWM/FAULT1,2 pin is in FPWM/FAULT low resistor range $R_{FPWM/FAULT(L)}$:

- The frequency of PWM engine is adjusted in f_{PWMO} range
- The faults are reported on FPWM/FAULT1,2 pin without a specific indication
- Voltage regulation loop is enabled and concurrent to current regulation loop

The frequency of embedded PWM generator can be calculated by:

$$f_{PWMO\_HR} = \frac{1}{\left(7.4 \cdot 10^{-8} \cdot R_{FPWM/FAULT}\right)} \quad (3)$$

for resistor $R_{FPWM/FAULT(H)}$ range

$$f_{PWMO\_LR} = \frac{1}{\left(7.4 \cdot 10^{-7} \cdot R_{FPWM/FAULT}\right)} \quad (4)$$

for resistor $R_{FPWM/FAULT(L)}$ range.

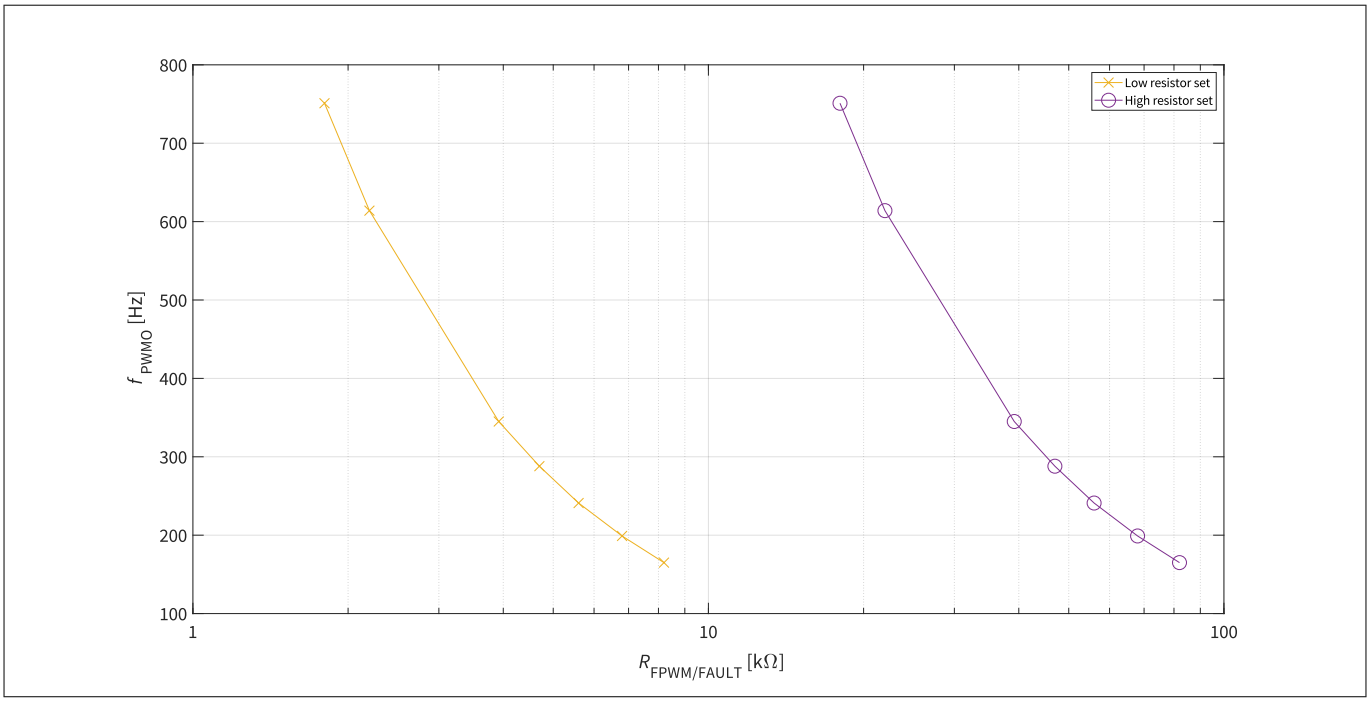


Figure 15 Relationship between $R_{FPWM/FAULT}$ and the frequency of PWMO

The table below summarizes the differences between two resistor sets on FPWM/FAULT pin

Table 13 Resistor differences on fault pin

	$R_{FPWM/FAULT(H)}$	$R_{FPWM/FAULT(L)}$
Fault report	Each fault reported with a dedicated duty cycle on the respective FPWM/FAULT1,2	The faults are reported by raising the voltage on the respective FPWM/FAULT1,2 pin until the faulty status is removed
Voltage loop	Disabled	Enabled

8.3.1 Electrical characteristics

Table 14 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
DCPWMI1 DC/PWMI2 input voltage 0% dimming	$V_{DC/PWMI1,2(0\%)}$	0.965	1	1.035	V	V_{IVCC} = 5 V	PRQ-211
DC/PWMI1 DC/PWMI2 input voltage 100% dimming	$V_{DC/PWMI1,2(100\%)}$	3.53	3.6	3.67	V	V_{IVCC} = 5 V	PRQ-212
DC/PWMI1 DC/PWMI2 equivalent pull down resistor	$R_{DC/PWMI1,2}$	1.5	2.5	3.5	MΩ	$V_{DC/PWMI1,2}$ = 4 V *1)*	PRQ-434
PWMO duty cycle	DC_{PWMO}	8	10	12	%	V_{PWMI} = 1.26 V V_{IVCC} = 5 V	PRQ-112
FPWM/FAULT1, FPWM/FAULT2 reference voltage	$V_{FPWM/FAULT1,2(REF)}$	0.72	0.80	0.88	V	–	PRQ-214
FPWM/FAULT1, FPWM/FAULT2 output current	$I_{FPWM/FAULT1,2}$	–	–	3	mA	$V_{FPWM1,2}$ = 0 V	PRQ-215
PWMO1, PWMO2 dimming frequency	$f_{PWMO1,2}$	315	345	375	Hz	$R_{FPWM1,2}$ = 3.92 kΩ	PRQ-216
PWMO1, PWMO2 dimming frequency	$f_{PWMO1,2}$	315	345	375	Hz	$R_{FPWM/FAULT1,2}$ = 39.2 kΩ	PRQ-374
DC/PWMI duty cycle resolution	$n_{DC/PWMI}$	–	10	–	bit	*1) 2)*	PRQ-313
FPWM/FAULT high range resistor	$R_{FPWM/FAULT(H)}$	18	–	90	kΩ	*1) 2)*	PRQ-590
FPWM/FAULT low range resistor	$R_{FPWM/FAULT(L)}$	1.8	–	9	kΩ	*1)* *2)*	PRQ-591

1) Not subject to production test, specified by design
2) Not subject to production test, specified by design

9 Protections and fault management

The fault conditions are identified by checking the status of PWMO1,2, IVCC and FPWM/FAULT1,2 pins. The faults on the two channels are independently managed and reported.

Each channel of the device disables the gate drivers and reports fault on its FPWM/FAULT1,2 pin if it detects:

- Short to ground
- Overvoltage on VFB1,2 pin
- Overtemperature
- Overvoltage on FBH1,2 pin
- Overcurrent

The faults are reported by raising the voltage on the respective FPWM/FAULT1,2 pin to $V_{FPWM/FAULT1,2(FAULT)}$.

The output waveform of the fault reporting depends on the resistor connected to FPWM/FAULT1,2 pin.

The status of FPWM/FAULT1,2 pin can be monitored by a microcontroller. In this case a series resistor (10 kΩ minimum) has to be used between FPWM/FAULT1,2 and the input pin of the microcontroller.

The PWMO1,2 gate driver biases the respective PMOS in OFF state to disconnect the load from the DC-DC output during:

- Overvoltage on VFB1,2 pin,
- Overvoltage on FBH1,2 pin
- Overtemperature
- Overcurrent

During a short to ground, the PMOS is biased in OFF state during the t_{S2G} and it is biased in ON state every t_{FAULT} for a (t_{SS}) to detect if the fault has been removed.

9.1 Electrical characteristics

Table 15 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FPWM/FAULT1,2 output voltage with fault	$V_{FPWM/FAULT1,2(FAULT)}$	4	–	–	V	*2)*	PRQ-609
Fault period	t_{FAULT}	9	10	11	ms	*1) 2)*	PRQ-133

1) Not subject to production test, specify by design
2) Not subject to production test, specify by design

9.2 Short to ground

The short to ground detection feature protects each channel from an excess of current during a short circuit.

Each channel detects this fault if the voltage of VFB1,2 pin is lower than short to ground voltage threshold $V_{FB1,2\_S2G}$ for a time longer than short to ground reaction time t_{S2G_RT}. After a fault time with short to ground t_{S2G} a soft start routine is triggered. The fault is released if the voltage on VFB1,2 pin is higher than ($V_{FB1,2\_S2G}$+$V_{FB1,2\_S2G\_HYST}$) at the end of the soft start

During soft-start routine, the short to ground detection is disabled and the voltage of FPWM/FAULT1,2 pin is kept at $V_{FPWM/FAULT1,2(REF)}$.

The reaction to short to ground is:

1. The voltage on FPWM/FAULT1,2 pin is raised to $V_{FPWM/FAULT1,2(FAULT)}$ for t_{S2G} time

2. After a t_{S2G} time the soft-start routine is performed
3. At the end of soft-start routine, the check on the voltage $V_{VFB1,2}$ is redone

If the fault is still present, the procedure is repeated, otherwise the channel restarts.
This routine is valid whatever resistor used on FPWM/FAULT pin.

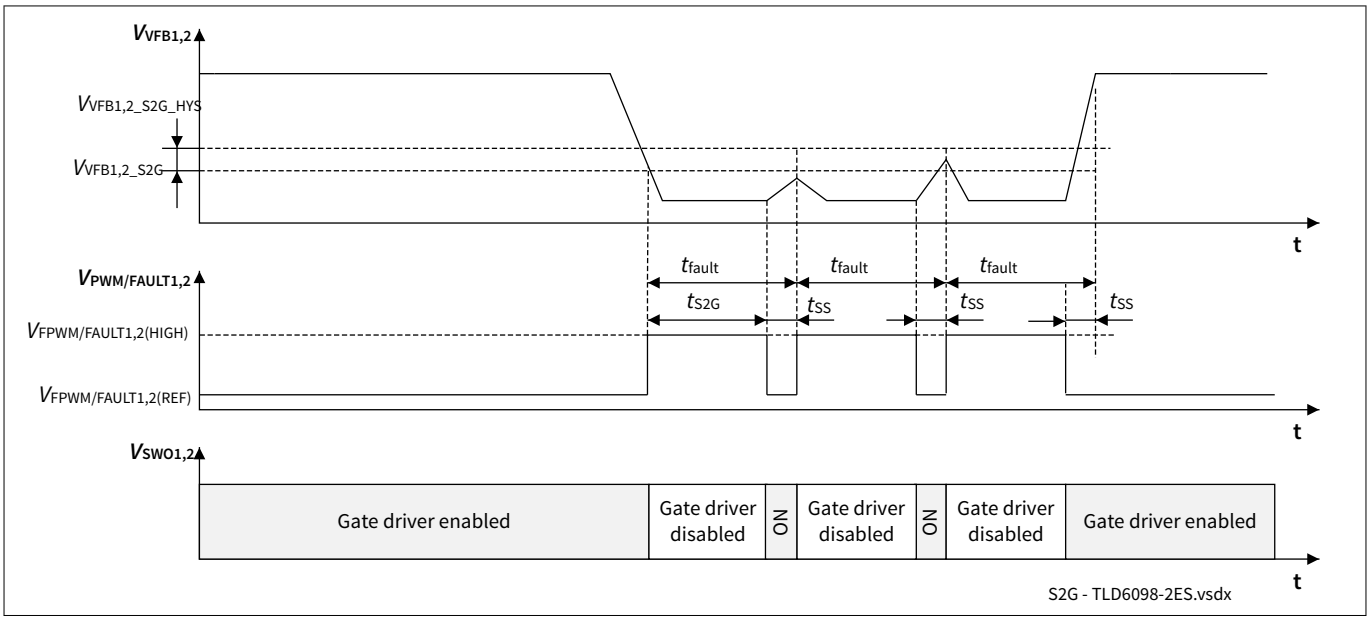


Figure 16 Timing diagram during short to ground detection

A short to ground event simultaneous with an overcurrent event is detected once even the voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(OFF)}$.
In all the other cases, the short to ground is not detected when the voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(OFF)}$.

9.2.1 Electrical characteristics

Table 16 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fault time with short to ground	t_{S2G}	7.2	8	8.8	ms	1)	PRQ-134
Short to ground reaction time	t_{S2G_RT}	4	–	20	µs	–	PRQ-121
Short to ground voltage threshold	$V_{FB1,2\_S2G}$	93	100	107	mV	Voltage decreasing	PRQ-218
Short to ground voltage hysteresis	$V_{FB1,2\_S2G\_HYST}$	–	5	10	mV	1)	PRQ-219

1) Not subject to production test, specified by design

9.3 Output overvoltage and voltage regulation

Based on the resistor used on FPWM/FAULT1,2 pin the channel implements an overvoltage detection with a comparator or enabling a voltage regulation by using the internal voltage loop.

If the resistor connected to FPWM/FAULT1,2 pin is in the $R_{FPWM/FAULT(H)}$ range, the overvoltage comparator is enabled with VFB1 VFB2 overvoltage threshold $V_{VFB1,2\_OV.}$ The fault is detected when the VFB voltage is above this threshold.

The channel reacts by:

- raising the respective $V_{FPWM/FAULT1,2}$ to $V_{FPWM/FAULT1,2(FAULT)}$ for a fault time with overvoltage t_{OVFB}
- disabling the respective NMOS gate driver for t_{FAULT}

after t_{FAULT} the voltage on VFB1,2 is rechecked and if it is still higher than ($V_{VFB1,2\_OV}$ -$V_{VFB1,2\_OV,HYS}$) the routine is repeated, else the device restarts with a soft-start routine.

if the resistor connected to FPWM/FAULT1,2 pin is in the $R_{FPWM/FAULT(H)}$ range, the fault is detected even the voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(OFF)}$.

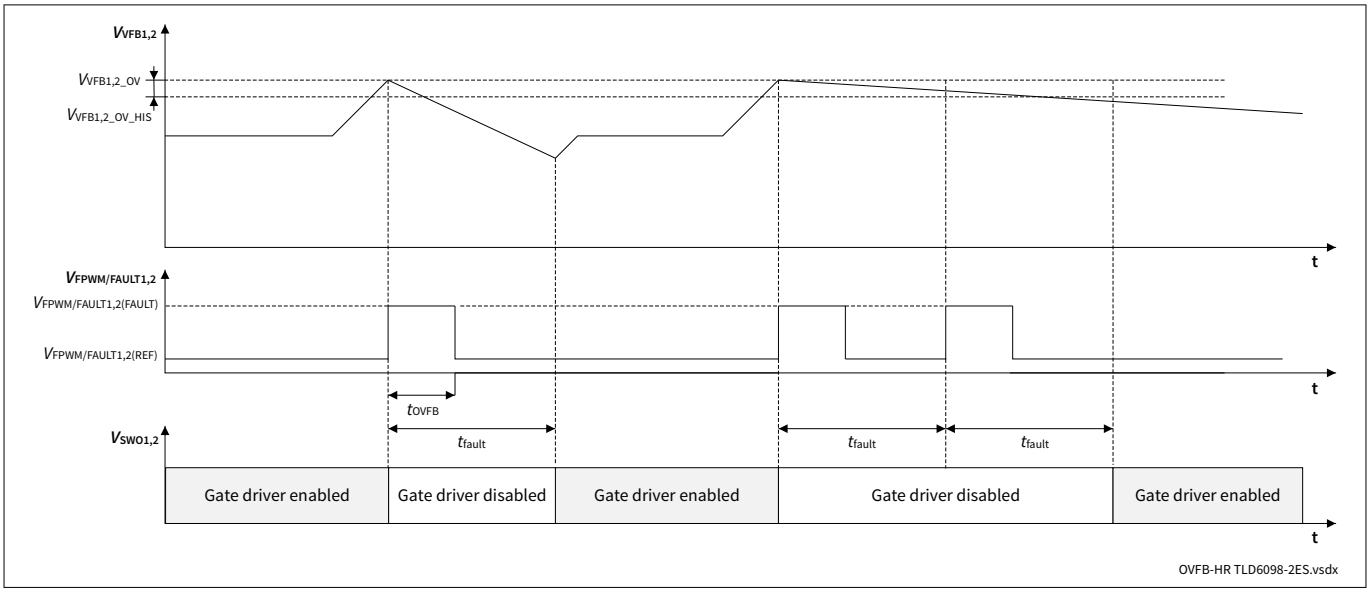


Figure 17 Timing diagram during overvoltage detection

The channel works as a voltage regulator with the voltage loop enabled if the resistor connected to FPWM/FAULT1,2 pin is in the $R_{FPWM/FAULT(L)}$ range.

If the voltage on DC/PWMI1,2 pin is higher than $V_{DC/PWMI1,2(ON)}$ the channel behaves as follow:

The voltage loop is taking over the regulation when the voltage on VFB1,2 pin goes higher than $V_{FB1,2\_VM(ON)}$. At this time the voltage on FPWM/FAULT1,2 pin is raised to $V_{FPWM/FAULT1,2(FAULT)}$.

The channel also reports when the voltage on VFB1,2 pin goes below $V_{FB1,2\_VM(OFF)}$ to highlight the voltage loop is ineffective. In this condition the voltage on FPWM/FAULT pin is $V_{FPWM/FAULT1,2(REF)}$.

If the voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(ON)}$ the channel behaves as follow:

The voltage loop is taking over the regulation when the voltage on VFB1,2 pin goes higher than $V_{FB1,2\_VM(ON)}$. the voltage of FPWM/FAULT1,2 pin is kept to $V_{FPWM/FAULT1,2(REF)}$.

The channel also reports when the voltage on VFB1,2 pin goes below $V_{FB1,2\_VM(OFF)}$ to highlight the voltage loop is ineffective. In this condition the voltage on FPWM/FAULT pin is kept to $V_{FPWM/FAULT1,2(REF)}$.

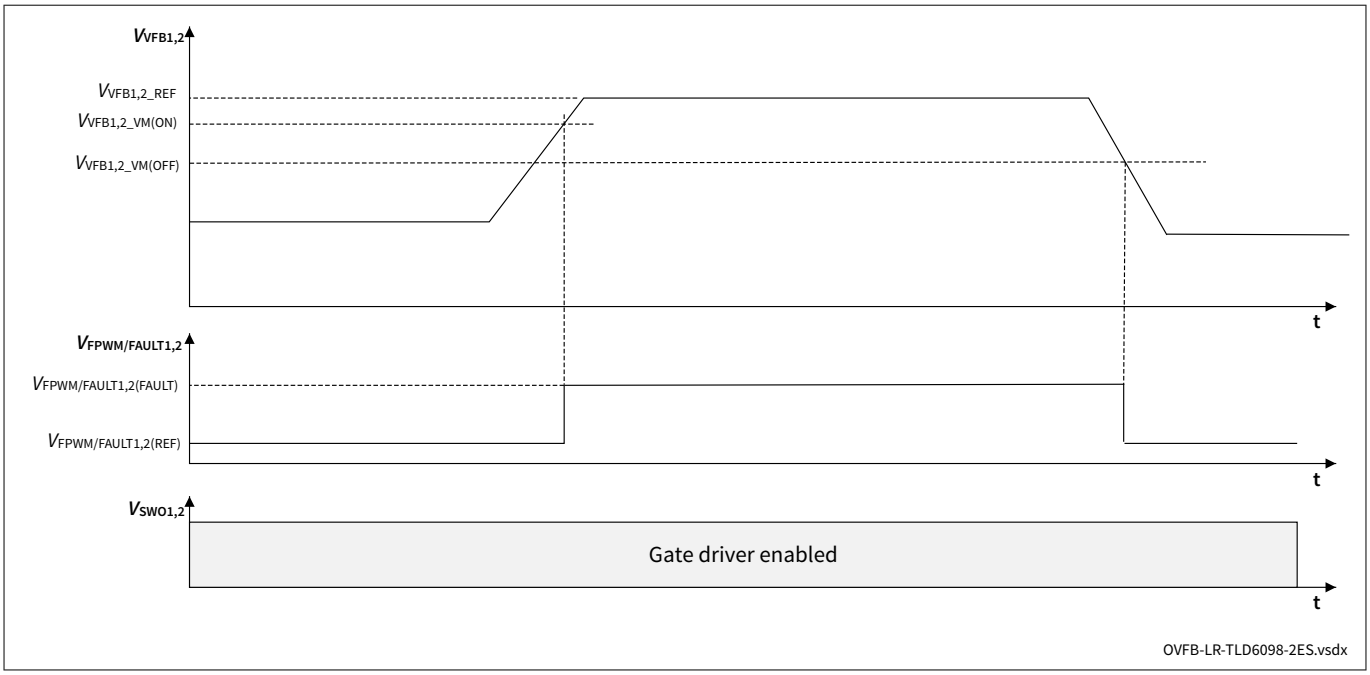


Figure 18 Timing diagram in voltage regulation

9.3.1 Electrical characteristics

Table 17 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VFB1, VFB2 overvoltage threshold	$V_{VFB1,2\_OV}$	1.568	1.6	1.632	V	Voltage increasing	PRQ-217
VFB overvoltage hysteresis	$V_{VFB\_OV\_HYS}$	180	200	220	mV	1)	PRQ-323
VFB1, VFB2 input current	$I_{VFB1,2}$	-1	-0.1	1	µA	$V_{FB1,2}$ = 1.6 V	PRQ-221
VFB1, VFB2 voltage mode ON thresholds	$V_{VFB1,2\_VM(ON)}$	1.45	1.5	1.55	V	Voltage increasing	PRQ-408
VFB1, VFB2 voltage mode OFF threshold	$V_{VFB1,2\_VM(OFF)}$	1.3	1.35	1.4	V	Voltage decreasing	PRQ-409
Fault time with overvoltage	t_{OVFB}	3.6	4	4.4	ms	1)	PRQ-135

1) Not subject to production test, specified by design

9.4 Overvoltage on FBH pin

The channels have a protection feature to prevent an excess voltage on FBH1,2 pin. The report of this fault depends on the resistor connected to FPWM/FAULT1,2 pin.

An overvoltage on FBH1,2 pin fault is detected if the voltage $V_{FBH1,2}$ is higher than FBH1,2 overvoltage high threshold $V_{FBH1,2(H)}$ and the fault is released when the voltage $V_{FB1,2}$ is below the FBH overvoltage low threshold $V_{FBH1,2(L)}$.
With a resistor on FPWM/FAULT1,2 pin in $R_{FPWM/FAULT(H)}$ range the channel reacts by:

- Disabling the respective NMOS gate driver
- Raising the voltage of FPWM/FAULT1,2 pin to $V_{FPWM/FAULT1,2(FAULT)}$ for t_{FBH} time
- After t_{FAULT} period, the device checks if $V_{FBH1,2}$ is still higher than $V_{FBH1,2(L)}$

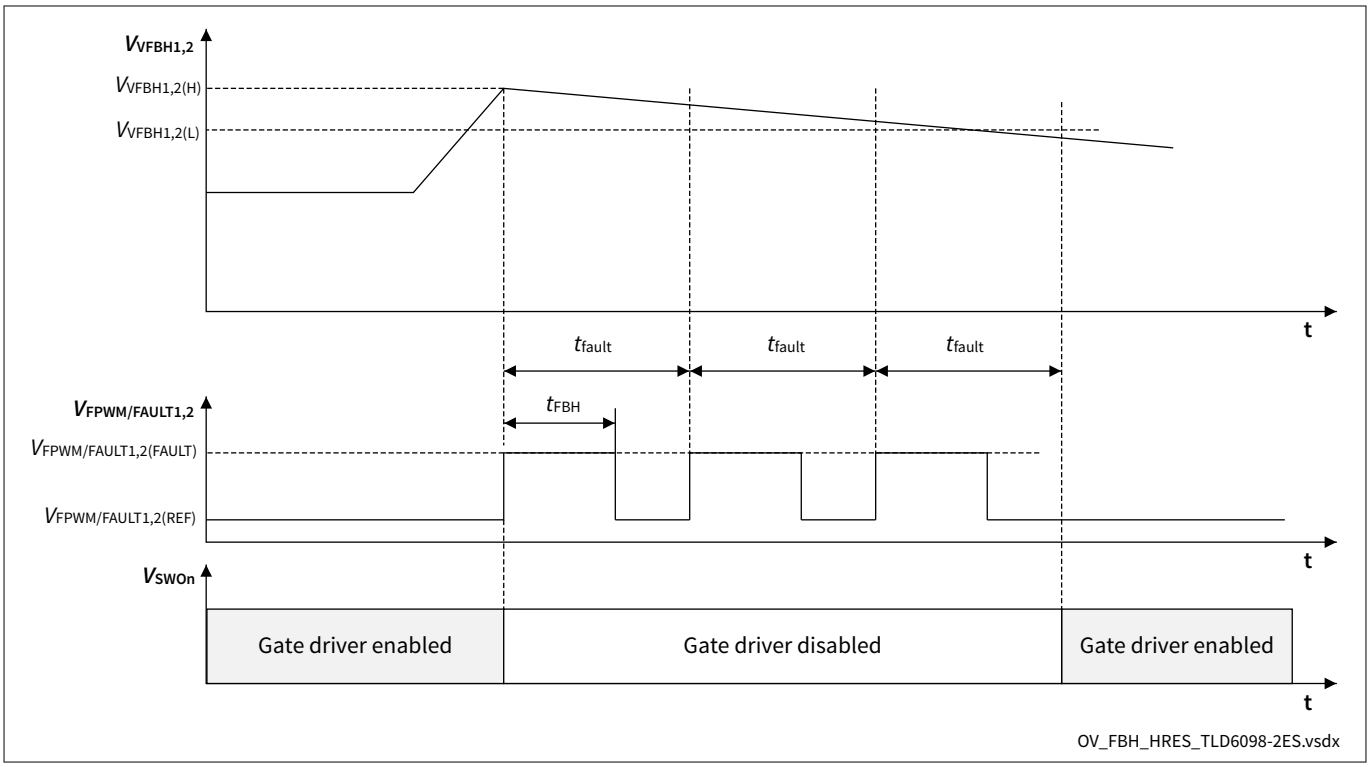


Figure 19 Timing diagram during overvoltage on FBH1,2 detection with $R_{FPWM/FAULT(H)}$ used on FPWM/FAULT1,2 pin

With a resistor on FPWM/FAULT1,2 pin in $R_{FPWM/FAULT(L)}$ range the channel reacts to the fault by:

- Disabling the respective NMOS gate driver
- Raising the voltage of respective FPWM/FAULTn pin to $V_{FPWM/FAULT1,2(FAULT)}$
- After t_{FAULT} period, the device checks if the voltage on FBH pin is still higher than $V_{FBH1,2(L)}$

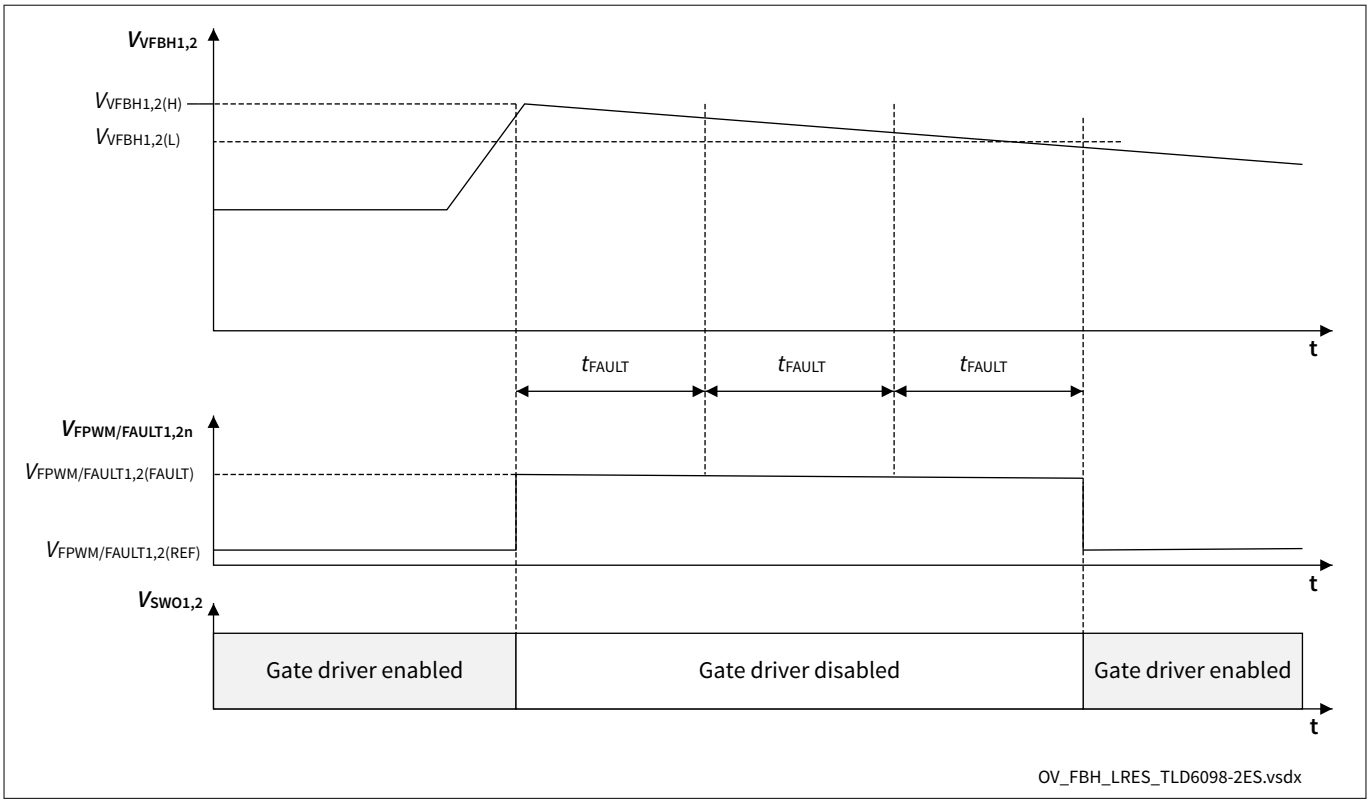


Figure 20 Timing diagram during overvoltage on FBH detection with $R_{FPWM/FAULT(L)}$ used on FPWM/FAULT1,2 pin

When the fault disappears, the channel restarts with soft-start routine and lowers the voltage of FPWM/FAULT1,2 pin to $V_{FPWM/FAULT1,2(REF)}$.

If the fault appears during the soft-start routine, it interrupts the soft-start for a t_{FAULT} time and then the routine restarts.

The fault is detected even when the voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(OFF)}$.

9.4.1 Electrical characteristics

Table 18 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
FBH1 FBH2 overvoltage upper threshold	$V_{FBH1,2(H)}$	70	–	75	V	$V_{FBH1,2}$ increasing	PRQ-414
FBH1 FBH2 overvoltage lower threshold	$V_{FBH1,2(L)}$	65	–	–	V	$V_{FBH1,2}$ decreasing	PRQ-415
Fault time FBH	t_{FBH}	5.4	6	6.6	ms	1)	PRQ-329

1) Not subject to production test, specified by design

9.5 Output overcurrent

An output overcurrent event could damage the load if the current exceed the load specification. The output overcurrent detection increases the system reliability by reducing the load average current.

The output overcurrent detection acts independently for each channel.

The output overcurrent is detected when voltage across FBH1,2 and FBL1,2 is higher than overcurrent detection threshold $V_{OC\_200\%}$.

The channel reacts in overcurrent detection time $t_{OC\_200\%}$ by increasing the voltage of PWMO1,2 pin to $V_{PWMO1,2(OFF)}$ and disabling the respective NMOS gate driver.

The protection is released when the voltage across FBH1,2 and FBL1,2 drops below ($V_{OC\_200\%}$ - V_{OC_HYS}). At this time the NMOS gate driver is enabled again and the voltage of PWMO1,2 pin evolves as demanded by the dimming features.

A continuously re-triggering of the protection could cause an overheating of the PMOS. Then a timer records the period in which the channel is in over current state. The fault reporting depends on the resistor used on FPWM/FAULT pin.

With a resistor on FPWM/FAULT1,2 pin in $R_{FPWM/FAULT(H)}$ range, the channel reacts to an overcurrent by:

- Entering into overcurrent state
- Disables the NMOS gate driver and raises the voltage on PWMO1,2 pin to $V_{PWMO1,2(OFF)}$
- As soon as ($V_{FBH1,2}$ - $V_{FBL1,2}$) < ($V_{OC\_200\%}$ - V_{OC_HYS}) the NMOS gate driver is enabled again
- PWMO1,2 pin is again controlled by the dimming features
- Exiting from the overcurrent state

When the cumulative time in which the channel is in overcurrent state reaches the overcurrent detection t_{OC} in a time window of 8*t_{FAULT} the channel:

- Raises the voltage of FPWM/FAULT1,2 pin at $V_{FPWM/FAULT1,2(FAULT)}$ for the overcurrent fault time $t_{FBH-FBL}$ and then releases it to $V_{FPWM/FAULT1,2(REF)}$ for (t_{FAULT} - $t_{FBH-FBL}$)
- Repeats this sequence 8 times

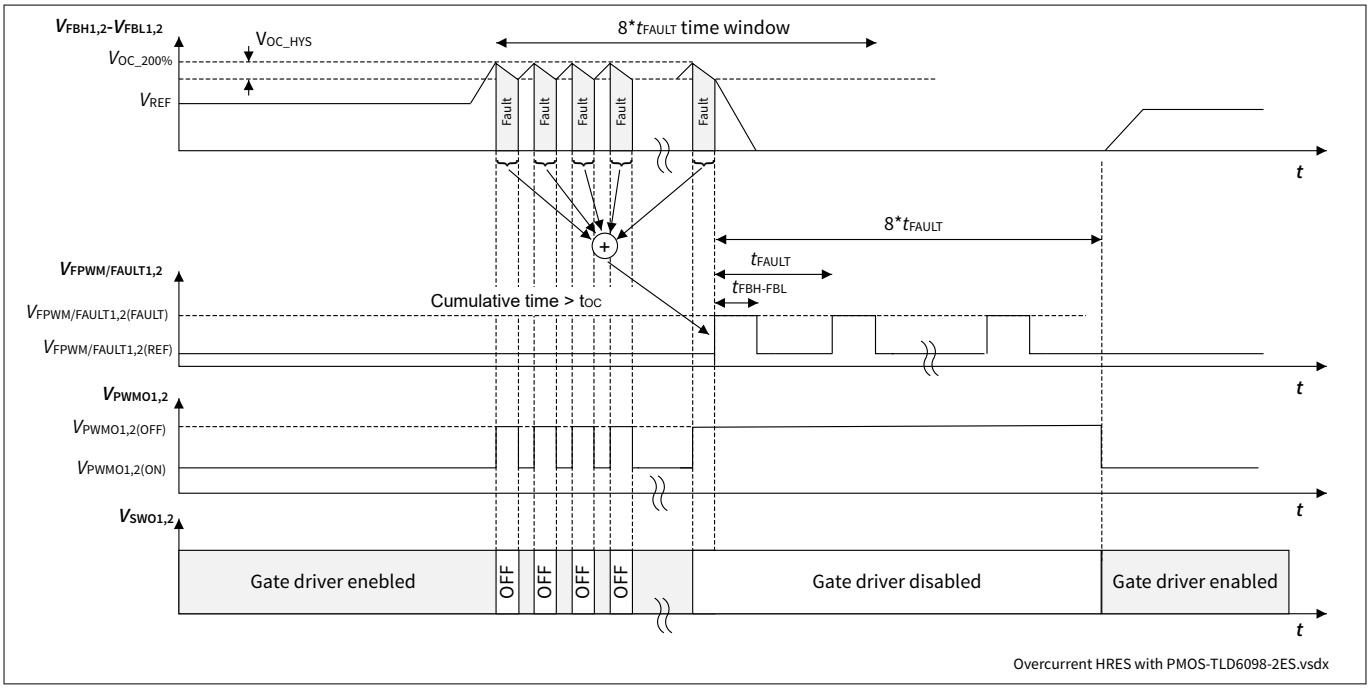


Figure 21 System behavior with $R_{FPWM/FAULT(H)}$ during overcurrent detection with PMOS as dimming/protection element

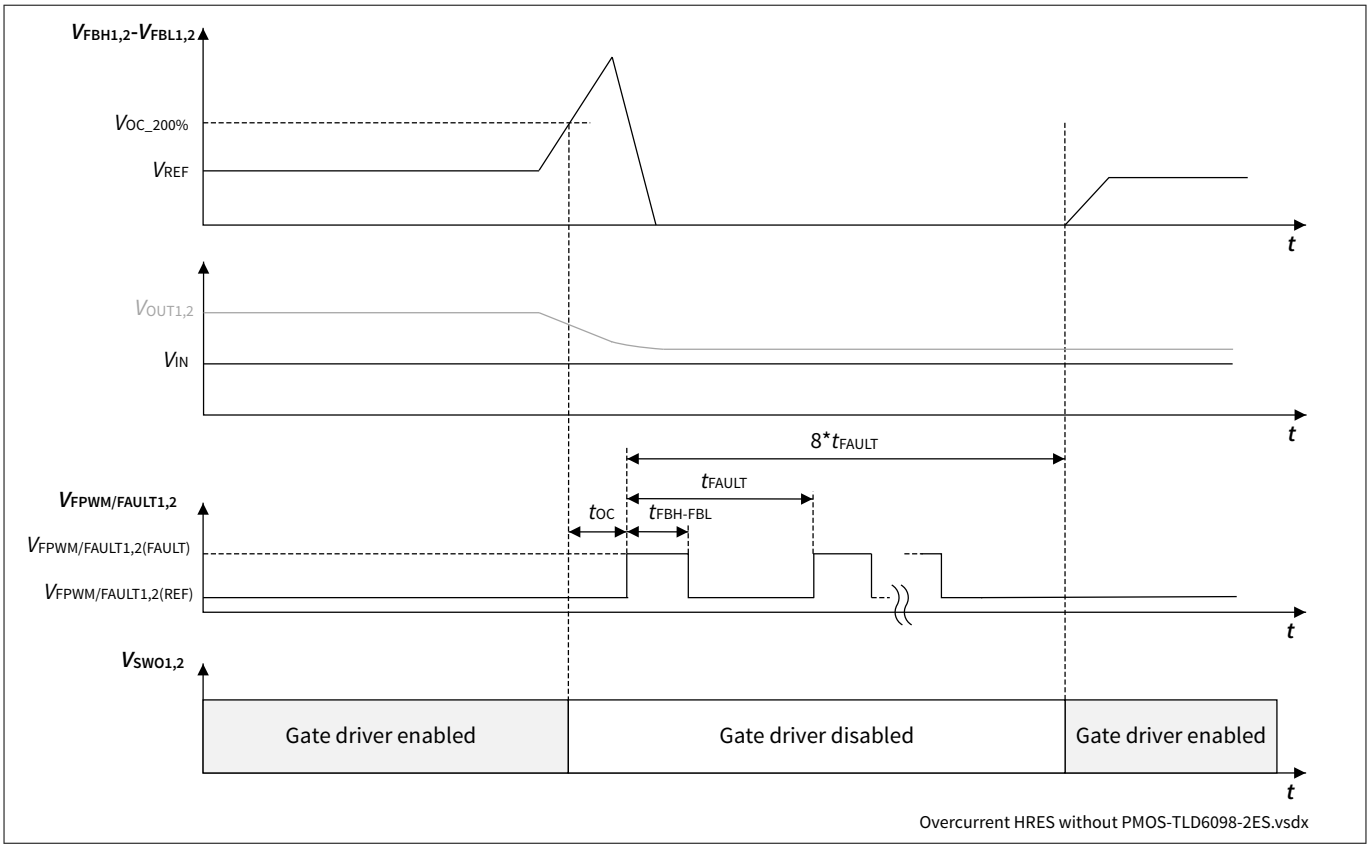


Figure 22 System behavior with $R_{FPWM/FAULT(H)}$ during overcurrent detection without PMOS as dimming/protection element

With a resistor on FPWM/FAULT pin in $R_{FPWM/FAULT(L)}$ range, the channel reacts to an overcurrent by:

- Entering into the overcurrent state
- Disabling the NMOS gate driver and raises the voltage on PWMO1,2 pin to $V_{PWMO1,2(OFF)}$
- As soon as ($V_{FBH1,2}$ - $V_{FBL1,2}$) < ($V_{OC\_200\%}$ - V_{OC_HYS}) the NMOS gate driver is enabled again
- PWMO1,2 pin is again controlled by the dimming feature
- Exiting from the overcurrent state

When the cumulative time in which the device is in overcurrent state reaches t_{OC} in a time window of 8*t_{FAULT}

- Raises the voltage of FPWM/FAULT1,2 pin at $V_{FPWM/FAULT1,2(FAULT)}$ for a time 8*t_{FAULT} and then releases it to $V_{FPWM/FAULT1,2(REF)}$

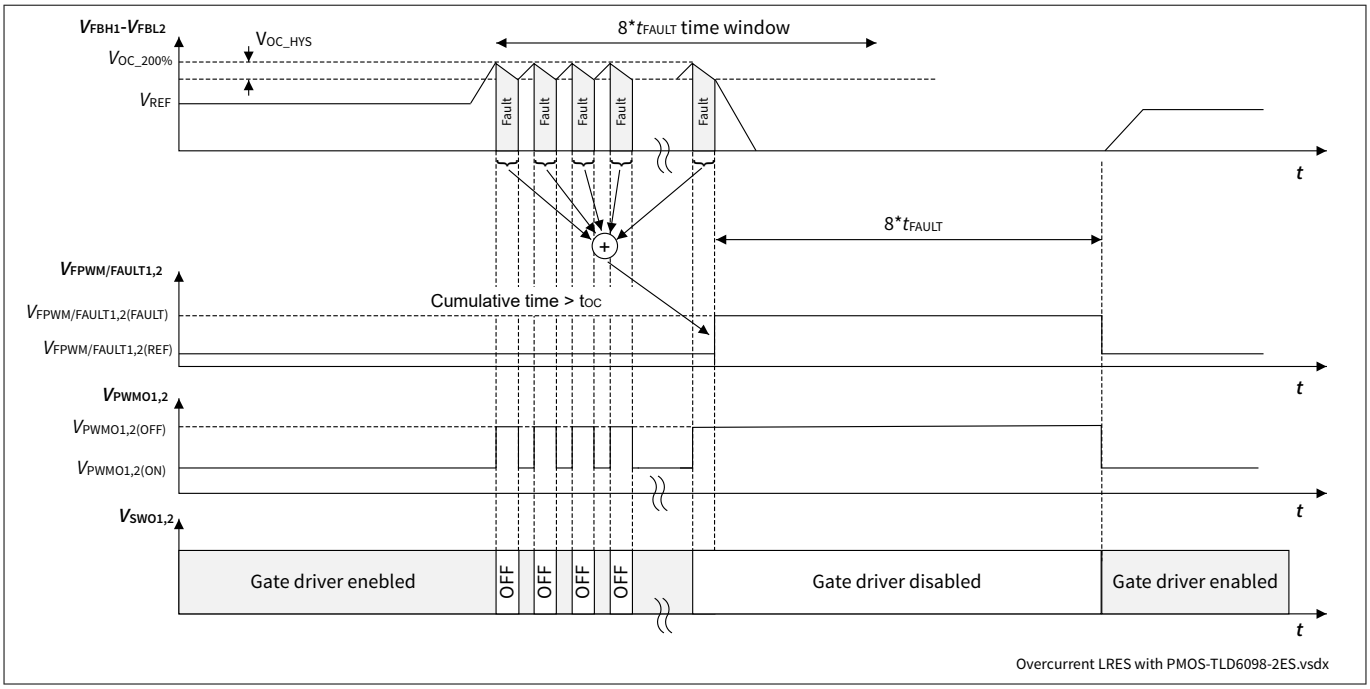


Figure 23 System behavior with $R_{FPWM/FAULT(L)}$ during overcurrent detection with PMOS as dimming/protection element

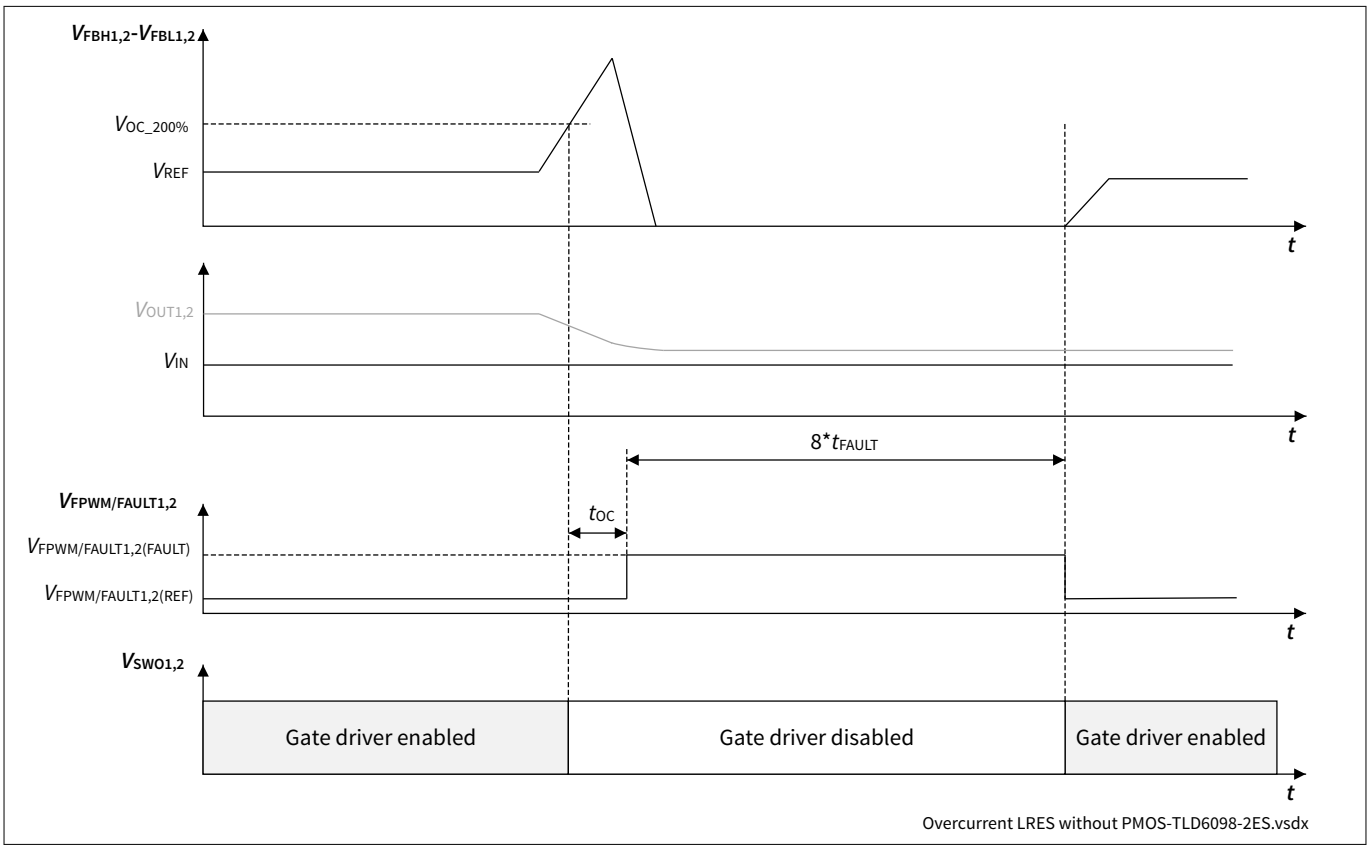


Figure 24 System behavior with $R_{FPWM/FAULT(L)}$ during overcurrent detection without PMOS as dimming/protection element

During the overcurrent detection, the t_{S2G_RT} filter time is bypassed. In case of simultaneous short to ground detection and overcurrent detection, the channel reacts to short to ground failure, cumulating the time in

which the channel is in overcurrent state. When the cumulated time reaches the t_{OC}, in a time window of 8*t_{FAULT}, the overcurrent is detected.

The fault is detected even the voltage on DC/PWMI1,2 pin is lower than $V_{DC/PWMI1,2(OFF)}$.

9.5.1 Electrical characteristics

Table 19 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overcurrent detection threshold	$V_{OC\_200\%}$	280	300	–	mV	$V_{FBH1,2}$-$V_{FBL1,2}$ increasing	PRQ-604
Overcurrent detection hysteresis	V_{OC_HYS}	15	–	35	mV	1)	PRQ-532
Overcurrent detection time	t_{OC}	3.6	4	4.4	ms	1)	PRQ-533
Overcurrent fault time	$t_{FBH-FBL}$	1.8	2	2.2	ms	1)	PRQ-555
Reaction time during overcurrent detection	$t_{OC\_200\%}$	–	–	2	µs	1)	PRQ-538

1) Not subject to production test, specified by design

9.6 Overtemperature

Thermal shutdown is an internal feature designed to prevent the device destruction and it is not intended for continuous use in normal operation.

If the junction temperature reaches the overtemperature shutdown $T_{J(SD)}$, the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator.

The junction temperature is checked each t_{FAULT} period, and when it is cooled down to ($T_{J(SD)}$-$T_{J(SD\_HYS)}$) the device will automatically restart with a soft-start.

The thermal shutdown operates on both the channels

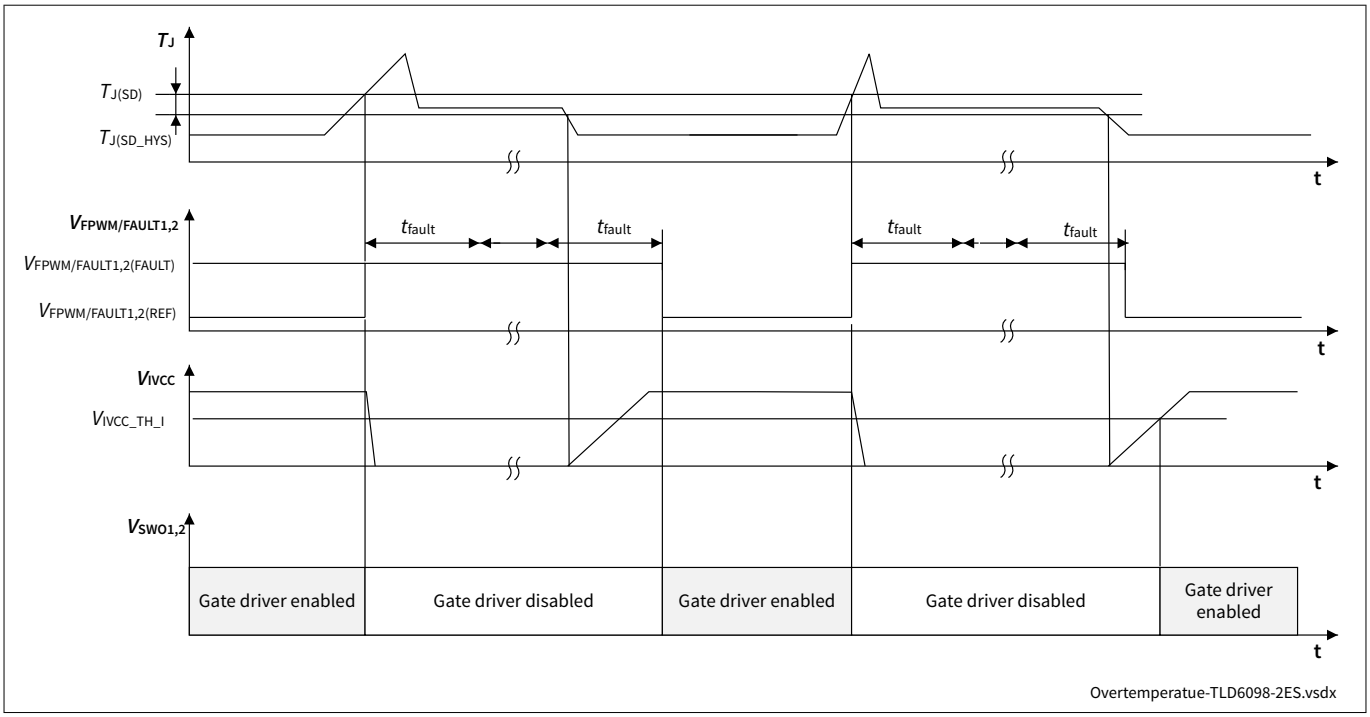


Figure 25 Timing diagram during overtemperature protection

9.6.1 Electrical characteristics

Table 20 Electrical characteristics

V_{IN} = 8 V to 36 V; T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overtemperature shutdown	$T_{J(SD)}$	160	175	190	°C	1)	PRQ-336
Overtemperature shutdown hysteresis	$T_{J(SD\_HYS)}$	–	10	–	°C	1)	PRQ-337

1) Not subject to production test, specified by design

10 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device*

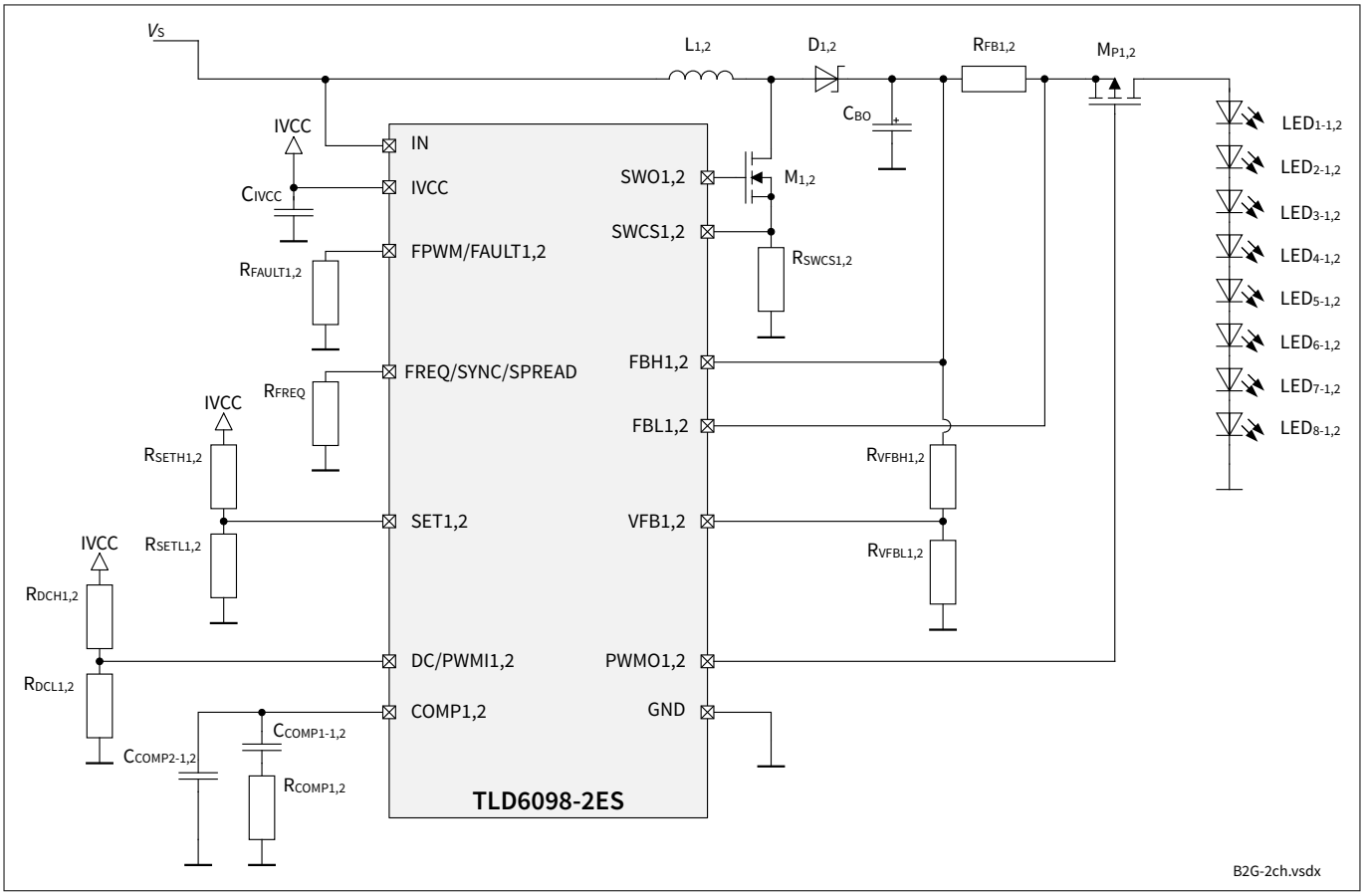


Figure 26 Boost to battery application schematic

***Note**: The figure applies whether looking at a single channel or both channels. The channels are identical and independent.*

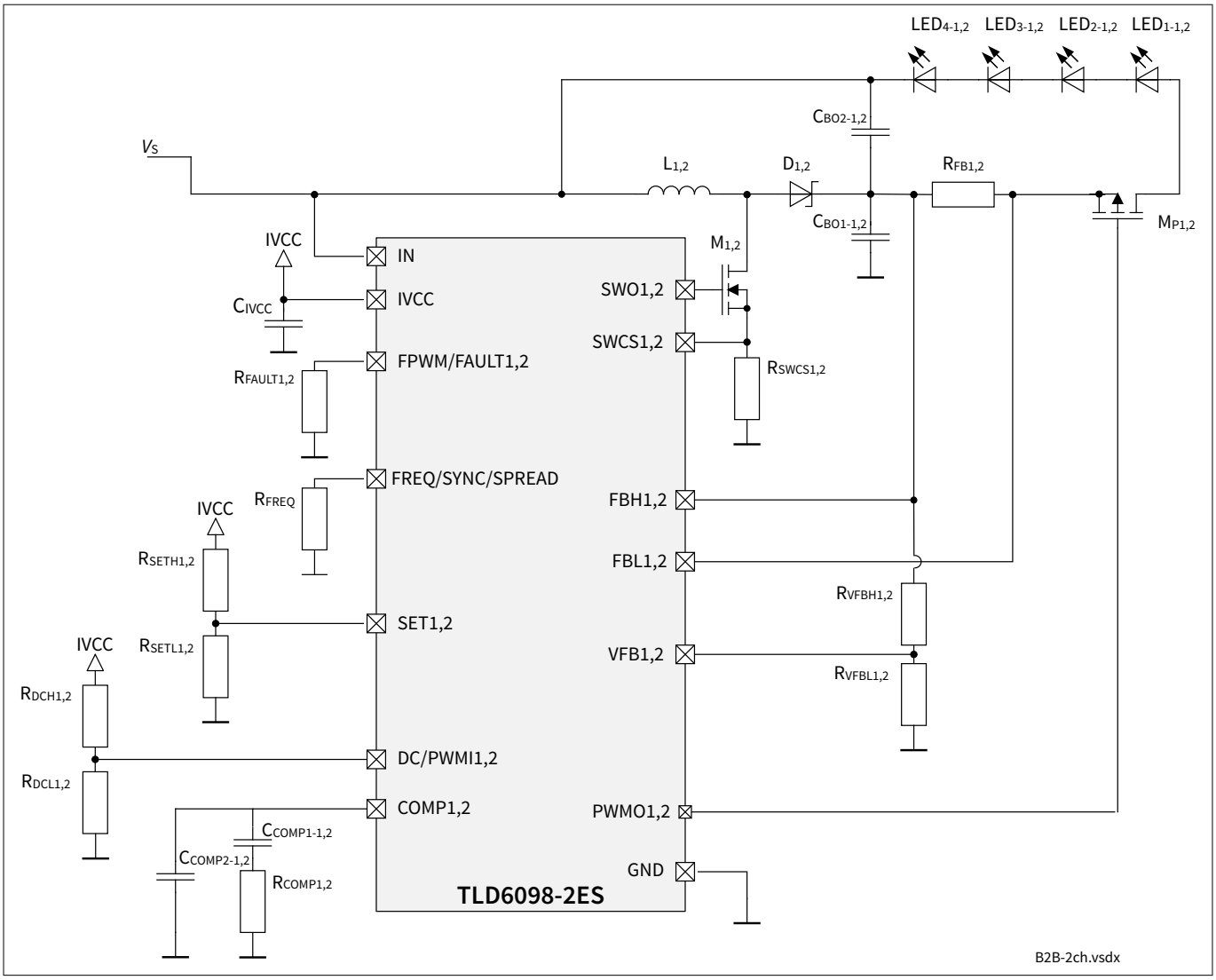


Figure 27 Boost to battery application schematic

***Note**: The figure applies whether looking at a single channel or both channels. The channels are identical and independent.*

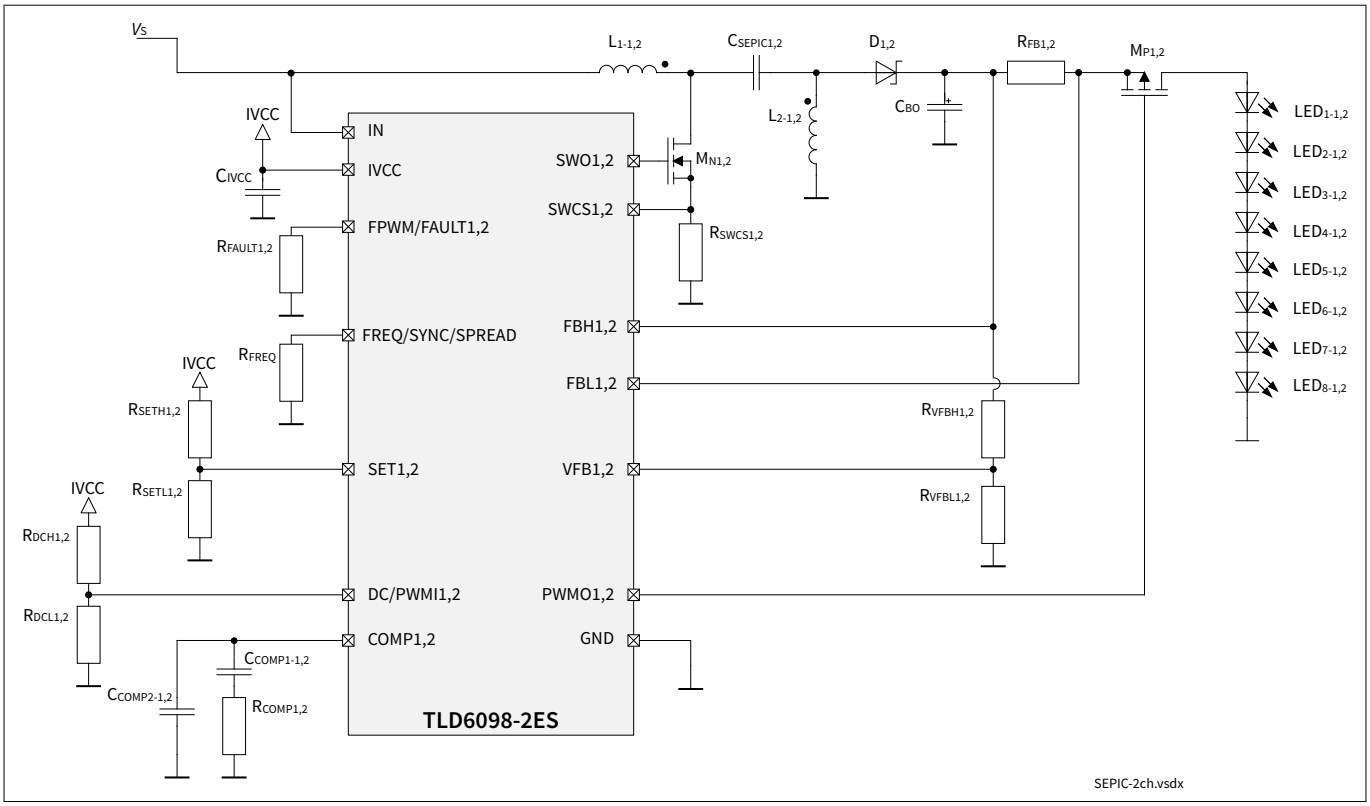


Figure 28 SEPIC application schematic

***Note**: The figure applies whether looking at a single channel or both channels. The channels are identical and independent.*

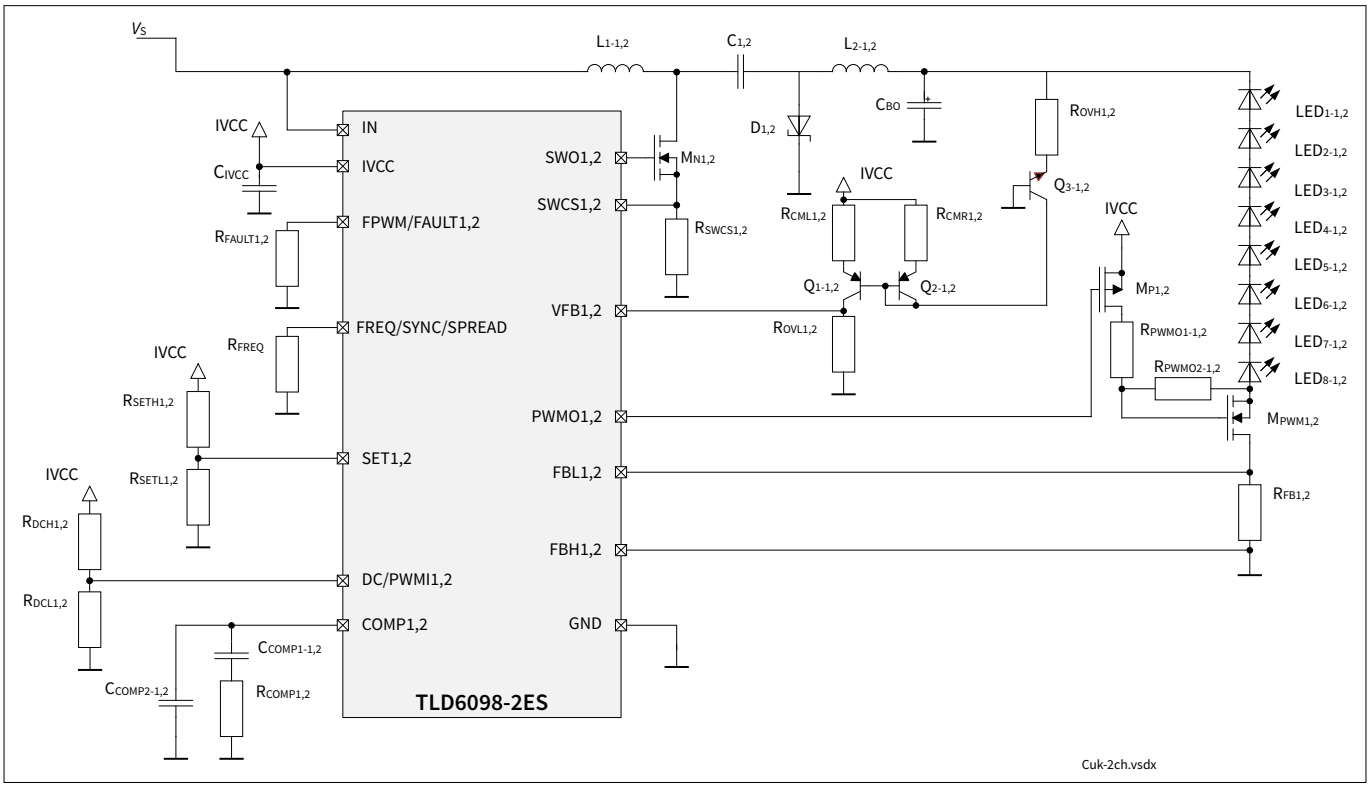


Figure 29 Cuk application schematic

***Note**: The figure applies whether looking at a single channel or both channels. The channels are identical and independent.*

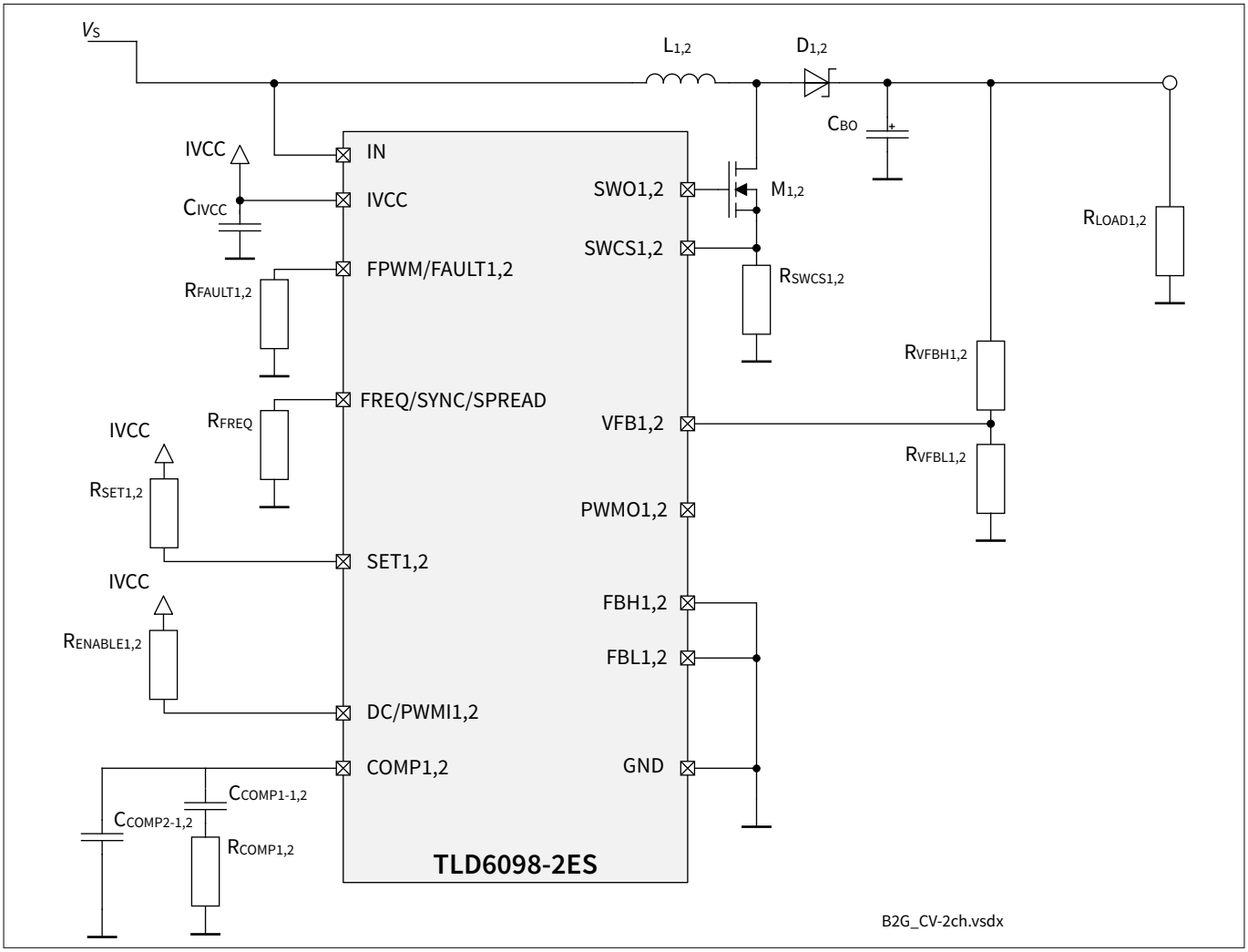


Figure 30 Constant output voltage boost to ground DC-DC application schematic

***Note**: The figure applies whether looking at a single channel or both channels. The channels are identical and independent.*

11 Package

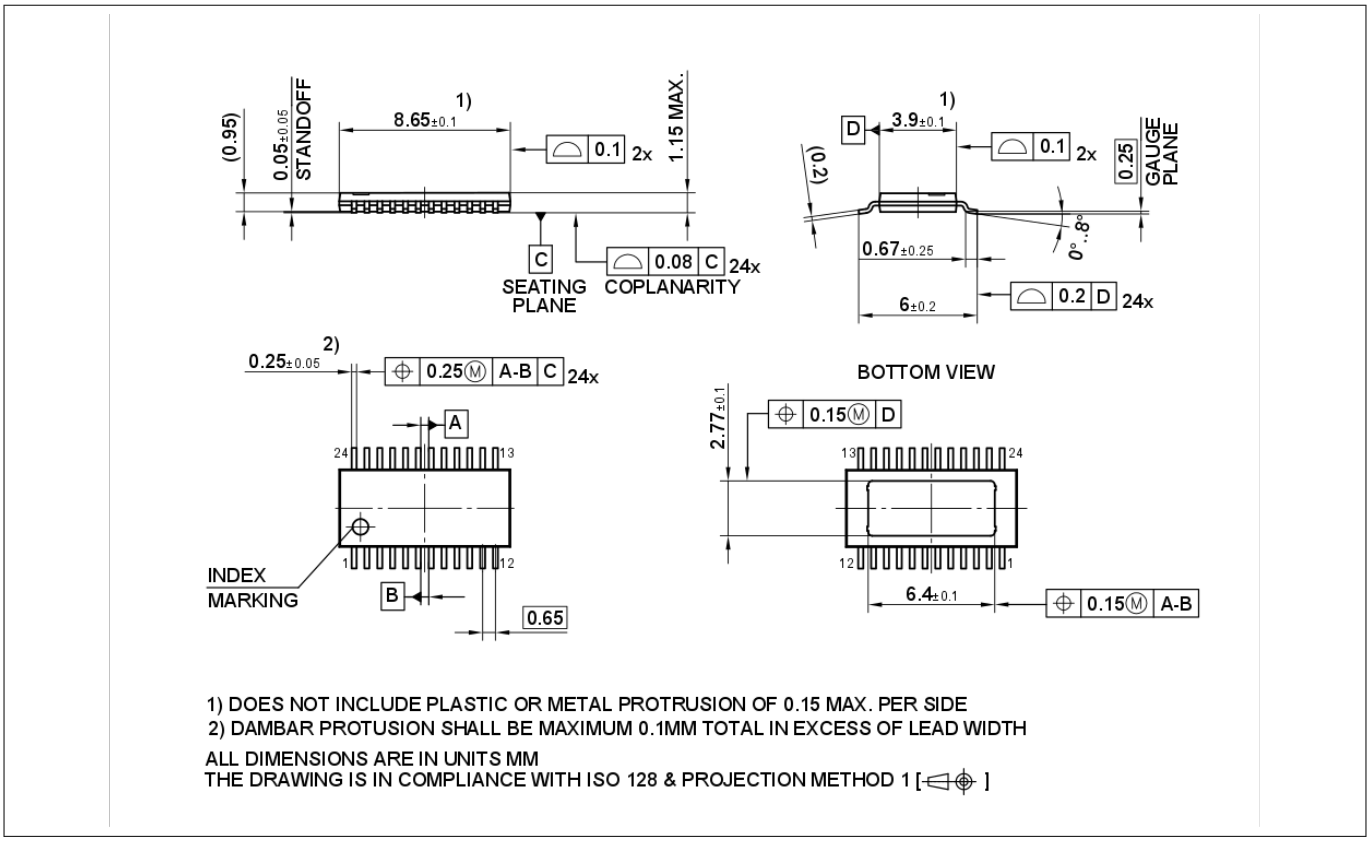


Figure 31 Package dimensions PG-TSDSO-24

Note**:* ***Green product (RoHS compliant) *To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).*

Further information on packages *https://www.infineon.com/packages*

12 Revision history

Document version	Date of release	Description of changes
Rev.1.20	2024-09-27	• Description update of voltage regulation
Rev.1.10	2021-09-30	• Editorial changes • New application schematics
Rev.1.00	2021-04-16	Initial Datasheet

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-09-27

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-xem1632149255298

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.