IRFF110

PD-90423E

Repetitive Avalanche and dv/dt Rated Power MOSFET
Thru-Hole (TO-205AF / TO-39)
100V, 3.5A, N-channel

Features

- Repetitive avalanche ratings
- Dynamic dv/dt rating
- Hermetically sealed
- Simple drive requirements
- ESD rating: Class 1A per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Product Summary

- **BV_{DSS}:** 100V
- **I_D:** 3.5A
- **$R_{DS(on),max}$:** 0.6Ω
- **$Q_{G,max}$:** 8.1nC

TO-205AF / TO-39

Description

HEXFET POWER MOSFET technology is the key to IR HiRel's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high trans conductance; superior reverse energy and diode recovery dv/dt capability. The HEXFET transistors also feature all of the well-established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters. They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level
IRFF110	TO-205AF / TO-39	COTS
2N6782	TO-205AF / TO-39	COTS
JANTX2N6782	TO-205AF / TO-39	JANTX
JANTXV2N6782	TO-205AF / TO-39	JANTXV

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	3.5	A
I_{D2} @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	2.25	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	14	A
P_D @ T_C = 25°C	Maximum Power Dissipation	15	W
	Linear Derating Factor	0.12	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	68	mJ
I_{AR}	Avalanche Current [1]	3.5	A
E_{AR}	Repetitive Avalanche Energy [1]	1.5	mJ
dv/dt	Peak Diode Reverse Recovery [3]	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	0.98 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 25V, starting T_J = 25°C, L = 11.1mH, Peak I_L = 3.5A

[3] $I_{SD} \leq$ 3.5A, di/dt ≤ 75A/µs, $V_{DD} \leq$100 V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D =1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.60	Ω	V_{GS} =10 V, I_{D2} = 2.25A [1]
		—	—	0.61		V_{GS} = 10V, I_{D2} = 3.5A [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
Gfs	Forward Transconductance	0.8	—	—	S	V_{DS} = 15V, I_{D2} = 2.25A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS} = 80V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge		—	8.1	nC	I_{D1} = 3.5A V_{DS} = 50V V_{GS} = 10V
Q_{GS}	Gate-to-Source Charge		—	1.7		
Q_{GD}	Gate-to-Drain (‘Miller’) Charge		—	4.5		
$t_{d(on)}$	Turn-On Delay Time	—	—	15	ns	I_{D1} = 3.5A ** V_{DD} = 50V R_G = 7.5Ω V_{GS} = 10V
t_r	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	25		
t_f	Fall Time	—	—	20		
L_s +L_D	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C_{iss}	Input Capacitance	—	180	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	82	—		
C_{rss}	Reverse Transfer Capacitance	—	15	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.5	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	14	A	
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J = 25°C, I_S = 3.5A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	180	ns	T_J = 25°C, I_F = 3.5A, V_{DD} ≤ 50V di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	—	1.3	—	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	8.33	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	175	

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

3 Electrical Characteristics Curves

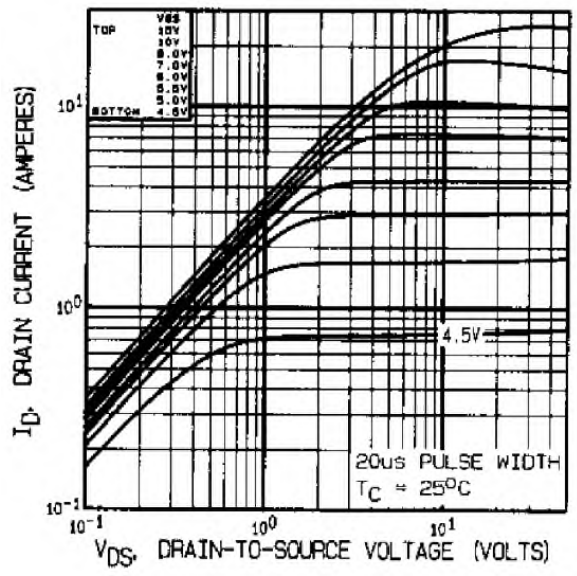


Figure 1 Typical Output Characteristics

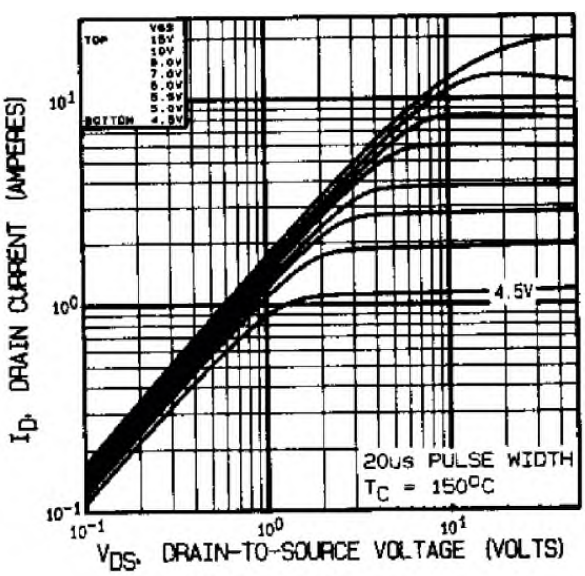


Figure 2 Typical Output Characteristics

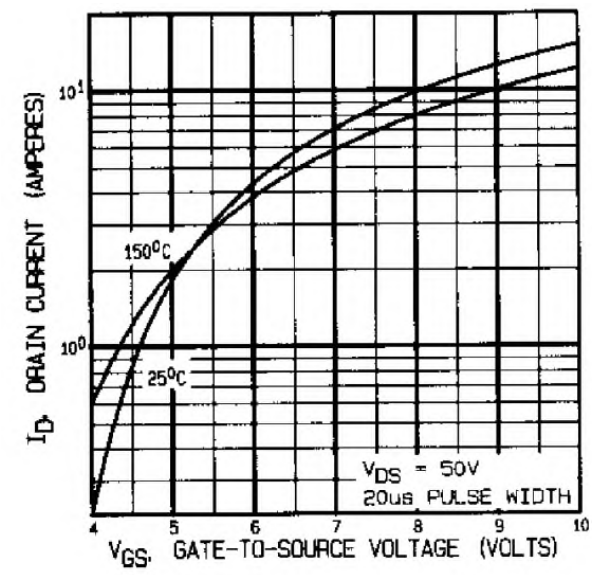


Figure 3 Typical Transfer Characteristics

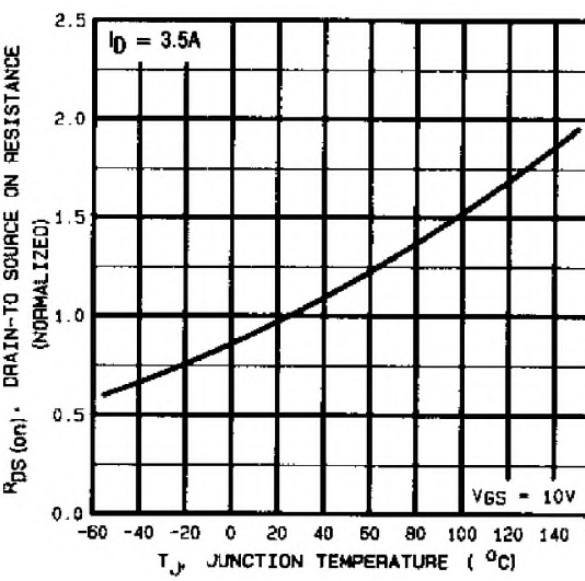


Figure 4 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves

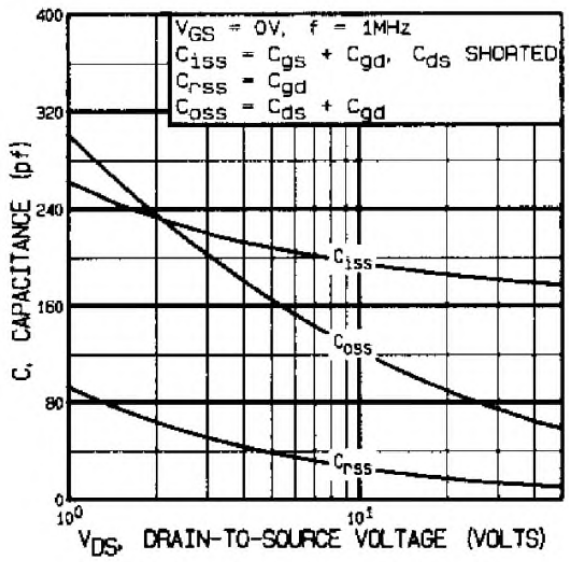


Figure 5 **Typical Capacitance Vs. Drain-to-Source Voltage**

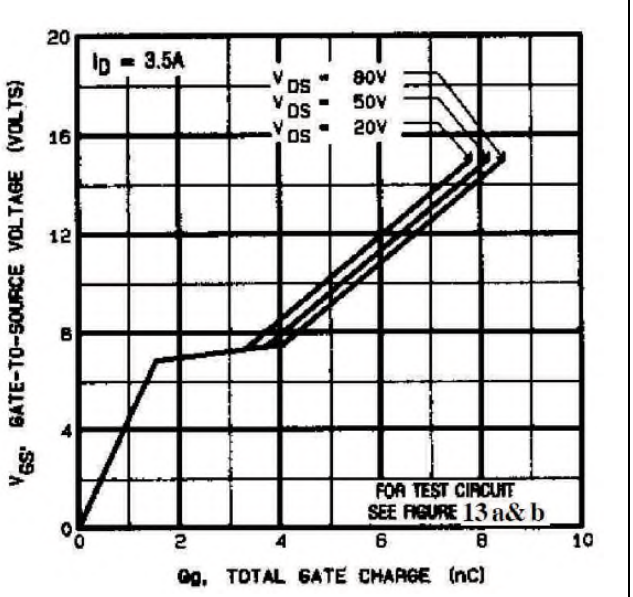


Figure 6 **Typical Gate Charge Vs. Gate-to-Source Voltage**

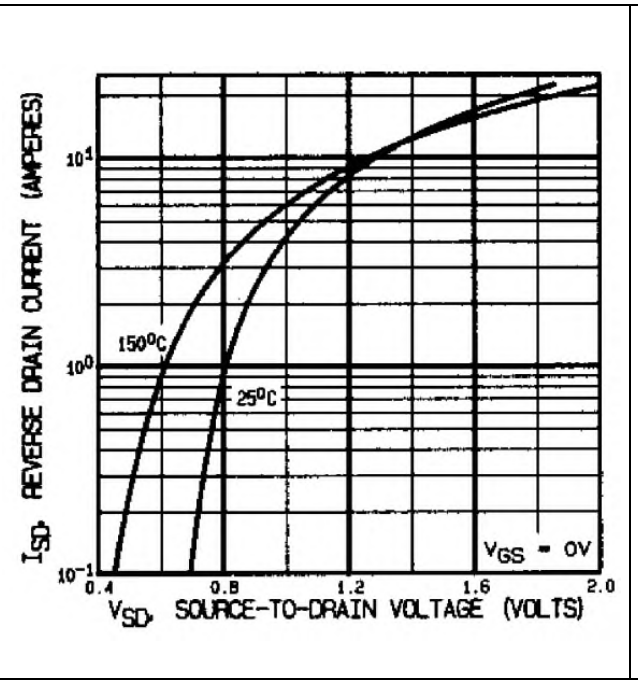


Figure 7 **Typical Source-Drain Diode Forward Voltage**

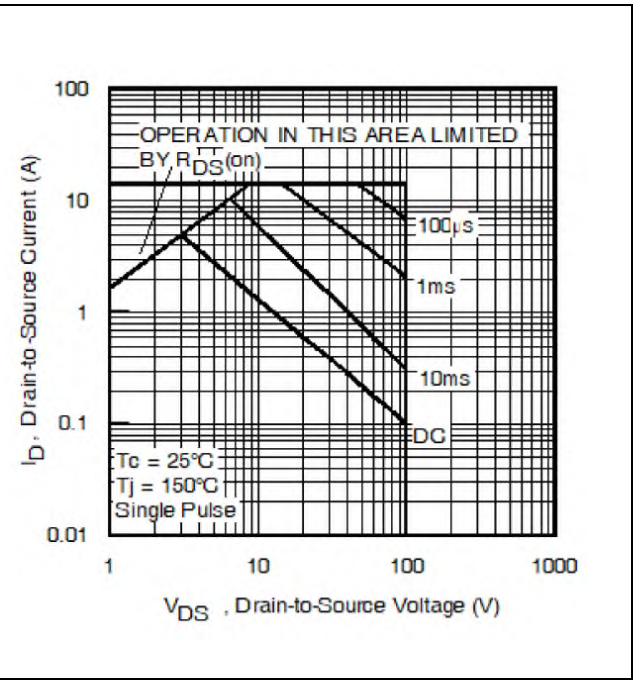


Figure 8 **Maximum Safe Operating Area**

Electrical Characteristics Curves

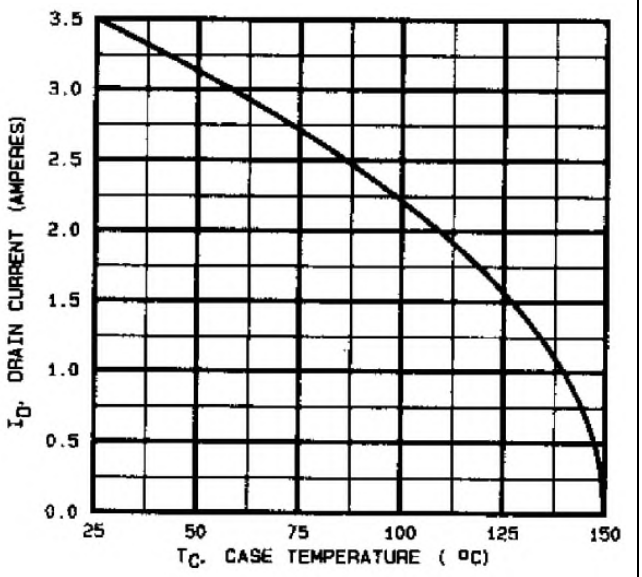


Figure 9 Maximum Drain Current Vs. Case Temperature

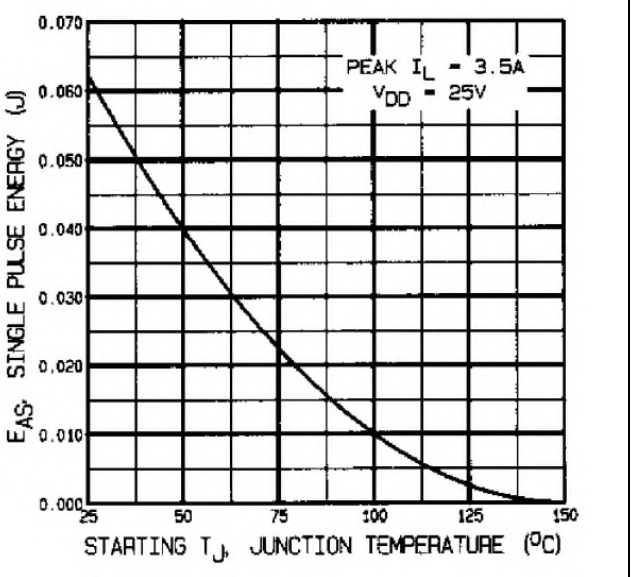


Figure 10 Maximum Avalanche Energy Vs. Junction Temperature

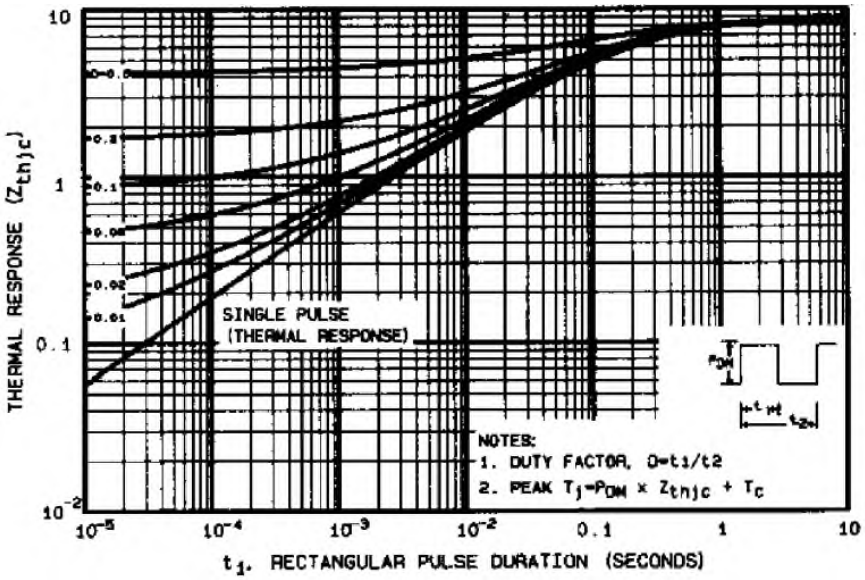


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits

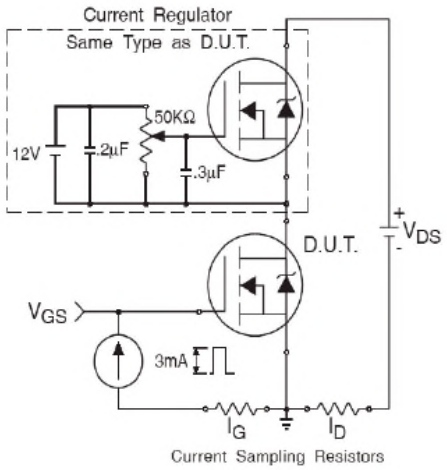


Figure 12 Gate Charge Test Circuit

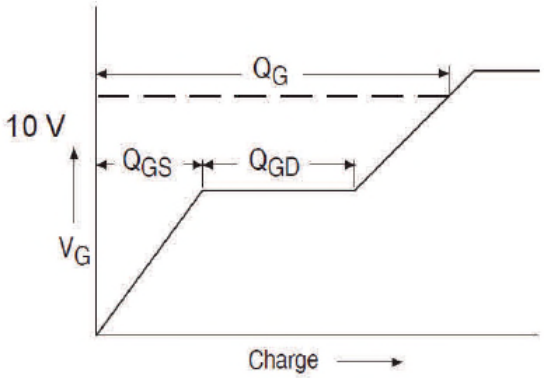


Figure 13 Gate Charge Waveform

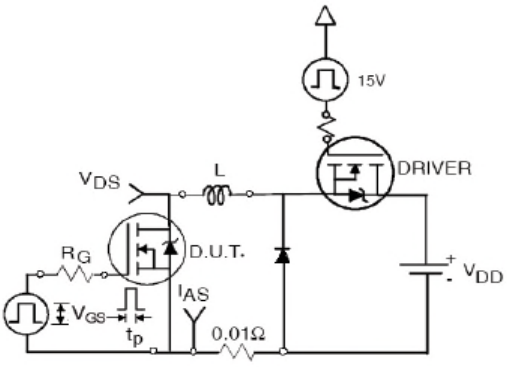


Figure 14 Unclamped Inductive Test Circuit

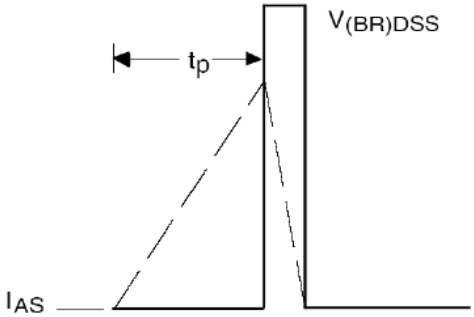


Figure 15 Unclamped Inductive Waveform

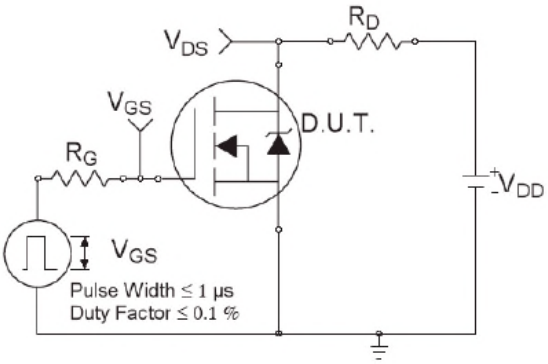


Figure 16 Switching Time Test Circuit

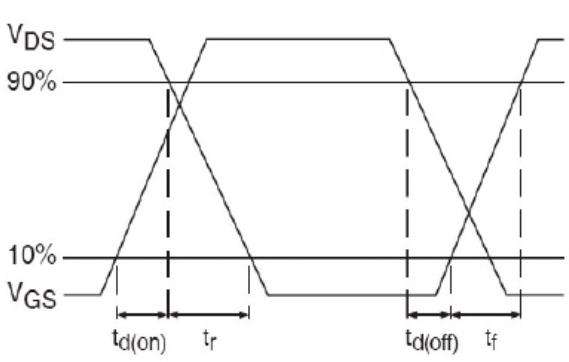
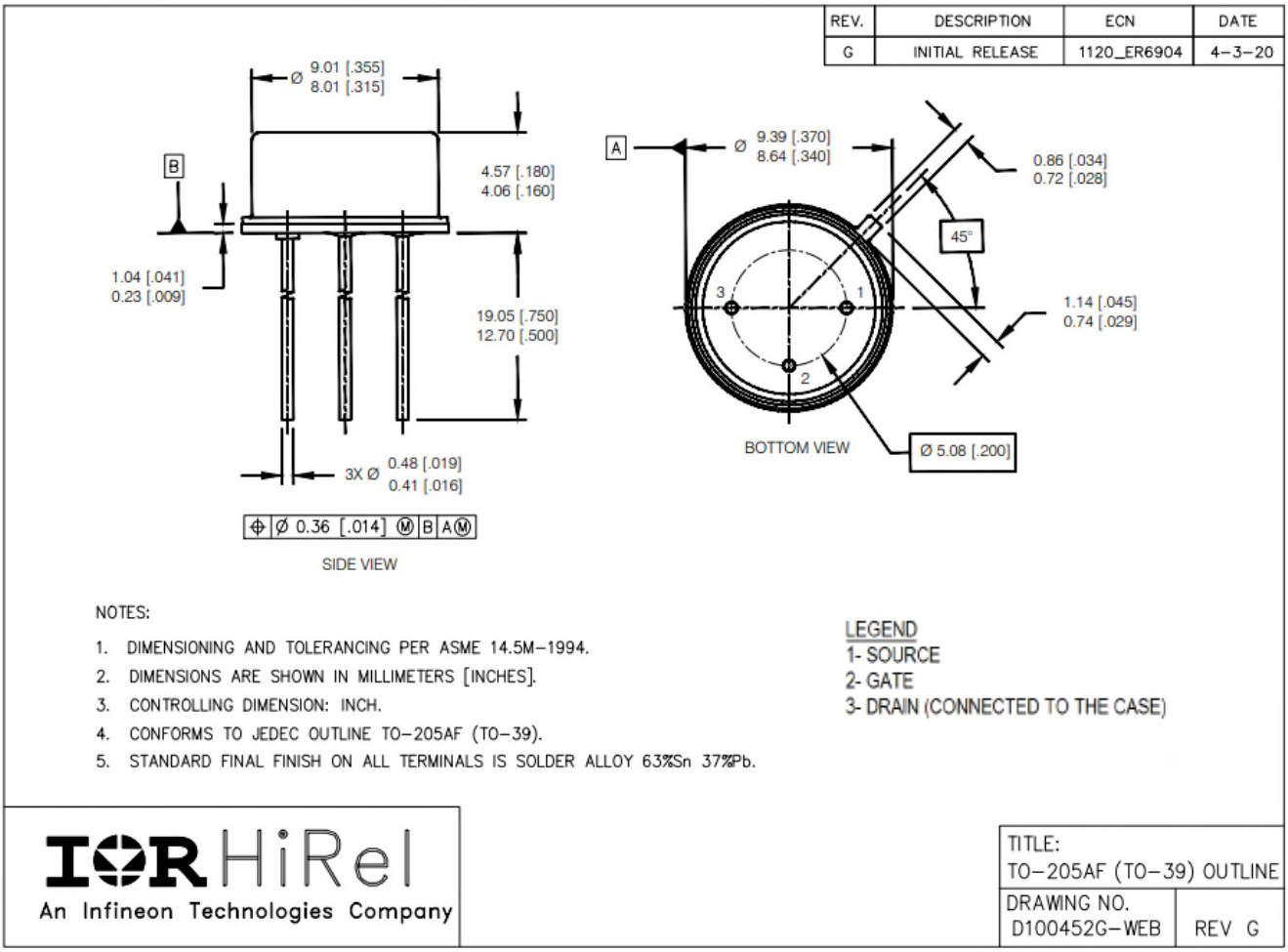


Figure 17 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: [TO-205AF / TO-39]



Revision history

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	01/26/2001	Datasheet (PD-90423C)
Rev D	12/04/2018	Updated based on ECN-1120_06255
Rev E	01/16/2023	Updated based on ECN-1120_09384

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