

IRFF9130 (JANS2N6849)

PD-90550H

Repetitive Avalanche and dv/dt Rated Power MOSFET Thru-Hole (TO-205AF / TO-39) -100V, -6.5A, P-channel

Features

- Repetitive avalanche ratings
- Dynamic dv/dt rating
- Hermetically sealed
- Simple drive requirements
- ESD rating: Class 1C per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

Description

HEXFET POWER MOSFET technology is the key to IR HiRel's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance. The HEXFET transistors also feature all of the well-established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters. They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Ordering Information

Table 1 Ordering options

0		
Part number	Package	Screening Level
IRFF9130	TO-205AF / TO-39	COTS
JANS2N6849	TO-205AF / TO-39	JANS
JANTX2N6849	TO-205AF / TO-39	JANTX
JANTXV2N6849	TO-205AF / TO-39	JANTXV



Product Summary

 $\mathbf{R}_{\text{DS(on),max}}$: 0.30 Ω

Q_{G, max}: 34.8nC

BV_{DSS}: -100V

lp:-6.5A



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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Cable 2 Absolute Maximum Ratings						
Symbol	Parameter	Value	Unit			
$I_{D1} @ V_{GS} = -10V, T_C = 25^{\circ}C$	Continuous Drain Current	-6.5	А			
$I_{D2} @ V_{GS} = -10V, T_C = 100^{\circ}C$	Continuous Drain Current	-4.1	А			
I _{DM} @ T _c = 25°С	Pulsed Drain Current ¹	-25	А			
$P_{D} @ T_{C} = 25^{\circ}C$	Maximum Power Dissipation	25	W			
	Linear Derating Factor	0.20	W/°C			
V _{GS}	Gate-to-Source Voltage	± 20	V			
E _{AS}	Single Pulse Avalanche Energy ²	92	mJ			
AR	Avalanche Current ¹	-6.5	Α			
E _{AR}	Repetitive Avalanche Energy ¹	2.5	mJ			
dv/dt	Peak Diode Reverse Recovery ³	-5.5	V/ns			
TJ Tstg	Operating Junction and Storage Temperature Range	-55 to +150	°C			
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				
	Weight	0.98 (Typical)	g			

 $^{^{\}rm 1}$ Repetitive Rating; Pulse width limited by maximum junction temperature.

 $^{^2}$ V_{DD} = -25V, starting T_J = 25°C, , Peak I_L = -6.5A, V_{GS} = -10V 3 I_{SD} \leq -6.5A, di/dt \leq -140A/µs, V_{DD} \leq -100 V, T_J \leq 150°C



Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	l	_	V	$V_{GS} = 0V, I_{D} = -1.0mA$	
$\Delta BV_{DSS} / \Delta T_{J}$	Breakdown Voltage Temp. Coefficient	_	-0.10	_	V/°C	Reference to 25°C, I_D = -1.0mA	
Р	Static Drain-to-Source On-State	—		0.30	Ω	V_{GS} =-10 V, I_{D2} = -4.1A ¹	
R _{DS(on)}	Resistance	—	-	0.32	\$2	V_{GS} = -10V, I_{D1} = -6.5A ¹	
V _{GS(th)}	Gate Threshold Voltage	-2.0		-4.0	V	$V_{DS} = V_{GS}$, $I_{D} = -250 \mu A$	
	Zara Cata Valtaga Drain Current	—	l	-25	۵	$V_{DS} = -80V, V_{GS} = 0V$	
DSS	Zero Gate Voltage Drain Current	—		-250	μΑ	$V_{DS} = -80V, V_{GS} = 0V, T_{J} = 125^{\circ}C$	
	Gate-to-Source Leakage Forward	—		-100	20	V _{GS} = -20V	
GSS	Gate-to-Source Leakage Reverse	—		100	nA	$V_{GS} = 20V$	
Q _G	Total Gate Charge	14.7		34.8		I _{D1} = -6.5A	
Q _{GS}	Gate-to-Source Charge	1.0		6.8	nC	$V_{DS} = -50V$ $V_{GS} = -10V$	
Q _{GD}	Gate-to-Drain ('Miller') Charge	2.0		23.1			
td(on)	Turn-On Delay Time	—		60		I _{D1} = -6.5A **	
tr	Rise Time	—		140		$V_{DD} = -40V$ R _G = 7.5Ω	
t _{d(off)}	Turn-Off Delay Time	—		140	ns		
t _f	Fall Time	—		140		V _{GS} = -10V	
L _s +L _D	Total Inductance	_	7.0	_	nH	Measured from Drain lead (6mm / 0.25 in from packag to Source lead (6mm/ 0.25 in from package) with Sourc wire internally bonded from Source pin to Drain pin	
C _{iss}	Input Capacitance	_	800	_		$V_{GS} = 0V$	
C _{oss}	Output Capacitance	_	350	_	pF	$V_{DS} = -25V$	
C _{rss}	Reverse Transfer Capacitance	_	125	_		<i>f</i> = 1.0MHz	

** Switching speed maximum limits are based on manufacturing test equipment and capability.

 $^{^1}$ Pulse width \leq 300 μs ; Duty Cycle \leq 2%



Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics

Table 4Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
ls	Continuous Source Current (Body Diode)		_	-6.5	А	
I _{SM}	Pulsed Source Current (Body Diode) ¹	-	_	-25	А	
V _{SD}	Diode Forward Voltage	-	_	-4.3	V	$T_J = 25^{\circ}C$, $I_S = -6.5A$, $V_{GS} = 0V^{-2}$
t _{rr}	Reverse Recovery Time	-	_	250	ns	$T_J = 25^{\circ}C, I_F = -6.5A, V_{DD} \le -50V$
Q _{rr} Reverse Recovery Charge			2.0	_	μC	di/dt = -100A/µs
t _{on}	Forward Turn-On Time		sic turn-	on time i	is negligi	ible (turn-on is dominated by $L_{S}+L_{D}$)

2.3 Thermal Characteristics

Table 5Thermal Resistance

Symbol	Parameter	Min.	Тур.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	_	-	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	_	_	175	C/W

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width \leq 300 µs; Duty Cycle \leq 2%



Electrical Characteristics Curves

3 Electrical Characteristics Curves

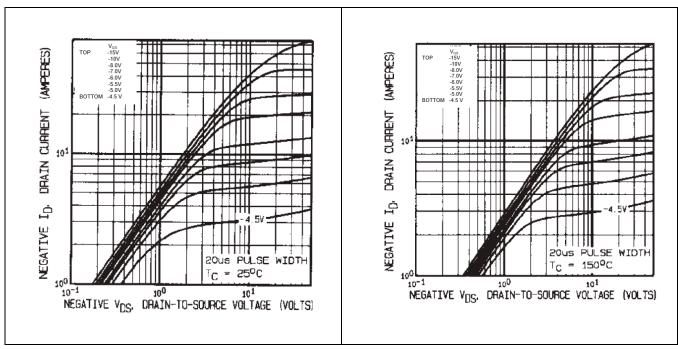
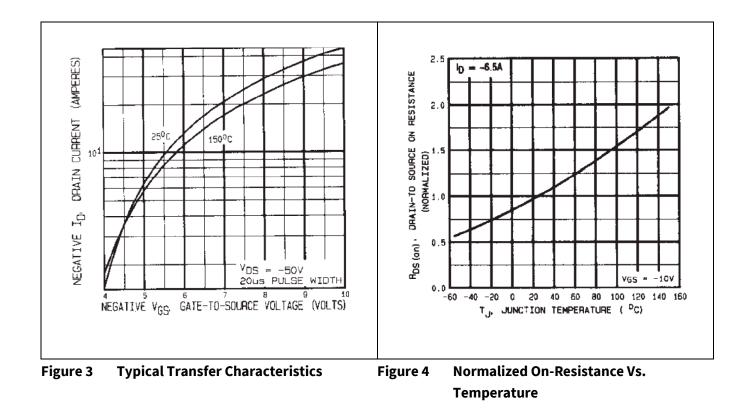


Figure 1 Typical Output Characteristics

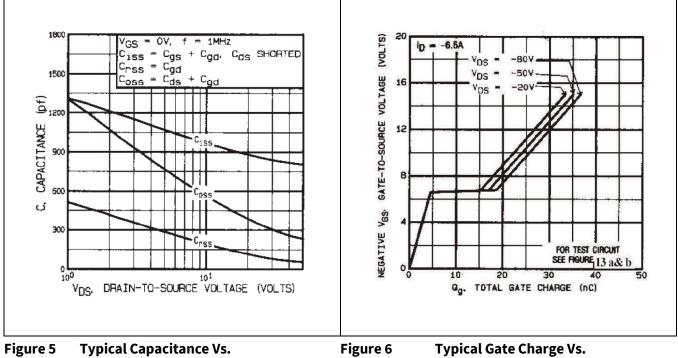
Figure 2

2 Typical Output Characteristics





Electrical Characteristics Curves



Drain-to-Source Voltage

Gate-to-Source Voltage

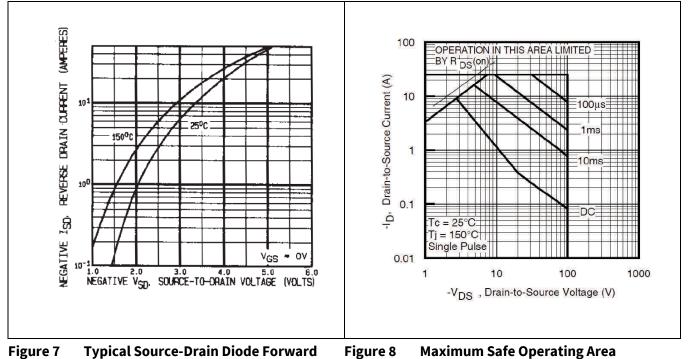
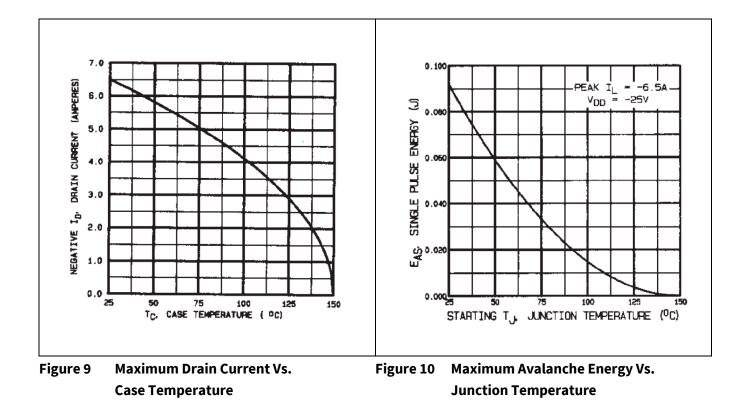


Figure 8 **Maximum Safe Operating Area**



Electrical Characteristics Curves



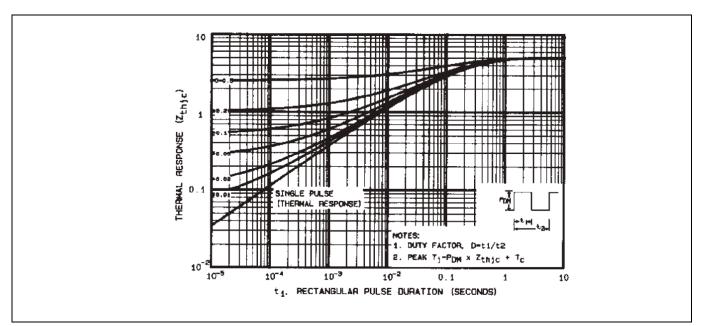


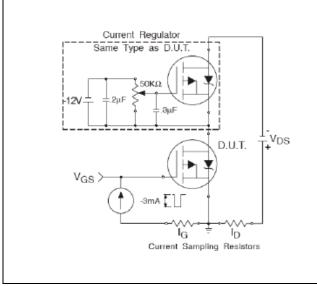
Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

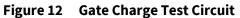


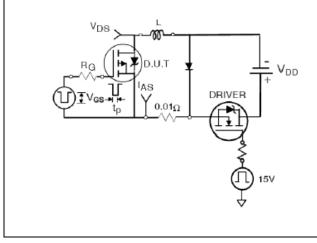
Test Circuits



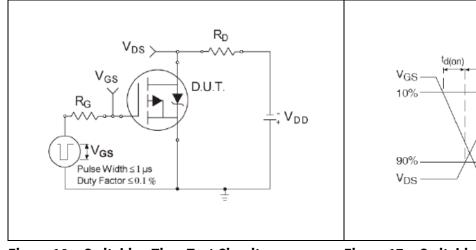
Test Circuits



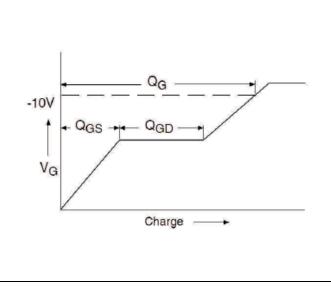














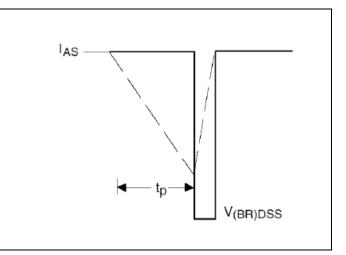


Figure 15 Unclamped Inductive Waveform

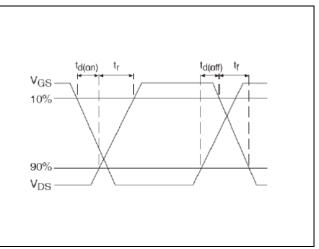


Figure 17 Switching Time Waveforms



Package Outline

5 Package Outline

DESCRIPTION REV. DATE ECN G INITIAL RELEASE 1120_ER6904 4-3-20 9.01 [.355] Ø 8.01 [.315] 9.39 [.370] А Ø 8.64 [.340] 0.86 [.034] 0.72 [.028] В 4.57 [.180] 4.06 [.160] 45° 1.04 [.041] 0.23 [.009] 1.14 [.045] 19.05 [.750] 0.74 [.029] 12.70 [.500] BOTTOM VIEW Ø 5.08 [.200] 0.48 [.019] зх Ø 0.41 [.016] ∲Ø0.36 [.014] @ B A @ SIDE VIEW NOTES: LEGEND 1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994. 1- SOURCE 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]. 2- GATE 3- DRAIN (CONNECTED TO THE CASE) 3. CONTROLLING DIMENSION: INCH. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39). 4. 5. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb. TITLE: 2K TO-205AF (TO-39) OUTLINE DRAWING NO. An Infineon Technologies Company D100452G-WEB REV G

Note: For the most updated package outline, please see the website: TO-205AF / TO-39



Revision history

Document version	Date of release	Description of changes
	01/26/2001	Datasheet (PD-90550C)
Rev D	04/20/2001	Added switch time test condition V_{GS} =-10V
Rev E	07/28/2015	Updated based on ECN-1120_03204
Rev F	11/20/2018	Updated based on ECN-1120_06256
Rev G	02/16/2019	Updated based on ECN-1120_06822
Rev H	12/06/2024	Updated based on ECN-1120_10116

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Document reference

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