Lightning surge discharge design for SMPS applications

Line filter design guidelines with focus on CoolMOS™ P7

Authors: Lin Lawrence, Eslam Alfawy

Scope and purpose

Surge is the most common source of overstress. Overstress in the form of overvoltage and overcurrent that can occur in consumer equipment such as LED drivers, TV SMPS, etc. Customers generally perform surge tests on their products before going into volume production. This is done to ensure that the equipment is not interrupted during operation or damaged by possible surge events. This application note introduces the concept of lightning surge and discusses solutions for lightning surge discharge. Some case studies are used to show different applications and system simulations are demonstrated as well.

Intended audience

This application note is intended to advise designers of SMPS for consumer equipments on how to properly design their systems to avoid the disruptive influence and the damaging effects caused by surge overstress and to optimize the susceptibility of the lightning surge.

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1 Introduction

Lightning surge discharge is the most common source of overstress. Externally generated surges are due to induced lightning, grid switching or from adjacent buildings. Surges related to lightning strikes, in particular, can produce surge energies of hundreds of joules. An unexpected and transient voltage or current spike is caused by nearby electronics or the environment. Internal surges are due to switching transients caused by switching on/off motors, transformers. Surges in distribution systems are generally affected by system configuration and connected loads. Voltage or current surges arising from lightning strikes are experienced in SMPS. These surges can cause damage or malfunction of electronic equipment connected to the systems. In general, surges are complicated and can have many different causes. A critical part of system design is being able to prevent these failures by safely shunting the transient spikes to ground and ensuring that they do not cause any damage.

1.1 What happens during lightning surge?

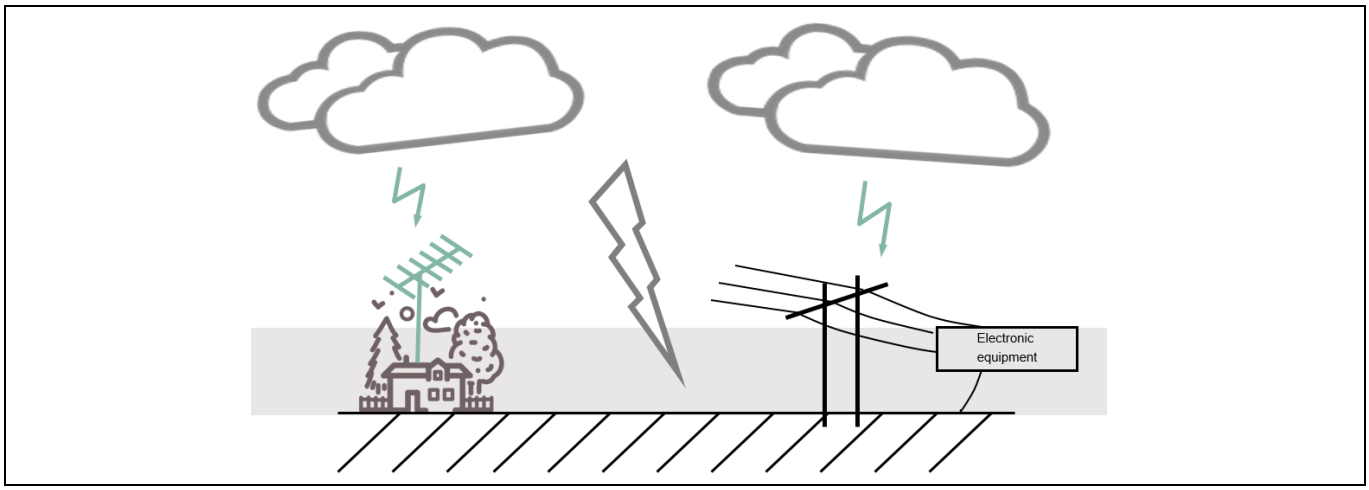


Figure 1 Lightning surge discharge

Lightning strikes are electrostatic discharges, which usually travel from cloud to cloud or cloud to ground, with magnitudes of millions of volts. Indirect lightning strikes, even those that occur several miles away, can induce magnetic fields that generate surges of thousands of volts through current-carrying copper wires, such as the overhead and underground cables that power streetlights. These indirect strikes, which produce levels of energy with magnitudes greater than 1000 A^2s, can be characterized by specific waveforms. Sudden rises in voltage or current to a connected load mean that standard household equipment can be damaged by surges of 500 V or more. These can be caused by incidents involving electrical lines and power equipment failures.

1.2 Lightning surge test

The lightning surge test is modeled by IEC 61000-4-5. The aim of the lightning surge immunity test is to provide a model to simulate the surges and then check if the equipment can survive. The test can be divided into differential mode (DM) and common mode (CM) transient.

1.2.1 Understanding differential mode and common mode

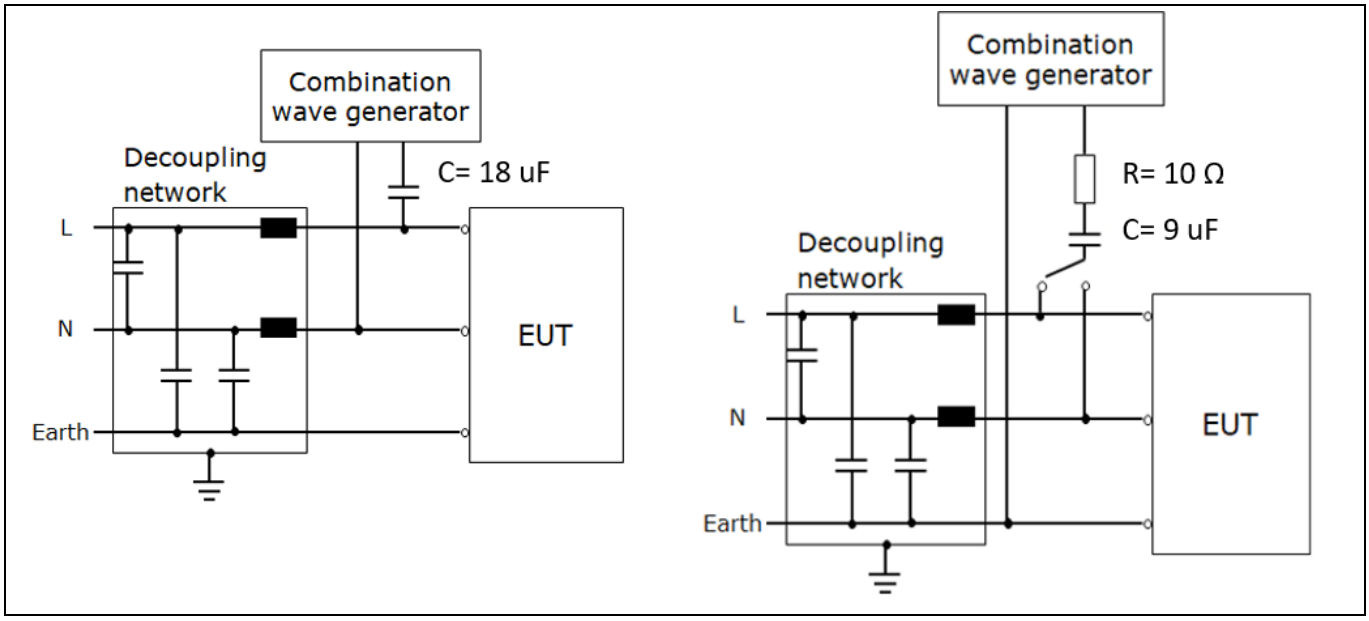


Figure 2 Combination wave generator for DM (left) and CM (right) surge immunity test

Differential mode (DM) is the transient with major power system switching disturbances, minor switching activity in the power distribution system, resonating circuits, various system faults, etc.; i.e. line to neutral.

High voltage (HV) or current transients between the line and neutral terminals could damage components in the power supply unit. The CM transient is a direct lightning strike to an external circuit, an indirect lightning strike to a nearby object, a lightning earth current coupling to common earth, etc.; i.e. earth-to-line or line-to-earth. HV or current transients between the line and earth or neutral and earth terminals could damage safety insulation in the power supply unit.

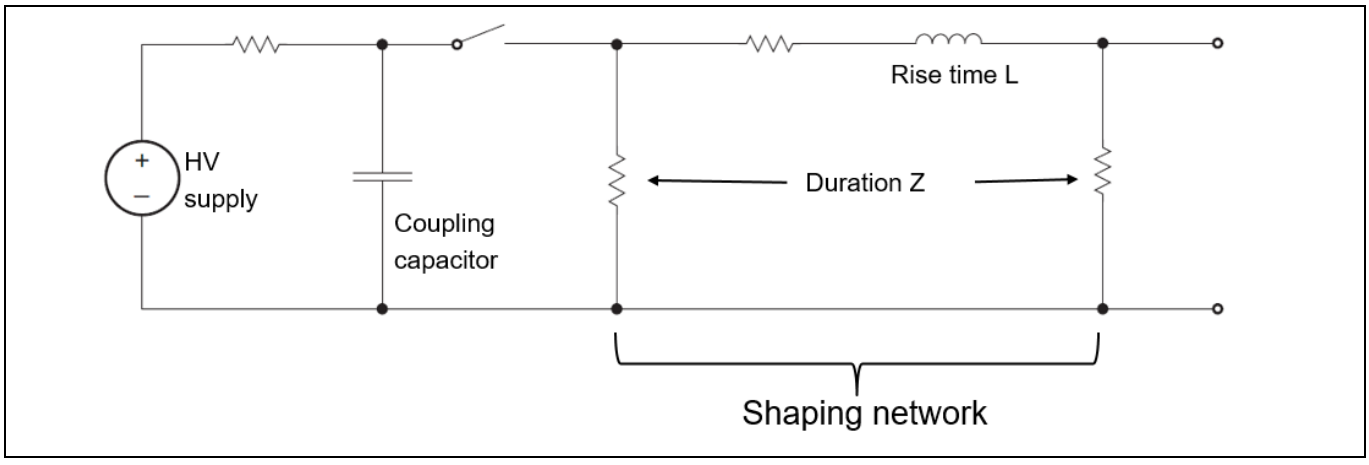


Figure 3 Surge generator source

A simplified surge generator as shown in **Figure 3** has a power supply that charges the coupling capacitor, through a resistance. Upon the closing of the switch, the coupling capacitor discharges through a pulse shaping network. The inductor L determines the rise time of the pulse, and the pulse duration depends on the impedance Z. The values of these components are tuned to yield the compliance waveforms in short-circuit and open-circuit conditions according to IEC 61000-4-5.

1.2.2 Voltage and current waveforms

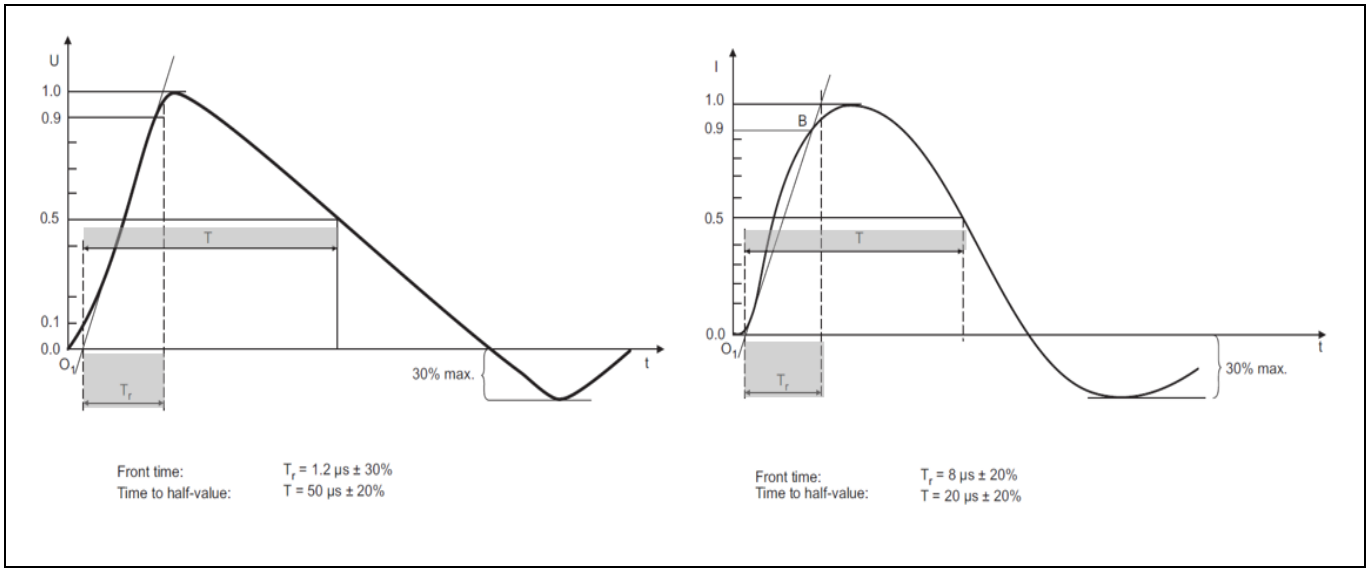


Figure 4 Open-circuit voltage (left) and short-circuit current (right) waveforms

Figure 4(a) shows the open-circuit voltage waveform shape, which has a front time of 1.2 µs and a time to half value of 50 µs. The short-circuit current waveform of the same generator has an 8 µs front time and a 20 µs time to half value in **Figure 4(b)**.

1.2.3 Test level and environment

The surge tests comply with the IEC 61000-4-5 standard. Depending on what environment a system is designed for, IEC 61000-4-5 specifies several levels of tests in association with an environment. **Table 1** summarizes the surge voltages of different test levels and the test environments. From level 1 and up, the applications require protection devices to minimize the surge energy seen by the internal circuitry.

Table 1 Surge voltages of different test levels and the test environments

Class	Test environment	Voltage level
0	Well-protected environment, often in a special room	25 V
1	Partially protected environment	500 V
2	Electrical environment where the cables are well separated, even at short runs	1 kV
3	Electrical environment where power and signal cables run in parallel	2 kV
4	Electrical environment where the interconnections include outdoor cables along with the power cable, and cables are used for both electronics and electric circuits	4 kV
x	Special conditions specified in the product specification	Custom

The level of surge voltage, together with the impedance from the surge strike, determines how much surge current the protection device takes. Different kinds of equipment setups entail different impedances used in the tests. A 2 Ω impedance models the source impedance of a low voltage power supply and is the inherent source impedance of the combinational waveform generator. It represents the case where the surge is coupled onto the power AC or DC mains in a differential way. This impedance gives the highest level of surge current for a certain surge voltage level. A 12 Ω impedance models the impedance of the power source and the ground

network. It is used when the surge happens between the mains and the ground. A 42 Ω impedance represents the impedance between all the other lines and ground. Data lines are one example where this impedance level is used.

Table 2 Level of surge voltage, together with impedance from surge strike

	Class 0 25 V	Class 1 500 V	Class 2 1 kV	Class 3 2 kV	Class 4 4 kV
R_{equ} = 42 Ω	0.6 A	12 A	24 A	48 A	96 A
R_{equ} = 12 Ω	2.1 A	42 A	84 A	167 A	334 A
R_{equ} = 2 Ω	12.5 A	250 A	500 A	1000 A	2000 A

1.2.4 Test procedures of IEC61000-4-5

The test procedures of IEC 61000-4-5 are shown in **Table 3**. For each polarity, the test requires the pulse to be applied for various angles (0 degrees, 90 degrees, 180 degrees, etc.) of the different power input wave format angles, and the number of strikes is five at each voltage step. The maximum repetition rate is one minute. The equipment under test (EUT) must pass the lower level before proceeding to the higher level. According to the requirement, the EUT must be undamaged, with automatic or manual recovery of function, and continue to operate properly after the surge is applied.

Table 3 Test procedures of IEC 61000-4-5

Ambient temperature	15°C ~ 35°C
Relative humidity	10 ~ 75
Atmospheric pressure	86 kPa ~ 106 kPa
Polarity	Positive, negative
Phase shift	0°, 90°, 180°, 270°
Number of tests	At least five times
Repetition rate	Maxiumum one minute

1.2.5 Test setup

The test setup of lightning surge discharge is shown in **Figure 5**. AC input power is isolated with an isolation transformer for protection purposes. The lightning surge tester generates the voltage or current surge wave to the power line of the EUT. The EUT is placed on a wooden table with insulation.

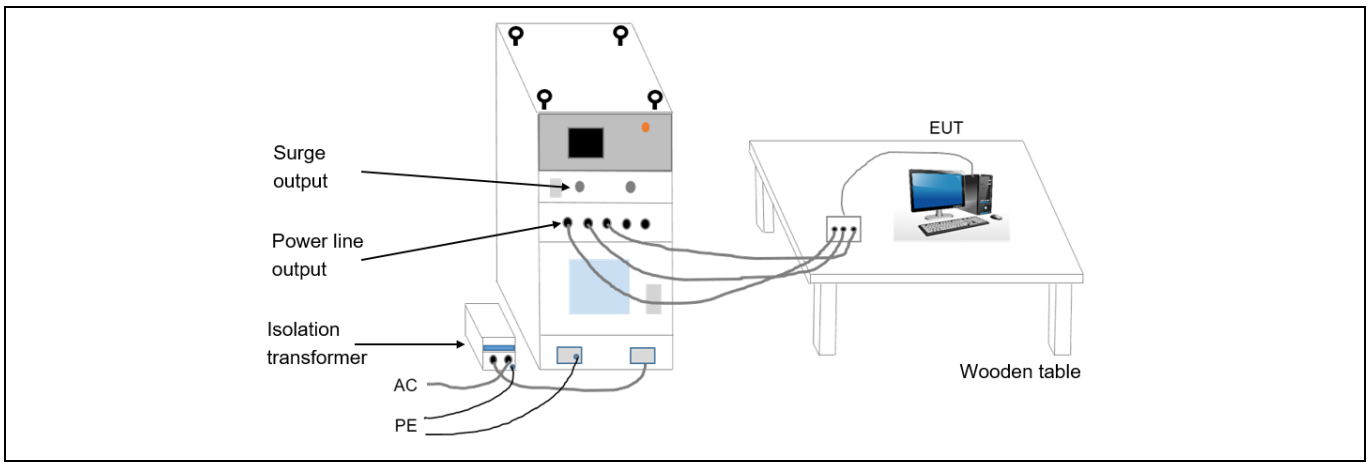


Figure 5 Test setup

Figure 6 is an example of lightning surge test setup. An LCD TV with external SMPS adapter is used as the EUT. The lightning surge generator is an ideal voltage source with the specified waveform, which is connected to its output ports with the known fixed resistance. It as well as the SMPS adapter gets the AC power from the isolation transformer. For the differential surge test, the surge voltage is applied across the AC lines of the SMPS adapter, whereas for the CM surge test, it is applied across one of the AC lines and the equipment's ground connection at the tuner's input socket of the TV set.

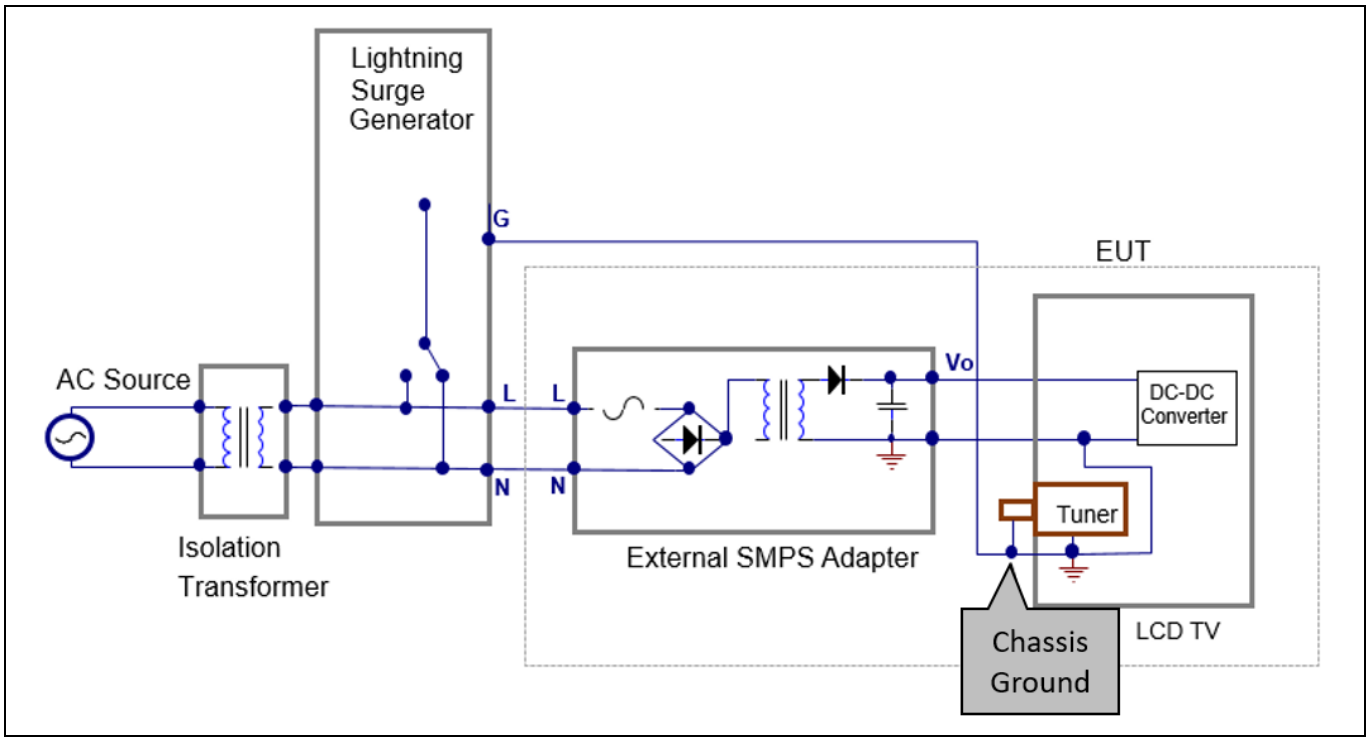


Figure 6 Example of LCD TV Power test setup

1.3 Effects of PCB layout on lightning surge

Random selection of PCB layout and placement of the surge protection devices in the circuitry results in a large overshoot with oscillatory response. At high voltage and high frequency, the PCB tracks behave as transmission lines and become resonant depending on the capacitance between the lines. The length and the width of the tracks have an effect on track inductance and can cause destructive overshoots. The PCB track with the capacitance of varistors or filter capacitor can be represented by an equivalent circuit, as shown in Figure 7. With the track resistance in the circuit, the circuit behaves as an RLC circuit. The resonance caused by the circuit results in a damped oscillation output.

The oscillations cause an overshoot, which can be dangerous to the equipment connected or easily exceed the safety limit. The oscillation frequency is given as:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Where L consists of track inductance and component lead inductance. The inductance of PCB track is given by:

$$L = 0.0002l\left[\ln\left(\frac{2l}{w+t}\right) + 0.2235\left(\frac{w+t}{l}\right) + 0.5\right] uH$$

Where l = length of PCB track, w = width of PCB track, t = thickness of PCB track.The value of C depends on the tracks, the suppression device capacitance and the filter capacitor placed in the circuit.

Introduction

The placement of the filter capacitor and varistor is very important as it will cause a very large capacitance and hence the overshoot will be very large. The overshoot can be reduced by arranging them with proper spacing along the track. The damped oscillations cause a voltage overshoot, which can be given by:

Maximum voltage overshoot: $$\Phi_{max} = e^{-\frac{\pi\xi}{1-\xi^2}}$$

Where ξ is the damping ratio. $$\xi = \frac{R}{2}\left(\sqrt{\frac{C}{L}}\right)$$

The value of ξ decides the behavior of the circuit. If ξ is less than one, then the response will be underdamped. If ξ is more than one, the response will be overdamped. If ξis equal to one, the response will be critically damped. DC resistance of the track can be given by:

$$R = \frac{\rho l}{wt}$$

Where ρ is the resistivity of the copper at room temperature and *t* stands for the thickness of the copper.

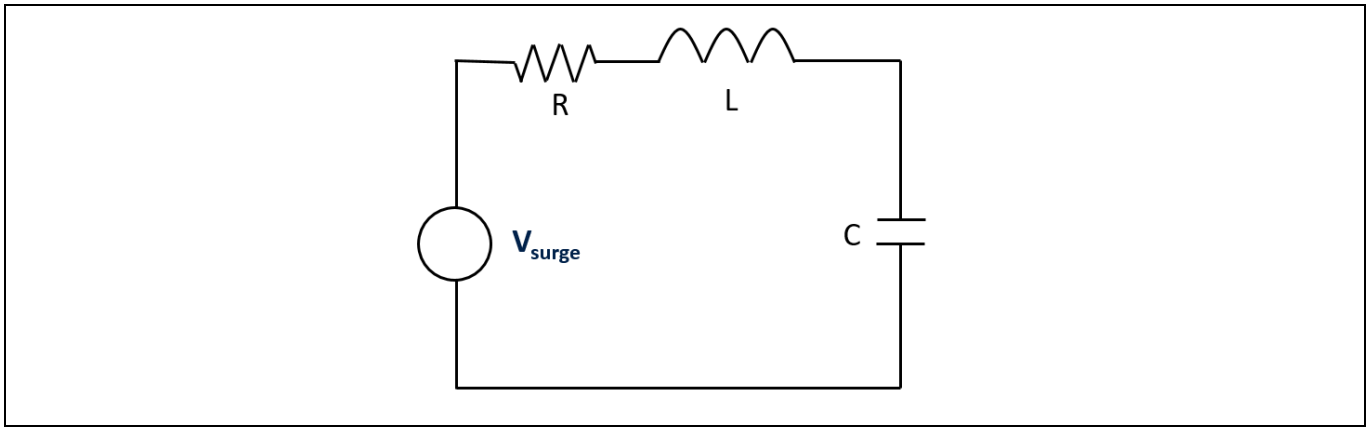


Figure 7 Equivalent circuit for PCB track with filter and metal oxide varistor (MOV) capacitance

1.4 The reason why combination wave at 90° is the worst case

The surge test requires the pulse to be applied for various angles (0°, 90°, 180°etc.) of the power AC input waveform at different voltage steps. Now, looking at the amount of avalanche energy that a MOSFET sees in an off-the-shelf power supply, we can see that the worst-case conditions are at 90° surge pulse with a positive polarity and 270° with a negative polarity applied on the AC input. This is because the system has the highest bulk capacitance voltage at this point, and then the surge pulse adds to this voltage.

Table 4 MOSFET energy seen during a surge pulse

Surge applied	Polarity	0°	90°	180°	270°
L-N	Positive	30 mJ	**211 mJ**	41 mJ	3 mJ
L-N	Negative	73 mJ	3 mJ	59 mJ	**211 mJ**
L-E	Positive	10 mJ	50 mJ	13 mJ	3 mJ
L-E	Negative	14 mJ	3 mJ	17 mJ	55 mJ
N-E	Positive	30 mJ	12 mJ	30 mJ	8 mJ
N-E	Negative	30 mJ	3 mJ	27 mJ	3 mJ

1.5 Difficulties for high power factor flyback topology

To understand the possible avalanche modes of a flyback converter we need to first look at what determines the drain-to-source voltage of a MOSFET in a flyback converter and then what factors can contribute to pushing this drain-to-source voltage over the limit.

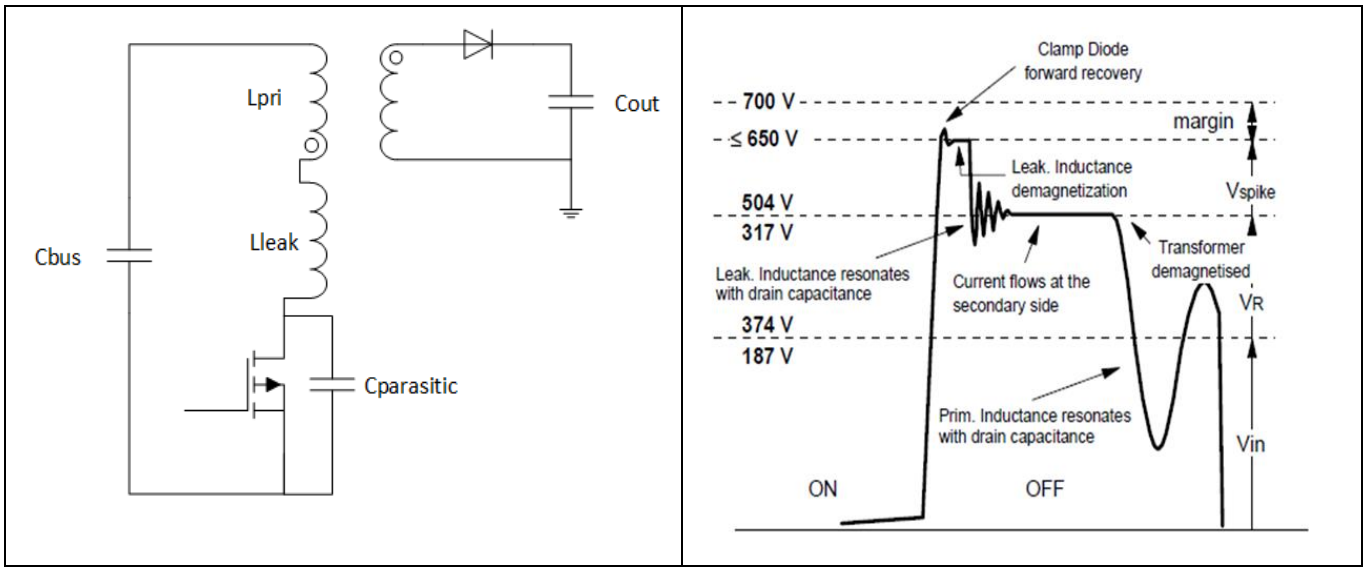


Figure 8 Basic flyback schematic (left); primary MOSFET drain-to-source waveform (right)

The overall drain-to-source voltage (**Figure 8**) of the primary MOSET with a flyback using an RCD snubber can be described with the following equation:

$$V_{ds} = V_{Bus} + V_{Reflected} + V_{Ringing}$$

$$Vds = V_{AC}\sqrt{2} + \frac{N_P}{N_S}\,(V_{out} + V_{diode}) + \frac{1}{2}\left(\sqrt{{V_{Reflected}}^2 + 2\frac{L_{leak}I_{pri}^2 R_{snub}}{T_S}} - V_{Reflected}\right)$$

This can be broken into three main regions: the input bus voltage, the reflected voltage, and the parasitic ringing. If the total sum of these three voltages exceeds V_{DS} then avalanche will occur.

The input bus voltage is just the rectified input AC waveform. This will vary over the AC power cycle, but the absolute maximum that this will achieve during typical operation is:

$$V_{Bus} = V_{AC} \,.\sqrt{2}$$

This is affected by the input AC voltage requirement and, as we will discuss later, the surge requirement, line filter design and surge protection circuitries.

The reflected voltage occurs when the primary MOSFET turns off. The inductor continues to flow current in the same direction into $C_{parasitic}$ until the voltage pumps up above V_{BUS}. It continues to do so until the secondary diode conducts and charges C_{out}. When the secondary diode is conducting the primary inductor voltage is clamped at the output voltage + the diode forward drop reflected by the turns ratio of the transformer:

$$V_{Reflected} = \frac{N_P}{N_S}\,(V_{out} + V_{diode})$$

The last part of the equation is the ringing calculation, which is going to be dependent on the snubber design of the flyback converter. The equation presented is for an RCD snubber circuit since this is the most commonly

used snubber in offline flyback converters. As can be seen, this equation is reliant on the leakage inductance of the transformer, which will be explained further.

$$V_{Ringing} = \frac{1}{2}\left(\sqrt{V_{Reflected}{}^2 + 2\frac{L_{leak} \cdot I_{pri}^2 \cdot R_{snub}}{T_S}} - V_{Reflected}\right)$$

When avalanche occurs the amount of energy that is transferred into the MOSFET depends on which elements have exceeded the V_{DS} maximum rating. Initially, when just the ringing voltage is exceeding the drain-to-source voltage, the absolute maximum amount of energy that can be transferred into the FET is going to be the energy stored in the leakage inductance. This is shown in line two of **Table 5**.

If the bus voltage rises high enough to push the reflected voltage above the rated avalanche voltage, then the amount of energy that is stored is going to increase, as shown in line three of **Table 5**. This will typically be on the order of 100 times the energy that is stored in the leakage inductance.

As soon as the bus voltage increases beyond the rated V_{DS} of the FET, all of the line energy will transfer into the FET, only to be limited by the fuse. This scenario would only happen if a Metal Oxide Varistor - MOV with a too-high voltage rating is selected.

Table 5 Avalanche energy

Condition	Avalanche energy
$V_{DS} > V_{Bus} + V_{Reflected} + V_{Ringing}$	No avalanche
$V_{DS} < V_{Bus} + V_{Reflected} + V_{Ringing}$	$E_{Avalanche} = \frac{1}{2} L_{leakage} I_{pk}^2$ every switching cycle
$V_{DS} < V_{Bus} + V_{Reflected}$	$E_{Avalanche} = \frac{1}{2} I_{pk}^2 (L_{Leakage} + L_{Primary})$ every switching cycle
$V_{DS} < V_{Bus}$	$E_{Avalanche} = V_{DS} I_{fuse} T_{Fuse\ blow} + \frac{1}{2} I_{pk}^2 (L_{Leakage} + L_{Primary})$ until the fuse blows

How high the bus voltage can pump up is determined by the size of the capacitor – **Figure 9** shows the increase of the voltage at the bus capacitor during a surge event.

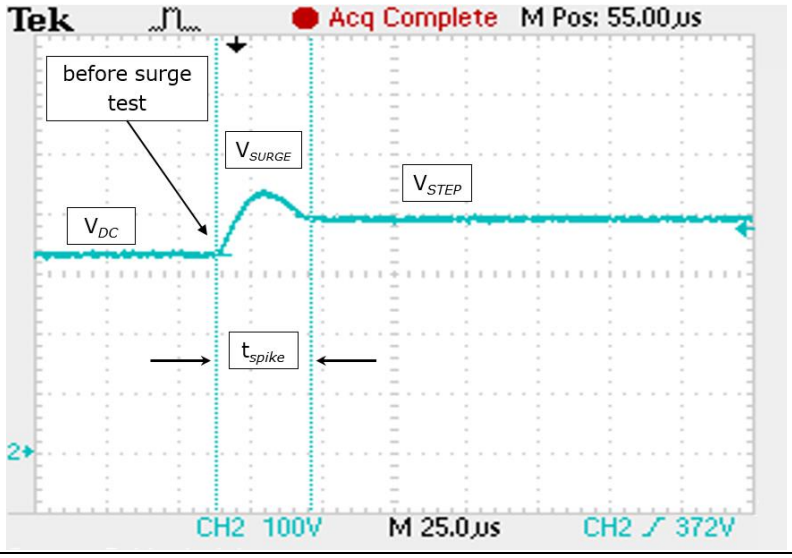


Figure 9 C_{BUS} voltage rise during a surge event

Designing power supplies for surge becomes more difficult as the bus capacitance used by the power supply gets smaller. This is especially an issue in low power supplies as well as lighting supplies where the high power factor flyback topology is used. The principle remains the same regardless of the power rating or the application. The graph below shows the bus capacitance's influence on the surge requirements and where the line filter design is typically critical.

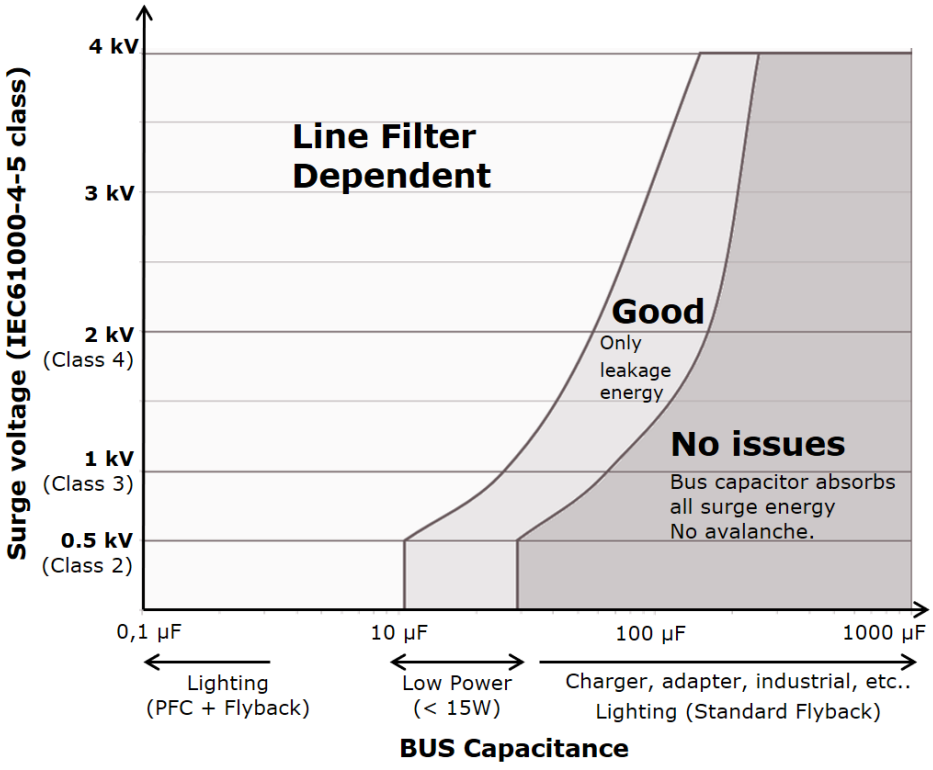


Figure 10 Bus voltage vs. Surge voltage

Note: Based on simulations with 460 V MOV, 10µH inductance, and bus capacitor. Assuming 15 percent drain source margin from a 600 V MOSFET. For the leakage energy region it is assumed that there is 100 V of ringing

Introduction

The bus capacitor size plays a key role in how much surge energy the power supply can handle. Here, we compare the surge handling capability of a power supply vs. the bus capacitor size.

Considering the surge energy directly transfers into the bus capacitor with only a 460 V MOV with no additional filter components, we can see the regions where the avalanche capability of the MOSFET does not need to be considered. With a large bus capacitor, the energy from the surge event can be completely absorbed by the capacitor with no avalanche occurring.

As the surge event becomes larger, the capacitor required to absorb this energy also becomes larger, taking 1 kV as a reference point, which is the common required IEC surge standard level – but practically, many customers run tests beyond this minimum requirement.

From around 70 µF, most power supplies should not have trouble avalanching the MOSFET during a surge event due to the large bus capacitor.

From around 25 µF, the MOSFET can go to avalanche, but only with leakage energy stored in the transformer. In this condition the avalanche energy that is stored in the leakage inductor is several orders of magnitude lower than the avalanche rating of a MOSFET and thus would not cause any issues.

With bus capacitors lower than 25 µF, the overall system needs to be considered in order to judge whether an issue with surge ratings may arise – this is where the avalanche rating of the device could become an issue, depending on the system design.

Now comparing applications vs. bus capacitor, as shown on the bottom of the graph, it can be noticed that single stage PFC + flyback converters which are used in LED lighting for low cost power factor correction and low power chargers, are the key areas where we see very small bus capacitors and the surge capability of the MOSFET can become critical.

In LED lighting applications with a separate PFC stage as well as in all other applications, the line filter design and avalanche rating of the MOSFET do not become an issue for customers.

1.6 Surge effect on MOSFET

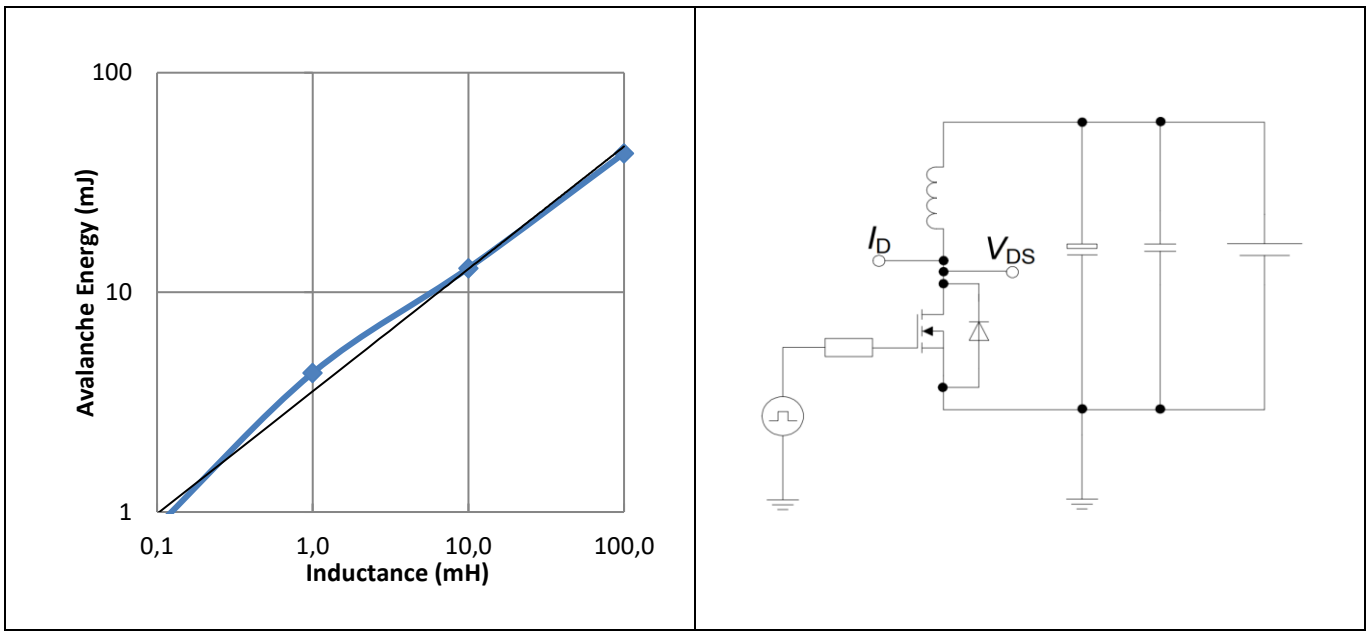


Figure 11 Avalanche energy vs. test inductance, data for IPx80R900P7 [2]

Introduction

The latest generation of Infineon's **CoolMOS™ P7** technology offers undisputed best-in-class $R_{DS(on)}$ in voltage classes ranging from 600 V up to 950 V. The technology leadership of Infineon enables not only new and smaller packages (such as **ThinPAK 5x6** or **SOT-223**), but also CoolMOS™ products with much smaller $R_{DS(on)}$ values in existing packages.

Similar power semiconductors which were produced merely a decade ago needed at least a threefold of the area to achieve the same performance. In other words, the previous generations of power MOSFETs suffered from at least three times more $R_{DS(on)}$ than modern **CoolMOS™ P7** chips (at the same chip area).

However, the advance of superjunction MOSFET technology towards ultrafast switching comes with certain disadvantages. As much as modern high-voltage superjunction MOSFETs are appreciated for switching mode operation, they offer some limitations undesirable for some applications.

Now if we look at the CoolMOS™ P7 datasheet compared to previous Infineon CoolMOS™ generations and to competitor devices, it is clear that the avalanche capability of the P7 devices are lower, as competitors use different peak currents and test inductances, preventing direct comparison. This can be seen if one try to translate the avalanche energy to the equivalent compatitor datasheet conditions. As the test inductance gets larger, the energy is transferred over a longer period of time. This gives the MOSFET time to dissipate the heat and avoid thermal destruction.

$$t_{AV} = \frac{I_{AV} \cdot L_{AV}}{V_{DSBRR}}$$

$$E_{AS} = 0.5.L.I_{AS}^2 \left(\frac{V_{DSBRR}}{V_{DSBRR}-V_{DD}}\right)$$

To get the actual in-application avalanche capability E_{AS}, converting the IPx80R900P7 (900 mΩ) avalanche characterization to the equivalent test inductance as competitors, shows IPx80R900P7 is not as far off in rating as is shown on the datasheet. This puts the IPx80R900P7 E_{AS} closer to 60 mJ than the rated value of 13 mJ [2].

2 Solutions for lightning surge

2.1 Solution for differential mode surge

Differential mode (DM) surge is applied on line-to-neutral as shown in **Figure 12(a)**. The surge energy of DM can be blocked by the thermistor or absorbed by the varistor and bulk capacitor. The resistance of the NTC thermistor decreases with the increase in its temperature. The thermistor can limit inrush current and also help with limiting surge current. The varistor has symmetrical bidirectional characteristics – it operates in both directions. When not conducting, the I-V curve shows a linear relationship as the current flowing through the varistor remains constant and low at only a few µA of leakage current. This is due to its high resistance acting as an open circuit and remains constant until the voltage across the varistor reaches a particular rated voltage. When the transient voltage across the varistor is equal to or greater than the rated value, the resistance of the device suddenly becomes very low, turning the varistor into a conductor due to the avalanche effect of its semiconductor material. In other words, the varistor self-regulates the transient voltage across it by allowing more current to flow through it.

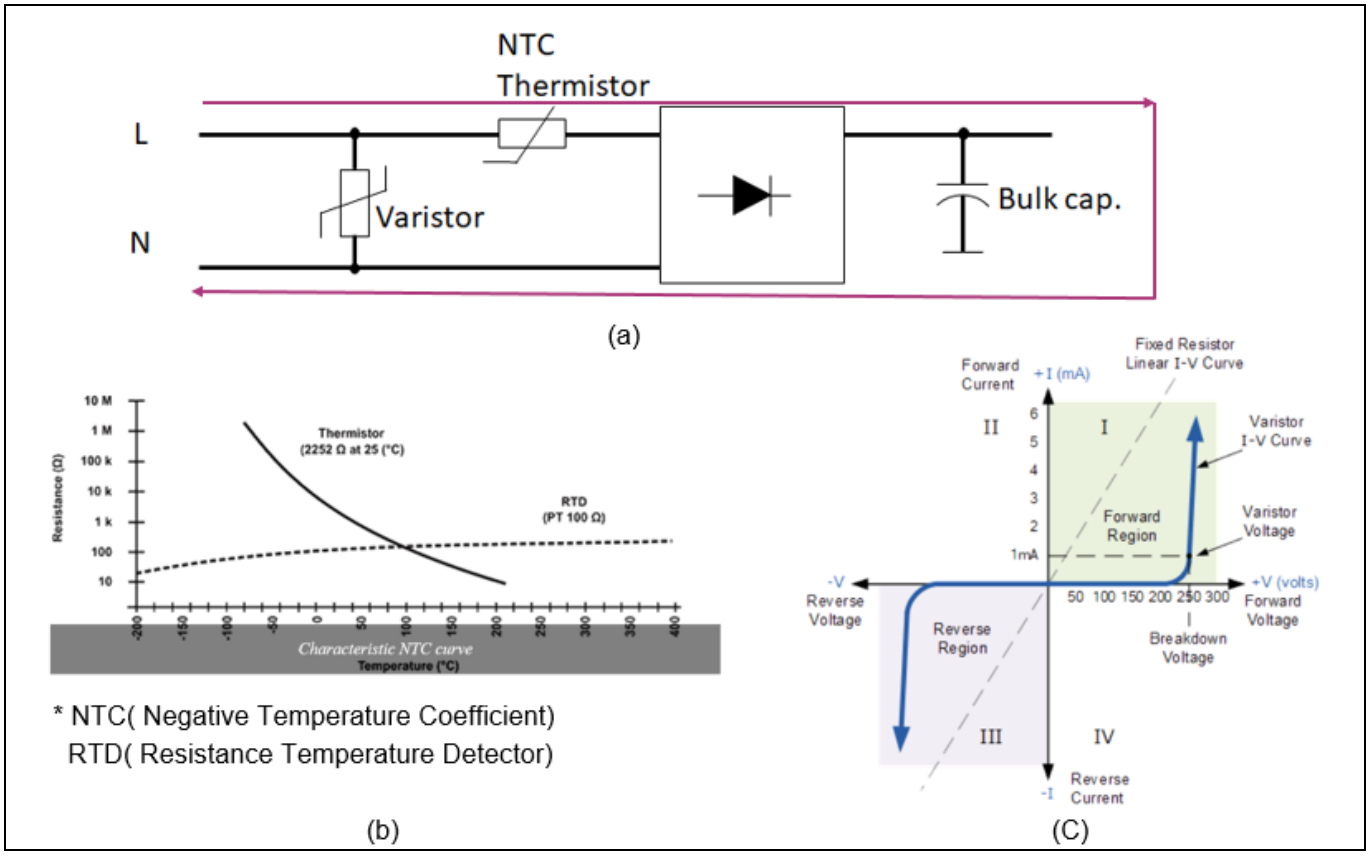


Figure 12 DM surge (a), Characteristic curve of NTC (b), Characteristic curve of varistor (c)

2.2 Solution for common mode surge

Common mode (CM) surge is applied on line-to-earth or neutral-to-earth. CM surge immunity will be influenced by the distance between the primary and secondary side, common choke, and Y-capacitor. The surge current generates voltage difference on the earth loop, and coupling to small signal then influences the control signal. Enlarging the trace of the Y-capacitor from line or neutral to earth can bypass the surge current disturbance.

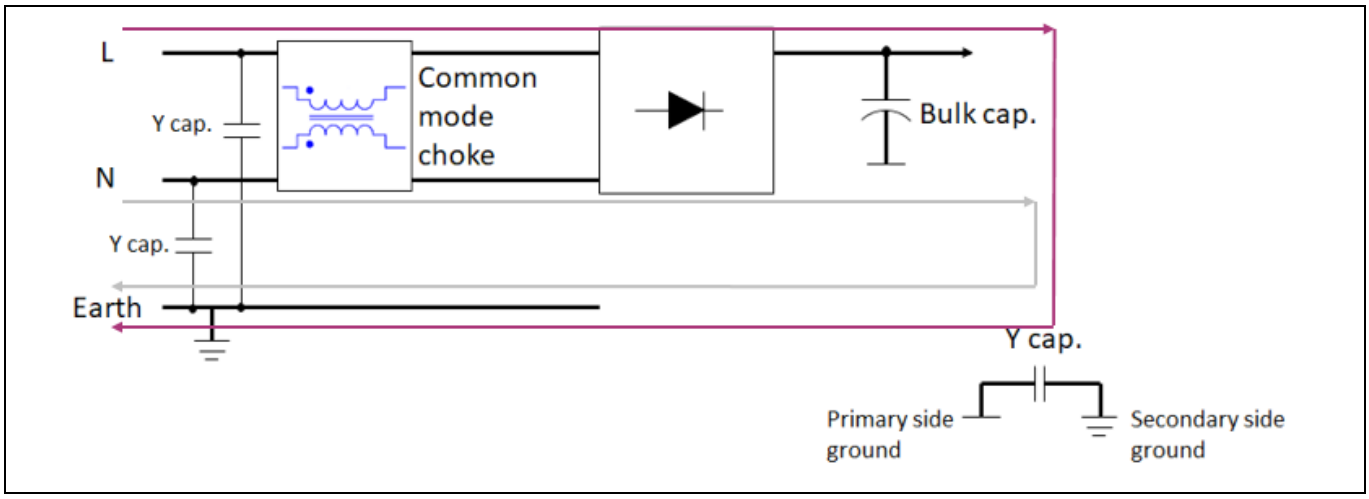


Figure 13 Solutions for common mode surge

The solutions for using a Y-capacitor for CM surge are shown in **Figure 13**, and are as follows:

1. Keep the size of the Y-capacitor smaller between primary-side and secondary-side ground.
2. Decreasing the value of the Y-capacitor between primary-side and secondary-side ground can decrease the surge current impact.
3. Enlarge the ground trace and keep enough distance between primary and secondary ground.
4. Keep enough distance from line and neutral to primary-side ground.
5. Adding the bead core at the pins of the Y-capacitor can also reduce the surge current. It is better to close to the bridge rectifier for the ground point of the Y-capacitor.
6. The Y-capacitor should not be placed on the small signal ground.

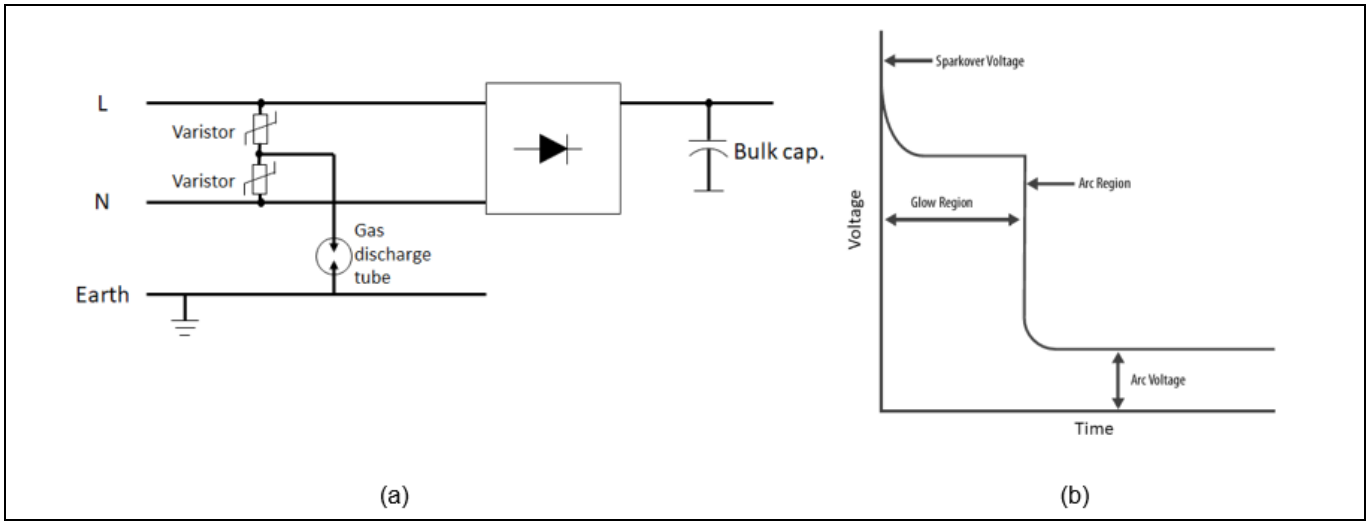


Figure 14 GDT for CM surge (a), characteristic curve of GDT (b)

A gas discharge tube (GDT) combined with varistors can offer an ideal solution to protect all kinds of installations from being damaged by transient overvoltage coupled into AC power networks. At normal operating voltages below the GDT sparkover voltage, the GDT remains in a high impedance off-state. With an increase in voltage across its conductors, the GDT will enter its glow voltage region. The glow region is where the gas in the tube starts to ionize due to the charge developed across it. In the glow region the increased current flow will create an avalanche effect in gas ionization that will transition the GDT into a virtually short-circuit mode, and current will pass between the two conductors. When a voltage disturbance reaches the GDT

sparkover value, the GDT will switch into a virtual short, diverting the surge current through the GDT to ground, and removing the voltage surge from the plant and equipment.

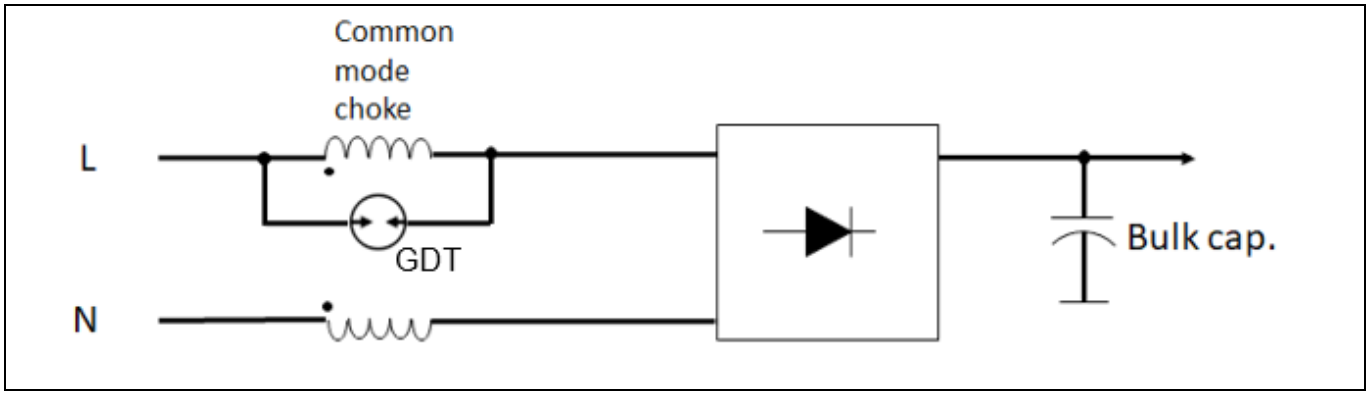


Figure 15 GDT paralleled with CM choke for CM surge

When a surge voltage is generated, the instant HV will cause the EMI CM choke to be saturated. The leakage inductance and capacitance oscillate and generate a higher resonant voltage and current. This will seriously impact the post circuit and may even damage the power devices and IC. For this reason, the GDT can be paralleled with one side of the CM choke, as shown in **Figure 15**, to suppress the oscillation with the short-circuit characteristic of GDT and reduce the voltage peak effectively.

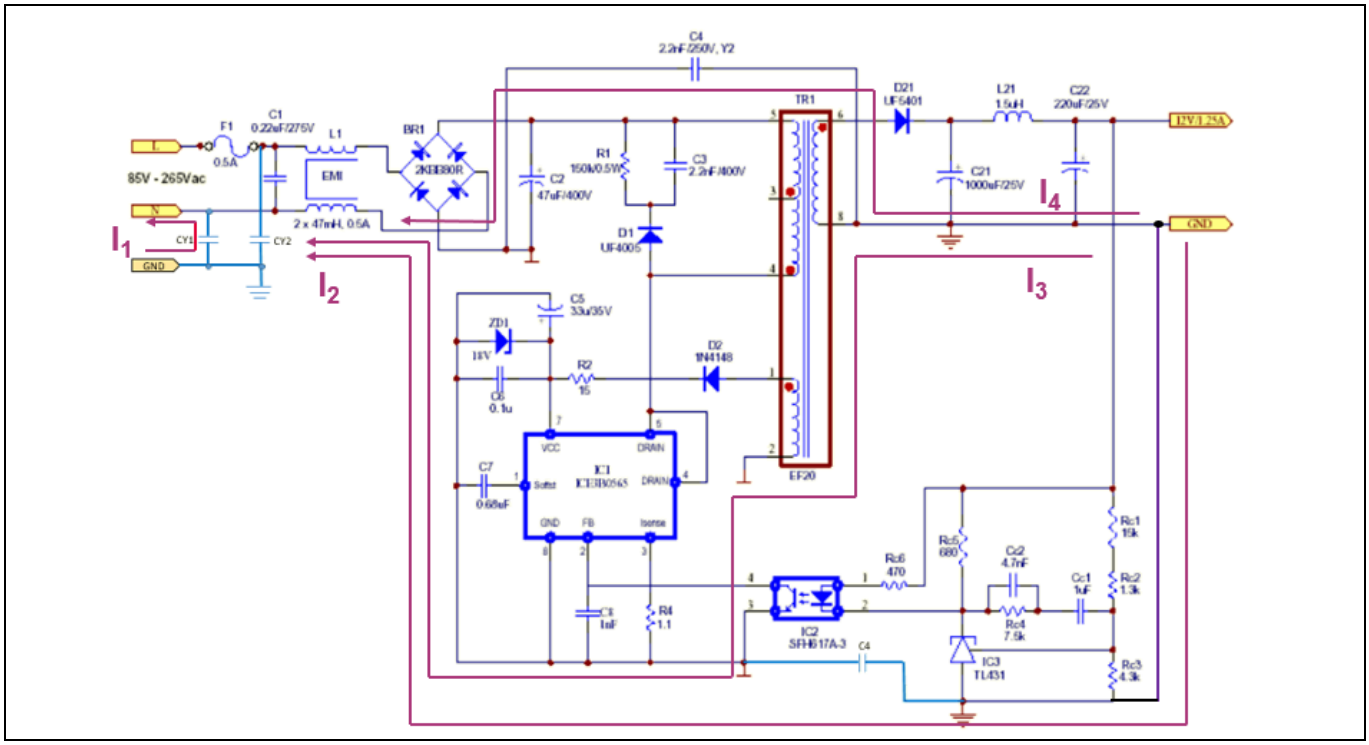


Figure 16 Example of SMPS for surge test

Figure 16 shows a circuit example under lightning surge test. The surge signal is applied between neutral and earth ground. Possible surge current paths I1, I2, I3 and I4 are shown in the diagram. I1 is the current which is passing through the safety Y-capacitor, CY1, between neutral and earth. In general, I1 is limited before the bridge rectifier and not observed by PWM IC. I2 is the current passing through EMI capacitor C4, and I3 is the current passing through the transformer from secondary ground to primary ground. I4 is the current that is also passing through the transformer, but from secondary ground to primary bulk positive. I4 will influence the IC as well if the IC has the pins directly connected to the positive HV bulk.

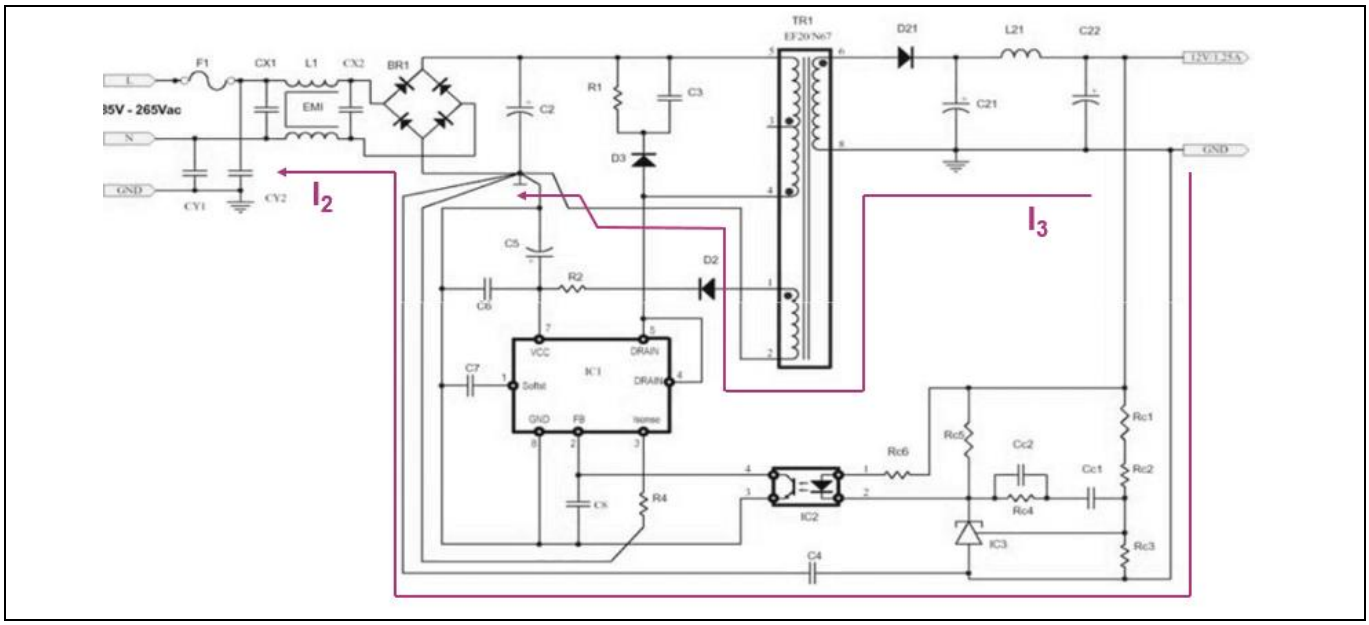


Figure 17 Star connection for primary ground

IC pins may observe the noise signal and are highly dependent on PCB design. “Star” connection is highly recommended for the following grounds, which must be separated and connected together in the bulk capacitor negative pin. With the proper star connection, I2 and I3 will not pass through the PCB track and IC voltage between pins will not observe the noise signal any more. In addition, the filter capacitor should be across the IC_VCC and IC_ground pin as far as possible.

2.3 Other considerations

2.3.1 Transformer design

If transformer insulation is lower than lightning surge voltage, a short duration time breakdown between primary and secondary will occur and a very high surge current will be generated. The shielding layer is inserted between primary and secondary and connected to the bulk capacitor positive. Because the shielding layer is much closer to the secondary side, the parasitic capacitance between secondary ground and the shielding layer is higher compared to secondary ground to the auxiliary winding. So, during a lightning surge test, the surge current is more likely via the shielding layer going into the bulk positive instead of the primary ground, which may influence IC ground.

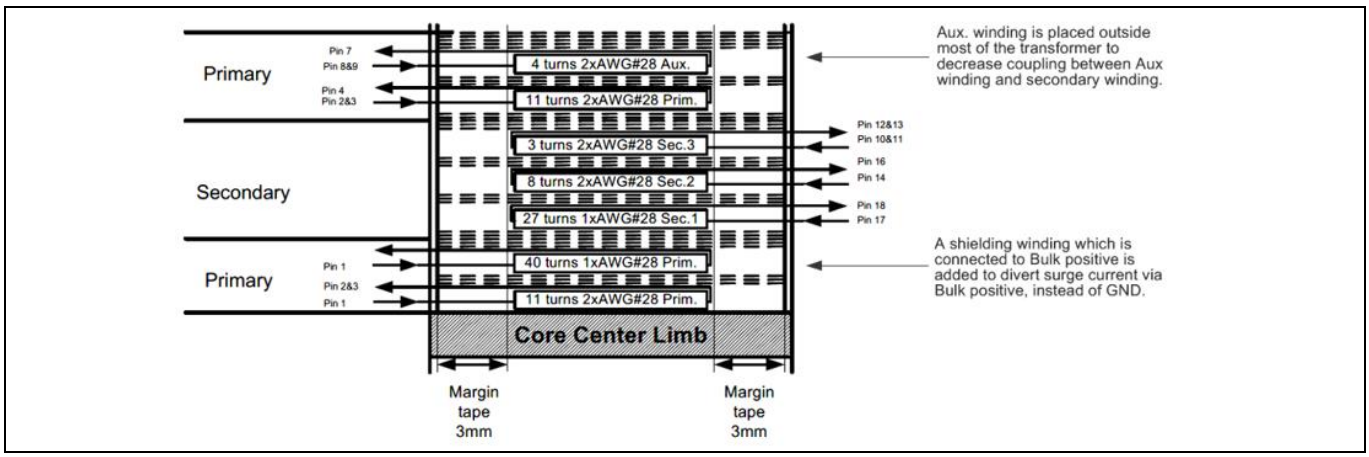
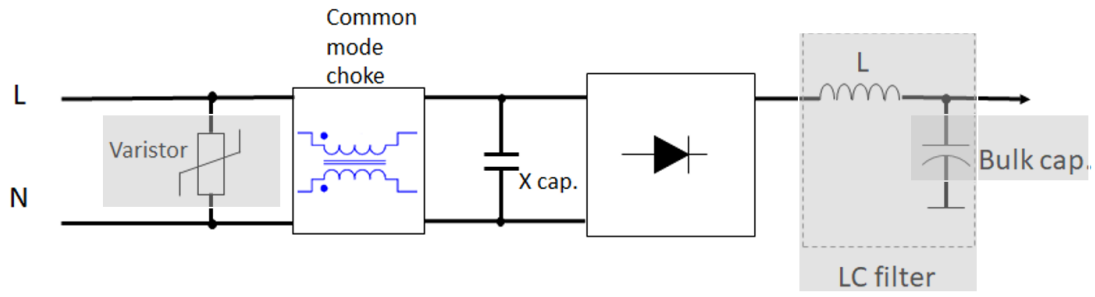


Figure 18 Transformer winding design with shielding layer

2.3.2 Line filter design

Regarding the other considerations for lightning surge test, the bulk capacitor helps to absorb the energy from the surge event. The size of the capacitor determines how much surge energy it absorbs. The LC filter helps by filtering the HV peak of the incoming surge event. Line filter design can be improved to increase the system surge rating. Changing the bulk capacitor value and varistor rating can be helpful to pass a 2 kV DM surge test.



Line Filter	0.22 µF Bulk cap. & 570 V varistor	0.68 µF Bulk cap. & 460 V varistor
2 KV	x	PASS
1 KV	PASS	PASS
0.5 KV	PASS	PASS

Figure 19 Bulk capacitor and varistor optimization for line filter design

2.3.3 IC pin filter capacitor and HV pin

Most of the IC pins have a filtering capacitor to reject the RF noise caused by lightning surge. This capacitor should be located as close as possible to the IC pin for better performance. Some ICs have an integrated start-up cell. The lightning surge current may go through the bulk capacitor positive. If the start-up cell pin is connected directly to positive, the lightning noise will be radiated as the transmitter from the PCB track, which is connected to the start-up cell with bulk capacitor positive. So it is necessary to keep this track as thin as possible and enough clearance from other small signal tracks. If this is not possible, a 100 kΩ resistor can be connected between the bulk capacitor positive and start-up cell pin.

3 Applications case study

3.1 40 W – indoor LED driver case study

This case study is for a 40 W LED driver designed with single-stage HPF flyback topology. The flyback MOSFET is IPD80R1K0CE. The bulk capacitor is only 220 nF, which is critical to absorb surge energy. This is why the surge capability of the MOSFET in this case becomes critical. Moving the design to latest generation of **CoolMOS™ P7** using equivalent $R_{DS(on)}$ **IPD80R900P7**, the flyback MOSFET fails at 1 kV DM surge testing.

The solution can be simple, just by rearranging the line filter components. The design passes 2 kV surge voltage, which is enough to pass the standard required for indoor lighting applications.

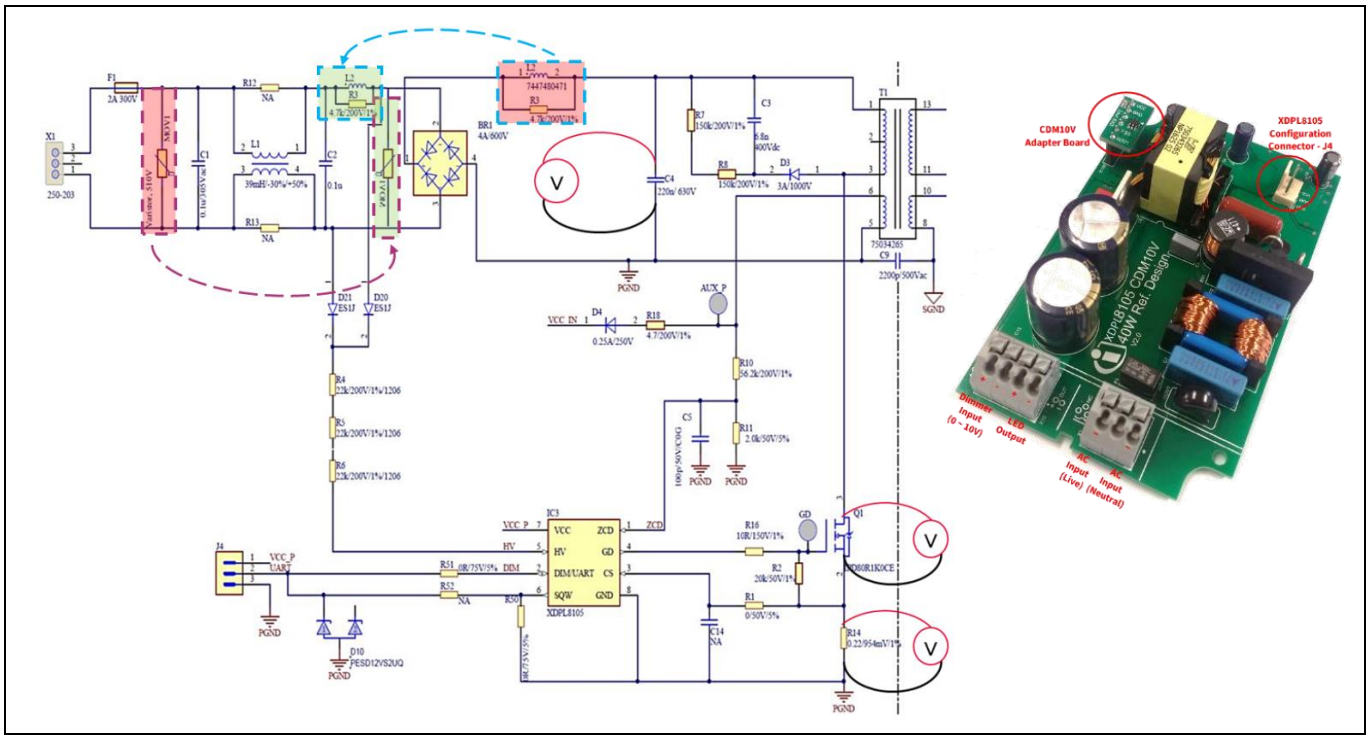


Figure 20 Line filter – original and rearranged design for the REF-XDPL8105-CDM10V [3]

Figure 20 showes the implementation of the line filter design for the **XDPL8015** reference design. Highlighted in red is the original position of the line filter components typically seen in most customer designs for high power factor flybacks, where the MOV is placed at the very beginning of the line filter, and the DM choke is placed at the DC side.

Highlighted in green is the line filter configuration, which shows the recommended rearrangement of the line filter, where the DM choke was moved to the AC side followed by the MOV.

The MOV is more effective after the CM choke, because the series resistance of the CM choke helps to reduce the surge current seen by the MOV. This helps to make the MOV clamp at a lower voltage, thus reducing the total energy seen by the MOV.

The DM choke is used to improve conducted EMI by suppressing the DM EMI caused by the flyback switching frequency and its harmonics. In its typical position on the DC side after the rectifier bridge, it ends up storing energy during surge events, which then avalanches the MOSFET/power semiconductor device.

3.1.1 Surge test simulation for original and recommended line filter design

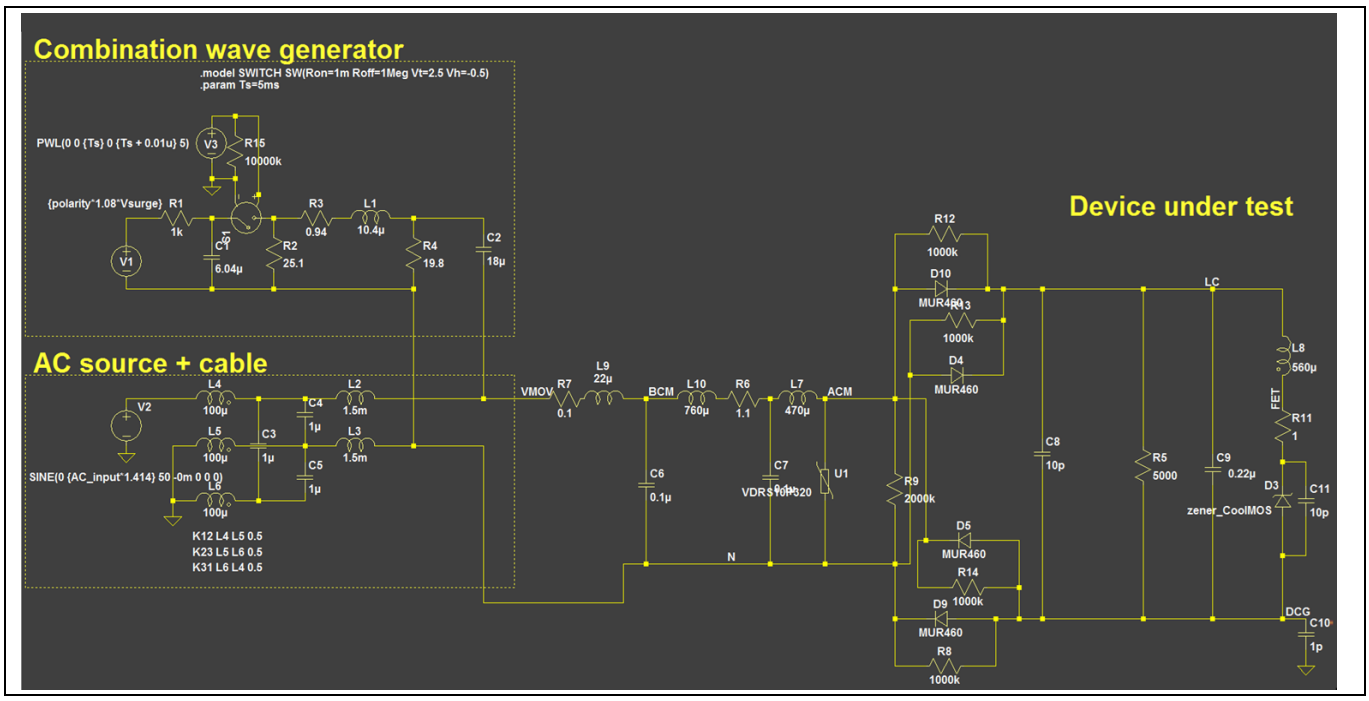


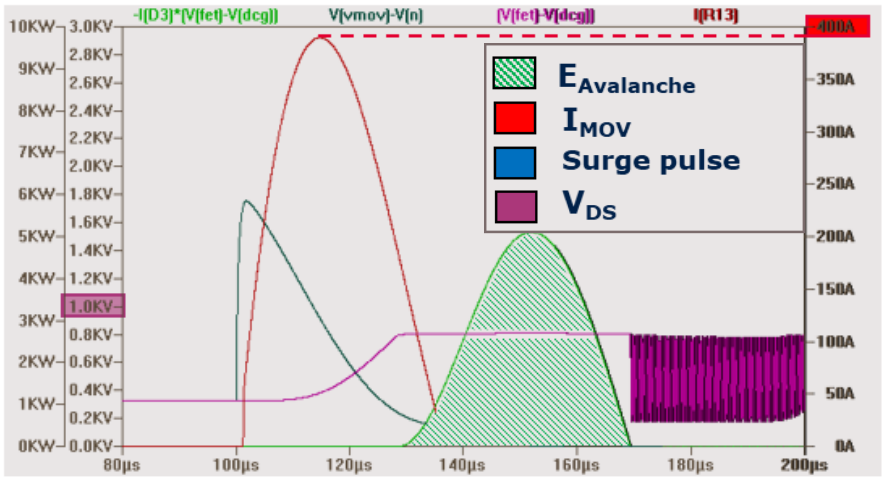
Figure 21 Line filter simulation using LTSPICE

Figure 21 show the simulation circuit done using LTSPICE, by considering the **XDPL8105** demo board line filter design as a reference circuit. Looking at the simulation results in **Figure 22**, first the original line filter configuration is shown, which leads to an avalanche energy of 116.9 mJ of energy seen by the MOSFET during a 2 kV surge event.

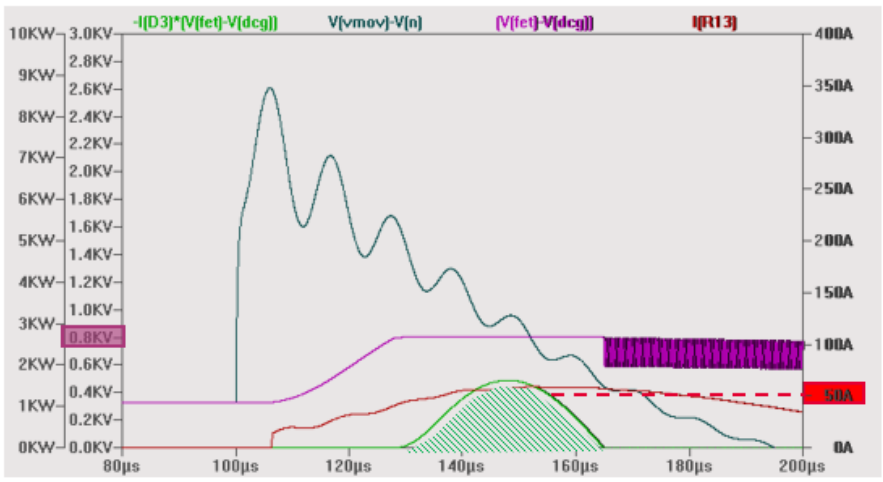
By moving just the MOV position as explained, avalanche energy is reduced to 35 mJ, and finally by moving the DM choke position to the AC side no avalanche energy was observed even with a 2 kV incoming surge pulse.

With this rearrangement of the line filter, the MOV clamping voltage is below the breakdown voltage of the MOSFET, so the system will have a higher surge immunity.

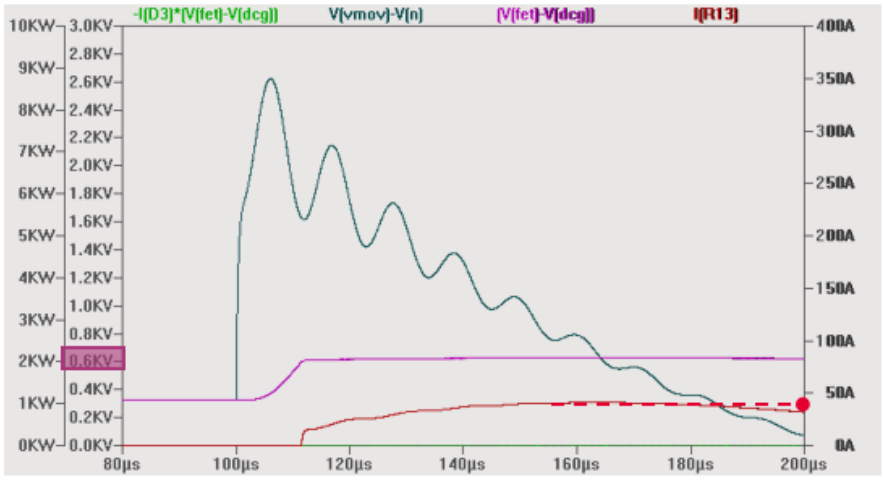
*Note: The simulation file can be downloaded from Infineon's website **here**.*



Original Filter Design	
V_{DS}	1 kV
I_{MOV}	400A
$E_{avalanche}$	116.9 mJ



Change MOV position only	
V_{DS}	850 V
I_{MOV}	50 A
$E_{avalanche}$	35.05 mJ

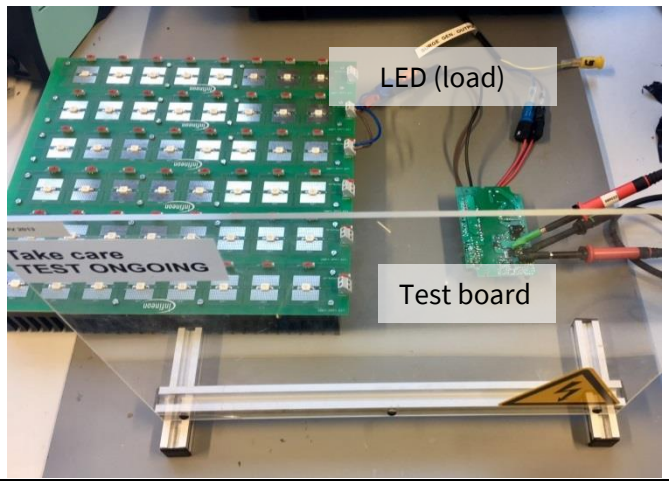


Change MOV and DM choke position	
V_{DS}	600 V
I_{MOV}	40 A
$E_{avalanche}$	**0 mJ**

Figure 22 $E_{Avalanche}$ (green), I_{MOV} (red), input surge pulse (blue), V_{DS} (purple)

Simulated results show in steps the effect of the proposed rearrangement of the line filter components on MOSFET stress during a surge event, by reducing the overall avalanche energy seen by the MOSFET.

3.1.2 Surge test measurements on the REF-XDPL8105-CDM10V



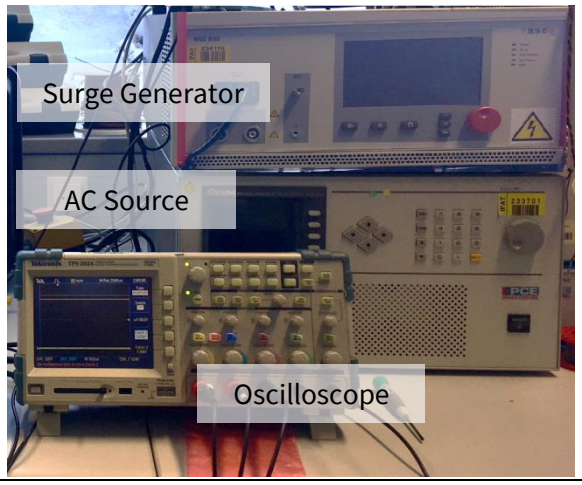


Figure 23 Line-to-line measurement setup

Figure 23 shows the complete surge test setup. The **XDPL8105** LED driver has an external LED stripe adapter used as a load. The surge generator is an ideal voltage source with the specified waveform, which is connected to its output ports with the known fixed resistance as in **Table 6**. It, as well as the XDPL8105, gets the AC power from the isolation transformer.

For the differential surge test, the surge voltage is applied across the AC lines of the **XDPL8105** board. The number of strikes is 8 at each voltage step (from 600 V up to 2 kV) at 90 positive polarity.

Table 6 Surge test conditions

Mains input voltage	230 V AC
Surge voltage	Variable up to 2 kV
Waveform	Fixed V_{CS} 500 surge generator
Output impedance, Z	2 Ω
Surge current waveform	1.2/50 µs
Polarity	Positive, only one impulse
Phase angle	90 degrees
Repetition rate	3 minutes, the converter is switched on/off (chip temperature 25°C)
Coupling	L and N

Table 7 show the test results, taking into account the original design with **IPD80R1K0CE** as reference, and the design change to **IPD80R900P7** with and without the line filter modifications.

It can be noted the significant reduction in the avalanche energy measured at the MOSFET with the proposed line filter modifications, the E_{av}, is reduced to 2 mJ at 2 kV surge pulse, which is several orders of magnitude lower than the avalanche rating of a MOSFET and thus would not cause an issue.

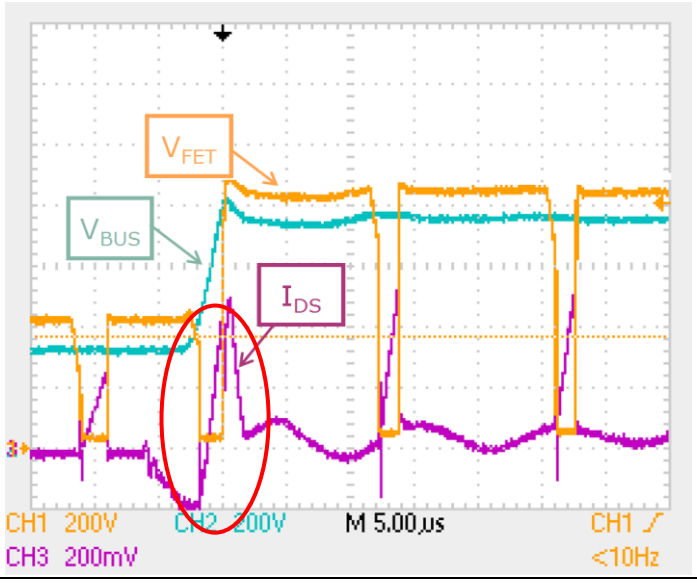


Figure 24 Change MOV and DM position – MOSFET experiences 2 mJ avalanche energy at 2 kV

Table 7 Test results

Coupling L-N Phase angle = 90° Positive polarity	**Original design with CoolMOS™ CE**			**Original design with CoolMOS™ P7**			**Changed MOV and DM position**		
	IPD80R1K0CE			**IPD80R900P7**			**IPD80R900P7**		
Surge voltage	**V(BUS)**	**V(FET)**	**∑Impulse**	**V(BUS)**	**V(FET)**	**∑Impulse**	**V(BUS)**	**V(FET)**	**∑Impulse**
600 V	936	920	32.5 mJ	840	912	10.1 mJ	696	784	0 mJ
800 V	1020	952	52.2 mJ	888	920	15.2 mJ	736	816	0 mJ
1000 V	1060	976	95.9 mJ	**Device failed**			760	840	0 mJ
1200 V	1111	968	107.5 mJ				784	848	0 mJ
1400 V	1100	1000	122.1 mJ				792	848	0 mJ
1600 V	1100	1040	146.1 mJ				808	848	0 mJ
1800 V	1120	1060	176.4 mJ				816	872	0 mJ
2000 V	1170	1160	**229.1 mJ**				824	896	**2 mJ**

3.1.3 Conducted emissions measurements according to the EN 55015 standard

The conducted emissions test was performed according to the EN 55015 standard class B limits (frequency range 9 kHz up to 30 MHz) at full load output current (I_{out} = 0.8 A). The measurements show no impact on the conducted emissions with the recommended line filter changes, for both coupling L and N.

3.2 150 W – monitor SMPS case study

This case study is for a 150 W monitor power supply with the topology CRM boost PFC followed by a DC-DC half-bridge LLC. The LLC MOSFETs are designed with **IPA60R360P7S**, which failed a 4.5 kV CM surge test. The original layout is as shown in **Figure 25**. On the V_{BUS} trace after the PFC block, the trace is split between a ferrite bead connected to the LLC stage, and then the signal goes to the bulk capacitor.

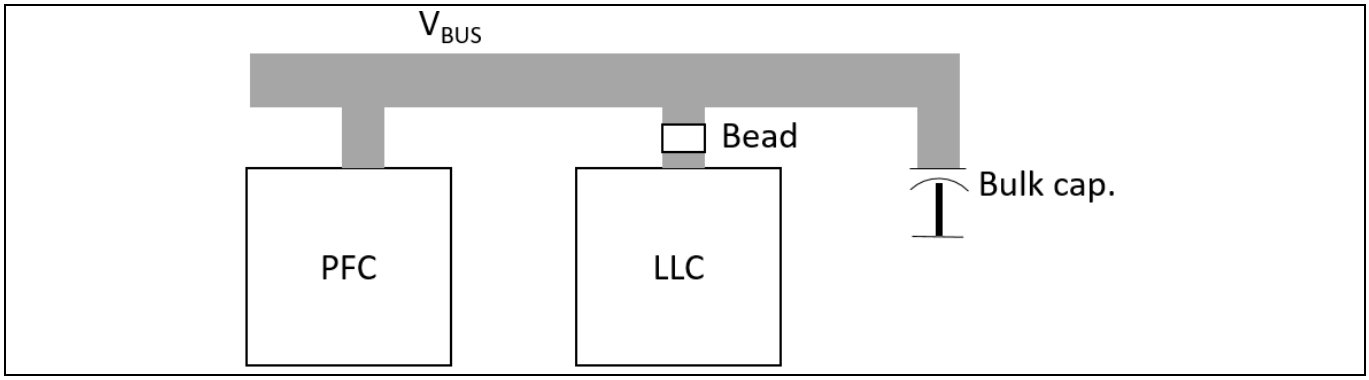


Figure 25 Original layout

Change the trace of V_{BUS} to the bulk capacitor first, then connect to the LLC stage. The bulk capacitor can absorb the surge energy first and soften the stress on the LLC MOSFETs. Furthermore, add the ferrite bead core at the Y-capacitor between primary-side ground and secondary-side ground. Finally, the 4.5 kV CM surge test can be passed with these solutions.

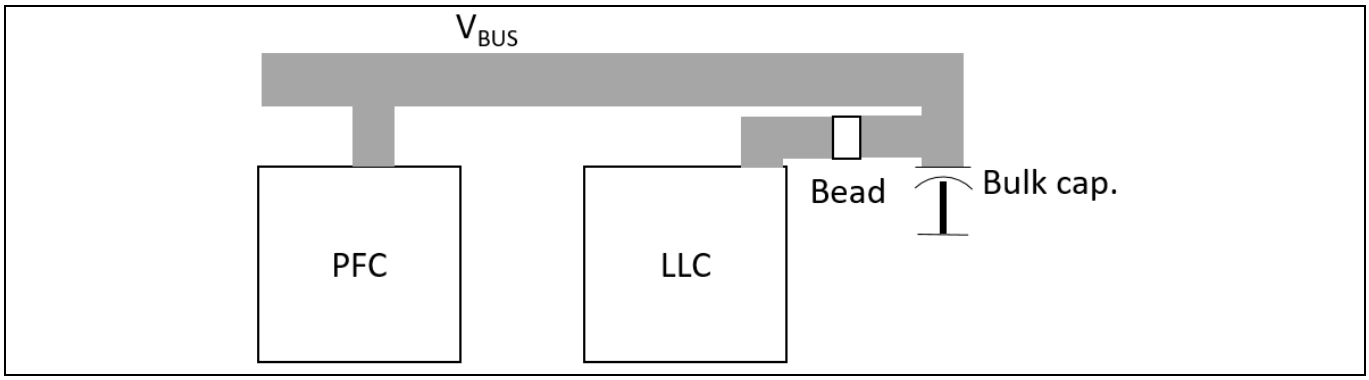


Figure 26 Layout changed

3.3 200 W – TV SMPS case study

This case study is for a 200 W TV power supply with the topology CRM boost PFC followed by a DC-DC half-bridge LLC. The PFC MOSFET is **IPA60R280P7S**, which failed a 2 kV DM surge test. The original HV sense layout trace of the LLC IC is too close to the primary-side ground trace. The solution is to change the layout. First, cut the original HV sense layout trace. Then increase the distance between the HV sense trace and the primary-side ground, since the coupling capacitance in between is inversely propotional to the distance of these two traces. Eventually, the 2 kV DM surge test can be passed.

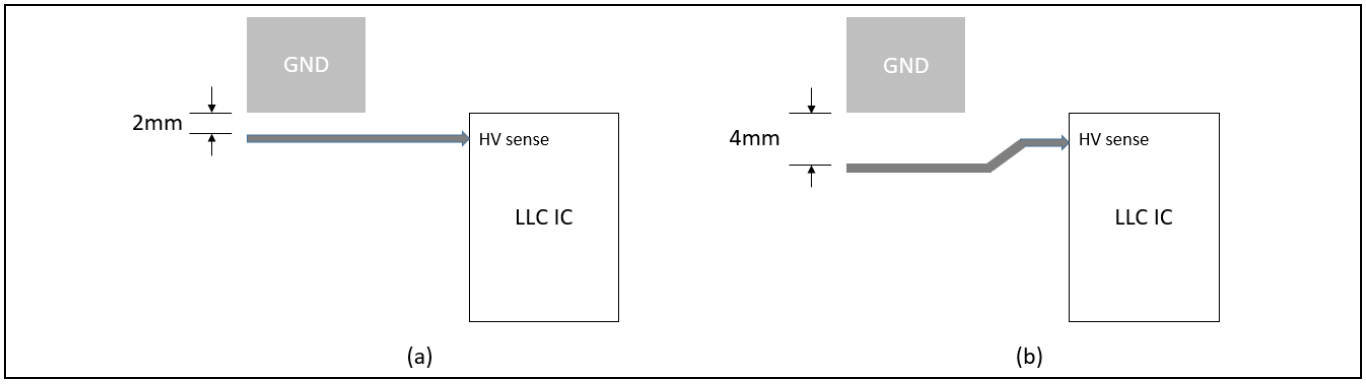


Figure 27 Original layout (a), changed layout (b)

3.4 170 W – TV SMPS case study

This case study is for a 170 W TV power supply with the topology CRM boost PFC followed by flyback. The flyback MOSFET is **IPA70R360P7S**, which failed a 6 kV tuner surge test, since the surge came from the secondary ground through the Y-capacitor. The tuner surge is one kind of CM surge test that is performed on TV SMPS to emulate a surge event coming from the connected TV antenna see section 1.2.5.

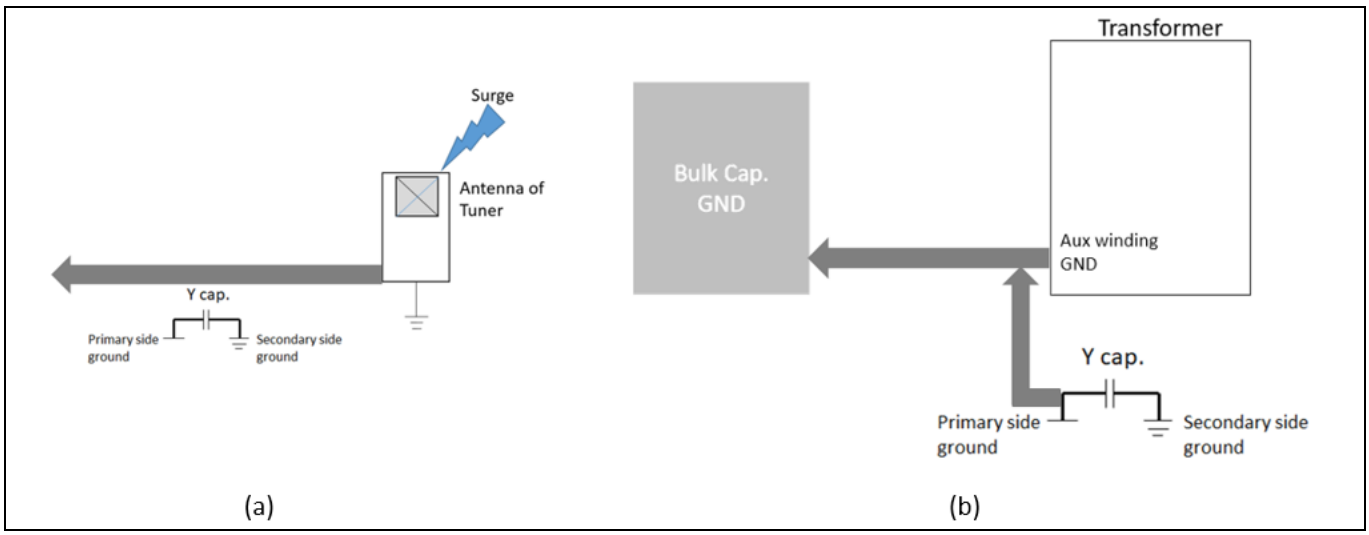


Figure 28 Route of surge (a), Original layout (b)

The solution is to change the layout. The original primary-side Y capacitor layout trace is connected to the auxiliary winding ground trace, then to the bulk capacitor ground.

First, cut the original Y-capacitor layout trace. Then connect the primary-side Y-capacitor layout trace to the bulk capacitor ground. This is to prevent interference from the primary-side ground surge noise on the auxiliary winding ground. With the separate layout, even the 9 kV tuner surge test can be finally passed.

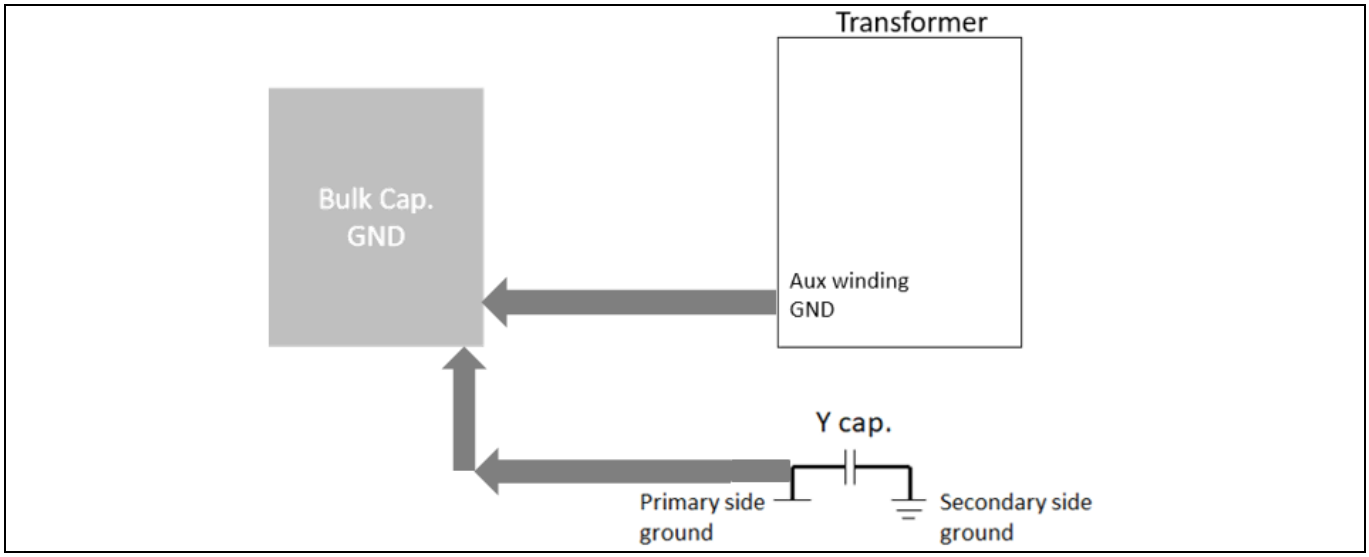


Figure 29 Separated layout trace of auxiliary winding GND and primary side GND

4 Conclusion

This application note has introduced the concept of lightning surge and presented the definition of lightning surge testing. Furthermore, solutions for lightning surge and application case studies have been discussed.

The surge suppression components such as MOV, GDT, chokes, and Y-cap can help the designers for softening the differential mode and common mode surge issues. In addition, the fundamental way is to optimize the PCB layout trace length and width, and the placement of the suppression components.

A well-designed PCB layout can not only reduce the effect of the parasitic inductance and capacitance on the system, but can also decrease the stresses on the main switch MOSFET. With proper design of the PCB layout and component placement, coupling of lightning surge to critical paths can be prevented, and thus the need for suppression components can be avoided and the total bill of materials (BOM) can be reduced.

5 References

[1] Infineon Technologies: “How to design SMPS to pass common mode lightning surge test”, application note, V1.0, September 2006.

[2] Infineon Technologies: Datasheet of CoolMOS™ IPP80R900P7, V2.2, January 2020.

[3] Infineon Technologies, “XDPL8105 single-stage PFC flyback dimmable constant current controller”, application note, 2019.

6 Revision history

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V 1.0	31-08-2020	First release

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