Product brief

OptiMOS™ power MOSFET Source-Down with dual-side cooling 25 V – 150 V

An innovative Source-Down PQFN 3.3x3.3 mm dual-side cooling package

Focusing on system level innovation, Infineon is working constantly on new ideas to supply the market with components that are solving challenges in end applications. Infineon is, once again, setting a new standard in MOSFET performance, reducing on-state resistance ($R_{DS(on)}$) and offering superior thermal management capability to provide industry benchmark products to the marketplace. This new Source-Down package concept supports the customer's requirement for high power density and optimized system level efficiency. The new generation of power MOSFETs is spanning over a wide voltage range of 25 V to 150 V.

The Source-Down concept

In this concept, the silicon die inside the package is flipped upside down. Instead of the drain potential being connected to the thermal pad, now the source potential is connected to it. This offers significant benefits over todays Drain-Down industry standard. Moreover, with the dual-side cooling package three times more power can be dissipated compared to the over molded package variant.

Lower $R_{DS(on)}$ and higher power density

In comparison to the standard Drain-Down concept, the latest Source-Down package technology enables a larger silicon die in the same package outline. In addition, the losses contributed by the package, limiting the overall performance of the device can be reduced. This enables a reduction in $R_{DS(on)}$ by up to 30 percent. The benefit at the system level is a shrink in the form factor due to the availability of a SuperSO8 5x6 mm benchmark $R_{DS(on)}$ in a PQFN 3.3x3.3 mm package. This allows for the available space to be used more effectively and enhances the power density in the end application.

Key features

- Major reduction in $R_{DS(on)}$ by up to 30% compared to current technology
- Improved R_{thJC} over current PQFN package technology
- Standard and center-gate footprints available
- New, optimized layout possibilities

Key benefits

- Enabling highest power density and performance
- Superior thermal performance
- Optimized layout possibilities for efficient use of real-estate
- Simplifying parallel configuration of multiple MOSFETs with
- Center-Gate footprint
- Improved PCB losses
- Reduced parasitics

Comparison of a standard Drain-Down device with a new Source-Down dual-side cooling footprints

PQFN 3.3x3.3 mm Drain-Down Standard-Gate	PQFN 3.3x3.3 mm Source-Down dual-side cooling	PQFN 3.3x3.3 mm Source-Down dual-side cooling Center-Gate footprint

Key applications

- Drives
- SMPS
  - Server
  - Telecom
  - OR-ing
- Battery management

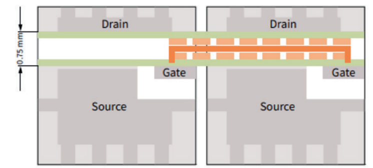
SMPS · Telecom · Server · Battery protection · Power Tools · Charger · BMS

www.infineon.com/PQFN-3-source-down

Standard vs Center-Gate

Infineon is releasing two different footprint versions in PQFN 3.3x3.3 mm: Source-Down Standard-Gate (same pinout as PQFN 3.3x3.3 products) and Source-Down Center-Gate. The standard Source-Down footprint is based on the current PQFN 3.3x3.3 mm pinout configuration. The pinout remains the same, simplifying the drop-in replacement of Drain-Down packages with the new Source-Down package. For the Center-Gate version, the gate-pin is moved to the center, supporting easy parallel configuration of multiple MOSFETs. With its larger drain-to-source creepage distance of 0.75 mm, it is possible to connect the gates of multiple devices on a single PCB layer. In addition, moving the gate connection to the center leads to a wider source area for improved electrical connection of devices.

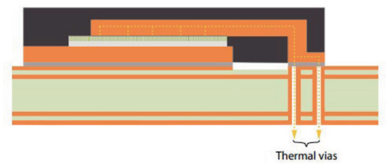
Source-Down - creepage distance



Optimized thermal management along with dual cooling package

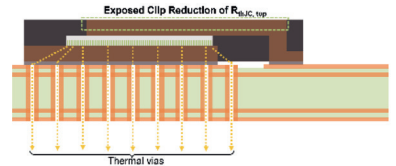
The active trenches on the source side of the silicon die are where the heat is generated. In the Source-Down concept, the heat is dissipated directly into the PCB through a thermal pad instead of over the bond wire or the copper clip. This improves the R_{thJC} of this product family from 1.8 K/W down to 1.4 K/W leading to an improvement of more than 20 percent. With the top side being exposed, the $R_{thJC,top}$ also improves from 20 K/W (for over molded) down to 0.7 K/W. Taking advantage of this very low $R_{thJC,top}$ by using a heatsink on top of the device, up to 3 times more overall power dissipation can be realized compared to an over molded package.

Drain-Down PQFN 3.3x3.3 mm



Considering a half-bridge configuration, in the Drain-Down concept the thermal pad of the low-side switch is connected to the switch node area. This area should be minimized to reduce noise emitted into the system. However, area minimization limits the thermal management capabilities of the low-side MOSFET. Thermal vias cannot be used on the noisy switch-node potential. With the Source-Down concept, the thermal pad of the low-side MOSFET is now on the ground potential, therefore enabling the use of thermal vias right underneath the device. This significantly improves the thermal performance and the power density in the end application.

Source-Down PQFN 3.3x3.3 mm



Product portfolio OptiMOS™ 25-150 V

Source-Down Standard-Gate DSC	Source-Down Center-Gate DSC	$R_{DS(on)}$ max.	V_{DS}
IQE006NE2LM5SC	IQE006NE2LM5CGSC	0.6 mΩ	25 V
IQE008N03LM5SC*	IQE008N03LM5CGSC*	0.7 mΩ	30 V
IQE013N04LM6SC	IQE013N04LM6CGSC	1.3 mΩ	40 V
IQE030N06NM5SC	IQE030N06NM5CGSC	3.0 mΩ	60 V
IQE050N08NM5SC	IQE050N08NM5CGSC	5.0 mΩ	80 V
IQE065N10NM5SC	IQE065N10NM5CGSC	6.5 mΩ	100 V
IQE220N15NM5SC*	IQE220N15NM5CGSC*	22 mΩ	150 V

*coming soon / product name subject to change based on final $R_{DS(on)}$ max. value.

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