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MOSFET Packaging Innovations For SWaP-Optimized Space Power Systems

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In space-rated power electronics, reliable attachment of surface-mount hermetically-packaged MOSFETs to printed circuit boards (PCBs) has been an elusive task for space system designers for many years. Material differences between the circuit board and surface mount device (SMD) package result in a mismatch between their coefficients of thermal expansion (CTEs). This CTE mismatch makes it difficult to maintain reliable solder joints between the PCB and the SMD package.

This article will look at how IR HiRel's advanced rad hard FET package design, the SupIR-SMD, solves these difficult challenges while enabling significant size, weight and power (SWaP) and cost advantages to the space power system design community. The SupIR-SMD has also been fully qualified under MIL-PRF-19500 JANS, which is the quality and reliability benchmark for space applications.

After reviewing the CTE characteristics of commonly used package and board materials, and offering examples of damage caused by CTE mismatch, we look at previous solutions to this problem. In particular, we'll discuss the lead-attach and carrier solutions, noting their benefits and drawbacks. With that as background, we'll explain how the construction of the SupIR-SMD overcomes the CTE mismatch issue while reducing the size and cost penalties associated with the existing solutions.

CTE Design Challenges

The varied CTEs of the materials themselves pose the first basic challenge. PCBs, ceramics, metals and glass expand and contract at different rates with temperature changes. The question is first finding the threshold before the material stresses cause connection problems in assemblies.

Table 1 lists the coefficients of thermal expansion, α, in units of 10^{-6}/°C for various materials used in hermetic packages of power devices and PCBs.

Table 1. Material properties in hermetic packages and PCBs.

Material	CTE α (10^{-6}/°C)
FR-4 circuit board	13-14
Polyimide circuit board	18
Copper	16-17
Ceramic/glass	6

CTE mismatch also makes it challenging to preserve the sealed integrity of a hermetically packaged device. Almost all space-grade components for long-life and/or deep space missions are housed in hermetic packages based on a combination of glass, ceramics, and metals. These materials are fundamentally different: glass and ceramic are brittle, while metal is ductile.

When stressed extensively, the latter will yield and sustain large strain without breaking. However, ceramic and glass will crack. Some examples of fractures in finished circuit card assemblies of power components can be seen in Fig. 1.

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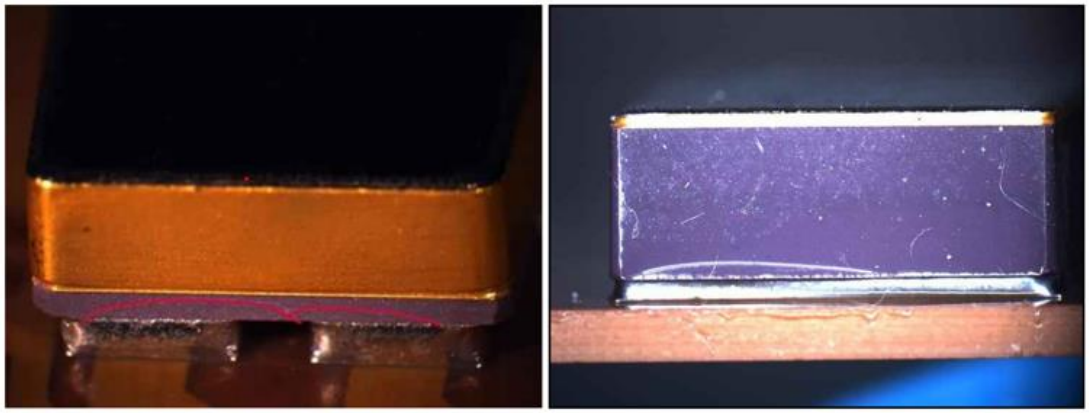

Fig. 1. Stress fractures of SMD packages mounted on PCBs.

The different CTEs of the materials make it extremely difficult to achieve good thermal design compatibility between large surface-mount hermetic power devices and most common PCBs, due to package cracking and the unreliable solder joints of power devices that are direct surface-mounted on PCBs.

Previous Solutions

Over the years both semiconductor suppliers and power system designers have tried to solve the problem of unreliable solder joints and package cracking. One concept attempted to change the PCB's local properties by inserting a low CTE material under the power device. Others have tried developing stronger ceramics. However, neither approach has been widely adopted in the industry. One solution that did gain traction is the use of package leads or carrier options to overcome the issues of CTE mismatch between device and PCB.

To support this solution, IR HiRel has long offered lead-attach options for its larger SMD power devices. With this approach, copper ribbons are attached to the SMD package to provide strain relief. A drawing of a lead-attach and mounting example is shown in Fig. 2. This approach mitigates the CTE mismatch, but increases assembly costs and board area size, while reducing overall power system performance.

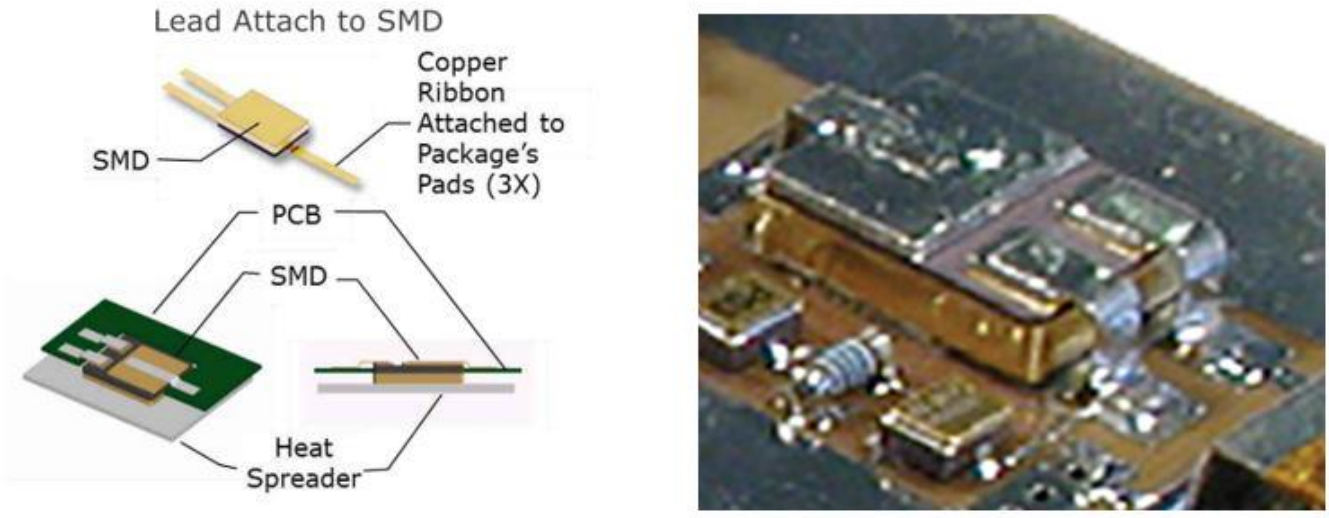

Fig. 2. The lead-attach option on an SMD package and a PCB mounting example.

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The other option that IR HiRel offers to overcome CTE mismatch is the SMD package carrier. In addition to strain relief, the carrier allows the heat to flow more directly down through the device mounting. An image of the carrier with a device mounted to it is shown in Fig. 3 along with an image of the carrier by itself that illustrates its physical construction at a high level.

The direct bond copper (DBC) substrate provides a more direct thermal path down through the carrier. While this solution addresses CTE mismatch and provides a better thermal path through the carrier, it increases design size and reduces performance.

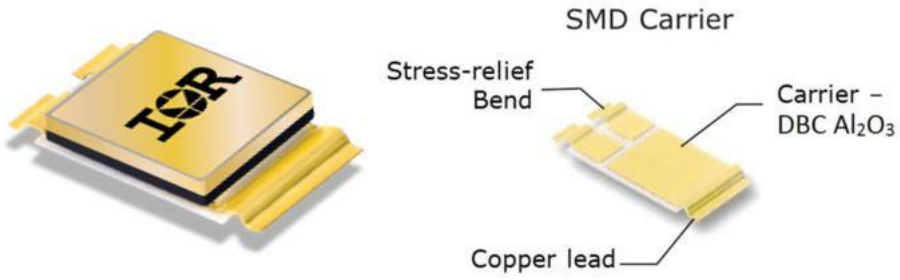

Fig. 3. Package carrier and physical construction.

Other Issues With The Previous Solutions

As discussed, the lead attach and carrier options provide better CTE matching, but are still suboptimal for high-performance space power supply design.

The most debilitating drawback of the lead-attach option is its suboptimal thermal path for heat removal from the device. The die is mounted on the terminal side of the package, thus optimal heat transfer occurs when the SMD device is soldered directly to the PCB. However, almost all customers using the lead-attach variant of the SMD package mount it dead bug style, as shown in Fig. 2. In this configuration, the heat must flow through the leads to the PCB and/or through the package sidewalls to the lid and down the heat spreader.

A second drawback for the lead-attach option is the added cost and time of manufacturing and assembly of the PCB board. Since the devices with lead attach are procured with straight leads, they must undergo an added lead forming step before they can be mounted on the PCB. Using this approach also requires manual soldering, as the lead-formed device is not conducive to automatic pick-and-place soldering methods.

The third drawback of the lead-attach or carrier options is the increase in the PCB footprint to accommodate them. The industry-standard SMD-2 package has an area of approximately 0.376 in^2, however, with a carrier, the package size increases by 57%. This can lead to a significant increase in solution size and weight.

A Purpose-Built SMD Package For Space

For a holistic approach, IR HiRel designed a new package to optimize CTE matching, while maximizing system performance in the smallest possible form factor at the lowest total cost of ownership. In order to solve the CTE mismatch, IR HiRel adopted a package design with a multiple-layer base as shown in Fig. 4.

In this design, the base has two layers: the layer that connects the ceramic body is a copper-based alloy that has a CTE matching the ceramic CTE, and the layer that connects to the circuit board is another copper-based alloy that has a CTE value between those of the first layer and the circuit board. In this way, the CTE changes gradually from ceramic to PCB and thus reduces the stress from a large CTE mismatch. Additionally, the new SupIR-SMD incorporates the stress relief of wide, flat leads with a curved structure and the more direct thermal path through the bottom of the package where the die is mounted.

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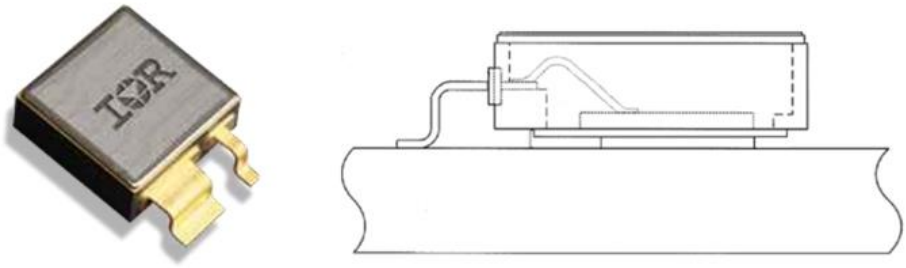

Fig. 4. A SupIR-SMD package (left) and a cross-sectional view (right) showing chip and wire bond for the package mounted to a PCB.

Overcoming The Drawbacks Of Leads And Carrier

In addition to overcoming the CTE mismatch, the SupIR-SMD package was designed to boost power system performance, reduce manufacturing cost, simplify thermal design and reduce solution size and weight.

The reduction in PCB manufacturing cost takes three aspects into consideration. The first is the physical PCB board saving that can be realized by using the smaller SupIR-SMD package. The second aspect is the time saved when using the new package compared to that of the manual assembly process that is required on the SMD with leads options. Lastly, comes the customer's savings by using a standard FR4 PCB material compared to polyimide.

Saving PCB-Board Space

The SupIR-SMD package is much smaller and lighter than the SMD-2 with leads or carrier. See Fig. 5 for a visual comparison of the SupIR-SMD, SMD-2 with leads and SMD-2 with carrier. The footprint is 37% smaller and the mass is 38% lighter than the SMD-2 with carrier option. In high-power dc-dc converters, this can lead to significant board size reduction and PCB cost savings.

Take for example a high-power full bridge converter with synchronous rectification utilizing six power MOSFETs. Using the SupIR-SMD package versus the lead attach can save up to 18% in the PCB cost.

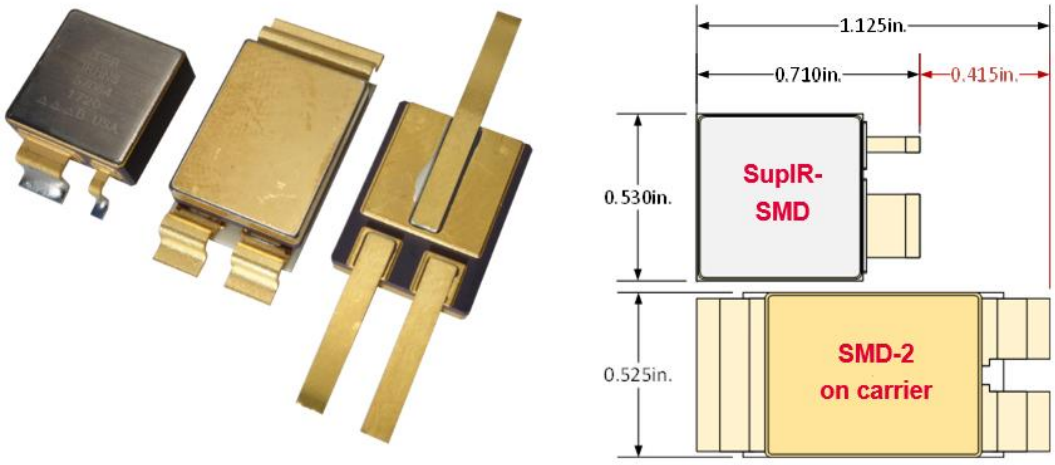

Fig. 5. A comparison of a SupIR-SMD, an SMD-2 with carrier and an SMD-2 with leads illustrates the board-space savings achieved by the new SMD package.

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Saving Manufacturing Costs And Assembly Time

The manufacturing cost reduction is realized through the SupIR-SMD package's compatibility with automated pick-and-place equipment. The estimated savings is based on our experience in designing and manufacturing space-grade PCB-based power solutions.

Taking the same example of a high-power dc-dc converter using six MOSFETs, we estimate lead forming and manual soldering of the SMD-2 with leads package takes an average of ten minutes per MOSFET for a total of 60 minutes per converter. With the pick-and-place machine, the time to mount the SupIR-SMD package on the PCB is just over seven minutes for all six MOSFETs. This leads to a time savings of up to 88% in this example.

Referring back to Table 1, the polyimide material has a CTE equal to 18 and is closer to the copper CTE of 16-17, compared to the FR4 material which has CTE of 13-14. With copper as the main metal used in the large pads of the SMD type package, most customers would choose polyimide PCB boards to match the PCB and package CTE.

However, with a SupIR-SMD package, using the more expensive polyimide material or costlier thermally compensated boards is no longer necessary. Based on our experience with PCB vendors, an FR4 board could cost up to 25% less than a polyimide board.

Improving Thermal Performance

In addition to manufacturing cost, the SupIR-SMD package can improve thermal performance of the design. The typical thermal resistance from junction to case for the SMD-2 and SupIR-SMD packages are very similar, 0.2°C/W and 0.3°C/W, respectively.

However, the SMD-2 with leads mounted in a dead-bug mount has a typical thermal resistance from junction to lead of 6°C/W. This is significantly higher than SupIR-SMD package thermal resistance of 0.3°C/W from junction to case. This reduction in the thermal resistance leads to a cooler system or the ability to increase the power density of the converter.

The example below shows the calculated temperature rise in a package level comparison for an SMD-2 with leads versus the SupIR-SMD package. The reference point for the SMD with leads is the lead which is sunk to 25°C. The SupIR-SMD is sunk at the case to 25°C.

Table 2. Calculated temperature rise comparison of SMD-2 with leads and SupIR-SMD.

	Parameter	SMD-2 with leads	SupIR-SMD	Unit
Reference temperature	T_{REF}	25	25	°C
Junction-to-lead	R_{lead}	6	N/A	°C/W
Junction-to-case	R_{JC}	N/A	0.3	°C/W
Power dissipation	R_{loss}	4	4	W
Junction temperature	T_J	49	26	°C
Temperature rise	ΔT	24	1	°C

In both examples, the power dissipated in the MOSFET is 3.96 W. However, the power transistor in the SupIR-SMD package would experience only a 1.12°C rise in its junction temperature. The device in the SMD-2 with

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leads would have a junction temperature rise of 23.76°C. The designer could now either simplify the thermal chassis design or increase the converter's power density using the SupIR-SMD package.

The simulated thermal image in Fig. 6 clearly shows the increased die temperature in the SMD-2 package with leads mounted dead-bug style. In order to overcome the increased thermal resistance of the SMD-2 with leads, many designers underutilize the MOSFET's full capability. In addition, this configuration degrades the device performance due to the increase in electrical resistance and inductance caused by the addition of the leads.

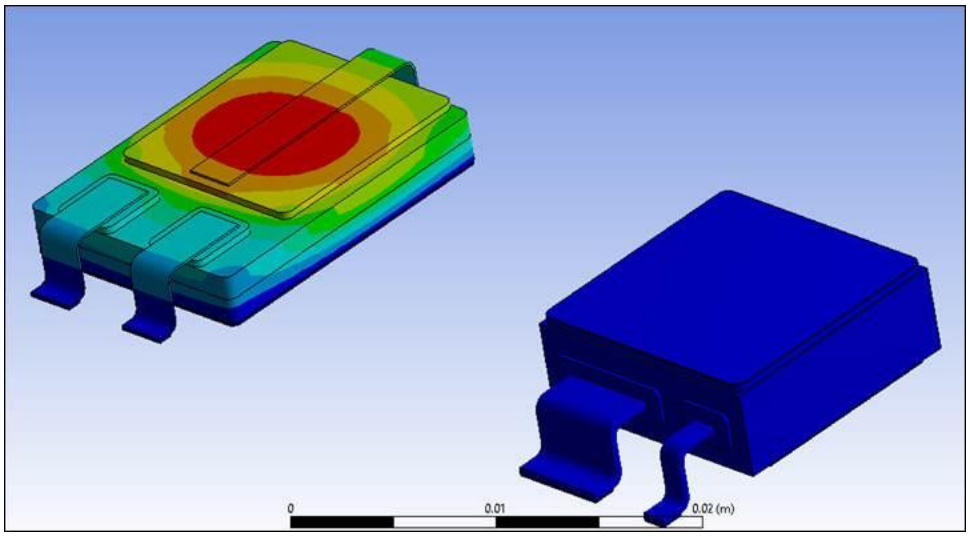

Fig. 6. Thermal image of SMD-2 with leads vs. SupIR-SMD.

Summary

IR HiRel developed the SupIR-SMD package as a way to overcome the issue of CTE mismatch between a power semiconductor and PCB. However, the benefits do not stop there. This novel package also boosts power system performance and flexibility for power designers to optimize their systems for size, weight and power.

Devices in the SupIR-SMD package have been qualified per MIL-PRF-19500. The slash sheets are published and the devices are also on DLA's Qualified Parts List (QPL). A link to available devices can be found in the reference section below.

Reference

Learn more at www.infineon.com/supir-smd.

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For more on MOSFET packaging, see How2Power's Design Guide, locate the "Design Area" category and select "Packaging And Interconnects". For more on space-grade power components and power converters in general, See How2Power's special section on Space Power.

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