ICE3xS03LJG

F3 Fixed Frequency PWM Controller (Latch & Jitter version) Design Guide

Power Management & Supply

Never stop thinking.

Published by
Infineon Technologies AG
81726 Munich, Germany

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ICE3xS03LJG

Revision History:	**2011-12**	V1.1
Previous Version:	V1.0	
Page	Subjects (major changes since last revision)	
5	Add 130kHz	
9	Add block diagram of ICE3GS03LJG	
12	Add schematic of ICE3GS03LJG	
13	Update equation (1)	
17	Add 130kHz	
20	Update table (1) Protection functions and failure conditions	
23	Update product portfolio	
25	Update references	

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Kyaw Zin Min
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1 Introduction

The **ICE3xS03LJG** is the latest development of the F3 fixed frequency PWM controller IC with latch and jitter features. It is a current mode PWM controller with startup cell in a DSO-8 package. The switching frequency is running at 65/100/130 kHz and it is suitable for AC/DC power supply such as LCD monitors, adapters for printers and notebook computers, DVD players and recorder, Blue-Ray DVD player and recorder, set-top boxes and industrial auxiliary power supplies. It is a current mode PWM controller and provides a cycle-by-cycle peak current control which can provide extended protection for the risk of transformer saturation.

The **ICE3xS03LJG** adopts the BICMOS technology and provides a wider Vcc operating range up to 24.5V. It inherits the proven good features of F3 FF PWM controller such as the active burst mode achieving the lowest standby power, the propagation delay compensation making the most precise current limit control in wide input voltage range, etc. In addition, it also adds on some useful features such as built-in soft start time, built-in basic with extendable blanking time for over load protection and built-in switching frequency modulation (frequency jittering), latch off protection enable pin, etc.

2 List of Features

500V Startup Cell switched off after Start Up
Active Burst Mode for lowest Standby Power
Fast load jump response in Active Burst Mode
65/100/130 kHz internally fixed switching frequency
Built-in Latched Off Protection Mode for Over-temperature, Overvoltage & Short Winding
Auto Restart Protection Mode for Overload, Open Loop, VCC Under-voltage & Short Optocoupler
Built-in Soft Start
Built-in blanking window with extendable blanking time for short duration high current
External latch off enable function
Max Duty Cycle 75%
Overall tolerance of Current Limiting < ±5%
Internal PWM Leading Edge Blanking
BiCMOS technology provide wide VCC range
Frequency jitter and soft gate driving for low EMI

3 Package

The package for F3 ICE3xS03LJG latch & Jitter mode product is DSO-8.

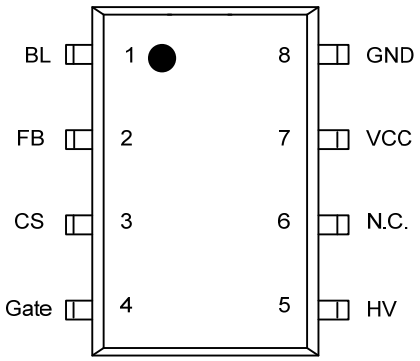

Figure 1 Pin assignment

Pin	Name	Description
1	BL	extended Blanking & Latch off enable
2	FB	FeedBack
3	CS	Current Sense
4	Gate	Gate driver output
5	HV	High Voltage input of startup cell
6	N.C.	Not Connected
7	VCC	Controller supply voltage
8	GND	Controller GrouND

4 Block Diagram

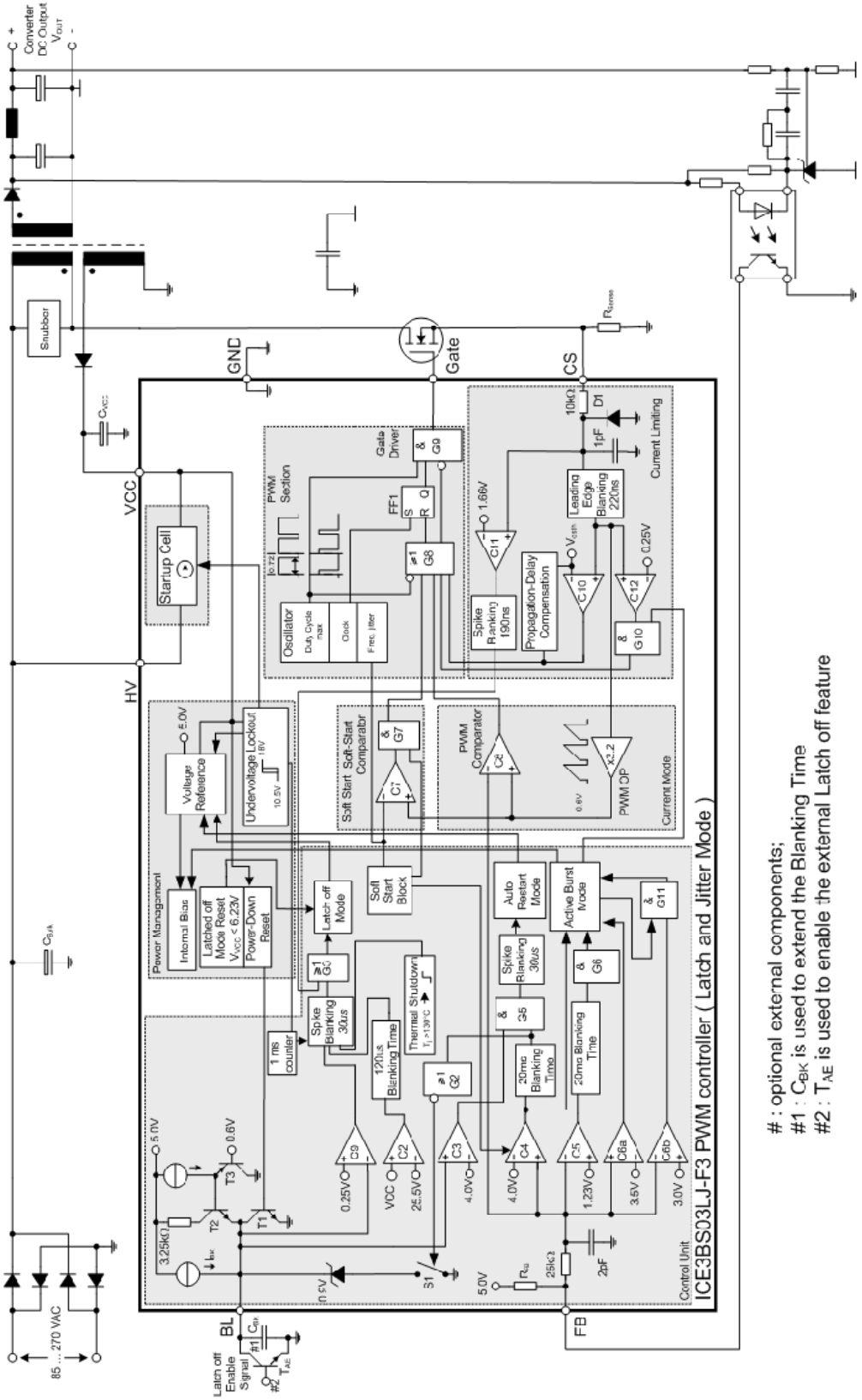

Figure 2 Block Diagram of ICE3BS03LJG

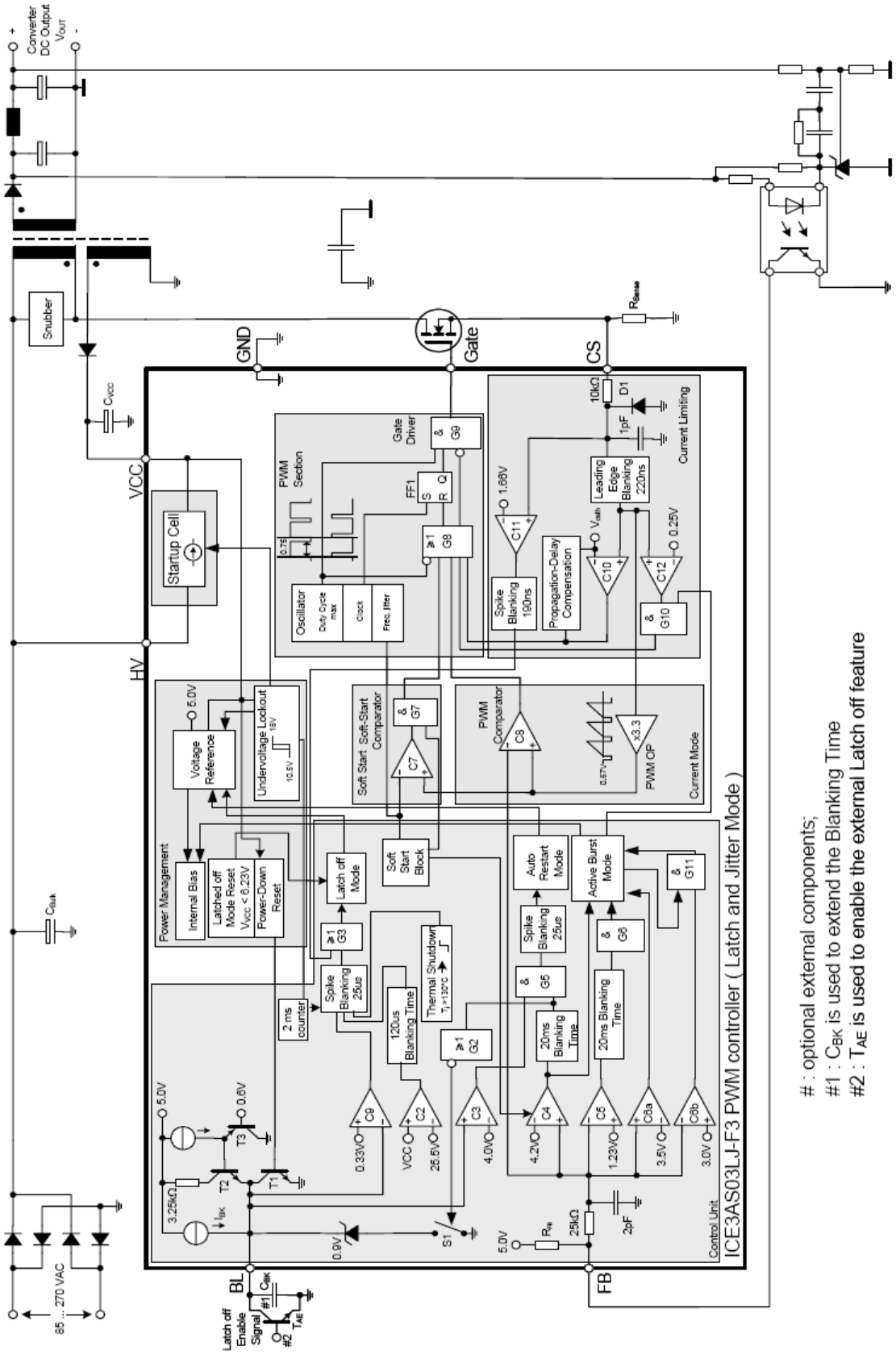

Figure 3 Block Diagram of ICE3AS03LJG

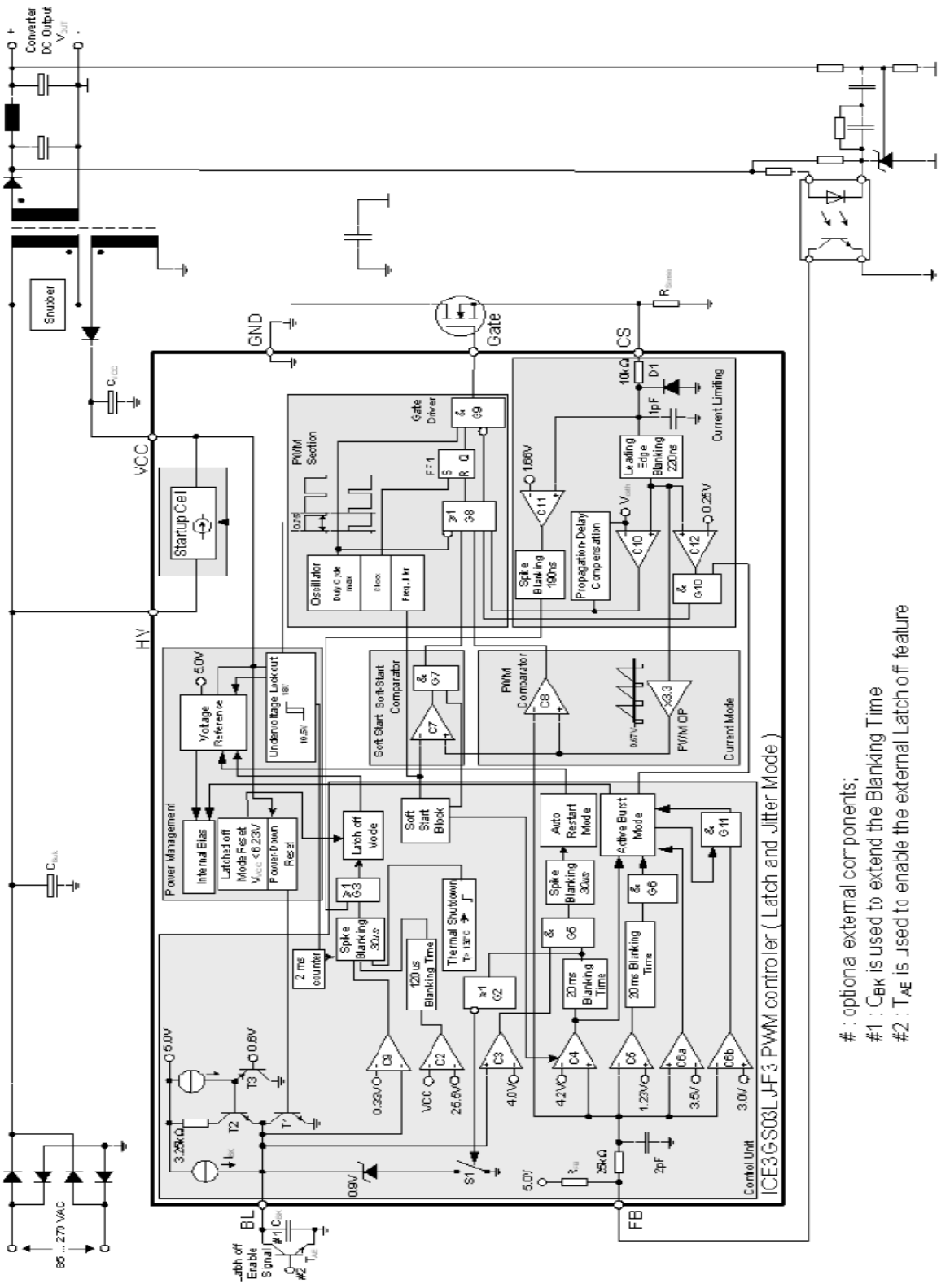

Figure 4 Block Diagram of ICE3GS03LJG

5 Typical Application Circuit

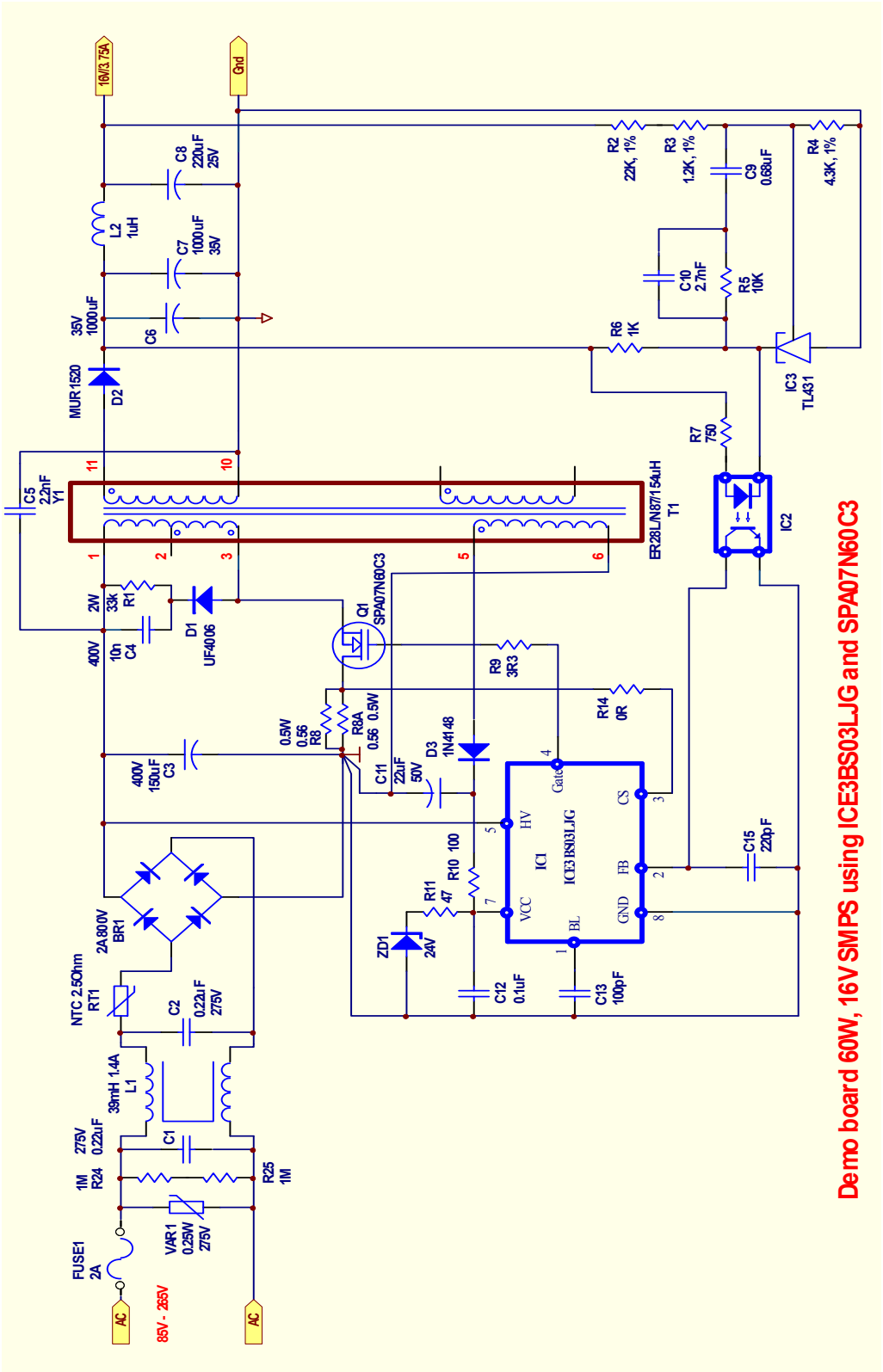

Figure 5 Typical application circuit with ICE3BS03LJG 60W 16V

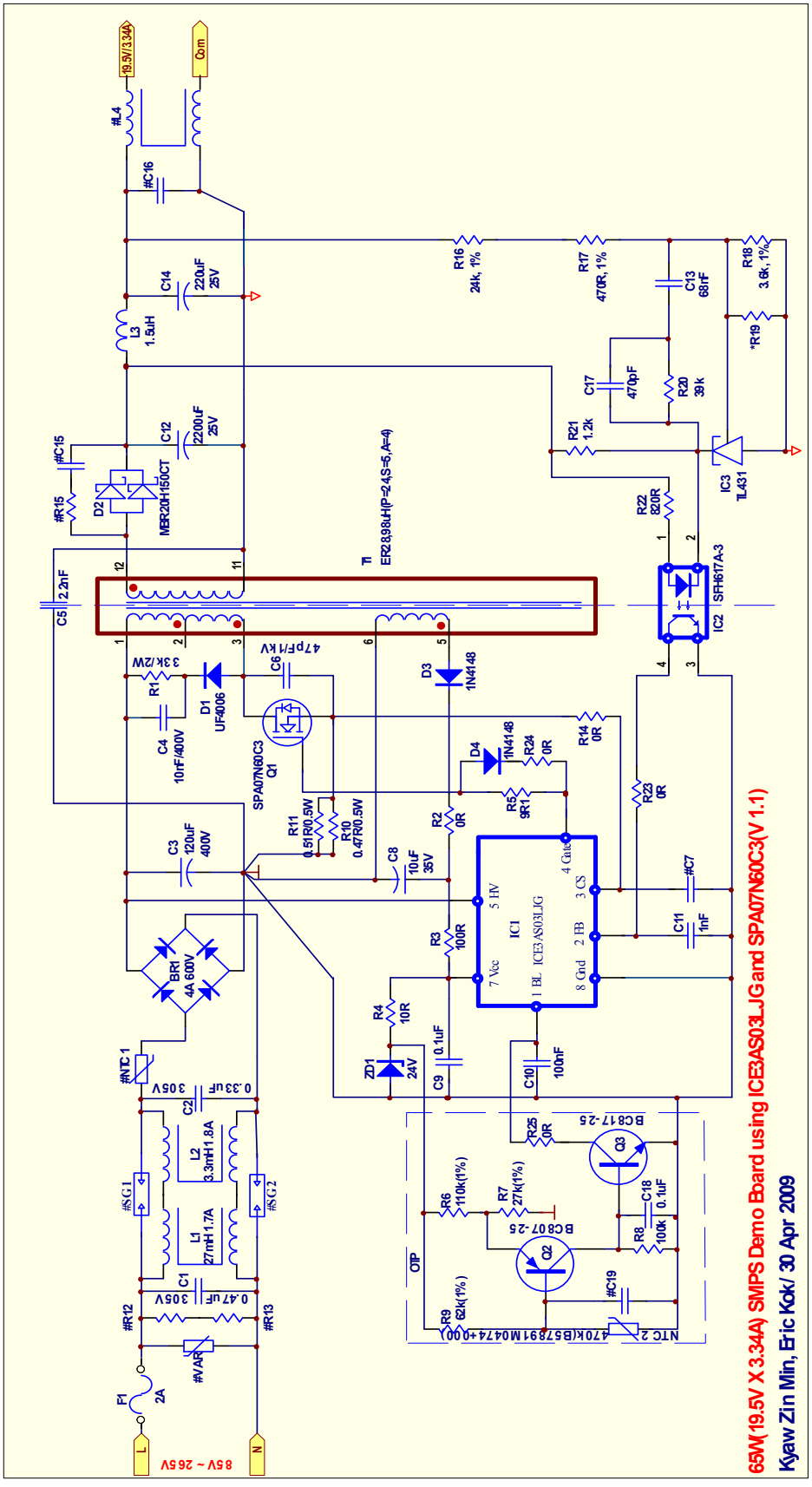

Figure 6 Typical application circuit with ICE3AS03LJG 65W 19.5V

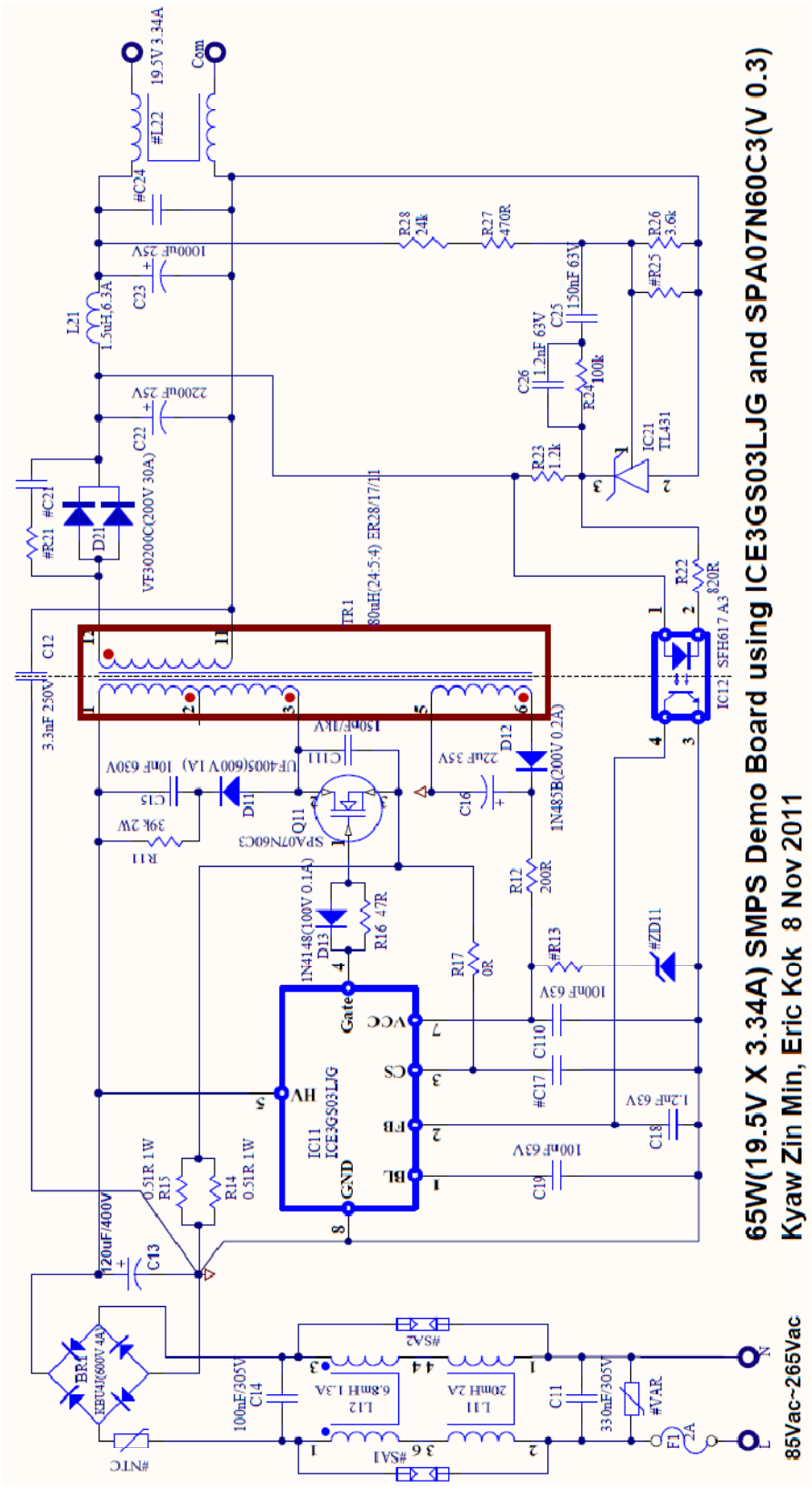

Figure 7 Typical application circuit with ICE3GS03LJG 65W 19.5V

6 Functional description and component design

6.1 Startup time

Startup time is counted from applying input voltage to IC turn on. ICE3xS03LJG has a startup cell which is connected to input bulk capacitor. When there is input voltage, the startup cell will act as a constant current source to charge up the Vcc capacitor and supply energy to the IC. When the Vcc capacitor reaches the Vcc_on threshold 18V, the IC turns on. Then the startup cell is turned off and the Vcc is supplied by the auxiliary winding. The startup time formula is expressed in equation (1).

$$t_{STARTUP} = \frac{V_{VCCon} \cdot C_{Vcc}}{I_{VCCCharge}} \quad (1)$$

where, $I_{VCCCharge}$: average of Vcc charge current of $I_{VCCCharge2}$ and $I_{VCCCharge3}$ (0.8mA),

V_{VCCon} : IC turns on threshold (18V), C_{VCC} : Vcc capacitor

Pls refer to the datasheet for the symbol used in the equation.

6.1.1 Vcc capacitor

The minimum value of the Vcc capacitor is determined by voltage drop during the soft start time. The formula is expressed in equation (2).

$$C_{VCC} = \frac{I_{VCC\,sup\,2} \cdot t_{soft}}{V_{CCHY}} \cdot \frac{2}{3} \quad (2)$$

where, $I_{VCCCsup2}$: IC consumption current (4.2mA), t_{soft} : soft start time (20(ICE3BS03LJG) or 10ms(ICE3AS03LJG & ICE3GS03LJG)),

V_{CCHY} : Vcc turn-on/off hysteresis voltage (7.5V)

Therefore, the minimum Vcc capacitance can be 7.4μF(ICE3BS03LJG) and 3.7μF(ICE3AS03LJG). In order to give more margins, 22μF(ICE3BS03LJG) and 10μF(ICE3AS03LJG) is taken for the design. The startup time $t_{STARTUP}$ is then 0.6/0.3s. The measured start up time is 0.54/0.23 s (Figure 6). A 0.1uF filtering capacitor is always needed to add as near as possible to the Vcc pin to filter the high frequency noise.

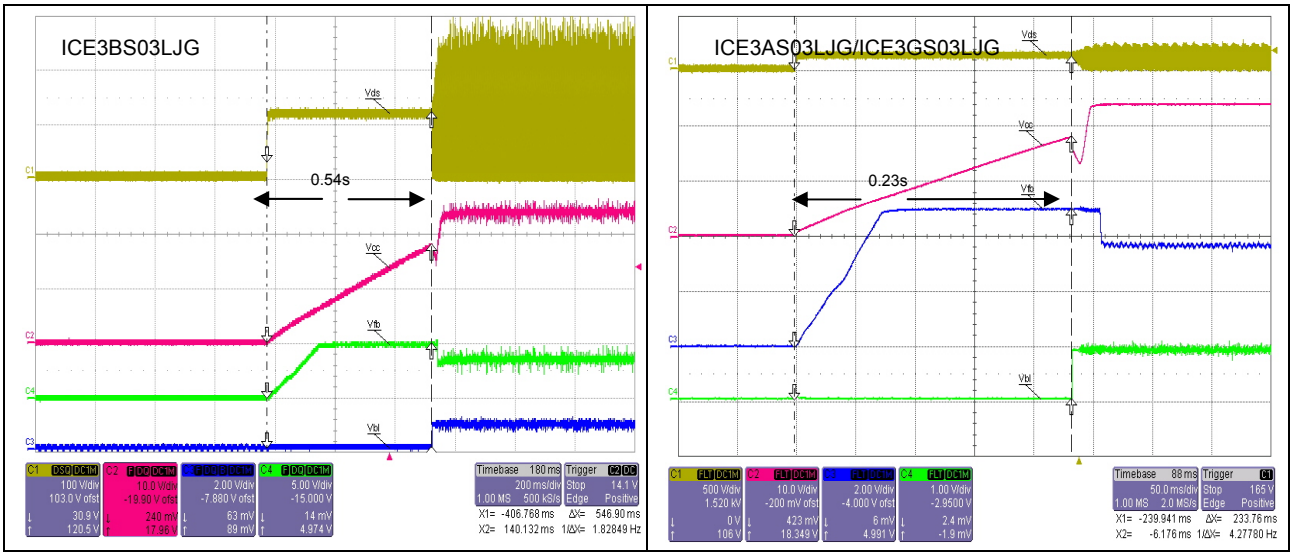

Figure 8 The startup delay time at AC line input voltage of 85Vac

Precaution : For a typical application, start up should be VCC ramps up first, other pin (such as FB pin) voltage will follow VCC voltage to ramp up. It is recommended not to have any voltage on other pins (such as FB; BA and CS) before VCC ramps up.

6.2 Soft Start

When the IC is turned on after the Startup time, a digital soft start circuit is activated. A gradually increased soft start voltage is emitted by the digital soft start circuit, which in turn releases the duty cycle gradually from 0. The duty cycle increases to maximum (which is limited by the transformer design) at the end of the soft start period. When the soft start time ends, IC goes into normal mode and the duty cycle is controlled by the FB signal. The soft start time is set at 20ms (ICE3BS03LJG) and 10ms (ICE3AS03LJG/ICE3GS03LJG) for maximum load. The soft start time is load dependent; shorter soft start time with lighter load.

Figure 9 shows the soft start behavior at 85Vac input. The primary peak current increases slowly to the maximum in the soft start period.

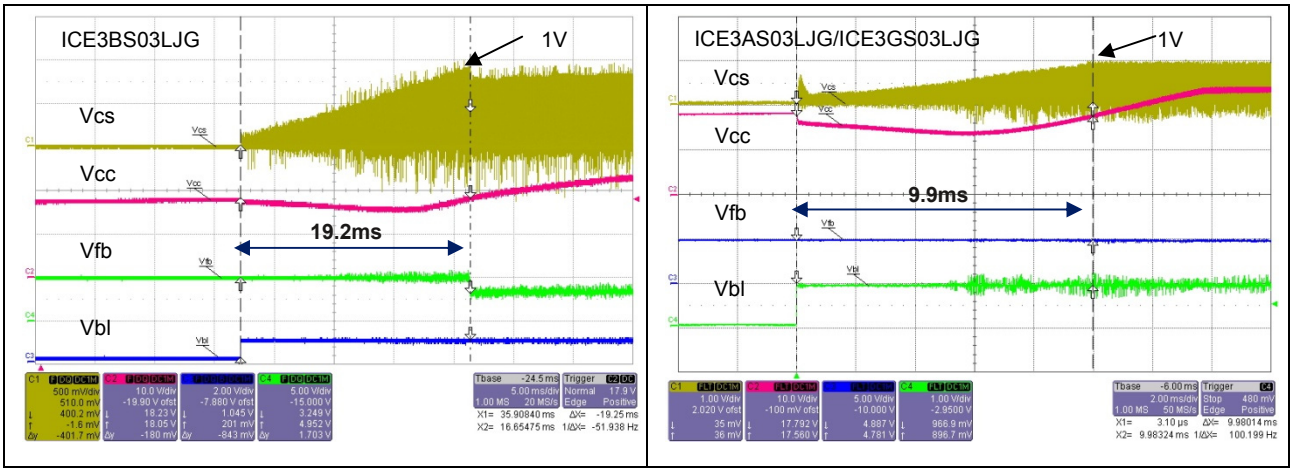

Figure 9 Soft start at AC line input voltage of 85Vac

6.3 Low standby power - Active Burst Mode

The IC will enter Active Burst Mode function at light load condition which enables the system to achieve the lowest standby power requirement of less than 100mW. Active Burst Mode means the IC is always in the active state and can therefore immediately response to any changes on the FB signal, V_{FB}.

6.3.1 Entering Active Burst Mode

Because of the current mode control scheme, the feedback voltage V_{FB} actually controls the power delivery to output. An important relationship between the V_{CS} and the V_{FB} is expressed in equation (3).

$$V_{FB} = V_{CS} \cdot A_V + V_{Offset-Ramp} \tag{3}$$

where, V_{FB}:feedback voltage, V_{CS}:current sense voltage, A_V:PWM OP gain, $V_{Offset-Ramp}$:voltage ramp offset

When the output load reduces, the feedback voltage V_{FB} drops. If the V_{FB} stays below 1.23V for 20ms, the IC enters into the Active Burst Mode. The threshold power to enter burst mode is expressed in equation (4).

$$P_{BURST\_enter} = \frac{1}{2} \cdot L_P \cdot I_p^2 \cdot f_{SW} = \frac{1}{2} \cdot L_P \cdot \left(\frac{V_{CS}}{R_{sense}}\right)^2 \cdot f_{SW} = \frac{1}{2} \cdot L_P \cdot \left(\frac{V_{FB\_enter} - V_{Offset-Ramp}}{R_{sense} \cdot A_V}\right)^2 \cdot f_{SW} \tag{4}$$

where, L_p : transformer primary inductance

R_{sense}:current sense resistance, f_{sw}:switching frequency, V_{FB_enter}:Feedback level to enter burst mode

Figure 8 shows the waveform with the load drops from nominal load to light load. After the 20ms blanking time IC goes into burst mode.

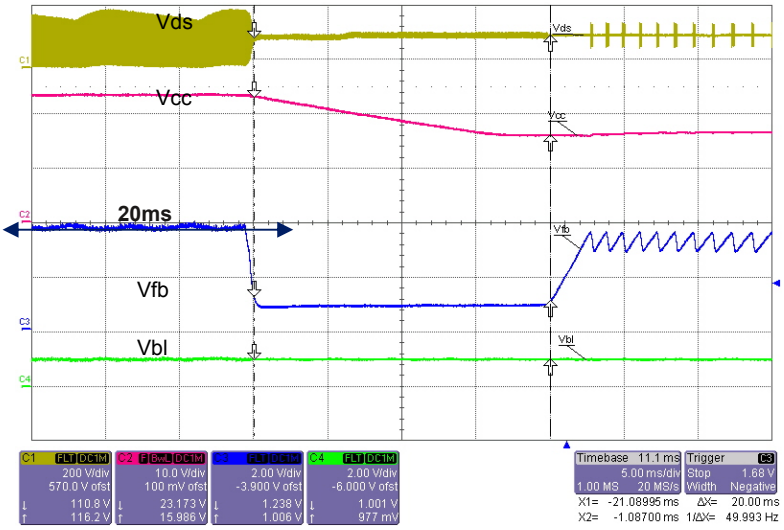

Figure 10 Entering Active Burst Mode

6.3.2 Working in Active Burst Mode

In the active burst mode, the IC is constantly monitoring the output voltage by feedback pin, V_{FB}, which controls burst duty cycle and burst frequency. The burst "ON" starts when V_{FB} reaches 3.5V and it stops when V_{FB} is dropped to 3.0V. During burst "ON", the primary current limit is set to 25% of maximum peak current (V_{CS}=0.25V) to reduce the conduction losses and to avoid audible noise. The FB voltage is changing like a saw tooth between 3.0V and 3.5V. The corresponding secondary output ripple (peak to peak) is controlled to be small. It can be calculated by equation (5).

$$V_{out\_ripple\_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB} \quad (5)$$

where, R_{opto} : series resistor with opto-coupler at secondary side (e.g. R7 in Figure 4)

R_{FB} : IC internal pull up resistor connected to FB pin (R_{FB}=15.4KΩ)

G_{opto} : current transfer gain of opto-coupler

G_{TL431} : voltage transfer gain of the loop compensation network (e.g. R2, R3,R4,R5,R6,R7,C9 & C10 in figure 5)

ΔV_{FB} : feedback voltage change (0.5V)

Usually there is a noise coupling capacitor at the FB pin to filter the switching noise and spike (e.g. C15 in Figure 4). However, if this capacitor is too large (>10nF), it would affect the normal operation of the controller. This capacitor should be as small as possible (without the capacitor is the best). In the mean time, it is found that this filter capacitor will also affect the output ripple voltage during burst mode; larger capacitance will get larger ripple voltage and smaller capacitance get lower ripple voltage.

Figure 11 is the output ripple waveform of the 60W demo board. The burst ripple voltage is about 50mV (exclude switching spikes).

Figure 11 Output ripple during Active Burst Mode at light load

6.3.3 Leaving Active Burst Mode

When the output load increases to be higher than the maximum burst power, P_{burst_max}, V_{out} will drop a little bit and V_{FB} will rise up fast to exceed 4.0V(ICE3BS03LJG) & 4.2V(ICE3AS03LJG/ ICE3GS03LJG). The system leaves burst mode immediately when V_{FB} reaches respective threshold voltage. Once system leaves burst mode, the current sense voltage limit, V_{CS_MAX}, is released to 1V, the feedback voltage V_{FB} swings back to the normal control level.

The leaving burst power threshold is (i.e. maximum power to be handled during burst operation) is expressed in equation (6).

$$P_{burst\_\max} = 0.5 \cdot L_P \cdot (0.25 \cdot i_{peak\_\max})^2 \cdot f_{SW} = 0.5 \cdot L_P \cdot (0.25 \cdot \frac{V_{CS\_\max}}{R_{sense}})^2 \cdot f_{SW} = 0.0625 \cdot P_{\max} \quad (6)$$

where, i_{peak_max} : maximum primary peak current, V_{CS_max}: current limit threshold at CS pin,

P_{max}: maximum output power

The calculated maximum power in burst mode is around 6.25% of P_{max}. However, the actual power can be higher as it would include propagation delay time.

The leave burst mode timing diagram is shown in Figure 10.

The maximum output drop during the transition can be estimated in equation (7).

$$V_{out\_drop\_\max} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot (V_{FBC4} - \frac{3.0 + 3.5}{2}) \quad (7)$$

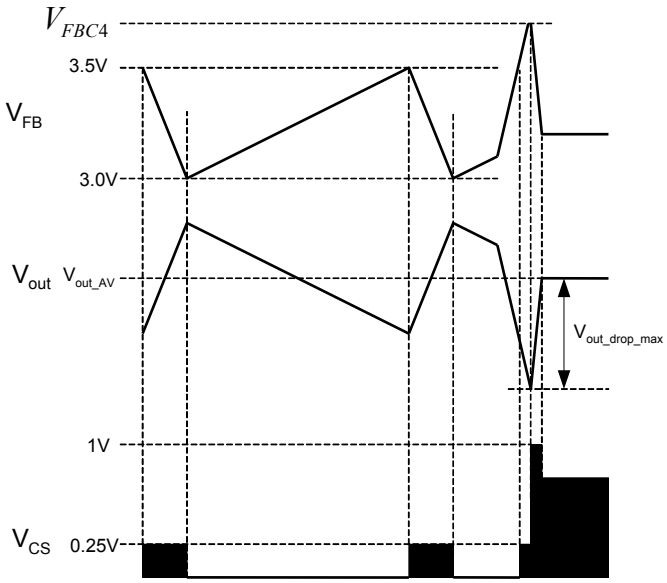

Figure 12 Timing diagram of leaving burst mode

Figure 13 is the captured waveform when there is a load jump from light load to full load. The output ripple drop during the transition is about 141mV (Figure 13 right).

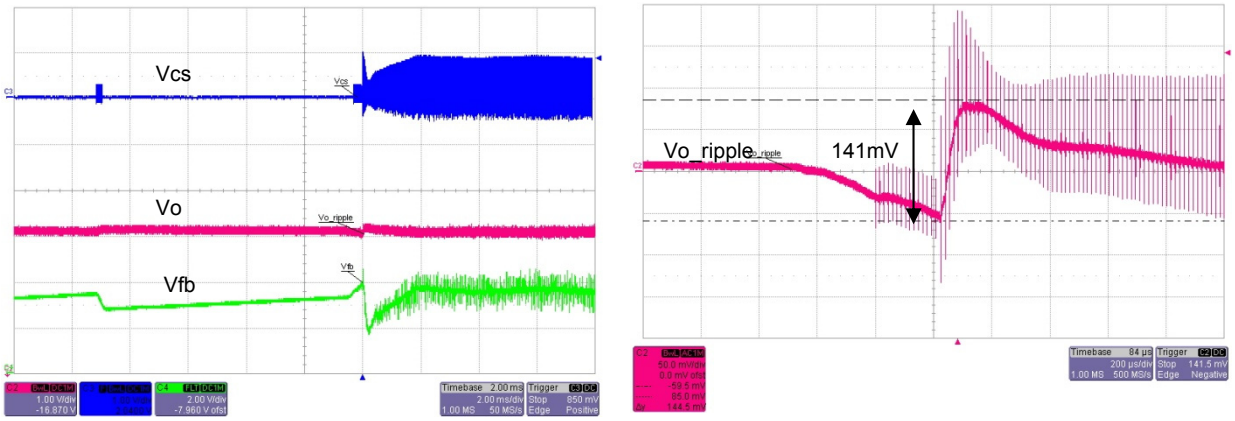

Figure 13 Leaving burst mode waveform; Vfb, Vcs and Vo (left); Vo_ripple (right)

6.3.4 Minimum V_{CC} supply voltage during burst mode

It is particularly important that the Vcc voltage must stay above V_{VCCoff} (i.e. 10.5V). Otherwise, the expected low standby power cannot be achieved. The IC will go into auto-restart mode instead of Active Burst Mode. A reference Vcc circuit is presented in Figure 5, 6 & 7. This is for a low cost transformer design where the transformer coupling is not too good. Thus the circuit(Fig. 5) R11 and ZD1 is added to clamp the Vcc voltage exceeding 25.5V in extreme case such as high load and the Vcc OVP protection is triggered. If the transformer coupling is good, this circuit is not needed.

6.4 Low EMI noise

6.4.1 Frequency jittering

The IC is running at a fixed frequency of 65/100/130 kHz with jittering frequency at ±2.6/±4/±5.2 kHz in a switching modulation period of 4ms. This kind of frequency modulation can effectively help to obtain a low EMI noise level particularly for conducted EMI. The jittering frequency measured is shown in the Fig.14.

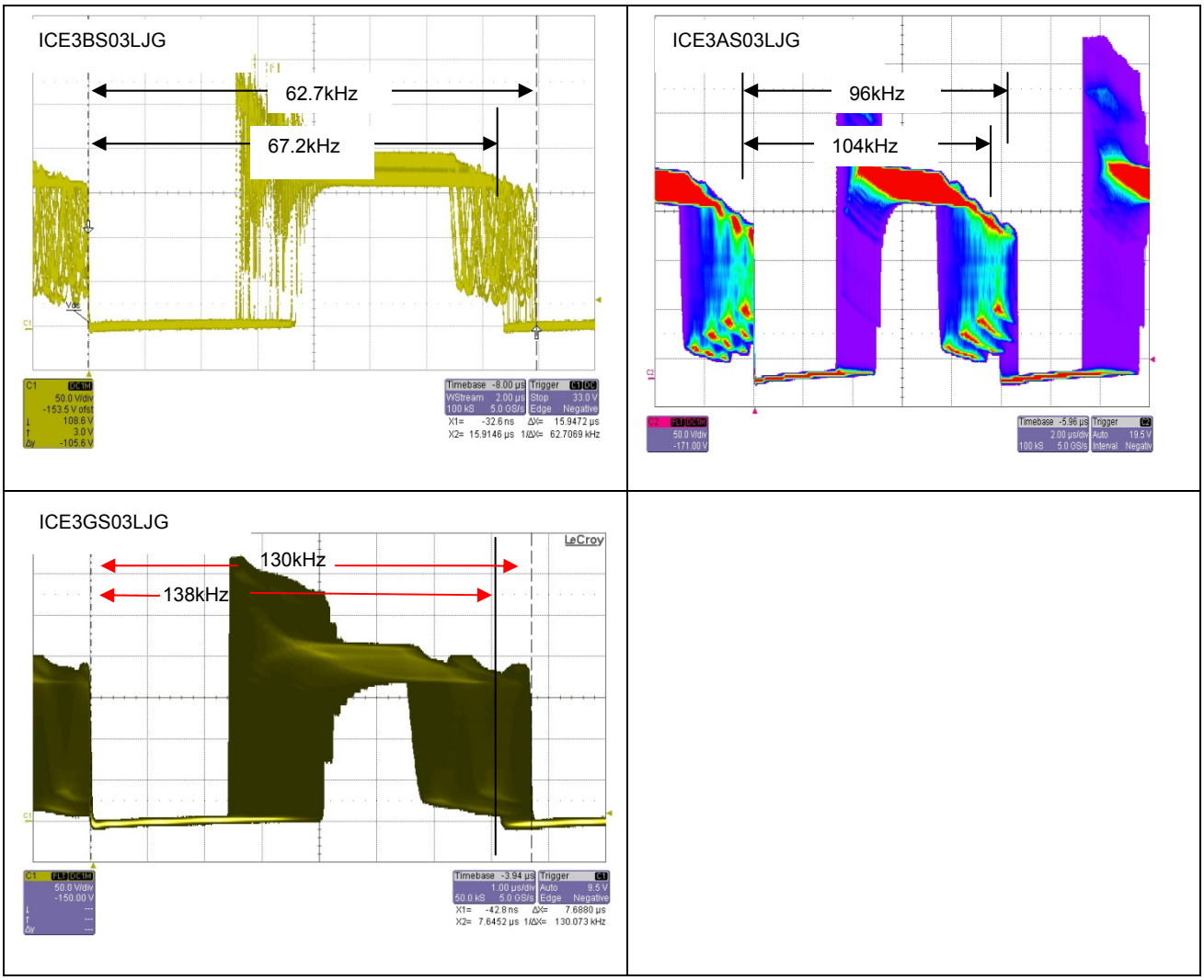

Figure 14 Switching frequency jittering (Vds)

6.4.2 Soft gate drive

The gate soft driving is to split the gate driving slope into 2 so that the MOSFET turns on speed is relatively slower comparing to a single slope drive (see Figure 15). In this way, the high ΔI/Δt noise is greatly reduced and the noise signal reflected in the EMI spectrum is also reduced.

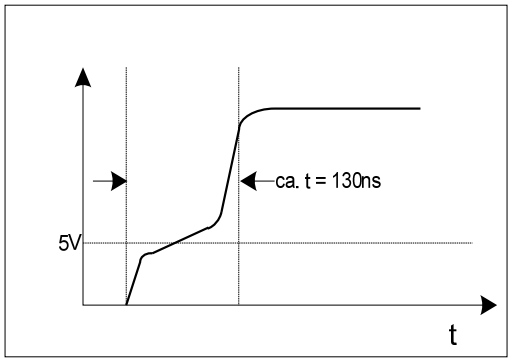

Figure 15 Soft gate drive waveform

6.4.3 Other suggestions to solve EMI issue

Some more suggestions to improve the EMI performance and is listed below.

1. Add capacitor (Cds) at the drain source pin (refer to Figure 16): it can slow down the turn off speed of the MOSFET and the high ΔV/Δt noise will be reduced and so is the EMI noise. The drawback is more energy will be dissipated due to slower turn off speed of MOSFET.
2. Adjust the turn on (R9) and turn off (R13 and D4) gate series resistor (refer to figure 16) : it can fine tune the turn on and turn off speed of the MOSFET so that the EMI noise in some particular frequency can be reduced. The drawback is it would dissipate more energy with slower turn on/off speed of MOSFET.
3. Add snubber circuit to the output rectifier : Most of the radiated EMI noise comes out from the output of the system esp. for a system with output cable. Adding snubber circuit (Rs and Cs) to the output rectifier is a more direct way to suppress those EMI noise (refer to Figure 17).
4. Add output common mode choke (L3) to the output : similar to item 3, adding the output common mode choke can help to reduce the noise of the radiated EMI emission (refer to Figure 17).

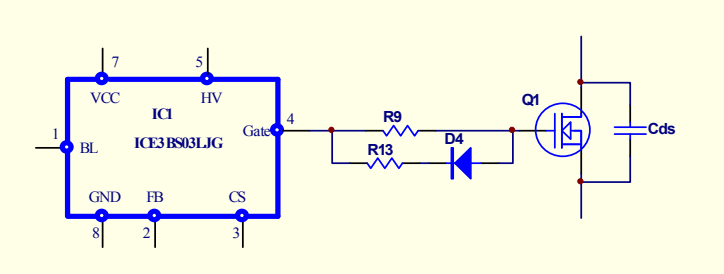

Figure 16 Drain-source capacitor and turn on/off drive resistor

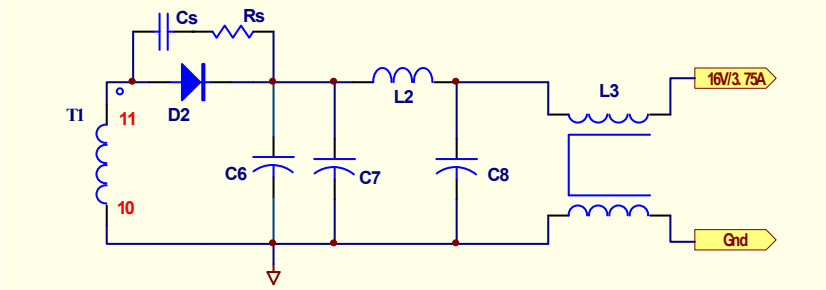

Figure 17 Output rectifier snubber and output common mode choke

6.5 Gate drive capability

The IC is designed for medium power supply. The target gate drive capability is 680pF. For higher power application or larger input capacitance MOSFET, a drive buffer circuit (Qb1, Qb2, Rb1 and Rb2) should be added. It is showed in Figure 18.

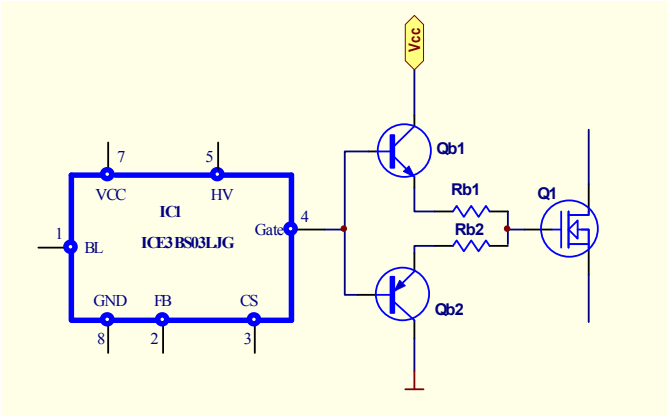

Figure 18 Gate drive buffer for larger MOSFET

6.6 Tight control in maximum power - Propagation delay compensation

The maximum power of the system is changed with the input voltage; higher voltage got higher maximum power. This is due to the propagation delay of the IC and the different rise time of the primary current under different input voltage. The propagation delay time is around 200ns. But if the primary current rise time is faster, the maximum power will increase. The power difference can be as high as >14% between high line and low line. In order to make the maximum power control become tight, a propagation delay compensation network is implemented so that the power difference is greatly reduced to best around 2%. Figure 19 shows the compensation scheme of the IC. The equation (8) explains the rate of change of the current sense voltage is directly proportional to the input voltage and current sense resistor. For a DCM operation, the operating range for the dV_{sense}/dt is from 0.1 to 0.7. It can show in Figure 15 that higher dV_{sense}/dt will give more compensation; i.e. lower value of V_{sense}.

$$\frac{dI_p}{dt} = \frac{V_{in}}{L_p} \Rightarrow R_{sense} \cdot \frac{dI_p}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \Rightarrow \frac{dV_{sense}}{dt} = R_{sense} \cdot \frac{V_{in}}{L_p} \quad (8)$$

where, I_p : primary peak current, V_{in} : input voltage, L_p : primary inductance of the transformer,

V_{sense} : current sense voltage, R_{sense} : current sense resistor

The measured maximum power for the 60W demo boards shows an output power difference of around +/- 3% between 85Vac and 265Vac input. This function is limited to discontinuous conduction mode flyback converter only.

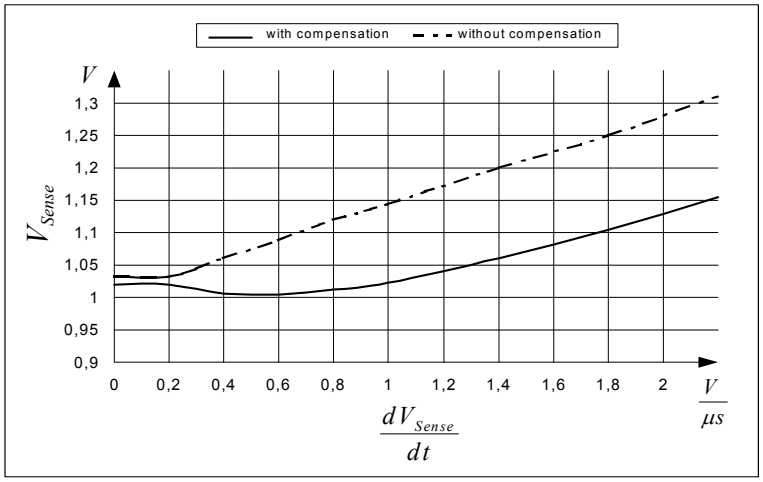

Figure 19 Propagation delay compensation curve

6.7 Protection Features

ICE3xS03LJG provides all the necessary protections to ensure the system is operating safely. Two kinds of protection are provided; auto-restart and latch off. The auto restart protections include over-load, open loop, Vcc under-voltage, short opto-coupler, etc. For those more severe faults such as Vcc over-voltage, over-temperature, short winding, etc., it goes into latch off protection. Once it enters the latch off protection, the Vcc voltage needs to drop below 6.23V before it can be reset to normal operation. There is a flexible protection enable pin which can fulfill the custom-made protections requirement such as output over voltage, MOSFET over temperature, etc. The protection is simply triggered by pulling down the BL pin to be < $\mathbf{V_{LE}}$ and the IC will go into latch off mode. A list of protections and the failure conditions is showed in Table 1.

Protection function		Failure condition	Protection Mode
Vcc Overvoltage	ICE3AS03LJG	V_{CC} > 25.5V & last for (120+25)µs (both normal & burst mode)	Latch Off
	ICE3BS03LJG	V_{CC} > 25.5V & last for (120+25)µs (normal mode only)	
	ICE3GS03LJG	V_{CC} > 25.5V & last for (120+30)µs (both normal & burst mode)	
Over-temperature (controller junction)		T_J > 130°C	Latch Off
Short Winding/Short Diode		V_{CS} > 1.66V & last for 190ns	Latch Off
Latch enable	ICE3AS03LJG	V_{BL} < 0.33V & last for 25µs	Latch Off
	ICE3BS03LJG	V_{BL} < 0.25V & last for 30µs	
	ICE3GS03LJG	V_{BL} < 0.33V & last for 30µs	
Over-load / Open loop	ICE3AS03LJG ICE3GS03LJG	V_{FB} > 4.2V and V_{BK} > 4.0V (Blanking time counted from charging V_{BK} from 0.9V to 4.0V)	Auto Restart
	ICE3BS03LJG	V_{FB} > 4.0V and V_{BK} > 4.0V (Blanking time counted from charging V_{BK} from 0.9V to 4.0V)	
Vcc Under-voltage / short Opto-coupler		V_{CC} < 10.5V	Auto Restart

Table 1 Protection functions and failure conditions

6.7.1 Auto Restart Protection Mode

When the failure condition meets the auto restart protection mode, the IC will go into auto-restart. The switching pulse will stop. Then the Vcc voltage will drop. When the Vcc voltage drops to 10.5V, the startup cell will turn on again. The Vcc voltage is then charged up. When it hits 18V, the IC will turn on and the startup cell will turn off. It would then start the startup phase with soft start. After the startup phase the failure condition is checked to determine whether the fault persists. If the fault is removed, it will go to normal operation. Otherwise, the IC will repeat the auto restart protection and the switching pulse stop again.

Figure 20 shows the switching waveform of the V_{CC} and the feedback voltage V_{FB} when the output is overloaded by shorting the outputs. The IC is turned on at V_{CC} = 18V. After going through the startup phase, IC is off again due to the presence of the fault. V_{CC} is discharged until 10.5V. Then, the Startup Cell is activated again to charge up capacitor at V_{CC} that initiates another restart cycle.

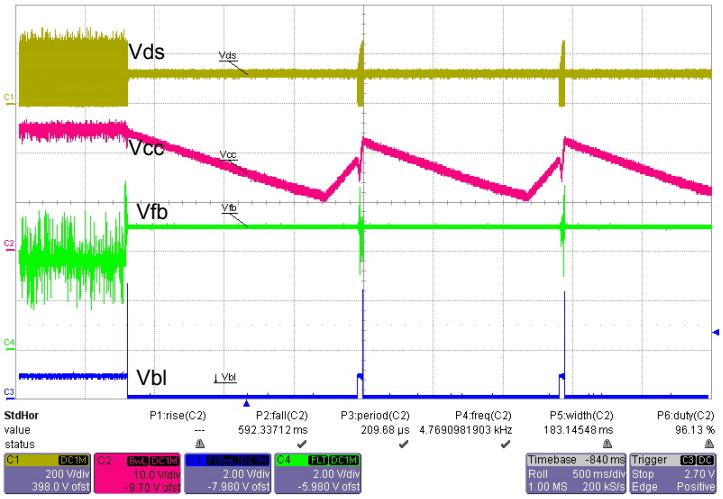

Figure 20 Auto Restart Mode (without extended blanking time)

6.7.2 Latch off Protection Mode

In case of Latched Off Protection Mode, there is no new startup phase any more. Once Latched Off Mode is entered, the internal Voltage Reference is switched off in order to reduce the current consumption of the IC. In this stage only the UVLO is working which switches on/off the startup cell at V_{CCoff}/V_{CCon}. Latched Off Mode can only be reset when AC line input is plugged out and V_{CC} is discharged to be lower than 6.23V. Figure 21 shows the Vcc waveform during latch off mode.

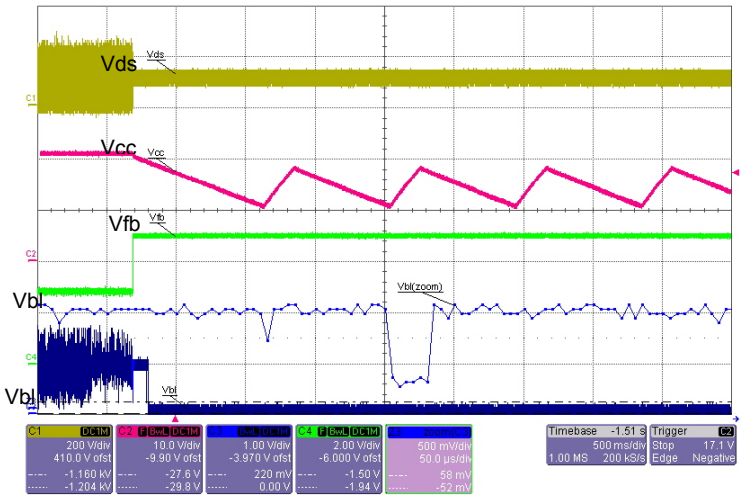

Figure 21 Latch off Mode (V_{BL} < V_{LE})

6.7.3 Blanking Time for over load protection

The IC controller provides a blanking window before entering into the auto restart mode due to output overload/short circuit. The purpose is to ensure that the system will not enter protection mode unintentionally. There are 2 kinds of the blanking time; basic and the extendable. The basic one is a built-in feature which is set at 20ms. The extendable one is to extend the basic one with a user defined additional blanking time. The extendable blanking time can be achieved by adding a capacitor, C_{BK} to the BL pin. When there is over load occurred (V_{FB} > V_{FBC4}), the C_{BK} capacitor will be charged up by an constant current source, I_{BK} (13uA) from 0.9V to 4.0V. Then the auto restart protection will be activated. The charging time from 0.9V to 4.0V to the C_{BK} capacitor is the extended blanking time. The total blanking time is the addition of the basic and the extended blanking time.

$$T_{blanking} = Basic + Extended = 20ms + \frac{(4.0-0.9)*C_{BK}}{I_{BK}} = 20ms + 238461.5*C_{BK} \quad (9)$$

The measured total blanking time showing in Figure 23 is 42ms using C_{BK}=0.1uF.

In case of output overload or short circuit, the transferred power during the blanking period is limited to the maximum power defined by the value of the sense resistor R_{sense}.

The noise level in BL pin can be quite high particularly in some high power application. In order to avoid mis-triggering of other protection features, it is recommended to add a minimum 100pF filter capacitor at BL pin to filter the noise.

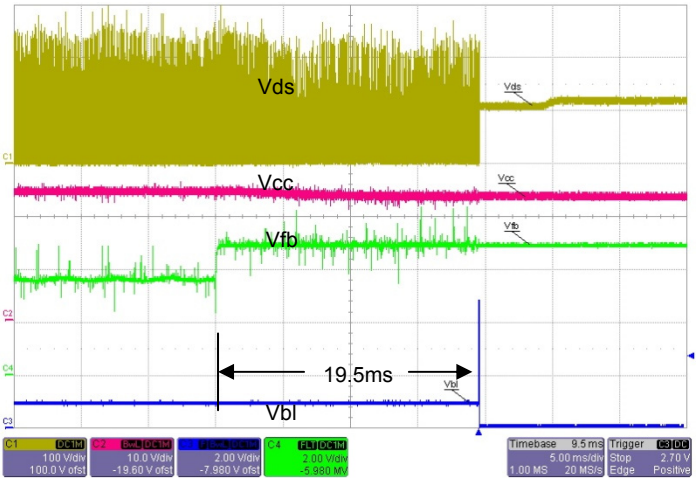

Figure 22 blanking window for output over load protection (basic blanking time)

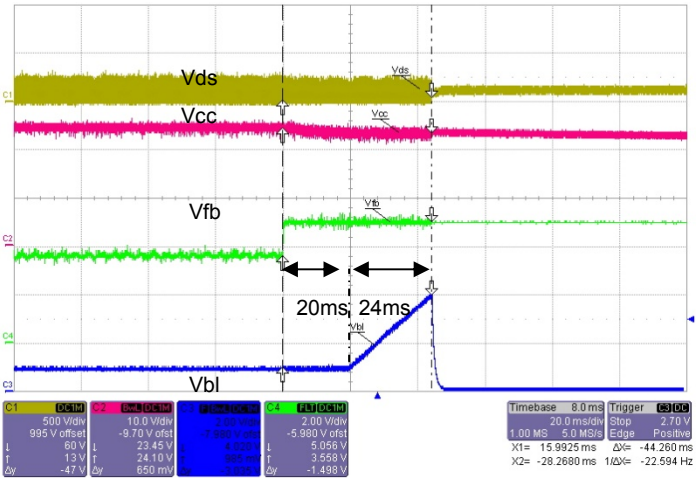

Figure 23 blanking window for output overload protection (extended blanking time=24ms with C_{BK}=0.1uF)

6.7.4 User defined protections by external protection enable pin

Although there are lots of protection conditions defined in the IC, customer still can have some tailor-made protection for the application needs. Some suggested protection circuits are recommended below.

1. Output over voltage : Figure 24 shows the output OVP latch circuit.
2. MOSFET over temperature : Figure 25 is an over temperature latch circuit. The thermistor R_{t2} is glued to the hot component such as MOSFET to protect the device to be over heated.

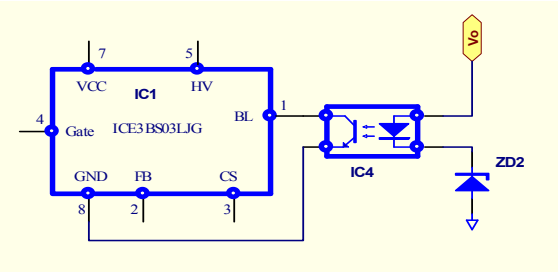

Figure 24 Output OVP circuit

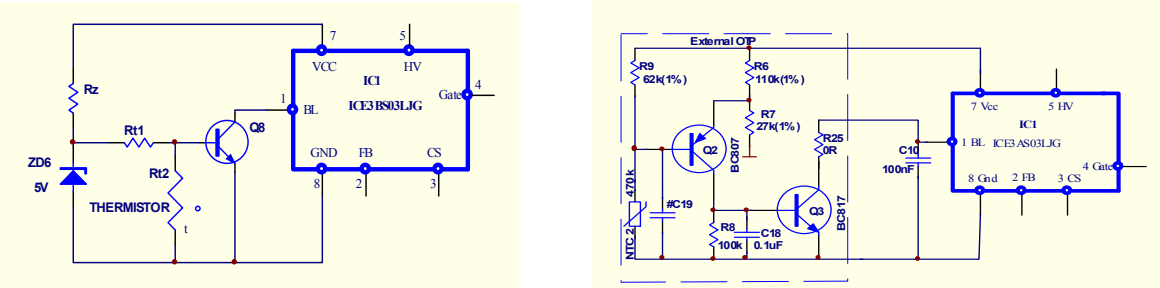

Figure 25 OTP circuit

7 Layout Recommendation

In order to get the optimized performance of the fixed frequency PWM controller ICE3GS03LJG, the grounding of the PCB layout must be connected carefully. From the circuit diagram in Figure 7, it indicates that the grounding for the controller can be split into several groups; signal ground, Vcc ground, Current sense resistor ground and EMI return ground. All the split grounds should be “star” connected to the bulk capacitor ground directly. The split grounds are described as below.

- Signal ground includes all small signal grounds connecting to the controller GND pin such as filter capacitor ground C17, C18, C19, C110 and opto-coupler ground.
- Vcc ground includes the Vcc capacitor ground C16 and the auxiliary winding ground, pin 5 of the power transformer.
- Current Sense resistor ground includes current sense resistor R14 and R15.
- EMI return ground includes Y capacitor C12.

8 FF PWM controller F3 version 3 (S03) portfolio

Device	Package	HV	Frequency / kHz
ICE3BS03LJG	PG-DSO-8	500V	65
ICE3AS03LJG	PG-DSO-8	500V	100
ICE3GS03LJG	PG-DSO-8	500V	130

9 Useful formula for the SMPS design

Transformer calculation (DCM flyback)	
Input data	Vin_min = 90Vdc, Vin_max = 380Vdc, Vds_max = 470V for 600V MOSFET, Vds_max = 650V for 800V MOSFET, *Dmax* ≤ 50%
Turn ratio	$Nratio = \frac{Vds\_\max - Vin\_\max}{Vout + Vdiode}$
Maximum Duty ratio	$D\max = \frac{(Vout + Vdiode) \cdot Nratio}{Vin\_\min + (Vout + Vdiode) \cdot Nratio}$
Primary Inductance	$Lp \le \frac{(Vin\_\min \cdot D\max)^2}{2 \cdot Pin \cdot fsw}$
Primary peak current	$Ip\_\max = \frac{Vin\_\min \cdot D\max}{Lp \cdot fsw}$
Primary turns	$Np \ge \frac{Ip\_\max \cdot Lp}{B\max \cdot A\min}$
Secondary turns	$Ns = \frac{Np}{Nratio}$
Auxiliary turns	$Naux = \frac{Vcc + Vdiode}{Vout + Vdiode} \cdot Ns$

ICE3xS03LJG external component design	
Current sense resistor	$Rsense \le \frac{Vcsth\_\max}{Ip\_\max}$
Soft start time	$tsoft = 20ms$ (ICE3BS03LJG) & $10ms$ (ICE3AS03LJG/ ICE3GS03LJG)
Vcc capacitor	$C_{VCC} = \frac{I_{VCC\sup 2} \cdot t_{soft}}{V_{CCHY}} \cdot \frac{2}{3}$
Startup time	$t_{STARTUP} = \frac{V_{VCCon} \cdot C_{Vcc}}{I_{Vcc\_Charge} - I_{Vcc\_Start}}$
Enter burst mode power	$P_{burst\_enter} = \frac{1}{2} \cdot L_P \cdot (\frac{V_{FB\_enter} - V_{Offset-Ramp}}{R_{sense} \cdot A_V})^2 \cdot f_{SW}$
Leave burst mode power	$P_{burst\_\max} = 0.0625 \cdot P_{\max}$

Output ripple during burst mode	$V_{out\_ripple\_pp} = \frac{R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}} \cdot \Delta V_{FB}$
Voltage drop when leave burst mode	$V_{out\_drop\_\max} = \frac{1.25 \cdot R_{opto}}{R_{FB} \cdot G_{opto} \cdot G_{TL431}}$
Total blanking time for over load protection	$T_{blanking} = 20ms + 238461.5 * C_{BK}$

10 References

[1] Infineon Technologies, Datasheet “F3 PWM controller ICE3BS03LJG Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell (Latched and frequency Jitter Mode)”

[2] Infineon Technologies, Datasheet “F3 PWM controller ICE3AS03LJG Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell (Latched and frequency Jitter Mode)”

[3] Infineon Technologies, Datasheet “F3 PWM controller ICE3GS03LJG Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell (Latched and frequency Jitter Mode)”

[4] Kyaw Zin Min, Eric Kok Siu Kam, Infineon Technologies, Application Note “AN-EVAL3BS03LJG, 60W 16V SMPS Evaluation Board with F3 controller ICE3BS03LJG “

[5] Kyaw Zin Min, Eric Kok Siu Kam, Infineon Technologies, Application Note “AN-EVAL3AS03LJG, 65W 19.5V SMPS Evaluation Board with F3 controller ICE3AS03LJG “

[6] Kyaw Zin Min, Eric Kok Siu Kam, Infineon Technologies, Application Note “AN-EVAL3GS03LJG, 65W 19.5V SMPS Evaluation Board with F3 controller ICE3GS03LJG “

[7] Harald Zoellinger, Rainer Kling, Infineon Technologies, Application Note “AN-SMPS-ICE2xXXX-1, CoolSET® ICE2xXXXX for Off-Line Switching Mode Power supply (SMPS)”