

REF_65W_HFACF_PAG2

About this document

Scope and purpose

This document provides instructions and a quick start guide for the EZ-PD™ PAG2S-2P controller-based Type-C charger and adapter solution (REF_65W_HFACF_PAG2).

Intended audience

This document is primarily intended for EZ-PD™ PAG2S-2P high-frequency active clamp flyback (ACF) charger and adapter solution developers.



Table of contents

Table of contents

Abo	ut this document	
Tabl	le of contents	
	Introduction	
	Specifications	
3	Board overview	
4	Test setup	
4.1	-	
4.2	Power adapter tester (PAT)	
5	Quick steps for demo	11
ReferencesRefision history		



Introduction

1 Introduction

The Active Clamp Flyback (ACF) converter is a popular flyback topology that offers ZVS for the FETs. This topology is suitable for higher frequency operation than the QR flyback because of the ZVS operation. There is also a complete energy recovery in transformer leakage inductance, which is dissipated in the QR flyback RCD clamp. ACF also has good electromagnetic interference (EMI) performance regarding ZVS operation and clamping of the primary FET voltage through the clamp capacitor.

There are two types of ACF control modes: Complementary (CP) and noncomplementary (NCP). In the CP mode, the main flyback and clamp switches are turned on/off alternatively to complement each other in every switching cycle, and the transformer current waveform is sinusoidal. Both the main flyback and clamp switches are under ZVS switching. In the CP mode, the switching frequency rises with load decrease. This may have an impact on light load and standby efficiency as well as EMI. Additionally, the full resonant current in the resonant tank increases the conduction loss in the transformer.

To overcome the increased conduction loss and improve the light-load efficiency, use the noncomplementary mode. This mode operates the active clamp FET so that it only turns on to accumulate enough magnetic energy to ensure the main FET ZVS operation. This way, the circulating clamp capacitor currents are mitigated to output. A few analog ACF controllers exist in the market. Some of them can only support either CP or NCP, but not both types of operation.

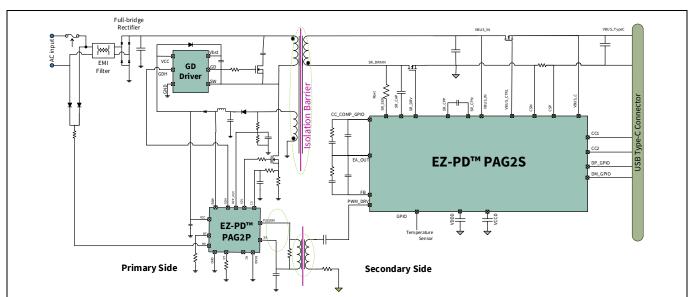


Figure 1 High-level block diagram of EZ-PD™ PAG2S-2P REF_65W_HFACF_PAG2 Solution

Infineon provides a comprehensive solution for ACF-based flyback adapters. Specifically, for AC-DC conversion, Infineon's EZ-PD™ PAG2x-based solution offers two chip solutions:

- EZ-PD™ PAG2P primary side startup controller with high and low side PWM drive
- EZ-PD™ PAG2S USB PD power adapter secondary side controller with synchronous rectification (SR)

EZ-PD™ PAG2S-2P based 65W active clamp flyback charger and adapter demonstrates this highly efficient topology.



Introduction

Table 1 Critical components bill of materials (BOM)

Designator	Description	Part number	Manufacturer Infineon Technologies	
U2	EZ-PD™ PAG2P primary side startup controller	CYPAP212A1-14SXQ		
U3 EZ-PD™ PAG2S USB PD power adapter secondary side controller		CYPAS212A1-32LQXQ	Infineon Technologies	
U1 High-side gate driver IC non-inverting		IRS25752LTRPBF	Infineon Technologies	
Q1	OptiMOS™ N-channel 30 V 19 A	BSZ0902NS	Infineon Technologies	
Q4	OptiMOS™ 6 N-channel 120 V 3.04 mΩ	ISC030N12NM6	Infineon Technologies	
Q2, Q3	700 V 150 mΩ E-mode GaN transistor	GS-065-009-6S-L	Infineon Technologies	
T1 118 µH ATQ23.7 power transformer		EF-239002	Better Magnetics Corp	
T2	Pulse edge transformer		Infineon Technologies	
C2, C3, C4, C5 Capacitor ALUM 33 µF 400 V 8x25 Radial		KCX 33 μF 400 V 8X25	Sh-ymin	
C9, C48 Aluminium organic polymer capacitors 560 µF 25 V (6.3x10)		NPX 560 μF 25 V 6.3x10	Sh-ymin	



Specifications

2 Specifications

Table 2 Test specifications

Parameter	Value	
Input voltage and frequency	100 to 240 V AC, 47 to 63 Hz	
Max output power	65 W, 20 V to 3.25 A max	
Output voltage	Fixed PDOs: 5.0 V / 3.0 A, 9.0 V / 3.0 A, 15.0 V / 3.0 A, 20.0 V / 3.25 A	
	PPS: 5 V to 11 V, 3.0 A; 5 V to 16 V, 3.0 A; 5 V to 21.0 V, 3.25 A with PPS power limit	
Peak efficiency	> 94%	
Protections	Input overvoltage protection	
	2. Input undervoltage protection	
	3. V _{BUS_C} overvoltage protection (OVP)	
	4. V _{BUS_C} undervoltage protection (UVP)	
	5. Overcurrent protection (OCP)	
	6. Short-circuit protection (SCP)	
	7. Over-temperature protection (OTP)	
	8. V _{BUS_C} to CC short protection	
Charging standards	1. USB-C PD v3.1 including programmable power supply (PPS) mode	
supported	2. Apple Charging 2.4 A	
	3. Qualcomm QC 2.0, 3.0, 4.0, 5.0	
	4. Samsung AFC	
	5. USB BC 1.2	
EMI/EMC	1. Conducted emissions, CISPR32 CLASS B, 4 dB margin at 115/220 V AC	
	2. ESD, IEC61000-4-2, ±8 kV contact, ±16 kV air, Criteria A	
	3. Surge, IEC61000-4-5, ±1 kV DM and ±2 kV CM, Criteria B	



Board overview

3 Board overview

The EZ-PD™ PAG2S-2P based 65 W active clamp flyback USB PD charger and adapter solution (REF_65W_HFACF_PAG2) shown in Figure 2 solution board is designed to meet the specifications shown in Table 2.



Figure 2 REF_65W_HFACF_PAG2 solution board

In this solution, the EZ-PD™ PAG2x operates with an optimal frequency of 150 kHz and functions as a secondary-side flyback, ACF controller, and SR controller. Additionally, a high-side driver is used externally to drive the ACF/high-side GaN FET. This solution board consists of three boards:

- Baseboard being primary board with EZ-PD™ PAG2P and other power components
- EMI Board with filters and bulk capacitors
- Secondary board with EZ-PD™ PAG2S, SR MOSFET, and Type-C connector

Figure 3 shows the schematic of EZ-PD™ PAG2S-2P based 65 W high frequency active clamp flyback charger and adapter solution.



Board overview

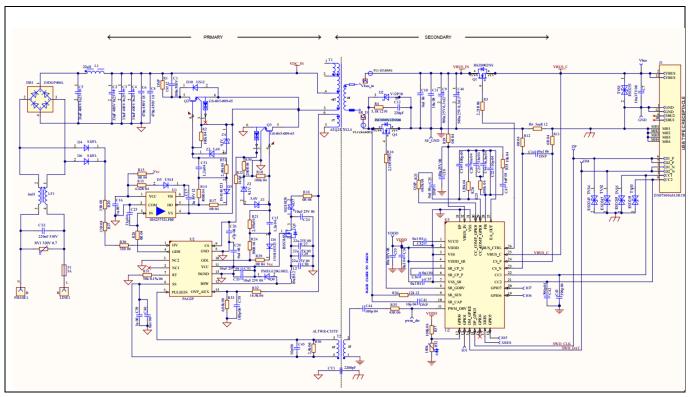


Figure 3 EZ-PD™ PAG2S-2P REF_65W_HFACF_PAG2 Schematic

EZ-PD™ PAG2S uses PSoC™ MiniProg4 (CY8CKIT-005) to program the EZ-PD™ controllers. The EZ-PD™ PAG2S-based board uses a PSoC™ MiniProg4 five-pin connection and a JTAG to Type-C connector board. In this way, one can simply program the EZ-PD™ PAG2S-2P based 65 W active clamp flyback charger and adapter board using a Type-C connector.



Figure 4 PSoC™ MiniProg4 (CY8CKIT-005) Programmer Kit

Programming interface and settings

The PSoC™ Programmer software is used as a programming interface to program the firmware (.hex file) in an EZ-PD™ PAG2S-based board. For programming, select the "CCGx" platform and update the settings as shown in Figure 5.



Board overview

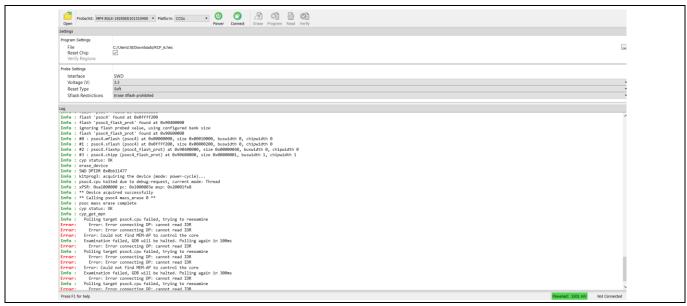


Figure 5 Programming interface to program EZ-PD™ PAG2S board



Test setup

4 Test setup

Figure 6 shows the test setup to capture the electrical data of the DUT. The following is the optimal setup to capture efficiency by capturing:

- Input power using a power meter
- Output power using high-resolution output multimeters

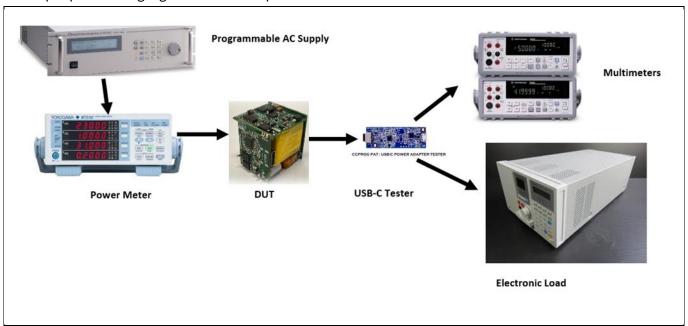


Figure 6 Test equipment connected to the standalone REF_65W_HFACF_PAG2 board

4.1 Test equipment

Table 3 shows the test equipment to measure performance parameters such as efficiency, ripple, regulation, and transient response.

Table 3 Test equipment details

Test setup	Description	
Programmable AC source	Chroma 61501	
AC power meter	Yokogawa WT310E	
PAT tester	USBCEE PAT	
Electronic load	Chroma 63102A	
Multimeters	Keysight 34465A	



Test setup

4.2 Power adapter tester (PAT)

Connect the DUT to a USB-C power adapter tester (PAT) using a USB Type-C cable. After the connection is established, the PAT UI does a PDO discovery and displays the results.

The EZ-PD™ PAG2S-2P based 65 W active clamp flyback charger and adapter solution is pre-configured with seven PDOs:

- Fixed PDOs: 5.0 V / 3.0 A; 9.0 V / 3.0 A; 15.0 V / 3.0 A; 20.0 V / 3.25 A
- **PPS**: 5 V to 11 V, 3.0 A; 5 V to 15.0 V, 3.0 A; 5 V to 21.0 V, 3.25 A (PPS power limited)

Choose a suitable pre-configured PDO or configure a new one using the EZ-PD™ Configuration Utility. Tests in the following sections use pre-configured PDOs.

To know more about the PAT tester, see USBCEE.

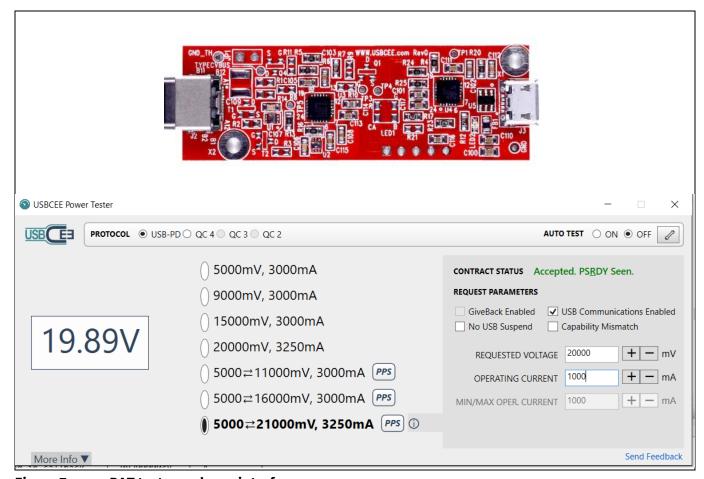


Figure 7 PAT tester and user interface



Quick steps for demo

5 Quick steps for demo

- 1. Connect the 65-W solution board to the power meter AC terminal (which is already connected to the programmable AC supply) as in Figure 6.
- 2. Connect a USB PD tester or a power adapter tester (PAT) to the port and ensure that the USB PD tester gets a successful Power Delivery contract as shown in Figure 7.
- 3. Connect the electronic load at the PAT tester load terminal as in Figure 6.
- 4. Select the desired voltage on PAT UI and ramp up the load on the electronic load.



References

References

Datasheets

- [1] CYPAP211A1-14SXI EZ-PD™ PAG2P, Primary-side startup controller
- [2] CYPAS212-32LQXQ EZ-PD™ PAG2S-AC integrated USB PD and secondary-side ACF controller



Revision history

Revision history

Document revision	Date	Description of changes
**	2024-02-15	Initial release

Trademarks

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