Whitepaper
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Infineon's recommendations and solutions for USB-C PD chargers

Debunking the most efficient 65 W fast charger designs

Abstract

The recent enhancements and technology advancements in the charger domain have made engineers face new challenges in their daily lives. Higher efficiency, smaller footprint with the same output power, or more power in the same footprint are among the key challenges in contemporary charger designs.

In this whitepaper, Infineon provides engineers with an overview of different solutions in the USB-C PD charging domain. Each of the described solutions can help engineers meet various specific design targets such as the highest efficiency, improved cost-performance, or enhanced design flexibility.

by
Tim Hu, *Director – Global Low-power SMPS Application*, Infineon Technologies,
Gautam Chinagundi, *Staff Specialist Product Marketing*, Infineon Technologies, and
Rashed Ahmed, *Principal Engineer*, Infineon Technologies

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1 Introduction

Over the last few years, the number of rechargeable battery-powered portable devices has increased substantially. But the lack of unification and standardization in the charger and adapter equipment domain led to a situation that each device required its own bulky charger and cables, inconvenient to the end-users. To solve this, recently, the USB power delivery (USB-PD) technology standard for fast-charging and data transfer gained significant importance. With the primary ambition of simplifying the end-user experience, USB-PD chargers promise a compact-sized charging solution with higher power, making charging faster and more efficient.

However, this convenience comes at the cost of higher engineering efforts. From the technology point-of-view, the unification headway poses many new challenges to the engineers while laying the foundations of a highly competitive environment for them. The latest technology and market trends in chargers and adapters push the envelope of form-factor, charging power, battery capacity, and charging time. These needs are translated into more stringent performance requirements, i.e., a significant increase in power density and efficiency. Engineering teams must fulfill these requirements and, at the same time, provide a comprehensive, customer-friendly, and high-quality solution at a competitive cost. In addition, ideally, all of these ahead of the competition to harvest the market by gaining larger market share through shorter time-to-market.

This whitepaper demonstrates the capabilities of Infineon’s available system solutions that enable high-density USB-C PD charger designs at a competitive cost. The paper also serves as an initial guideline for design engineers that need to find the best fit for their design requirements and quickly develop a highly-reliable, cost-effective, innovative USB-C PD charger solution in a timely market launch.

2 Overview of technologies and topologies for USB-C PD designs

2.1 How to choose the proper topology?

Currently, engineers can choose from different topologies for fast charger designs. Most popular within them are the following:

- Traditional flyback topology
- Soft-switching flyback topology, e.g., digital forced-frequency-resonant (FFR) converters
- Hybrid flyback topology, e.g., asymmetrical duty-cycle flyback converters
- Quasi-resonant flyback topology
- Active Clamp Flyback (ACF) topology

The flyback topology seems to be the most widely used in low-power charger designs due to its lower cost and ease of design compared to other topologies. However, since the transformer is used for energy storage in a traditional flyback topology, this results in a larger transformer. The result is limiting the maximum achievable power density. The solution to overcome this limitation coming from the transformer size is to increase the switching frequency. But as the frequency increases, the energy losses in the parasitic elements (mainly transformer leakage inductance) and MOSFET capacitance become more significant. To resolve the issues caused by the higher switching frequencies, different variants of the **soft-switching flyback topology** have become popular, such as the digital forced-frequency-resonant (FFR) enabled by the XDP™ XDPS21071[1] and **XDP™ XDPS21081** digital controllers from Infineon's portfolio.

In recent years, new technologies such as GaN-based devices together with soft-switching flybacks seemed to be able to achieve higher switching frequencies, solving the two main limitations of high-power-density adapters: recycling energy from the parasitic components while reducing the size of the transformer. Nevertheless, the higher switching frequencies are not exempt from problems. Faster switching frequencies raise new EMI challenges. Another limitation of this solution is the higher cost of the "special" devices – GaN power switch and zero-voltage switching (ZVS) controller - in a market where the total system cost is susceptible.

A new, creatively-titled **asymmetrical duty-cycle flyback** converter is a **hybrid** between a flyback and a forward converter. It addresses the main problems related to high-density adapters operating at moderate switching frequencies. The hybrid topology can ensure ZVS and zero-current switching (ZCS) over line and load. It lays the foundation for the highest conversion efficiency by using the magnetization current to achieve ZVS on the primary-side half-bridge and ZCS on the synchronous rectification switch.

Compared with other flyback topologies, hybrid flyback transformers need to store less energy, thus reducing the charger's size. Hybrid flyback can achieve full ZVS operation on the primary side and full

[1] XDP™ XDPS21071 product is discontinued. Please check the replacement product XDP™ XDPS21081

ZCS operation on the secondary side, and the leakage energy is recycled, thereby achieving high efficiency. The output voltage will change with the duty cycle (as shown in the below formula). For hybrid flyback, it's much easier to achieve a wide voltage range output, which overcomes the limitations of LLC topology in wide voltage output applications:

$$V_{out} = D \cdot V_{in} \cdot L_m / N / (L_m + L_r)$$

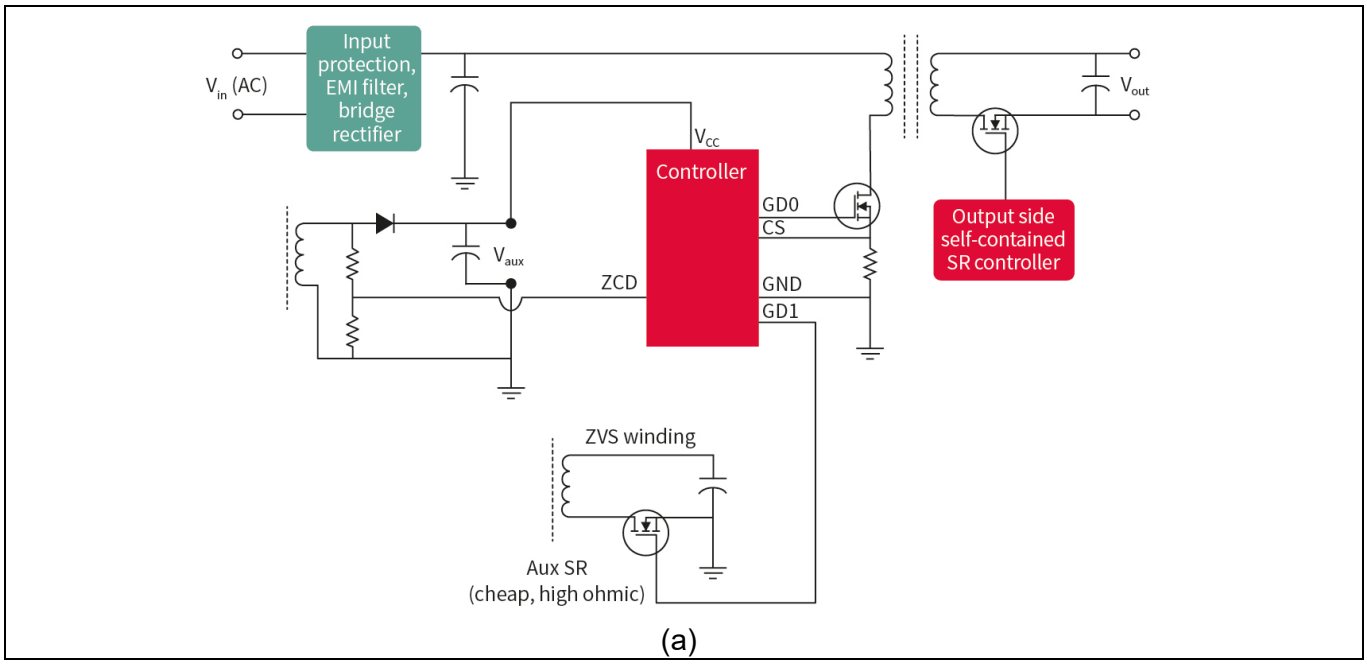
where V_{out}: output voltage, D: duty cycle, V_{in}: input voltage, L_{in}: transformer inductance, N: transformer turn ratio, and L_r: transformer leakage inductance

Due to its cost-performance ratio, **quasi-resonant (QR) flyback topology** is also widely used in the charger market. With this topology, valley switching can reduce switching losses, and this single-magnetic-component topology can also bring cost advantages. Although the QR needs to be improved with the increase of the charger's power, the zero-voltage turn-on in the full voltage input range cannot be guaranteed. Especially during the high voltage input period, the high drain-source voltage (V_{DS}) of the MOSFET results in significant switching power loss; hence high-frequency operation is not supported. Due to the substantial difference in operating frequency between the high- and low-voltage input, it isn't easy to optimize the transformer design.

Recently, the **active clamp flyback (ACF)** topology was introduced to improve the power density in chargers. ACF uses transformer leakage energy to improve efficiency by storing this leakage energy in a capacitor clamp and then delivering it to the output later in the switching cycle. By controlling the clamp, ZVS can be achieved on the FET, further increasing efficiency by eliminating another major source of loss. This allows for higher switching frequency and a reduction in the size of the power supply. To ensure zero-voltage turn-on, a resonant circulating current is needed even under light load conditions. But this resonant circulating current will result in an additional loss that reduces the average efficiency. Like in the case of the QR flyback, the significant difference in frequency during high- and low-line input will pose challenges to transformer designs.

With the intention to optimize flyback performance, Infineon introduced the forced-frequency resonant (FFR) flyback in the industry. This topology has several outstanding performance features, including but not limited to zero voltage turn-on, fewer external components, and smaller difference in frequency during high- and low-line input operation. Figure 1 shows the topology and the ZVS operation principles. After the primary MOSFET is turned off at t_0, the synchronous rectification (SR) MOSFET will turn on slightly delayed by a short blanking time. At t_1, when the demagnetizing current ideally goes to zero, the SR MOSFET is turned off, and then the magnetizing inductance L_p and C_{eqv} oscillate. The voltage of the primary MOSFET will oscillate from $V_{bulk}+V_{ref}$ to $V_{bulk}-V_{ref}$. In case the auxiliary MOSFET is turned on at t_2, the resonant peak of the primary MOSFET will mean the magnetizing current is zero, so the $I_{\_mag}$ value will accumulate to a negative value. During this controlled ZVS on-time, the V_{DS} of the primary MOSFET is clamped to $V_{bulk}+V_{ref}$. Once the peak current reaches $I_{\_zvs\_pk}$, the auxiliary MOSFET will turn off. Since this current is stored in the magnetizing inductance and in the reverse direction, it will continue to flow in that direction and release the energy stored in C_{eqv}. A configurable $t_{ZVSdead}$ parameter controls this duration in the IC. Therefore, at t_4, the primary MOSFET's drain voltage reaches its minimum and turns

on the primary MOSFET, significantly reducing turn-on losses, which is almost ZVS. As shown in Figure 1, energy is proportional to V_{bulk}, and so is the ZVS on-time.



(a)

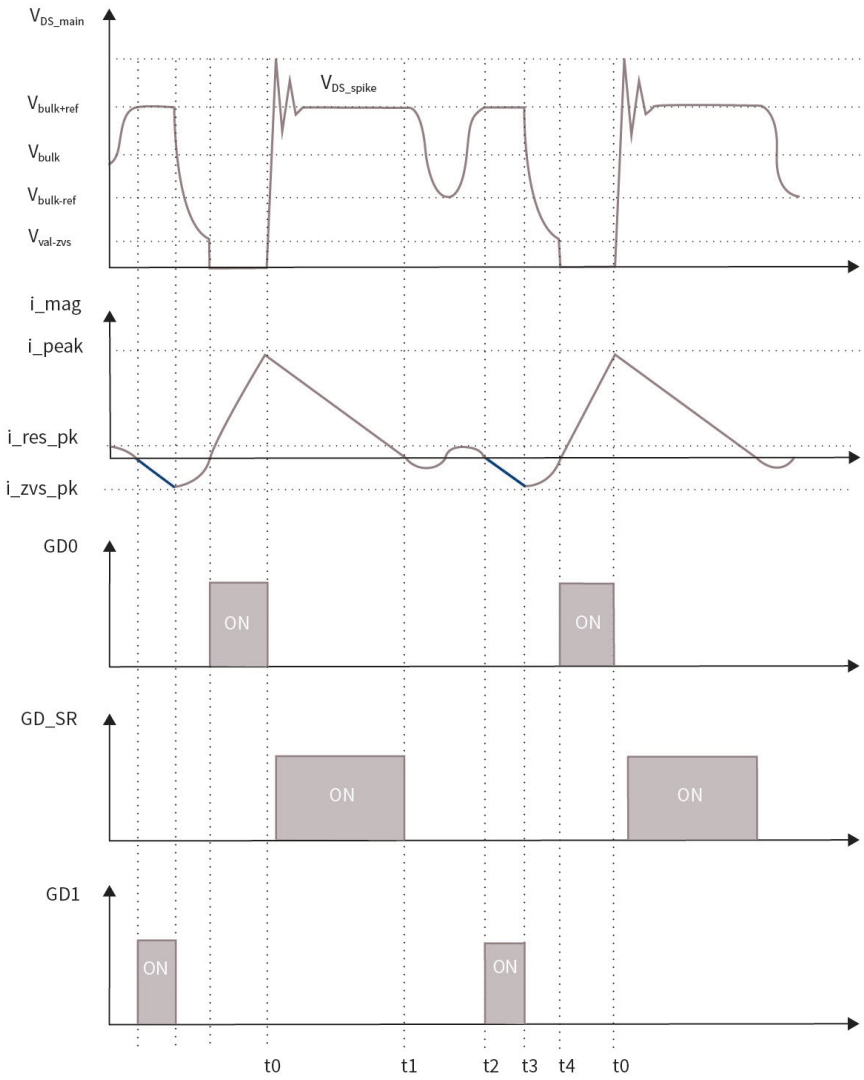


Figure 1 The recommended FFR ZVS topology (a) and the ZVS operation principles (b)

ZVS pulse insertion is based on nano-DSP core and memory info. The IC recognizes the next switching cycle period and ZVS dead-time and ZVS pulse on-time. Therefore, assuming the IC main gate turn-on time is also fixed, subtracting these two parts (the ZVS dead-time and the ZVS pulse-on time) from the switching period will decide the ZVS pulse starting point. When the CS signal reaches the current command, the main gate off-point can also be determined.

Infineon’s high-performance digital ZVS controller XDP™ XDPS21081 reference design is presented in Section 3. This 65 W reference design achieves up to 93 percent efficiency by implementing QR during low-line voltage input and FFR during high-line voltage input. When the controller is used together with **CoolMOS™** superjunction MOSFETs in a **ThinPAK** package, the charger can be placed in a compact case. In addition, the simple EMI filter design and low BOM cost can help design engineers improve charger design capabilities.

Section 4 introduces a ZVS hybrid flyback design based on Infineon’s XDP™ digital power **XDPS2201**, which can realize ZVS and ZCS under all input voltage and output current conditions. Additionally, it can

recycle the energy of the transformer leakage inductance. High-performance power MOSFETs can further contribute to achieving 94 percent efficiency for the 100 W USB-C PD design in a small, 60 mm x 40 mm x 18 mm form factor.

2.2 How to choose the right power switch?

In addition to selecting the fitting topology, choosing the suitable high-voltage MOSFET is also a key to a high-efficiency design.

Soft-switching techniques enable devices to operate in ZVS, which means that the MOSFET is turned on only after its drain-source voltage reaches 0 V (or a value close to 0 V). This strategy eliminates the turn-on loss of the device, which is typically the major contributor to the overall switching loss. Unfortunately, all high-voltage SJ MOSFETs suffer from another type of loss due to their “non-lossless” behavior of the output capacitance. This means that when the MOSFET output capacitance (C_{OSS}) is charged and subsequently discharged, some energy will be lost. Therefore, even when operating under ZVS conditions, all the energy stored in the output capacitance (E_{OSS}) will not be recovered. This phenomenon is related to the hysteretic behavior of the C_{OSS}, as shown in Figure 2, which can be observed performing a C_{OSS} charge/discharge cycle with a large signal measurement. This is why these losses are commonly known as C_{OSS} hysteresis losses ($E_{OSS,hys}$).

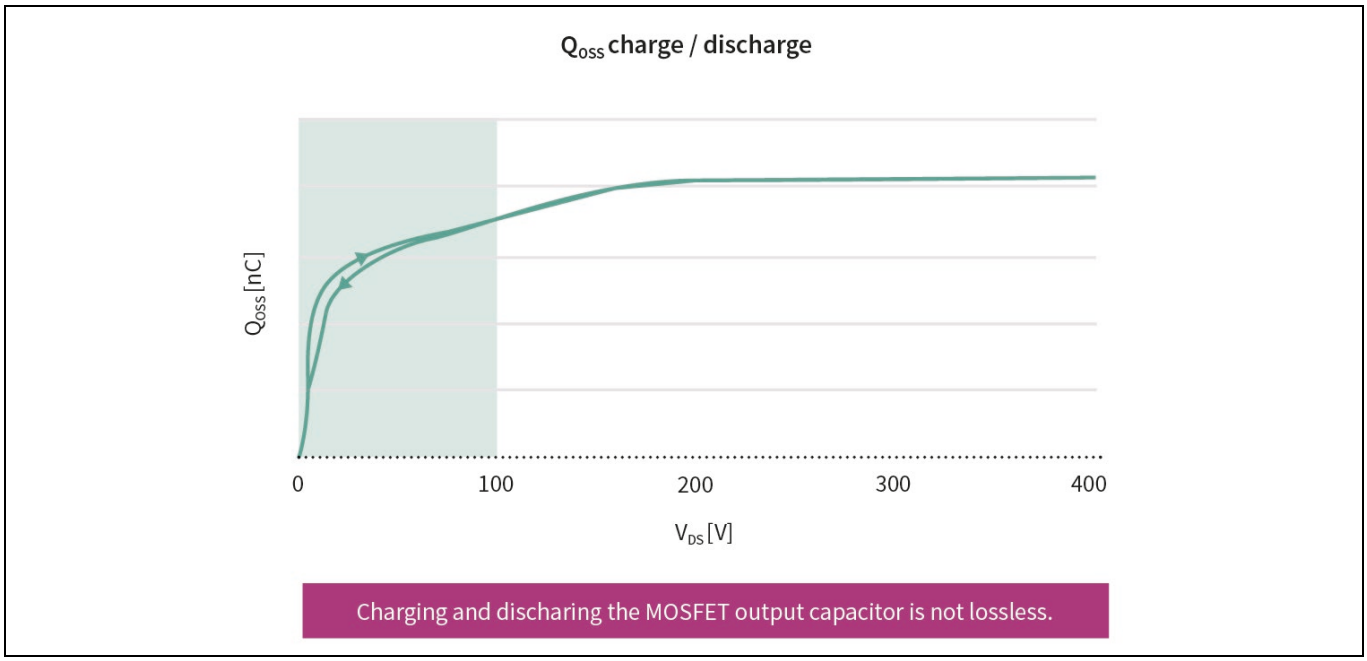


Figure 2 The C_{OSS} charge/discharge cycle of an SJ MOSFET

Thanks to the latest advancements in Infineon’s state-of-the-art SJ technology, the **CoolMOS™ PFD7** series has lower hysteresis losses than previous generations, improving efficiency further.

The new **600 V CoolMOS™ PFD7** series and the **700/800 V CoolMOS™ P7** series offer cost-competitiveness with improved technology that reduces switching- and conduction losses. Also, an

integrated gate-source Zener diode is featured for enhanced ESD protection and system reliability during operation.

By having a lower total gate charge (Q_g) as well as lower energy storage in the MOSFET output capacitance (which needs to be burned off every cycle during hard switching (E_{OSS})), the switching losses of the MOSFETs are improved. By reducing these total charges, which are dissipated in each switching cycle, the efficiency of the system at light loads can be improved.

Improved technology can reduce the conduction losses of the device, thereby improving the temperature coefficient of the device. The $R_{DS(on)}$ of a MOSFET is typically rated at 25°C, but the junction temperature will be higher during operation. Compared with the previous-generation C6 technology, the PFD7/P7 series offers a 10 percent reduction in $R_{DS(on)}$ at 100°C, thereby reducing the conduction losses. Although the common industry standard is that the $R_{DS(on)}$ is 2x the datasheet value at 125°C, now, with this latest technology, it is reduced to 1.9x only.

With these improvements in conduction losses and switching losses, the new technology provides the possibility to shift to higher $R_{DS(on)}$ MOSFETs to reduce overall system costs or increase overall system switching frequency to reduce the form factor and the cost of passive components.

Right-fit package selection helps to improve the performance of the USB-C PD charger solution. Let’s take the cost-effective **SOT-223** package as an example. It’s the perfect drop-in replacement for a **DPAK** package at a lower cost. Figure 3 shows that the SOT-223 package can achieve thermal performance similar to a DPAK package.

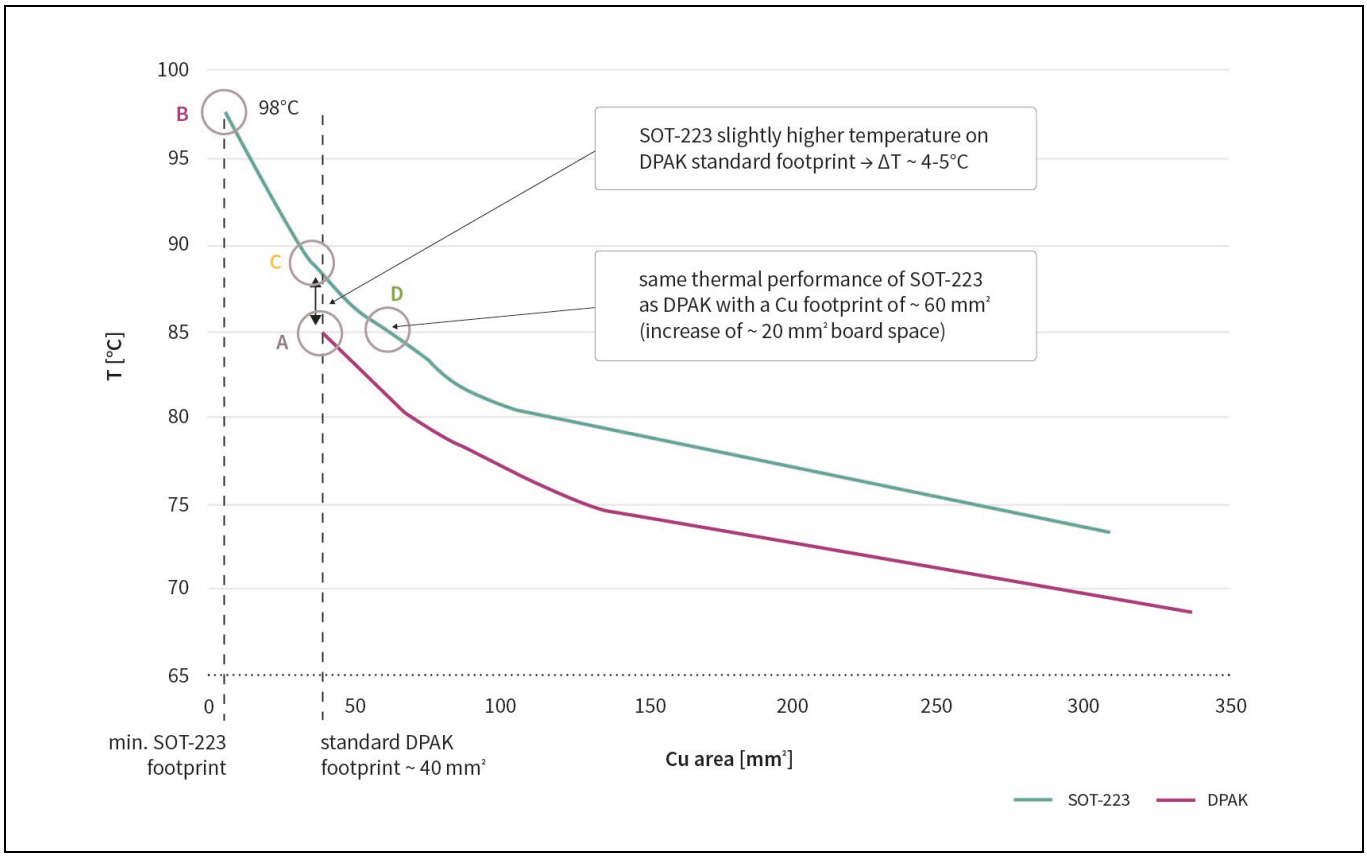


Figure 3 Thermal simulation of junction temperature at 250 mW and an ambient temperature of 55°C

In charger designs, the total loop inductance of the MOSFET (consisting of the gate-source and drain-source inductances) is important to prevent the MOSFET from turning on again and also to reduce electromagnetic interference (EMI). Compared with the DPAK or the FullPAK THD packages, ThinPAK offers a reduction in gate-, drain- and source inductances (shown in Figure 4). Compared with the DPAK package, the internal source inductance of the ThinPAK is also reduced by 63 percent.

The total gate-source inductance ($L_{gate\_loop} = L_{source} + L_{gate}$) is important to reduce the ringing on the MOSFET gate. When the LC resonant tank, formed by the gate capacitance (C_{ISS}) and the total gate loop inductance ($L_{source\_ext.} + L_{gate\_loop}$), is excited by a square wave driving waveform, this can cause ringing on the gate of the MOSFET. By reducing the total L_{gate_loop}, the amount of ringing seen on the MOSFET gate can be reduced.

In section 3, a 65 W charger reference design for USB-PD application in ThinPAK is presented.

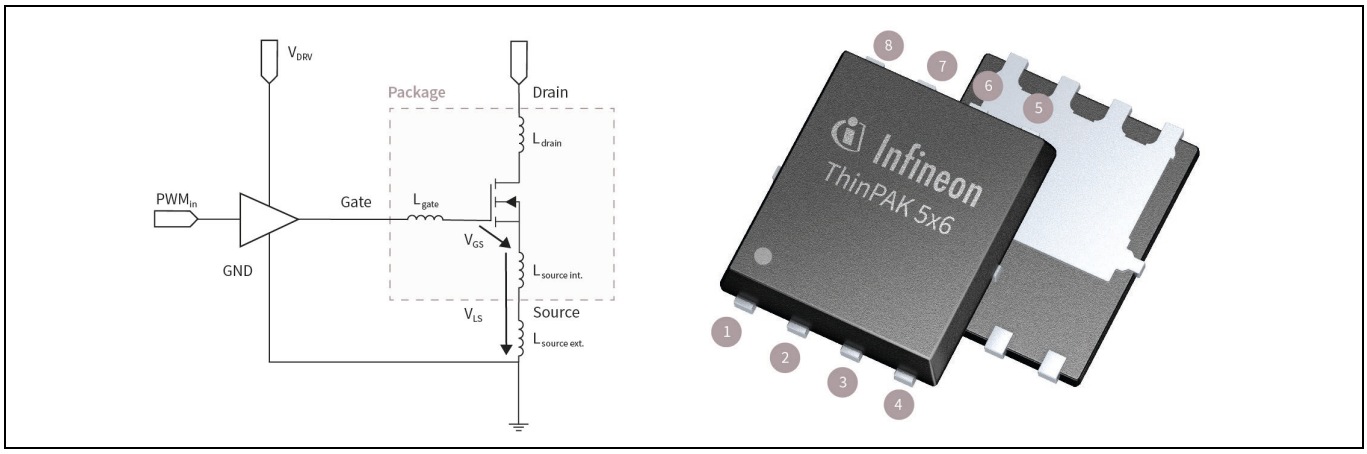


Figure 4 The ThinPAK package enables reduction of the parasitic inductance in the gate drive loop

For the secondary side, Infineon has released a tailor-made **OptiMOS™ PD** series for synchronous rectification and loading switching of USB-PD chargers. The family features MOSFETs offering low on-state resistance ($R_{DS(on)}$), lower switching losses, as well as low gate-, output- and reverse recovery charges. This reduction in overall losses results in an excellent price/performance ratio, which reduces the overall system BOM cost. The availability of logic-level variants allows these parts to be fully driven from 4.5 V or directly from microcontrollers, thereby reducing the part count in the application. In addition, the **PQFN 3.3 x 3.3** and **SuperSO8** packages can shrink the size of USB-PD chargers.

2.3 How to choose the right controller?

The proper selection of a USB-C protocol controller is also pivotal in order to improve the wired communication capabilities of the design.

The charger market is typically end-consumer-oriented and, as such, is quite cost-sensitive and focuses on high performance. For a design going beyond 91 percent efficiency, **the two-chip PAG1 solution** is highly recommended due to its excellent price-performance characteristic. The solution comprises a primary start-up controller PAG1P and a single-chip secondary-side controller PAG1S which integrates synchronous rectification control and USB-C PD protocol control. In particular, PAG1S is a programmable device offering great flexibility, allowing users to fine-tune the QR valley value at which the converter switches across line/load voltages. It makes it possible to optimize the system efficiency without changing the external hardware components.

To obtain better performance (e.g., 92 percent), the digital-based XDP™ XDPS21081 ZVS controller is the most suitable. This product is the industry's first flyback controller with ZVS on the primary side to achieve high efficiency with simplified circuitry and economical switches, thereby reducing BOM cost. By negative magnetization, the FFR switching scheme can reduce the losses associated with today's valley-switching type controllers without sacrificing the design simplicity of the fixed-frequency switching schemes. Besides, the digital controller can adjust many parameters to simplify the BOM. It also provides excellent flexibility, allowing engineers to tailor-make their designs according to different system

specifications. If even higher efficiency (e.g., 93 percent) is required, an asymmetric flyback topology is recommended. At Infineon, this topology is called hybrid flyback, introduced in section 2.1.

When the main design requirement is firm compatibility with the USB-C protocol, the highly integrated **USB Type-C port controller EZ-PD™ CCG3PA** is recommended. The CCG3PA complies with the latest USB Type-C and PD standards and targets PC power adapters, mobile chargers, car chargers, and power bank applications. In such applications, the CCG3PA provides additional functionalities and BOM integration advantages. The CCG3PA uses Cypress's proprietary M0S8 technology (*Cypress is part of Infineon Technologies)* with a 32-bit Arm® Cortex®-M0 processor, 64-KB flash memory, a complete type-C USB-PD transceiver, all termination resistors required for a type-C port, an integrated feedback control circuitry for voltage (V_{BUS}) regulation, and system-level ESD protection. It is available in 24-pin QFN and 16-pin SOIC packages.

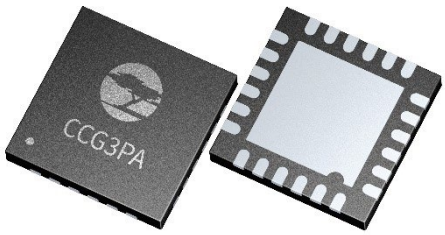


Figure 5 The highly integrated USB Type-C port controller EZ-PD™ CCG3PA in 24-pin QFN

In Section 5, PAG1-based reference designs are introduced. To enable faster time to market and cut down on the development costs, multiple PAG1-based reference designs are available across power levels. They come in competitive form factors and are tested as per the standards defined by DoE Level VI, CoC Tier 2, USB-C PD, and CISPR 32 Class B.

3 High-density 65 W solutions

The solution introduced in this article is based on a digital zero-voltage-switching (ZVS) controller – the XDPS21081 platform, which achieves 21 W/in^3 uncased power density. This **65 W reference design** uses a universal AC input and converts it to the typical 5 to 20 V_{DC} output supported by the USB-PD 3.0 protocol, widely used in most modern laptops and smartphones. Using the resonant switching transitions virtually eliminates the main MOSFET switching losses in the desired frequency band. This approach can achieve the high switching frequency required to allow the use of smaller components (i.e., transformers) while still maintaining (or even improving) the efficiency needed to manage heat dissipation in a very small form factor. In short, in all load and line ranges, the overall efficiency can be increased to more than 90 percent, and the peak efficiency can reach more than 93 percent.

The solution accepts a wide input range from 90 V_{AC} to 265 V_{AC}, and the output can vary from 5 V to 20 V, while the maximum output power is 65 W. A flyback topology and commodity components are selected to balance several factors such as cost, performance, or production. ZVS is enabled by an additional ZVS winding and ZVS circuit driven by the PWM controller XDPS21081 GD1 pin.

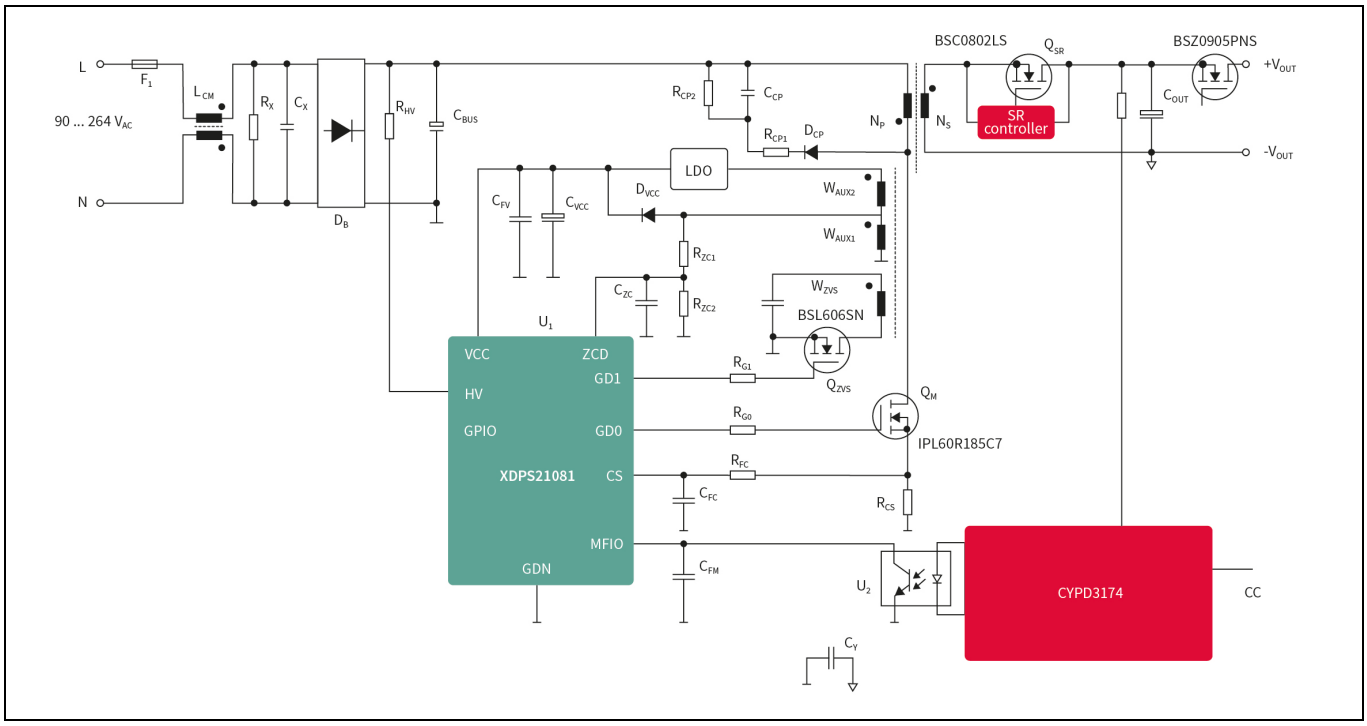


Figure 6 The forced quasi-resonant (FQR) 65 W USB-C PD charger block diagram

With the help of the ZVS function, the switching loss at the high line is significantly reduced so that the switching frequency can be set at about 140 kHz. For low-voltage lines, the system operates in quasi-resonant (QR) mode under heavy load, thereby producing a natural ZVS effect to reduce power loss. Frequency-reduction mode (FRM) and active burst mode (ABM) are implemented to maintain high efficiency at medium- and light loads. Figure 7 shows the efficiency under different conditions.

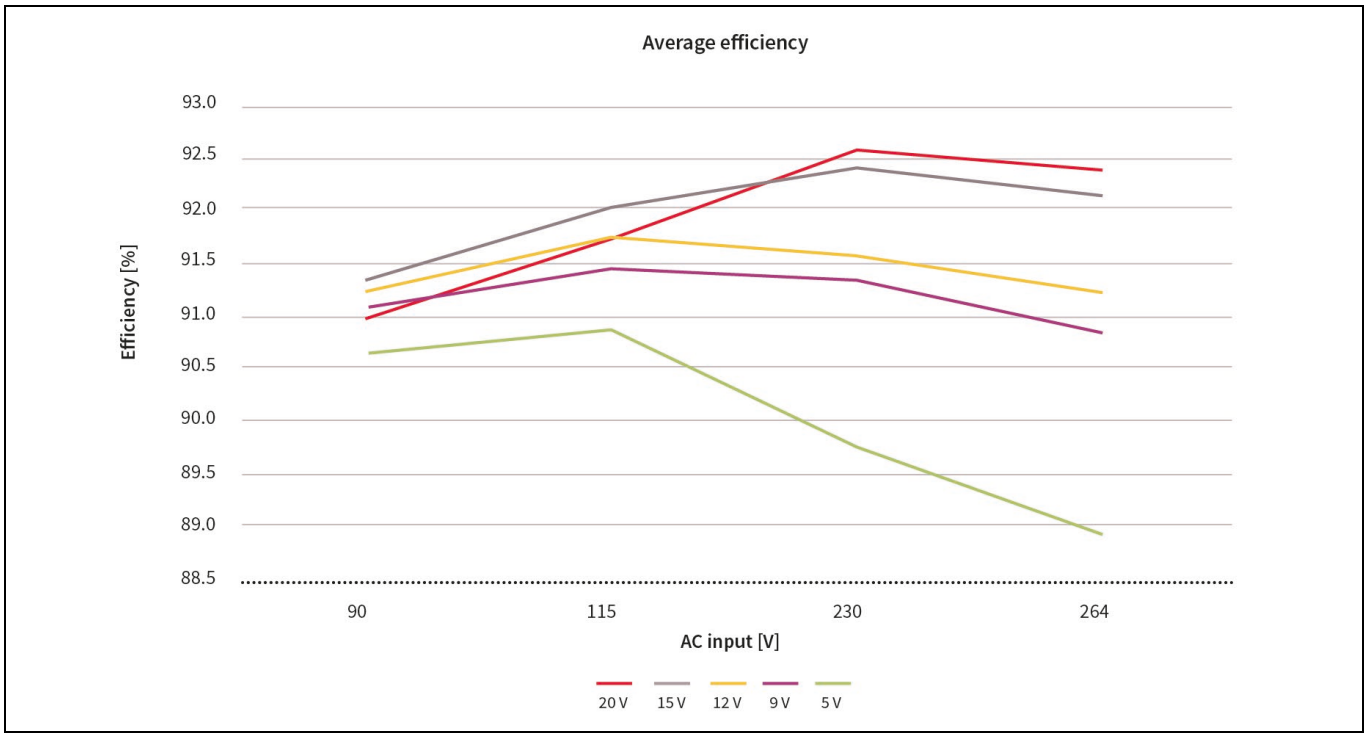


Figure 7 Four-point efficiency which surpasses regulation requirements

One can activate brown-in and brown-out by connecting a resistor between the XDPS21081 HV pin and the bulk capacitor. Also, the design has various protection features, such as, for example, OCP, V_{out} OVP, VCC OVP, OLP, OTP, latch enable, and CS-pin short protection before power-on.

Infineon has recently released the ready-to-use 65 W 20 W/in^3 (50 CC) USB-PD digital FQR XDPS21081 reference design (Figure 8). This silicon-based solution offers robustness, high power density, low cost, and an easily configurable design. Commodity components are used to reduce production complexity.

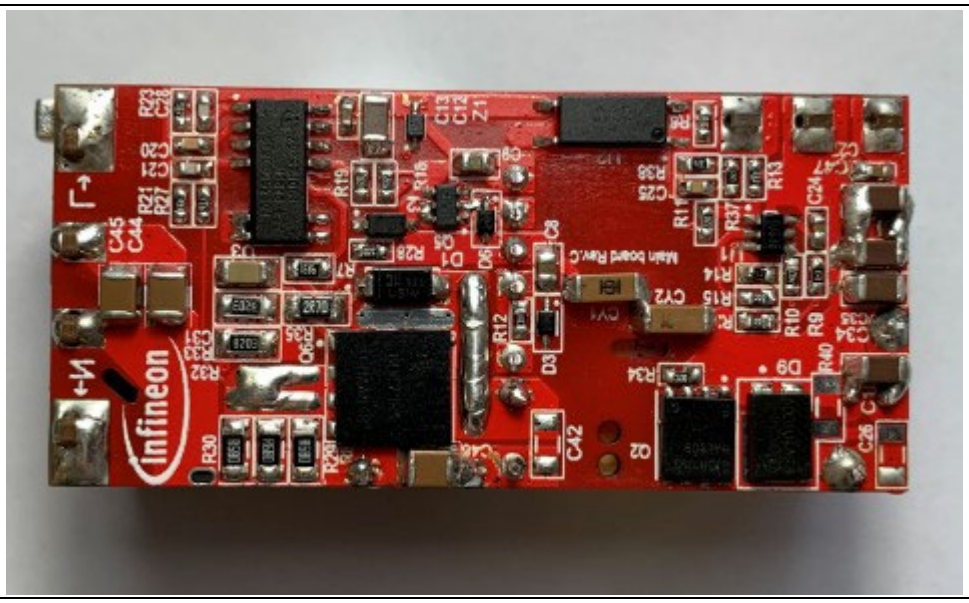


Figure 8 Infineon’s high-density 65 W reference design for high performance with ease-of-use at an affordable cost

4 Ultra-high-density 65 W design based on hybrid flyback control

A combination of the proper topology, dimensioning, and advanced control techniques is required to obtain excellent power density. Looking at the high-power mobile charger market, there are several solutions for high-power USB-PD chargers, such as PFC + QR and PFC + LLC. However, some drawbacks limit the broader usage of these: the QR cannot achieve soft switching, and it's challenging to use LLC topology for variable output voltage designs.

Aware of this situation, Infineon has introduced a new topology named hybrid flyback based on an asymmetric half-bridge control (as shown in Figure 9). The half-bridge is driving a conventional flyback transformer in conjunction with a serial capacitor. The main inductance of the flyback transformer and the serial capacitor form a resonant tank, which is used to realize a ZVS behavior of the half-bridge power switches and also provides resonant power transmission during the conventional demagnetization phase of the flyback transformer. During normal operation, the charging cycle and related power are controlled by direct peak current control, while the demagnetization phase is controlled by timing to ensure proper negative pre-magnetization, which is required for a ZVS condition of the half-bridge power switches.

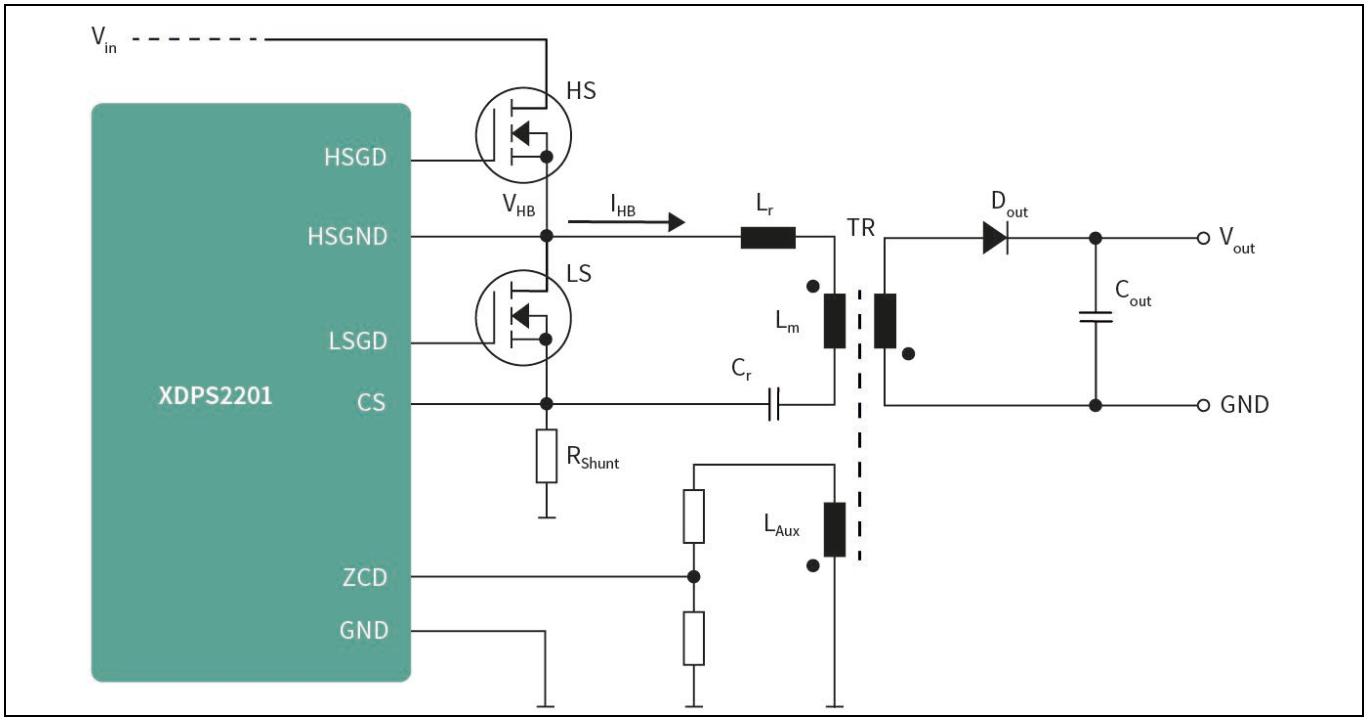


Figure 9 Simplified schematic of an asymmetric half-bridge flyback

The power circuit in the primary side is realized by an LC tank, driven by a half-bridge similar to an LLC converter. The resonant inductor L_r represents the series inductance, L_r being either the transformer leakage inductance or the leakage inductance plus an external inductor, and L_m represents the transformer's main inductance. The same converter can also be realized by connecting the resonant capacitor C_r and the transformer's primary coil between the positive node and the half-bridge midpoint. When the high-side switch HS is turned on, energy will be stored in C_r and L_m, and the respective stored energy will vary with the input voltage and switching frequency (as shown in Figure 10).

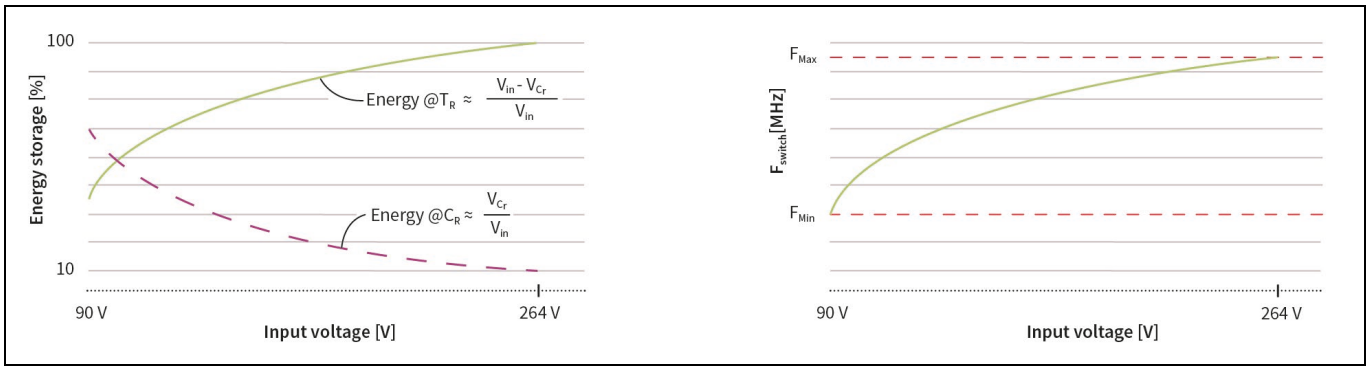


Figure 10 Energy storage distribution and frequency variation diagrams

When the high-side switch (HS) is turned off, the transformer current will force the half-bridge midpoint V_{HB} to drop until the body diode of the low-side switch clamps the voltage. Then, the low-side switch (LS) will be turned on at zero voltage, and at the same time, the transformer phase reverses, and energy is transferred to the secondary side. When the low-side switch is turned off, the negative current induced in the transformer in the previous phase will force the half-bridge midpoint V_{HB} to increase its voltage until it is clamped by the body diode of the high-side switch HS, similar to the previous phase. HS is switched on under the ZVS condition, and LS is switched off, but the current in the transformer resonant tank is still negative, which means that the excess energy in the tank will be sent back to the input.

The final converter dimensions (see Figure 11a) are 51.5 mm x 38 mm x 19 mm. It achieves a power density of 29 W/in^3. The prototype achieved a minimum efficiency of 93.4 percent at 90 V_{AC} input and 65 W load measured at board connectors (Figure 11 b).

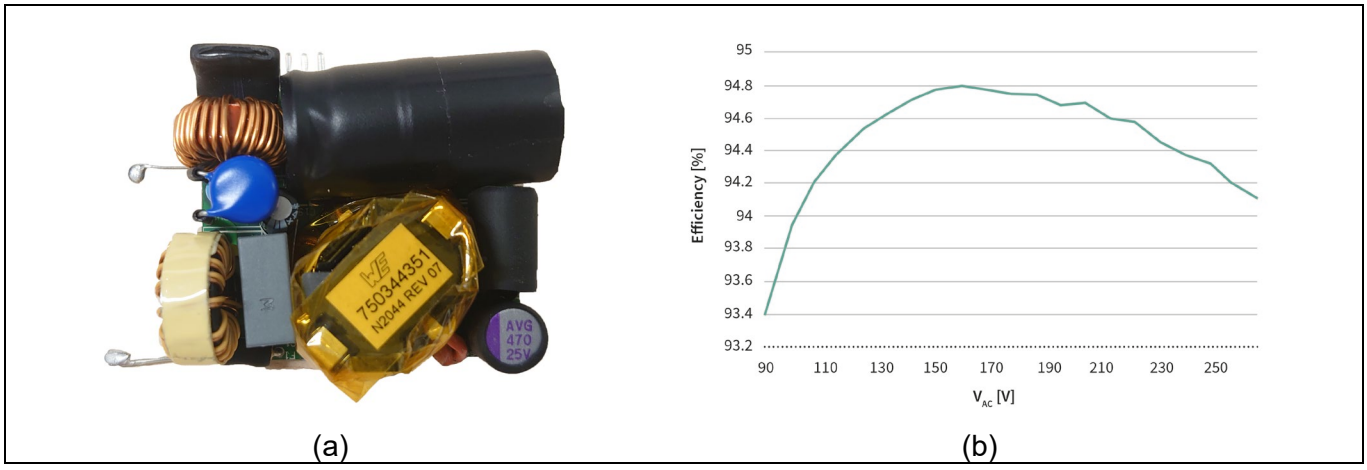


Figure 11 Infineon's 65 W high-density design (a) and achieved efficiency (b)

5 A novel, cost-effective USB-C PD solution with the EZ-PD™ PAG1 series

PAG1 is a complete AC-DC power solution with an integrated USB-C PD controller. It is a two-chip USB-C power adapter solution comprising a primary start-up controller (PAG1P) and a single-chip secondary-side controller (PAG1S). PAG1P and PAG1S together operate in a secondary-side controlled flyback architecture. PAG1P provides the start-up function, drives the primary FET, and responds to fault conditions. PAG1S is a single chip secondary-side controller that integrates the synchronous-rectification controller, PD controller, PWM controller, a 30 V regulator, high-voltage NFET gate drivers, and a protection circuitry.

Increasing needs for short charging times have led to multiple fast charging standards in the market, such as adaptive fast charging (AFC), quick charge (QC), Apple 2.4 A charging, Huawei FCP/SCP, or USB-C power delivery. Hence, retail manufacturers will hold a competitive edge if they can support multiple protocols on the same device. The PAG1 solution enables this by supporting AFC, QC4+, QC4, QC3, Apple 2.4A charging, and BC1.2 all on the same device with no additional bill-of-material (BOM) cost. In addition, PAG1 offers enough flash memory to implement other proprietary protocols defined by the customer, with Infineon supporting the firmware development and compliance.

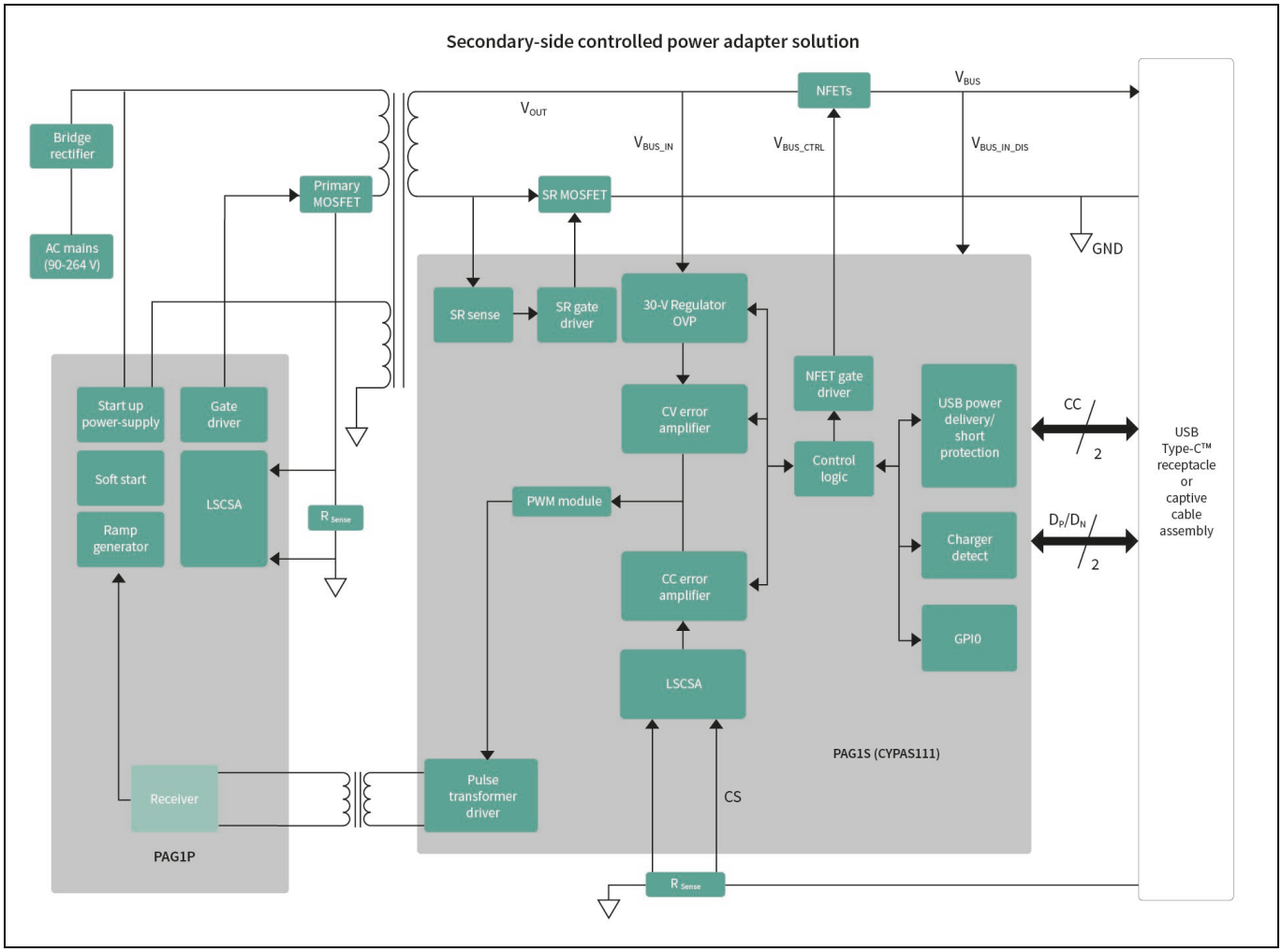


Figure 12 Block diagram of a secondary-side controlled power adapter using PAG1S and PAG1P

Typically, an SMPS operates as a voltage regulator, which means that a feedback link is needed from the output to control the power stage. The control loop compares the output voltage against a reference voltage to generate the PWM signal to drive the primary switch, thereby regulating the output voltage. In the commonly used primary-side controlled architecture, an optocoupler is used as a feedback link to transmit an error signal from the secondary side to the primary controller. However, such an architecture has limitations. Firstly, Optocouplers have limited loop bandwidth. Hence, their use in the feedback loop makes it difficult to achieve a fast-dynamic load response and maintain higher gain/phase across a variable output voltage. Also, the loop bandwidth and gain degrade over time. Secondly, every output-related function needs to be communicated over the isolation barrier to the PWM controller. This exchange adds lag time, thereby increasing the subsequent time required to adjust the PWM controller. The output-related function can be attributed to output current protection, over-voltage protection, under-voltage protection, load sharing, driving synchronous rectifiers, and so on.

To overcome the shortcomings of a primary side-controlled architecture, Infineon offers the PAG1 solution using a secondary side-controlled architecture. In this design, the regulation happens on the secondary side with PAG1S, and the primary controller (PAG1P) acts as a simple gate driver. This combo achieves isolation between the primary and secondary sides using a pulse transformer. The converter’s brain sits on the secondary side (PAG1S), where all decisions related to the output voltage regulation that make the control loop faster are made. Also, this architecture enables immediate reaction to any malfunction on the secondary side, thereby making the system more robust. By not using an optocoupler, the system behavior is more consistent and predictable from unit to unit over operating point, temperature, and product lifetime.

The secondary-side controlled architecture also enables direct control of the SR FET in a way that achieves zero voltage switching (ZVS). ZVS enables higher efficiency on an existing converter without the use of any extra circuitry. With the ability to support higher loop bandwidth and faster dynamic response times, the secondary-side controlled architecture is best suited to support higher switching frequency, thus higher power density designs. One issue with secondary side-controlled architecture is the initial power-up to jump-start the circuit using an extra power supply. We overcome this issue with PAG1P. PAG1P helps power up the secondary side during start-up. Once the system reaches the steady-state operation, it transfers the control to the secondary side and acts only as a primary-side gate driver with primary-side fault protection (OVP, UVP, and OCP).

The PAG1S is a programmable device and, as such, allows for great flexibility in power adapter designs. The user can adjust the QR valley where the converter switches across line/load and thereby optimize the system efficiency without changing the external hardware components. **EZ-PD™ configuration utility** tool allows the user to effortlessly fine-tune the value of the current sense resistor to account for the variations seen due to board designs without changing the hardware. The tool also offers the flexibility to configure the fault protection thresholds and the recovery mechanisms for overcurrent protection (OCP), overvoltage protection (OVP), short circuit protection (SCP), and overtemperature protection (OTP). Also, the PAG1S can be re-programmed on the field to cater to the latest USB-C PD standard or to address any newly discovered post-production bugs.

Figure 13 A 65 W reference design using PAG1S and PAG1P in a 52 mm x 42 mm x 22 mm board

Discover more reference designs, boards, and design support documents at **infineon.com/usb-pd.**

6 Summary

The USB-PD protocol is unifying the charger market. Infineon offers a comprehensive portfolio to enable high-density USB-PD charger designs at a competitive cost.

Many power switches, controllers, and reference designs are available to help design engineers find the best fit for their design requirements. The digital-based XDP™ controller, the XDPS21081 brings a new control method for ZVS/ZCS operation to enhance flyback converters; the tailor-made superjunction high-voltage CoolMOS™ and low-voltage OptiMOS™ families provide cost-effective solutions for power switches to improve market competitiveness; the extensive product portfolio of USB-C protocol controllers can improve wired communication capabilities.

With the flexibly variable reference designs, design engineers can quickly develop the right-fit USB-PD charger solution. To ensure that they can meet their design targets, Infineon offers a broad range of solutions with a comprehensive semiconductor portfolio of high- and low-voltage power MOSFETs, USB-PD protocol PAG1 solution, as well as digital soft-switching controllers that provide excellent power density (see Figure 14 and Figure 15).

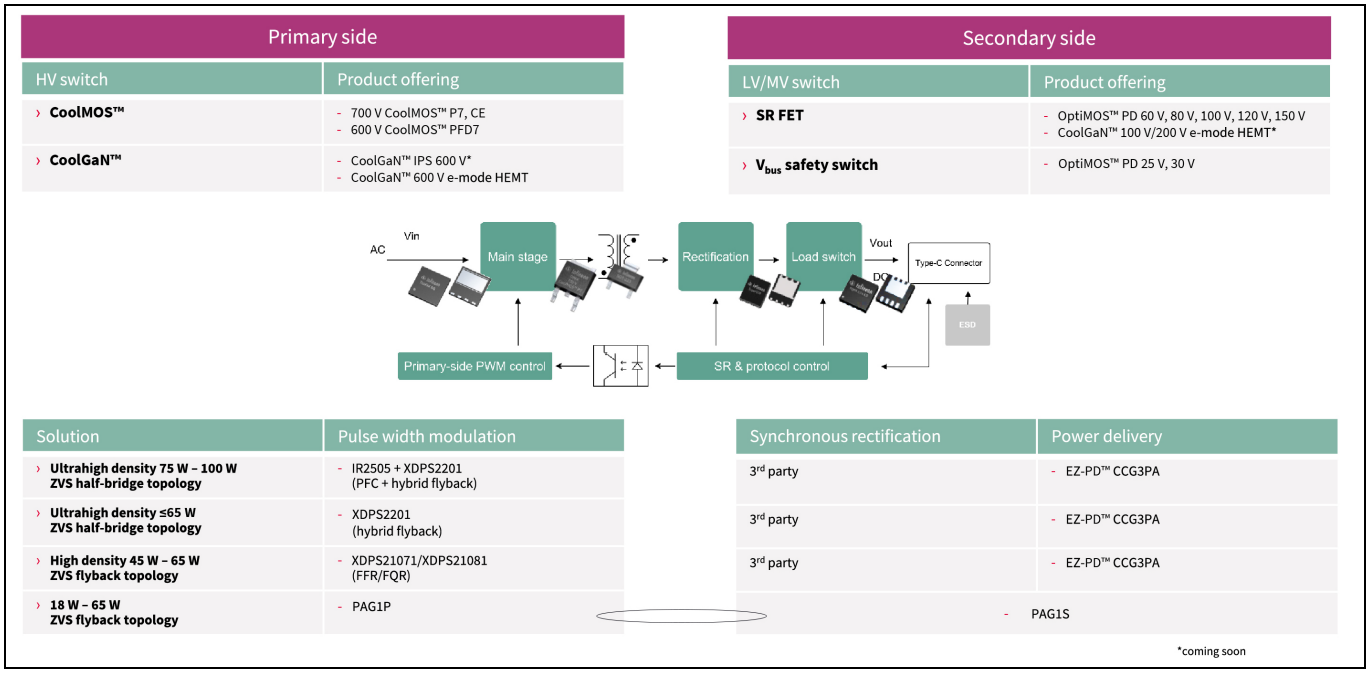


Figure 14 Infineon's broad array of products for USB-PD designs

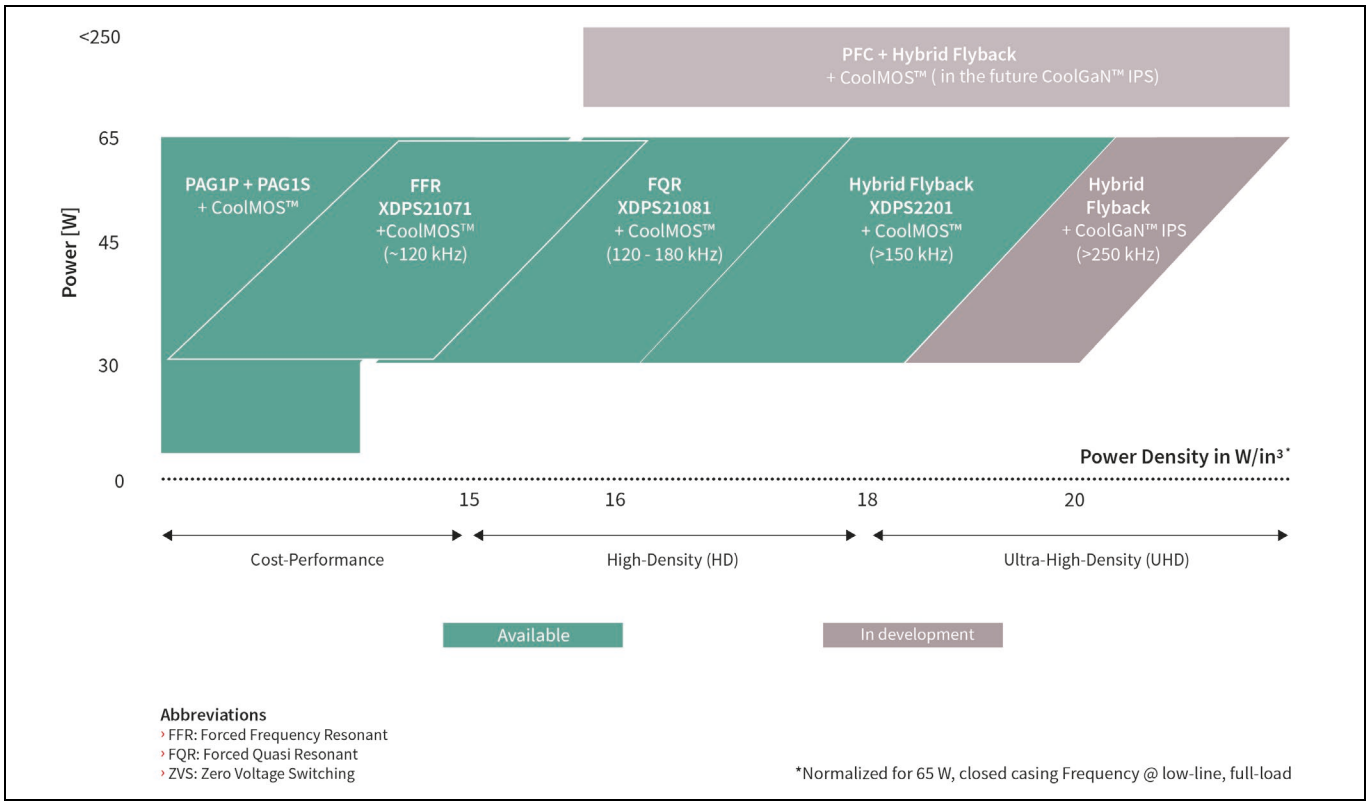


Figure 15 A comprehensive solution offering from Infineon, including power switches, micro-, digital- and protocol controllers to meet various requirements for USB-PD designs

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