The SMD-0.1

A New IR HiRel Surface Mount Device Package

About this document

Scope and purpose

This document introduces IR HiRel's new SMD-0.1 package designed specifically for the new R9 rad hard MOSFETs in die size 1. An overview of why the new package is necessary, how the SMD-0.1 solves the problems it faces, the package qualification, and recommendations for applications and PCB assembly are described.

Intended audience

This document is meant for IR HiRel's current and potential consumers to provide them more information about a new package they may find useful.

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1 Introduction

IR HiRel's R9 generation of radiation hardened MOSFETs has improved power density and class leading drain current per area (A/mm^2) figure of merit. In addition, the R9 technology enables wafer fabrication of power MOSFETs as small as 80mils x 80mils. This enables IR HiRel to develop radiation hardened power MOSFETs that are 55% smaller and still have high current capability and low $R_{DS(ON)}$. These improvements lead to new thermal problems with the package, in addition to, the thermal expansion problems that all surface mounted package face.

The newly developed SMD-0.1 package reduces the temperature problems caused by the increased power density in such a small die and incorporates all the learning of the SupIR-SMD and enhanced SMD package to reduce the impact of having materials with different thermal expansion coefficients.

This outline of this application note is:

- First, the thermal mismatch and temperature problems will be briefly described.
- Second, the prior solutions will be reviewed.
- Third, the SMD-0.1's new features will be described.
- Fourth, the PCB mounted environmental qualification testing for the SMD-0.1 package will be described.
- Fifth, recommendations for applications and PCB attach will be provided based on our own experiences with qualifying the part.

2 A Summary of the Design Challenges

As described in app note of SupIR-SMD package qualification, the thermal mismatch between the SMD package and PCB can cause a reliability problem. All materials will expand, or contract based on changing temperature, this is called the coefficient of thermal expansion, or CTE. However, different materials will have a different CTE. This doesn't cause any problems if the connected materials are the same or have similar CTEs, they will expand or contract at the same rate. But, if the materials have vastly different CTEs, then the disparity in expansion rates causes a possibility of inducing cracks in the solder joints and package.

Table 1 CTE of different materials in hermetic package and PCBs

Material	CTE α (10^{-6}/K)
FR-4 circuit board	13-14
Polyimide circuit board	18
Copper	16-17
Ceramic/glass	6

Thermal management is a major challenge as newer technologies lead to a reduction in die size with increased power density. Heat transfer can be represented with the following formula:

$$q = \frac{k}{s} Adt$$

Where:

- q is the heat transfer (W)
- k is the thermal conductivity of the material (W/(m.K))
- s is the material thickness (m)
- A is the heat transfer area (m^2)
- dt is the change in temperature (K)

A smaller die size leads to less area to dissipate heat, while the increased power density means there is more heat to dissipate. Both factors lead to a reduction in the heat transfer rate, increasing the temperature of the package. The higher temperatures could lead to increased stress and cracks. To compensate for this, the thermal conductance of the package needs to be very high to increase the heat transfer rate to keep the temperature and stress at safe operating levels.

3 Existing Solutions

IR HiRel developed a new die size 1 utilizing the R9 super-junction technology with size smaller than previously existing dice, being as small as 0.080" x 0.080". Despite being smaller than die sizes of 1.7 or 3, the R9 technology offers improved electrical performance compared to previous generation of rad hard MOSFETs. Some features of the R9 platform include low $R_{DS(on)}$, increased current capability, increased SEE ruggedness, and higher power density. The closest options to package a die size 1 are the SMD-0.2 and UB packages, however, these are suboptimal solutions.

The SMD-0.2 was designed for larger die sizes (size 1.7). So, the SMD-0.2 package would be oversized for the smallest R9 die (size 1) and the footprint is much larger than necessary for the die (Package outline shown in Figure 1).

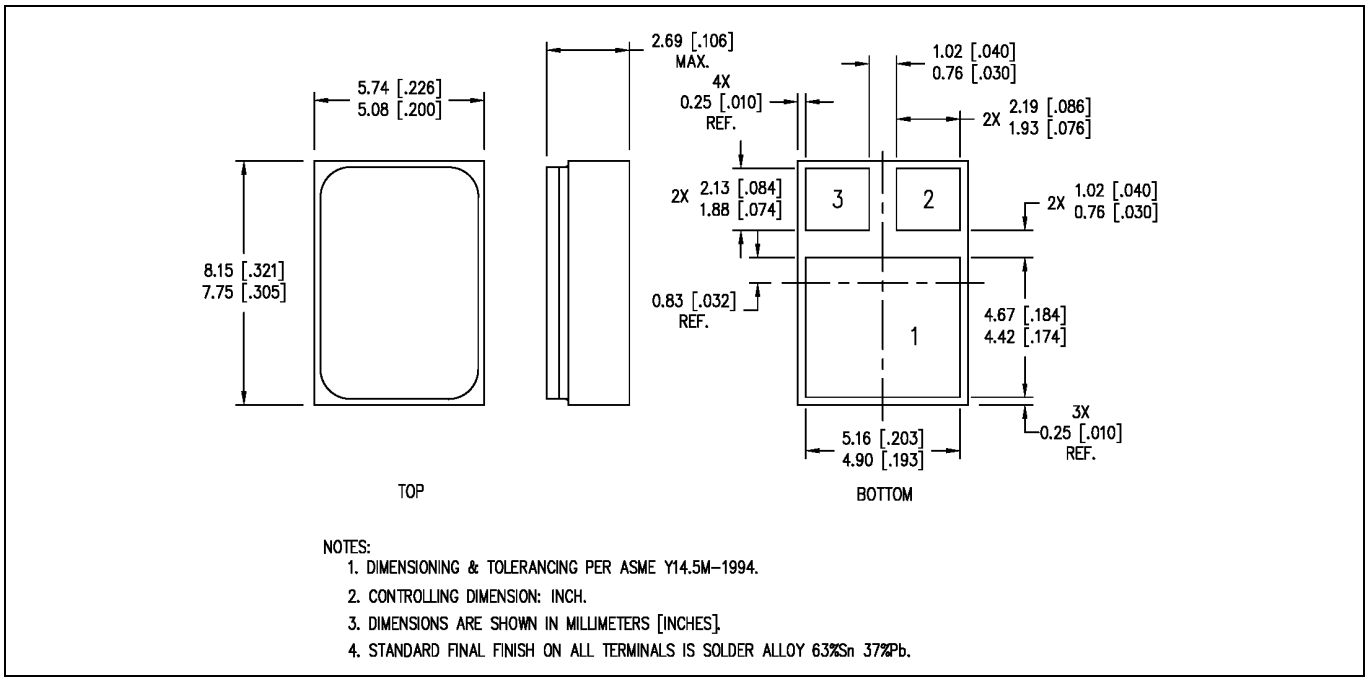


Figure 1 SMD-0.2 outline drawing (see website)

The UB packages are designed for small signal FETs, not for power FETs. The UB packages (Package outline shown in Figure 2) are made from alumina (Al_2O_3) which has a thermal conductivity of 20-30 W/(m.K), which is quite lower than materials used for other SMD packages. This means that there will be a slower transfer of heat out of the die. So, the UB package isn't suitable of housing the new R9 MOSFETs.

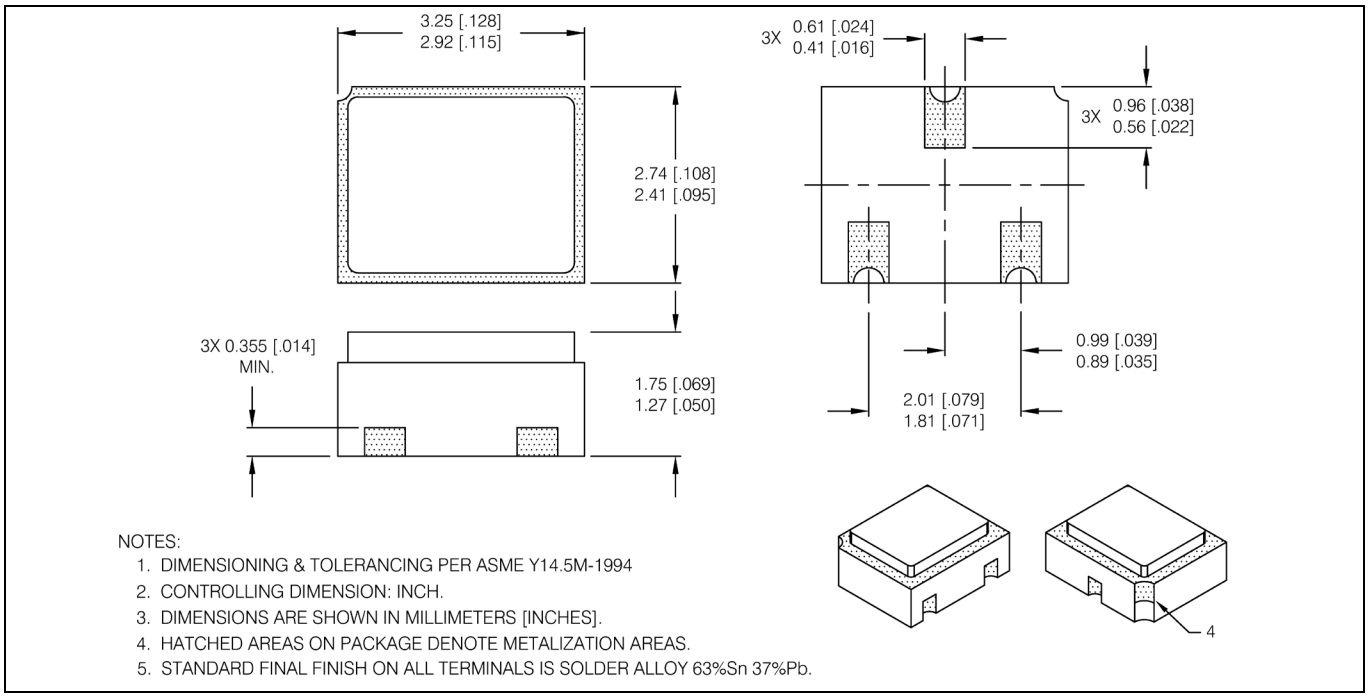


Figure 2 UB outline drawing (see website)

4 The SMD-0.1: A Better Solution

A new package was needed to accommodate the smaller die size and increased power requirements. IR HiRel invented SMD-0.1 package to meet this requirement. The patent was filed (US 2021/0407874) by Infineon Technologies, IR HiRel's parent company. The 3D view and dimensioned drawing of the design are shown in Figure 4 and Figure 5 respectively. Because of the small size of the package, using a ceramic and metal design like the SupIR-SMD wasn't an option. Instead, the SMD-0.1 is built with a single piece of aluminum nitride (AlN) with an AlN lid. AlN has a high thermal conductivity of 285 W/mK at 25 °C. This is much higher than the 25 W/mK thermal conductivity of alumina. This allows for a higher heat transfer rate out of the die. Figure 7 shows the size of SMD-0.1 in comparison to two other power packages: the SMD-0.2 and SMD-0.5e.

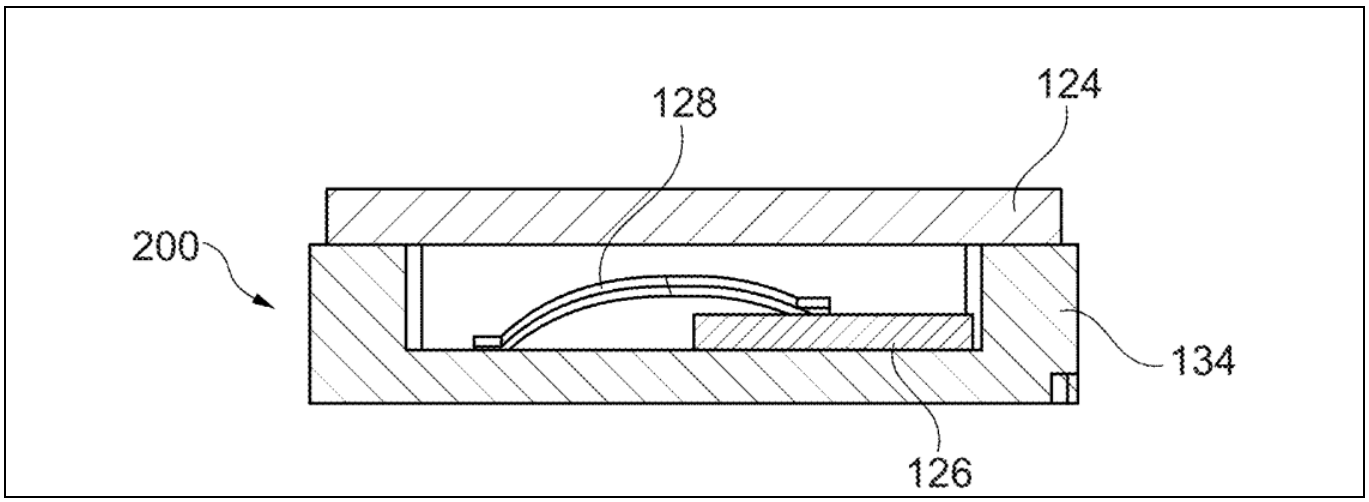


Figure 3 SMD-0.1 (cutaway view showing chip and wire-bond inside)

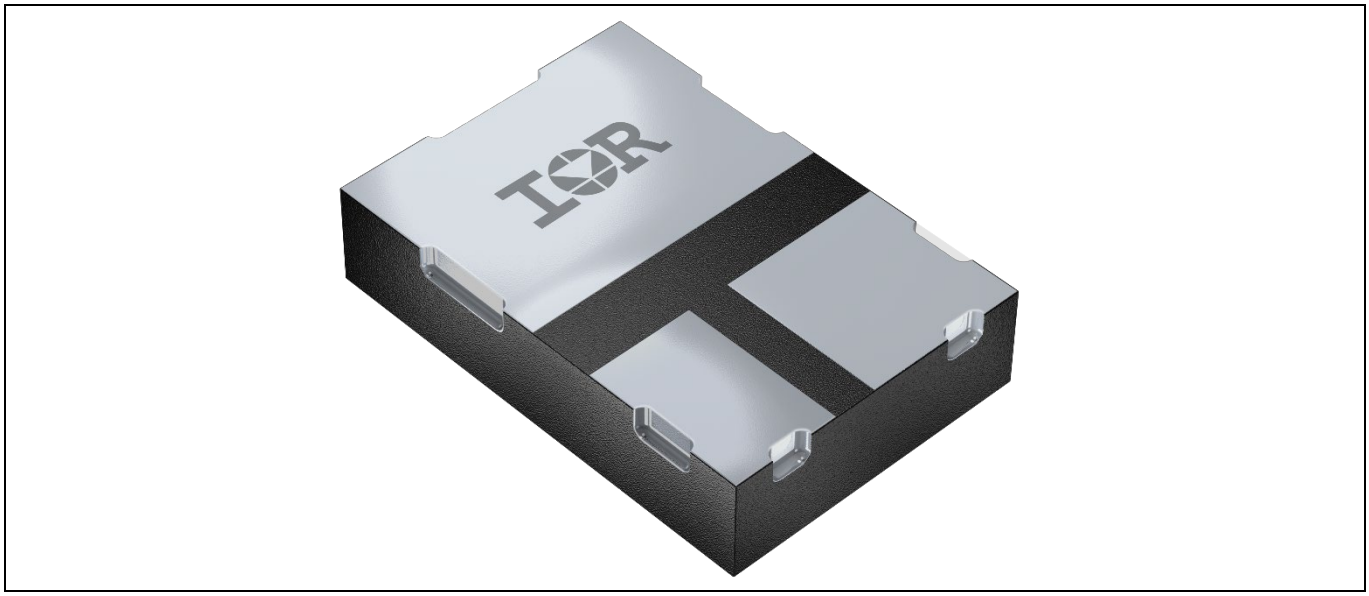
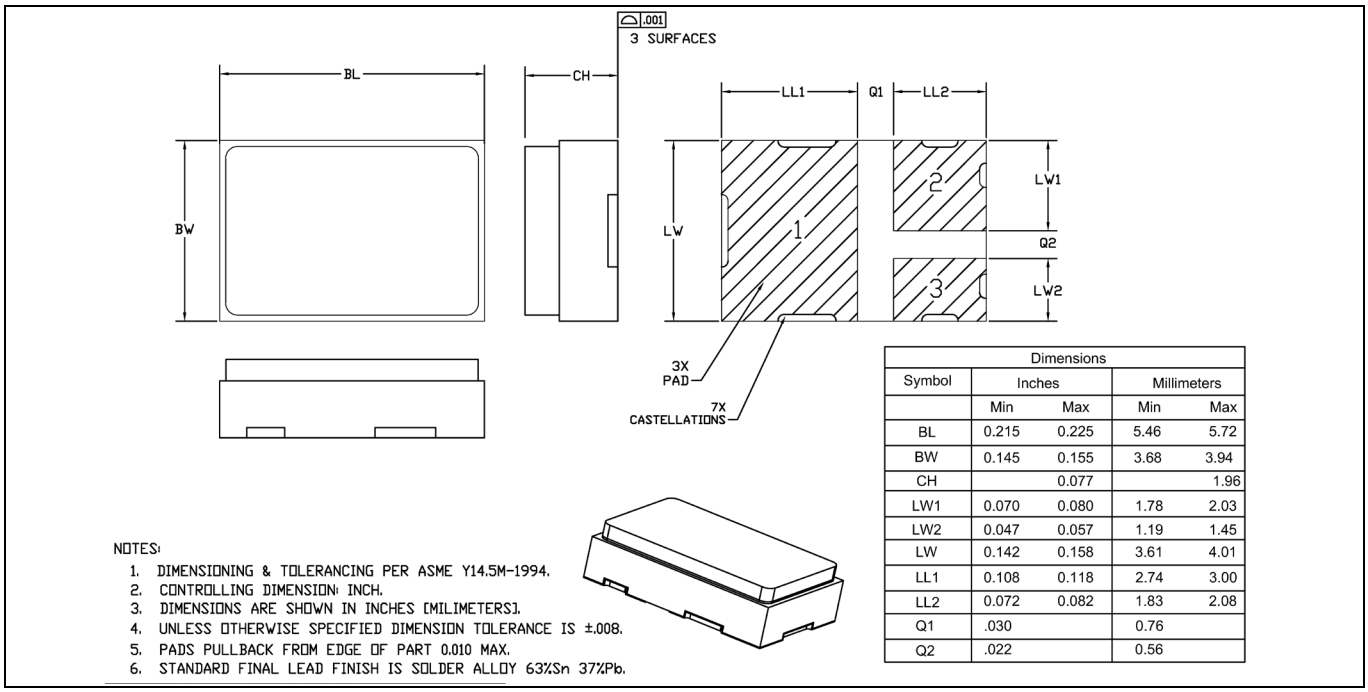


Figure 4 SMD-0.1 package, post solder-dipped



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
BL	0.215	0.225	5.46	5.72
BW	0.145	0.155	3.68	3.94
CH		0.077		1.96
LW1	0.070	0.080	1.78	2.03
LW2	0.047	0.057	1.19	1.45
LW	0.142	0.158	3.61	4.01
LL1	0.108	0.118	2.74	3.00
LL2	0.072	0.082	1.83	2.08
Q1	.030		0.76	
Q2	.022		0.56	

Figure 5 SMD-0.1, outline drawing (see website for current specification)

The SMD-0.1 features an asynchronous pad design. In previous packages, the source and gate pads are the same size. However, the SMD-0.1 reduced the size of the gate pad in favor of having a larger source pad, increasing the number of vias. This allowed more wires to be bonded between the source and drain pads, causing the cross-sectional area to increase. The asynchronous pad design maximizes size of the source pad to minimize electrical resistance of the package.

The SMD-0.1 also has added castellations in the package. The castellations help form a good solder bondline, resulting in more durable and lasting solder joints. The castellations also make the solder joints more visible and easier to inspect.

Table 2 shows the comparison of SMD-0.1, SMD-0.2, and UB (LCC-3 and LCC-4) packages with respect to size, current capability and die free package resistance (DFPR). Figure 6 shows drawings of the SMD-0.1 package in comparison to the SMD-0.2 and the UB packages.

Table 2 Package dimensions and DFPR

Package	Overall dimensions (mm)	Area (mm^2)	Current capability (A)	DFPR (mΩ)
SMD-0.1	5.58 x 3.81 x 1.96	21.3	10	3.5
SMD-0.2	7.95 x 5.41 x 2.46	43.0	25	8
LCC-3 (UB)	3.085 x 2.575 x 1.295	7.94	1	150
LCC-4 (UBN)	3.085 x 2.575 x 1.51			

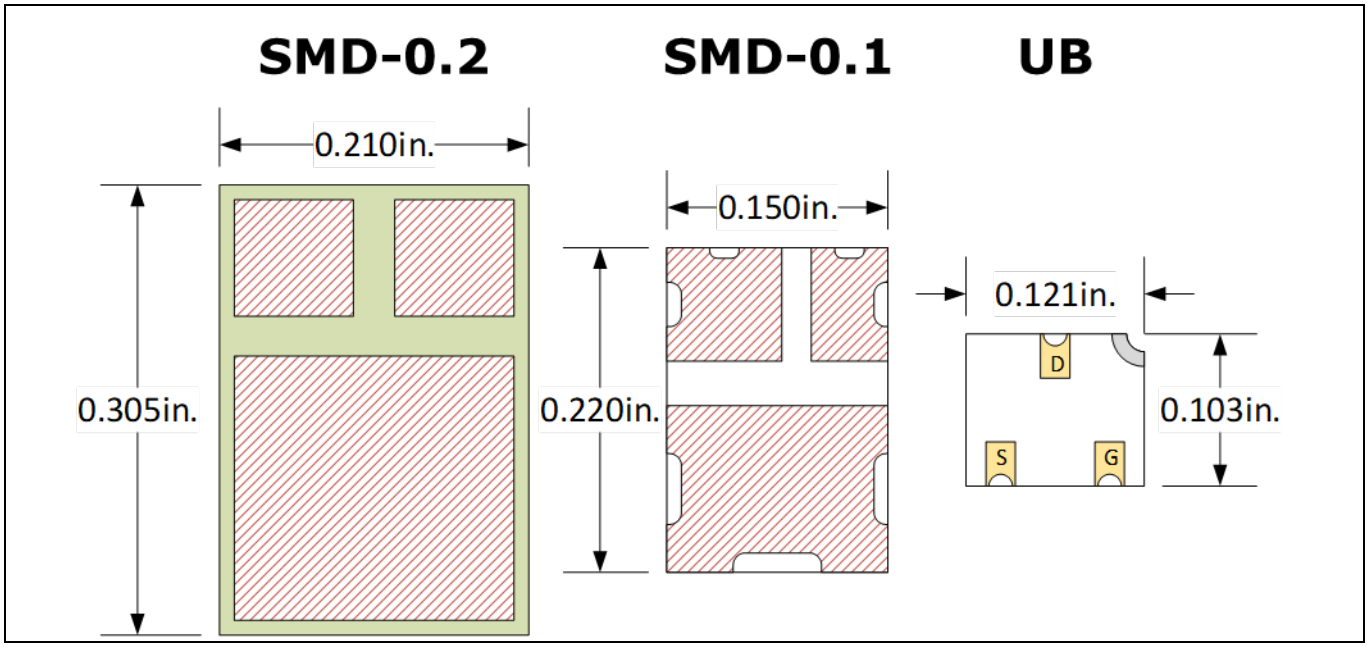


Figure 6 SMD-0.1 size and layout in comparison to the SMD-0.2 and the UB packages

The small size of the package and AlN material result in benefit of reducing the CTE mismatch problem, since they both reduce stress between the PCB and the package. This allows for the SMD-0.1 to be directly mounted to a PCB without the need for ribbon leads used in previous SMD packages (e.g., SMD-0.5, SMD-1, SMD-2). In our temperature cycling testing, there were no cracks in the ceramic while the SMD-0.1 was directly mounted to the PCB, even with the CTE of package and PCB material ranging from 7 to 18 ppm/°C.

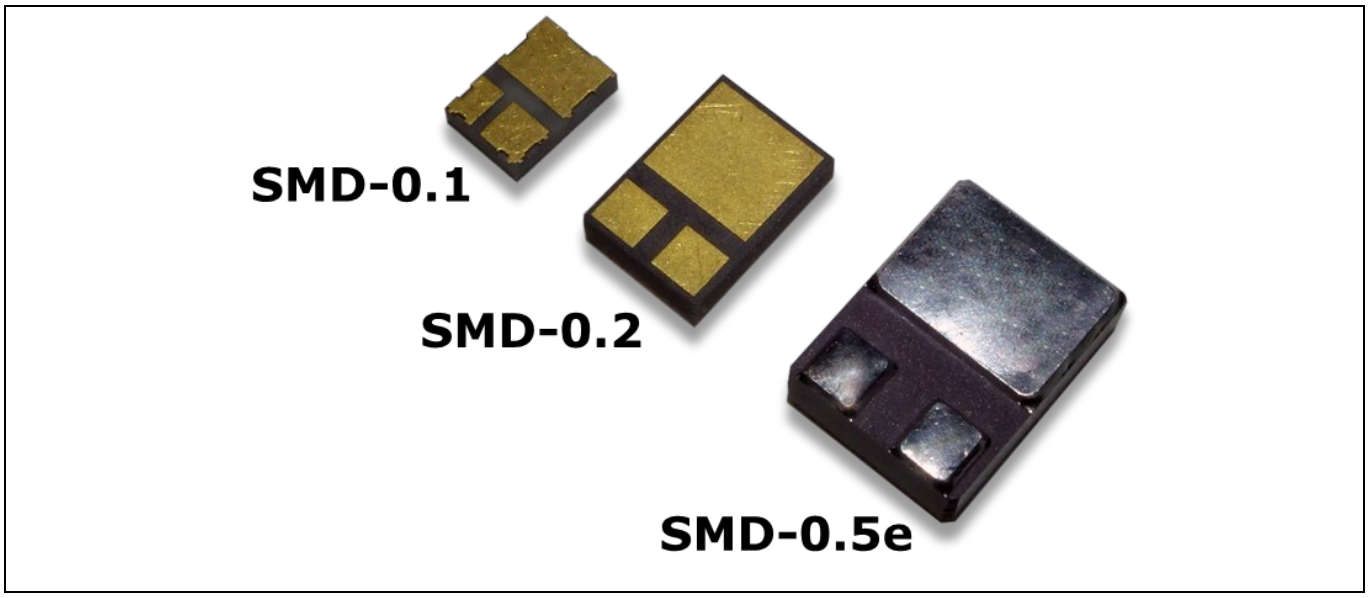


Figure 7 SMD-0.1, SMD-0.2, and SMD-0.5e

Finite Element Analysis (FEA) was used to create and evaluate different designs and finalize the new design. The key figure of merit is the ceramic stress, which was calculated to be at a maximum of 27 MPa at package level (see Figure 8) and 50 MPa (see Figure 9) when mounted on a PCB. This is much lower than the stress limit for flexural strength of the material at 310 MPa. Stress levels in the FEA correlated very well with package performance in the board level test assemblies during the design phase of SMD-0.1.

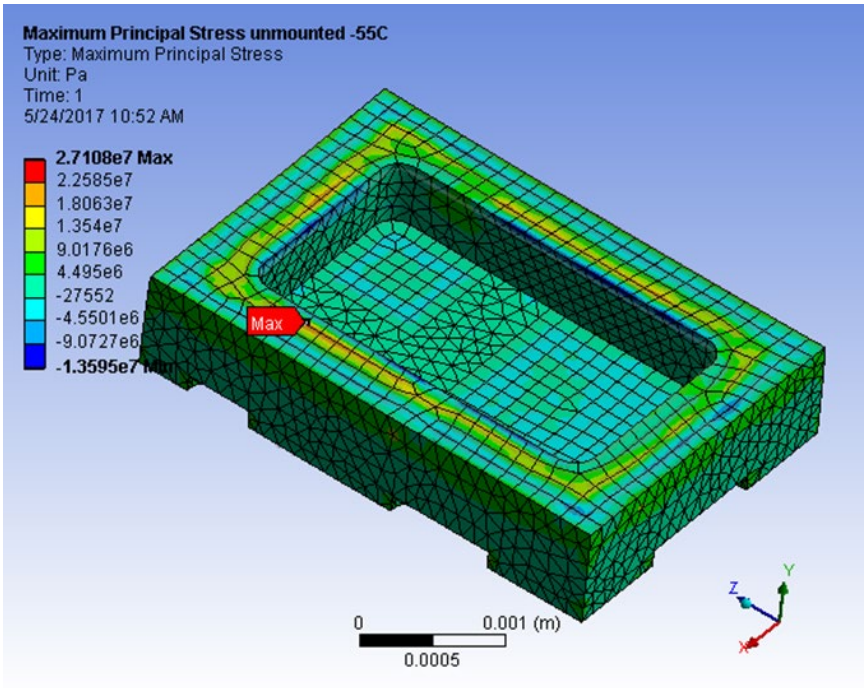


Figure 8 SMD-0.1 FEA model results, package only

Figure 8 shows package level FEA results at -55 °C which is the worst case for mechanical stress. The maximum stress is 27 MPa which is on the top of package. The maximum stress on bottom of package is very low (~2MPa) and is not shown here. The peak stress at 150 °C is low (~10 MPa) as well and is not shown here.

When the package is mounted on PCB, CTE mismatch causes higher mechanical stress as seen in Figure 9. The maximum stress is 52 MPa which is on the bottom of package. This is well below maximum limit. The peak stress at 150 °C is lower (~40 MPa) and is not shown here.

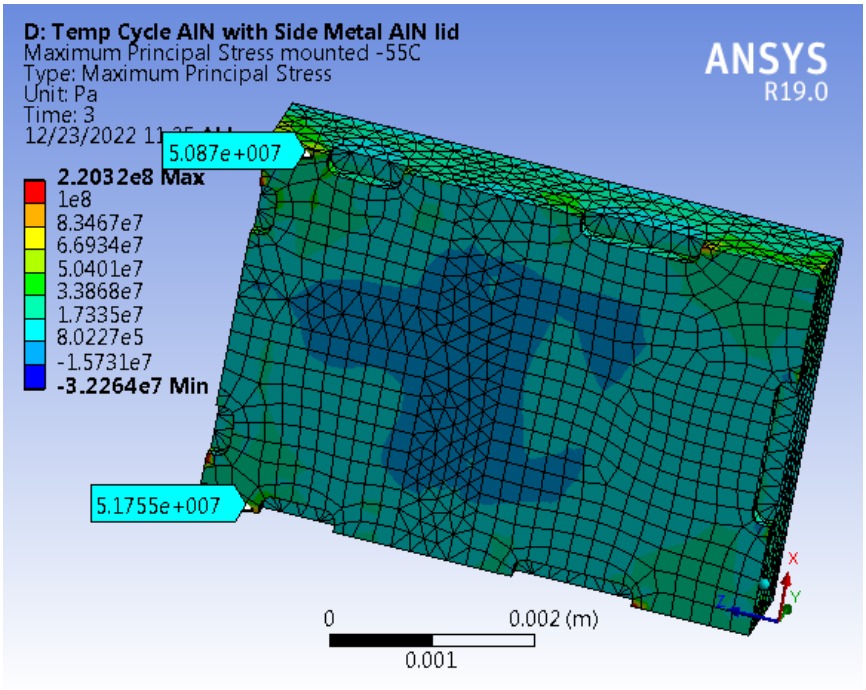


Figure 9 SMD-0.1 FEA model results, package mounted on PCB

5 Board Level Qualification Testing

Board-level qualification testing was performed on the SMD-0.1 package, according to internal test procedure. This testing is done by mounting the package on PCB and performing random vibration, mechanical shock and temperature cycling tests. The PCB used is 4”x6”, 8-layer, 0.071” thick polyimide PCB with 2 oz copper on inner layers and 3 oz copper on outer layers.

First, random vibration testing was done in accordance with ECSS-Q-ST-70-08. The test conditions are shown in Figure 10.

Axis	Frequency Range Hz	Level	Grms	Duration Sec.
X,Y,Z	20 – 100	+6dB/oct	39.9	300
	100 – 1000	1 SQR(g)/Hz		
	1000 – 1500	-3dB/oct		
	1500 – 2000	-6dB/oct		

Figure 10 Test conditions for random vibration testing

The Y-axis random vibration setup and representative graph are shown in Figure 11 and Figure 12.

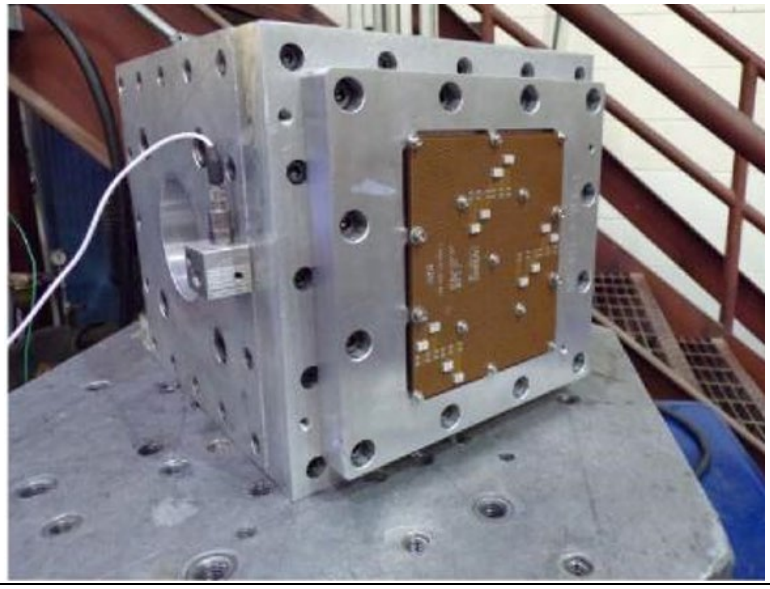


Figure 11 Random Vibration Y-Axis Test Setup

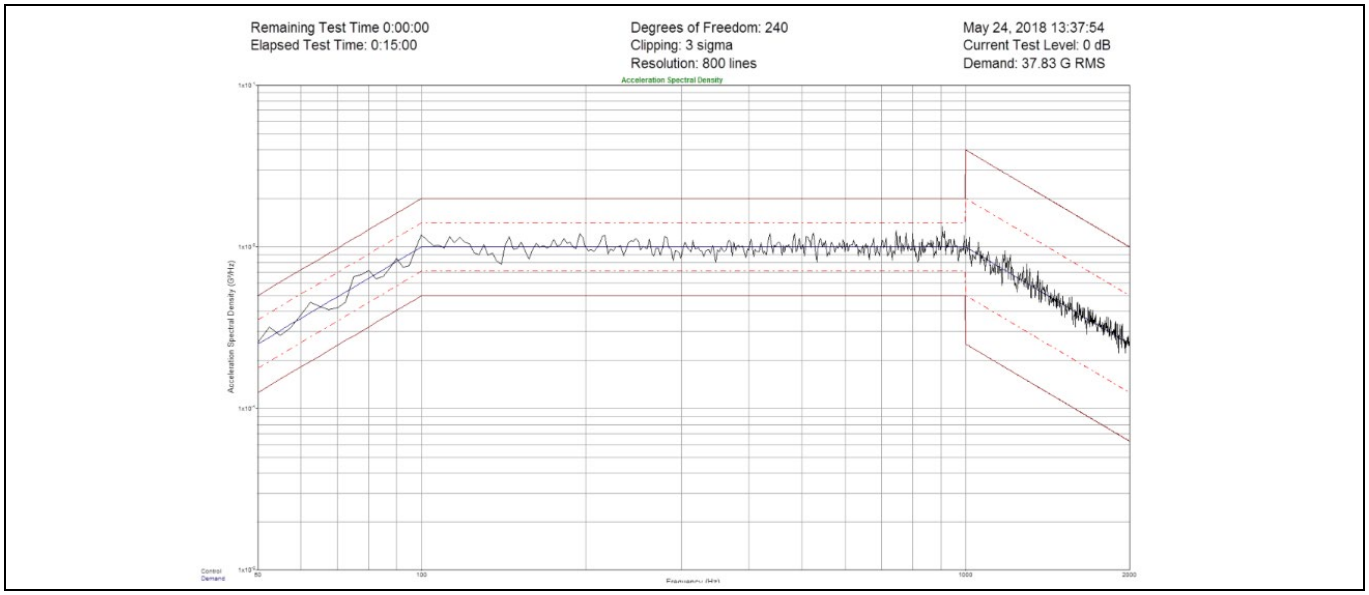


Figure 12 Random Vibration Y-Axis Graph

Next, mechanical shock testing was done in accordance with MIL-STD-883 TM2002 condition B. The test conditions were 1500G amplitude with 0.5 ms pulses, 5 shocks per axis, 3 times in each positive and negative direction resulting in a total of 30 shocks. The X-axis mechanical shock testing and graph are shown in Figure 13 and Figure 14.

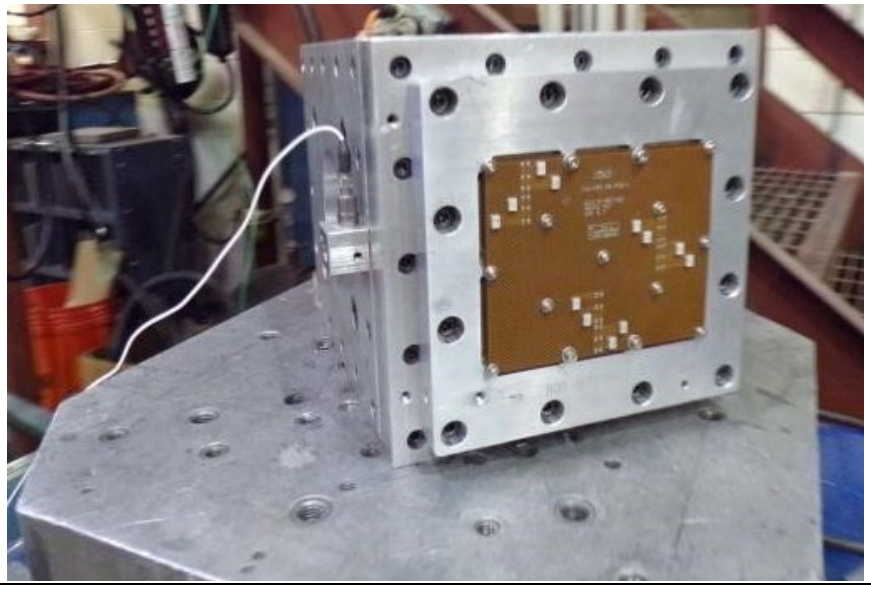


Figure 13 Mechanical Shock X-Axis Test Setup

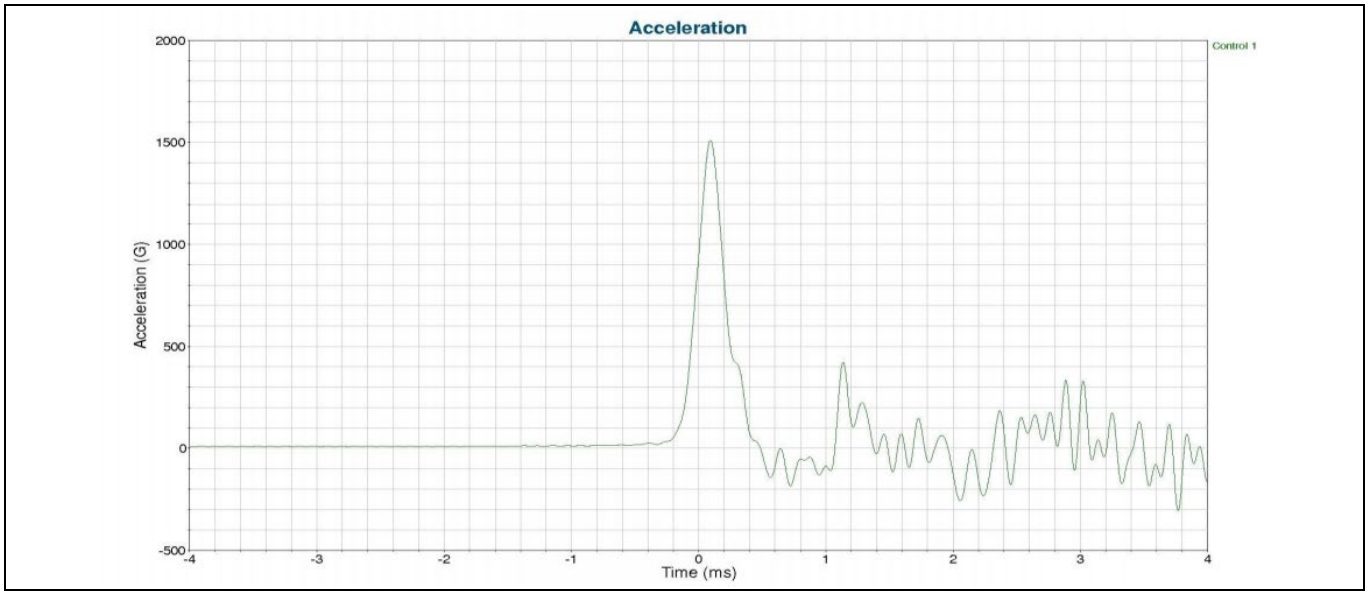


Figure 14 Mechanical Shock X-Axis Graph

Then, temperature cycling was performed in accordance with ECSS-Q-ST-70-08. The test conditions were -55 °C to +100 °C with a ramp of up to 10 °C/minute and a minimum of 15-minute dwell time for 500 cycles. The packages were inspected at 100 cycle intervals to ensure the parts passed before moving onto to the next stage of qualification.

The final step to board-level qualification is conducted per MIL-STD-750 TM2039 using FR-4 PCB. This includes temperature cycling, PCB flex, PCB twist and visual inspection (see summary in Table 3).

Table 3 Board-level testing per MIL-STD-750 TM2039

Sequence	Test	Test conditions
1	Temperature cycle 1	MIL-STD-750 TM1051 10 cycles, -20°C to +125°C
2	Temperature cycle 2	MIL-STD-750 TM1051 10 cycles, -40°C to +125°C
3	Temperature cycle 3	MIL-STD-750 TM1051 10 cycles, -60°C to +125°C
4	Temperature cycle 4	MIL-STD-750 TM1051 10 cycles, -65°C to +125°C
5	PCB flex	MIL-STD-750 TM2039
6	PCB twist	MIL-STD-750 TM2039
7	Visual inspection	MIL-STD-750 TM2071

6 Qualification Results

This section describes the results of the qualification testing performed. The package goes through the qualifications to verify the Finite Element Analysis simulations are accurate and the package is sufficiently durable. After passing the random vibration, mechanical shock, and temperature cycling tests, some packages were removed from the qualification PCB to undergo further testing. The removed packages were screened in accordance with external visual per MIL-STD-883 TM 2009, then underwent fine and gross leak testing in accordance with MIL-STD-750 TM 1071. All the removed packages passed all three tests, ensuring the integrity of the SMD-0.1.

Additional samples remained on the PCB and were cross-sectioned, and reviewed against ECSS-Q-ST-70-38. Acceptance criteria included no cracks longer than 25% of the lap connection of the solder joint between the package and PCB, and no cracks in the ceramic. Figure 15 shows the SMD-0.1 after cross-sectioning.

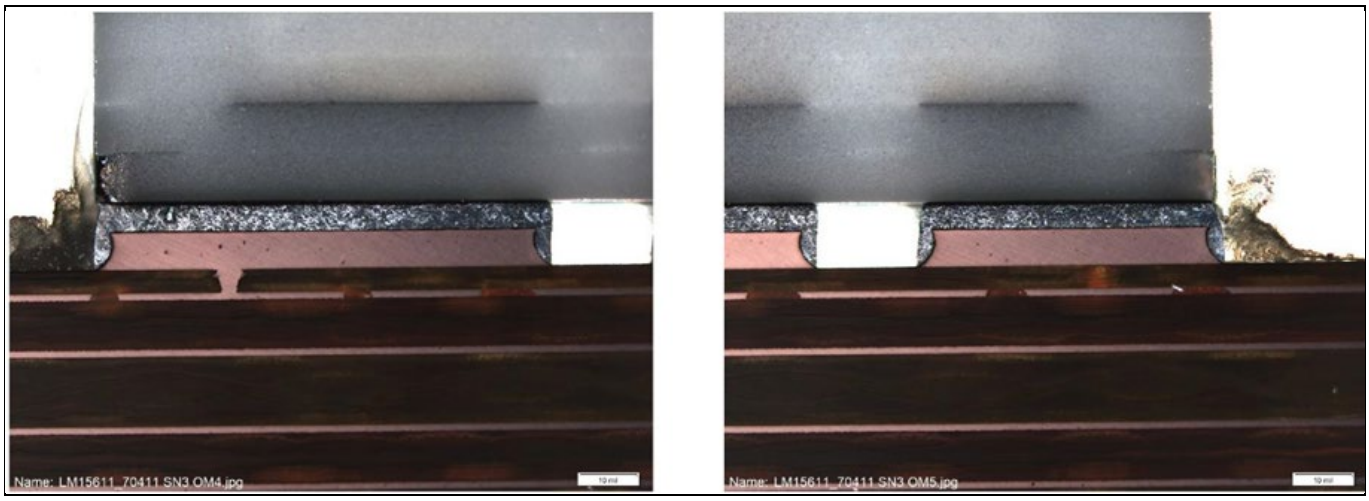


Figure 15 SMD-0.1, post-qualification external visual of solder interface of package to PCB (no cracks)

7 Soldering and assembly recommendations

The application of the SMD-0.1 is like any other surface mount device, it is meant to be assembled directly on a PCB. The SMD-0.1 is specifically designed for the R9 die size 1, however, it could also be used by other diodes that would fit in the package. The SMD-0.1 would work well with the most common PCB materials, such as FR-4 and polyimide. The most commonly used solder to mount the SMD-0.1 is Sn63Pb37. The suggested solder pad specifications for PCB layout are shown in Figure 16 . These solder pad layouts, PCB type, and solder worked well for us during assembly and testing.

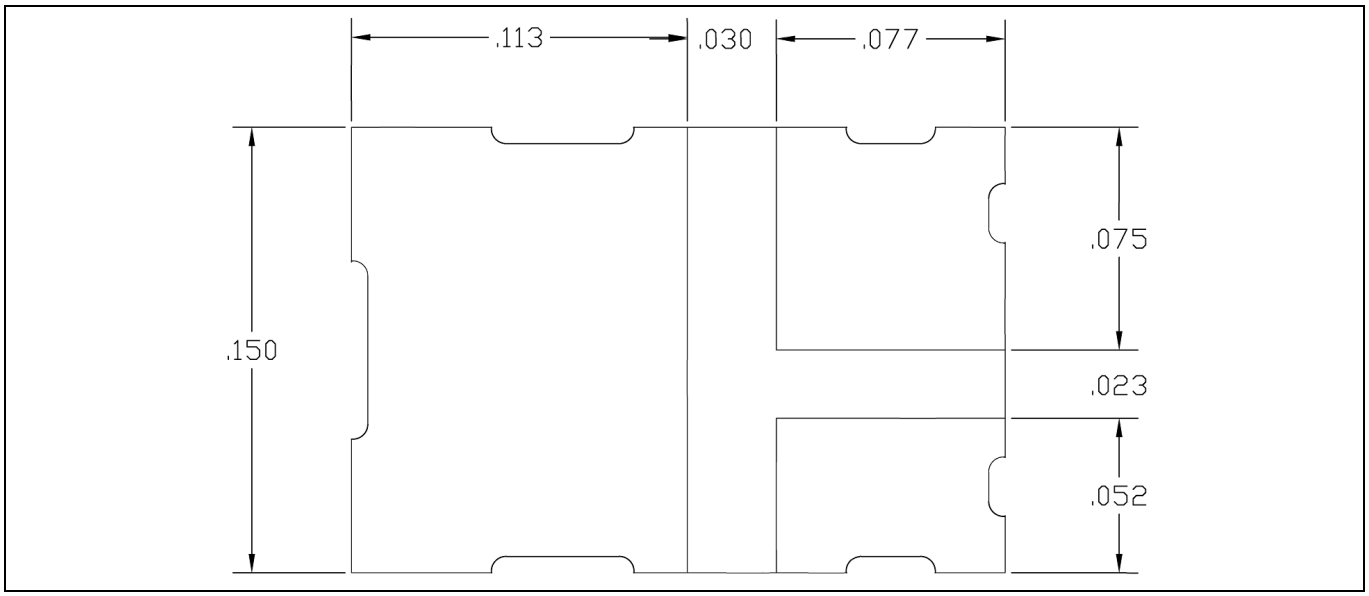


Figure 16 SMD-0.1, nominal, suggested solder pads, dimensions in inch

The product nomenclature for SMD-0.1 power discrete devices includes the term “NPC” (please check IR HiRel’s web site for complete listing of product nomenclatures). The product nomenclature of QPL devices includes the term “U9C” as suffix.

8 Conclusion

After extensive design and testing, the SMD-0.1 fulfills its role of housing the R9 die size 1. The SMD-0.1 can withstand the CTE problems that all surface mounted products must face. SMD-0.1 is a smaller package than previous power SMD packages and is also capable of handling higher current and power. More information about the parts being offered in SMD-0.1 package can be found on the Infineon website.

Revision history

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