Tire pressure monitoring sensor

Features

- Patented Glass-Silicon-Glass MEMS pressure sensor with best-in-class media compatibility
- High pressure measurement range up to 1600kPa
- Z-axis accelerometer for motion detection, angular position sensing, and contact patch length estimation
- Industry-standard power efficient 32 bit ARM® Cortex®(*) M0+ microcontroller
- 19 kbyte of flash memory for the application code and/or user data storage; also usable for a bootloader
- 1 kB RAM plus 192 bytes of retention RAM
- Best in class lifetime charge consumption

(*) ARM and Cortex are trademarks of ARM limited, UK

AEC Qualified

RoHS

ISO 26262 ready

Potential applications

- Valve based TPMS Modules
- On-Tire TPMS Module
- Intelligent Tire

for OEM and Aftermarket

Product validation

Product validation according to AEC-Q100, Grade 1. Qualified for automotive applications.

Description

The SP49 provides a very high level of integration, and is optimized to perform all of the functions necessary to implement a state-of-the-art Tire Pressure Monitoring System (TPMS) sensor module. With its integrated microcontroller, sensors, and convenient peripherals, the SP49 needs the addition of only a few passive components to form a complete TPMS sensor assembly. The device has been designed for lowest charge consumption making it ideal for battery powered applications.

Product Name	Ordering Code	Marking	Package	Product Code
SP49T-05-12	SP005957469	SP49T	PG-DSOSP-14-84	0x4400 ... 0x44FF(*)

(*) The product code can have any value within this range

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1 Specification

1.1 Absolute Maximum Ratings

Any stress exceeding the specified absolute maximum ratings may cause permanent damage to the device. The values given are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Max. Supply voltage	V_{DD_MAX}	-0.3		3.8	V	Voltage at VDDBAT pin
ESD robustness HBM	V_{HBM}	±2000			V	All pins tested according to AEC-Q100-002
ESD robustness CDM	V_{CDM}	±500			V	Non-corner pins tested according to AEC-Q100-011
ESD robustness CDM, Corner Pins	$V_{CDM\ C}$	±750			V	Corner pins tested according to AEC-Q100-011
Transient Latch-up Current	I_{LU}	±100			mA	Maximum transient current at any pin according JEDEC78 class II level A
Input voltage at PP0, PP1, PP2, PP3	V_{IN_PPx}	-0.3		V_{DD}+0.3	V	
Input voltage at Analog In	$V_{Analog\_In\_Max}$	-0.3		1.6	V	Voltage at PP0 or PP3 if configured as Analog In.
Input voltage at LFP, LFN, XIN	V_{LF_XIN}	-0.3		+1.8	V	
Differential Input voltage at LFP, LFN	V_{DIFF_LF}	-0.3		+0.3	V	
Peak Voltage PAOUT pin	V_{PAOUT_PEAK}			8	V	The matching network must be designed such that the peak-voltage at PA does not exceed this value.
Output Short-Circuit Capability	V_{SC}	0		3.8	V	Short to VDD, GND or neighbor pin for max. 10min at VDD=3.8V. Note: VDDREG and XOUT must not be shorted to VDD
DC Current	I_{DC}	-10		10	mA	Maximum Input/Output Current at any Pin
Maximum Pressure	p_{MAX}			2500	kPa	Static
Max. Static Acceleration	a_{MAX}			3500	g	24 hour continuously for +-x/+-y/+-z respectively

(table continues...)

Table 1 (continued) Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Mechanical shock	a_{SHOCK}			6000	g	0.3 ms half sine pulses. 5 shocks in ±x, ±y, and ±z direction (30 shocks in total) Device unpowered.
Storage temperature	$T_{STORAGE}$	-50		150	°C	Maximal 1000 hours accumulated over lifetime between 125°C and 150°C. Maximum 1000 hours between -40°C and -50°C. Device not powered. Temperature cycling only allowed between -40°C and 125°C.

1.2 Operating Range

The operating range defines the ambient conditions where the device operates as specified. Certain specified parameters in this document may depend on additional operating conditions. These additional conditions are indicated in the corresponding sections.

Table 2 Operating Range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply Voltage Range	V_{DD}	V_{UVR_A}		3.6	V	Device not in Power-Down State.
Supply Voltage Range in PD	V_{DD}	V_{UVR_PD}		3.6	V	Device in Power-Down State.
Ambient Temperature	T_{OP}	-40		125	°C	
Flash Programming Temperature Range	T_{FLASH}	-20		90	°C	Temperature range for flash erasing/programming.
Extended Temperature Range	T_{EXT}	-50		150	°C	Thermal shutdown functional. VDD=1.8 to 3.3V. Exposure to 125°C .. 150°C maximum 24h over lifetime.
z-Axis Acceleration	a_{OP}			+/-1600	g	Exceeding this acceleration will result in a higher pressure error as specified.
Programming bit rate	BR_{PROG}			1000	kbit/s	Bit rate for programming/ debugging via serial interface

(table continues...)

Table 2 (continued) Operating Range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External Capacitor at VDDBAT	C_{VDD_BAT}		10		nF	
External Capacitor at VDDREG	C_{VDD_REG}	7	10	13	nF	
External Capacitor at VDDPA	C_{VDD_PA}	7	10	13	nF	Capacitor only needed if pin 13 is used as VDDPA
PP0 Input Frequency Tolerance	TOL_{fin_PP0}	-500		500	ppm	Tolerance relating to a selected input frequency

1.3 Characteristics

1.3.1 Pressure Sensor

The specified pressure measurement error includes random error (noise) and is based on averaging 4 raw values for each measurement. Exceeding the maximum z-axis acceleration as defined in the operating range will result in a higher pressure measurement error than specified.

Table 3 Pressure Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pressure Range	p_{RANGE}	100		1600	kPa	Absolute Pressure
Pressure RMS Noise	p_{NOISE}			1.35	LSB	Each pressure reading is the mean of 4 ADC raw readings.
Pressure ADC resolution	p_{ADC_RES}			0.7	kPa/LSB	Refers to ADC raw readings
Measurement Error 100-1100kPa Temp1	$p_{ERROR\ 100\text{-}1100,\ T1}$	-19		+19	kPa	T_{OP} = 0°C to +60°C
Measurement Error 100-1100kPa Temp2	$p_{ERROR\ 100\text{-}1100,\ T2}$	-25		+25	kPa	T_{OP} = +60°C to +100°C
Measurement Error 100-1100kPa Temp3	$p_{ERROR\ 100\text{-}1100,\ T3}$	-30		+30	kPa	T_{OP} = +100°C to +125°C
Measurement Error 100-1100kPa Temp4	$p_{ERROR\ 100\text{-}1100,\ T4}$	-25		+25	kPa	T_{OP} = -20°C to 0°C
Measurement Error 100-1100kPa Temp5	$p_{ERROR\ 100\text{-}1100,\ T5}$	-30		+30	kPa	T_{OP} = -40°C to -20°C
Measurement Error 1100-1400kPa Temp1	$p_{ERROR\ 1100\text{-}1400,\ T1}$	-25		+25	kPa	T_{OP} = 0°C to +60°C
Measurement Error 1100-1400kPa Temp2	$p_{ERROR\ 1100\text{-}1400,\ T2}$	-30		+30	kPa	T_{OP} = +60°C to +100°C

(table continues...)

Table 3 (continued) Pressure Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Measurement Error 1100-1400kPa Temp3	$p_{ERROR\ 1100\text{-}1400,\ T3}$	-35		+35	kPa	T_{OP} = +100°C to +125°C
Measurement Error 1100-1400kPa Temp4	$p_{ERROR\ 1100\text{-}1400,\ T4}$	-30		+30	kPa	T_{OP} = -20°C to 0°C
Measurement Error 1100-1400kPa Temp5	$p_{ERROR\ 1100\text{-}1400,\ T5}$	-35		+35	kPa	T_{OP} = -40°C to -20°C
Measurement Error 1400-1600kPa Temp1	$p_{ERROR\ 1400\text{-}1600,\ T1}$	-35		+35	kPa	T_{OP} = 0°C to +125°C
Measurement Error 1400-1600kPa Temp2	$p_{ERROR\ 1400\text{-}1600,\ T2}$	-40		+40	kPa	T_{OP} = -40°C to 0°C

1.3.2 z-Axis Acceleration Sensor

Total acceleration error specifications include random error (noise). They are based on averaging 16 raw values for each measurement. The total acceleration error specification is valid under the condition that an appropriate auto-offset algorithm is used during the whole lifetime of the product. Further information about auto-offset calibration see the SP49 User Manual.

Note that the error specification requires proper acceleration measurement range selection (low range if $|a_{IN\_Z}| \leq$ 400g, high range if 400g < $|a_{IN\_Z}| \leq$ 600g), see also the SP49 User Manual.

Table 4 z-axis Acceleration Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Z-Acceleration Range	a_{IN_Z}	-600		+600	g	Measurement range for absolute acceleration
Total Acceleration Error, 20g, LT	$a_{ERR\_TOT\_20\_LT}$	-3.0		+3.0	g	$\|a_{IN\_Z}\|$ = 0g to 20g, T_{OP} = -40°C to 90°C
Total Acceleration Error, 20g, HT	$a_{ERR\_TOT\_20\_HT}$	-5.0		+5.0	g	$\|a_{IN\_Z}\|$ = 0g to 20g, T_{OP} = 90°C to 125°C
Total Acceleration Error, 100g, LT	$a_{ERR\_TOT\_100\_LT}$	-5.0		+5.0	g	$\|a_{IN\_Z}\|$ = 20g to 100g, T_{OP} = -40°C to 90°C
Total Acceleration Error, 100g, HT	$a_{ERR\_TOT\_100\_HT}$	-7.0		+7.0	g	$\|a_{IN\_Z}\|$ = 20g to 100g, T_{OP} = 90°C to 125°C
Total Acceleration Error, 200g, LT	$a_{ERR\_TOT\_200\_LT}$	-9.0		+9.0	g	$\|a_{IN\_Z}\|$ = 100g to 200g, T_{OP} = -40°C to 90°C

(table continues...)

Table 4 (continued) z-axis Acceleration Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total Acceleration Error, 200g, HT	$a_{ERR\_TOT\_200\_HT}$	-11.0		+11.0	g	$\|a_{IN\_Z}\|$ = 100g to 200g, T_{OP} = 90°C to 125°C
Total Acceleration Error, 400g, LT	$a_{ERR\_TOT\_400\_LT}$	-19.0		+19.0	g	$\|a_{IN\_Z}\|$ = 200g to 400g, T_{OP} = -40°C to 90°C
Total Acceleration Error, 400g, HT	$a_{ERR\_TOT\_400\_HT}$	-20.5		+20.5	g	$\|a_{IN\_Z}\|$ = 200g to 400g, T_{OP} = 90°C to 125°C
Total Acceleration Error, 600g	$a_{ERR\_TOT\_600}$	-40		40	g	$\|a_{IN\_Z}\|$ = 400g to 600g, T_{OP} = -40°C to 125°C
Total Acceleration Offset Drift	a_{OFF_DRIFT}	-5		5	g	Valid for all a_{in} ranges.
Acceleration ADC resolution	a_{ADC_RES}			0.175	g/LSB	a_{IN_Z+} = -100g ...+400g, a_{IN_Z-} = -400g ...+100g; Refers to ADC raw readings
Acceleration High Range ADC Resolution	$a_{ADC\_RES\_high}$			0.35	g/LSB	Refers to ADC Readings. Applies if High Acceleration Range is selected.
Acceleration RMS Noise	a_{NOISE}			0.9	LSB	$\|a_{IN\_Z}\|$ <= 600g. Each acceleration reading is the mean of 16 ADC raw readings. No external noise sources present.
Accelerometer resonance frequency	f_{RES_ACC}	5.1	6	6.9	kHz	Mechanical excitation of the device in this frequency range must be avoided (e.g. PCB sawing process)
Motion detection range	$a_{IN\_Z\_MD}$	±600		±1600	g	Acceleration signal used for motion detection only.
z-Accelerometer x-Axis Cross Sensitivity	$a_{Z\_CROSS\_X}$		5	9	%	
z-Accelerometer y-Axis Cross Sensitivity	$a_{Z\_CROSS\_Y}$			1.1	%	

1.3.3 z-Axis Acceleration FIR filter

The following specifications apply to the z-axis Acceleration sensor, if the function Lib_Meas_Acc_FIR is used to obtain the raw acceleration value.

Table 5 z-Axis Acceleration FIR filter

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Accelerometer Signal Attenuation at 25Hz	Att_{ACC_25Hz}		0.003	0.5	dB	
Accelerometer Low Pass Cut-off Frequency	f_{3dB_LP}		830	950	Hz	At -3dB. Valid only if WBC is activated.
Accelerometer Low Pass Attenuation at HF	Att_{LP_HF}	30			dB	$f_{signal} \geq 2500Hz$
Accelerometer Low Pass Attenuation at LF	Att_{LP_LF}			1.5	dB	$f_{signal} \leq 500Hz$. Valid only if WBC is activated.

1.3.4 Temperature Sensor

Table 6 Temperature Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Temperature Measurement Range	T_{MEAS_RANGE}	-40		125	°C	
Temperature Sensor Total Error	T_{ERR}	-3		3	°C	The measurement error is understood as total error, including random error (noise)
Temperature Sensor Total Error, RT	T_{ERR_RT}	-2		2	°C	T_{OP} = -20°C to +90°C
Temperature RMS Noise	T_{NOISE}			0.25	°C	Refers to compensated temperature values. Random Error is included in Total Error.
Temperature Sensor Physical Resolution	T_{RES}		0.2	1	°C	

1.3.5 Battery Sensor

Table 7 Battery Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage Measurement Range	V_{RANGE}	V_{UVR_A}		3.3	V	see section Under Voltage Reset Threshold for V_{UVR_A}

(table continues...)

Table 7 (continued) Battery Sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage Measurement Total Error	V_{BAT_ERR}	-3		3	%	V_{DD} = V_{UVR_A} to V_{DD_MAX}
Voltage Sensor Physical Resolution	V_{RES}			1.3	mV	Refers to ADC raw readings

1.3.6 Thermal Shutdown

Voltage operating range for active state V_{DD_AS} and extended temperature range T_{EXT} applies for Thermal Shutdown.

Table 8 Thermal Shutdown

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal Shutdown Entry HOT	T_{HOT_E}	119	122	125	°C	
Thermal Shutdown Release HOT	T_{HOT_REL}	115	120	123.5	°C	
Thermal Shutdown Hysteresis	T_{HYST}	1.5		4	°C	
Thermal Shutdown Entry COLD	T_{COLD_E}	-40	-37	-34	°C	
Thermal Shutdown Release COLD	T_{COLD_REL}	-38.5	-35	-30	°C	

1.3.7 General Purpose Digital I/O Pins

Table 9 General Purpose Digital I/O Pins

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	$0.8V_{DD}$			V	1)
Input Low Voltage	V_{IL}			$0.2V_{DD}$	V	1)
Output High Voltage	V_{OH}	V_{DD} -0.3			V	I_{load} = 1mA
Output Low Voltage	V_{OL}			0.3	V	I_{load} = -1mA
PP0/PP1/PP3 Pin Input Capacitance	C_{IN}			10	pF	
PP2 Pin Input Capacitance	C_{IN_PP2}			20	pF	
PP0, PP1, PP3 Leakage Current	$I_{IN\_PP0\_1\_3}$	-1		1	µA	PP0, PP1, PP3 configured as input

(table continues...)

Table 9 (continued) General Purpose Digital I/O Pins

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PP2 Leakage Current	I_{IN_PP2}	-1		1	µA	T_{OP} = -40°C to 90°C; PP2 configured as input
PP2 Leakage Current, HT	$I_{IN\_PP2\_HT}$	-2		2	µA	T_{OP} = 90°C to 125°C; PP2 configured as input
Resistance of low-side power switch	R_{LSPS}			5	Ohm	T_{OP} = -40°C to 90°C; low-side power switch on PP2 enabled and active
I2C Low Datarate	DR_{I2C_low}		100		kbit/s	2) , 3)
I2C Medium Datarate	DR_{I2C_med}		400		kbit/s	2) , 3) , 4)
I2C High Datarate	DR_{I2C_HIGH}			1000	kbit/s	2) , 3) , 5)
PP0 Input Frequency Range	f_{in_PP0}	1		26	MHz	
Equivalent pull resistor	R_{PULL_3V}	15		70	kΩ	V_{IN_PPx} = 1.5V, V_{DD}=3V; Valid for pull-down at PP0, PP1, PP2, PP3. Valid for pull-up at PP2, PP3.
Equivalent Pull Up Resistors at PP0 and PP1	R_{PULLUP}	5.9	8.4	11	kΩ	

1) If the digital I/O pins are used in the application, for lowest charge consumption the input high voltage should be V_{DD}-0.05V or higher. The input low voltage should be maximal 0.05V. If the digital I/O Pins are left open with the internal pull resistors activated the above critera for lowest charge consumption are fulfilled.
2) For I2C operation PP0 is configured as SCL and PP1 is configured as SDA
3) Depending on capacitive load and data rate external pull-up resistors may be required. The correct value of the pull-ups is in the responsibility of the system integrator.
4) If only internal pull-up resistors are used the maximal load capacitance at either pin is 32pF at 400 kbit/s
5) Even with external pull-up resistors the maximal load capacitance at either pin is 80pF at 1000 kbit/s

1.3.8 Analog Input

The following specification applies to measurements of an external analog voltage connected to PP0 or PP3 pin.

Table 10 Analog Input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Analog Voltage Range	V_{ANALOG_IN}	0		1.4	V	
Low Voltage Measurement Error	V_{ERROR_LOW}	-1.5		+1.5	mV	V_{ANALOG_IN} = 0 to 37.5 mV ; 95% of all measurements
Voltage Measurement Error	V_{ERROR}	-4		+4	%	V_{ANALOG_IN} = 37.5 mV to 1.4V ; 95% of all measurements

(table continues...)

Table 10 (continued) Analog Input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage Measurement Resolution	V_{ANALOG_RES}		0.4	1	mV/LSB	

1.3.9 Voltage Monitoring and Power On

Table 11 Voltage Monitoring and Power On

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Under Voltage reset	V_{UVR_A}	1.6		1.7	V	Measured at VDDBAT pin. Applies only in Run State, Idle, and if RF transmission is ongoing. Disabled in PD, Stand-By, and TSD.
Under Voltage reset in Power Down	V_{UVR_PD}	1.2		1.6	V	Measured at VDDBAT pin. Applies in all states.
Reset release threshold	V_{THR}	1.8		1.9	V	Applies for a Reset triggered by under-voltage or power-on reset. Device releases from Reset when voltage at VDDBAT pin exceeds V_{THR}.
TX Undervoltage Warning Level	V_{TX_MIN}	1.8	1.85	1.9	V	t_{drop} > 10µs; A flag is set if voltage at VDDBAT pin falls below V_{TX_MIN} during RF transmission.
TX Voltage Monitoring Threshold	V_{TX_MON}	1.7	1.75	1.8	V	RF-PA will be shut off if the voltage VDDBAT falls below this threshold.

1.3.10 Flash Memory

Table 12 Flash Memory

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Flash Retention Time	t_{RET_FLASH}	10			years	Defect rate < 1ppm over lifetime, N_{write} cycles not exceeded
Flash write cycles	N_{WRITE}	100				T_{OP} = -20°C to 90°C; No more than N_{WRITE} cycles allowed
Flash Programming Time	t_{FLASH_PROG}			3.5	s	Time for programming 19 kbyte flash

1.3.11 Supply Currents

All currents at 3.0V supply voltage.

Table 13 Supply Currents

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current in Power Down, LT	$I_{PWD\_3V\_LT}$		150	500	nA	T_{OP} = -40°C, V_{DD} = 3.0V
Supply current in Power Down, RT	$I_{PWD\_3V\_RT}$		240	500	nA	T_{OP} = +25°C, V_{DD} = 3.0V
Supply current in Power Down, MT	$I_{PWD\_3V\_MT}$		1	2.5	µA	T_{OP} = +70°C, V_{DD} = 3.0V
Supply current in Power Down, HT	$I_{PWD\_3.6V\_HT}$		9	20	µA	T_{OP} = 125°C, V_{DD} = 3.6V
Supply current in Stand-By, LT	I_{STBY_LT}		2.3	6	µA	T_{OP} = -40°C, V_{DD} = 3.0V
Supply current in Stand-By, RT	I_{STBY_RT}		2.3	6	µA	T_{OP} = 25°C, V_{DD} = 3.0V
Supply current in Stand-By, HT	I_{STBY_HT}		32	82	µA	T_{OP} = +125°C, V_{DD} = 3.6V
Supply Current in Thermal Shutdown, LT	I_{TSD_LT}		61	85	µA	T_{OP} = -40°C, V_{DD} = 3.0V; Average current for clocked operation is I_{TSD_avg}= I_{PWD} + (I_{TSD} -$_{PWD}$) * 2.9/16/ Interval_Mul_16ms
Supply Current in Thermal Shutdown, HT	I_{TSD_HT}		85	116	µA	T_{OP} = +125°C, V_{DD} = 3.0V; Average current for clocked operation is I_{TSD_avg}=I_{PWD}+(I_{TSD}-I_{PWD})*2.9/16/Interval_Mul_16ms
Supply current in IDLE, LT	I_{IDLE_LT}		370	460	µA	T_{OP} = -40°C, V_{DD} = 3.0V
Supply current in IDLE, RT	I_{IDLE_RT}		370	460	µA	T_{OP} = 25°C, V_{DD} = 3.0V
Supply current in IDLE, HT	I_{IDLE_HT}		450	600	µA	T_{OP} = +125°C, V_{DD} = 3.6V
Supply current in RUN state, LT	I_{RUN_LT}		1.57	1.8	mA	T_{OP} = -40°C, V_{DD} = 3.0V
Supply current in RUN state, RT	I_{RUN_RT}		1.57	1.8	mA	T_{OP} = +25°C, V_{DD} = 3.0V
Supply current in RUN State, HT	I_{RUN_HT}		1.66	2	mA	T_{OP} = +125°C, V_{DD} = 3.6V

(table continues...)

Table 13 (continued) Supply Currents

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LF-receiver supply current in CDM (digital filter off), LT	$I_{LF\_CDM\_LT}$		2.8	4	µA	T_{OP} = -40°C, V_{DD} = 3.0V; 100% receiver duty cycle
LF-receiver supply current in CDM (digital filter off), RT	$I_{LF\_CDM\_RT}$		3.3	4	µA	T_{OP} = +25°C, V_{DD} = 3.0V; 100% receiver duty cycle
LF-receiver supply current in CDM (digital filter off), HT	$I_{LF\_CDM\_HT}$		7.7	30	µA	T_{OP} = +125°C, V_{DD} = 3.6V; 100% receiver duty cycle
LF-receiver supply current in CDM (digital filter on), LT	$I_{LFCDFilter\_LT}$		3.2	6	µA	T_{OP} = -40°C, V_{DD} = 3.0V; 100% receiver duty cycle
LF-receiver supply current in CDM (digital filter on), RT	$I_{LFCDFilter\_RT}$		4	6	µA	T_{OP} = +25°C, V_{DD} = 3.0V; 100% receiver duty cycle
LF-receiver supply current in CDM (digital filter on), HT	$I_{LFCDFilter\_HT}$		8.2	30	µA	T_{OP} = +125°C, V_{DD} = 3.6V; 100% receiver duty cycle
LF-receiver supply current in DRM, LT	$I_{LF\_DRM\_LT}$		3.6	6	µA	T_{OP} = -40°C, V_{DD} = 3.0V; 100% receiver duty cycle
LF-receiver supply current in DRM, RT	$I_{LF\_DRM\_RT}$		3.85	6	µA	T_{op} = +25°C, V_{DD} = 3.0V; 100% receiver duty cycle
LF-receiver supply current in DRM, HT	$I_{LF\_DRM\_HT}$		8.3	30	µA	T_{OP} = +125°C, V_{DD} = 3.6V; 100% receiver duty cycle
Supply current at RF transmission CW or FSK	I_{RFTX}		5.5	6.7	mA	f_{TX} = 315MHz, f_{TX} = 434MHz
Inrush Current	I_{INRUSH}			8	mA	Peak supply current drawn from battery during startup of internal regulators; Capacitors C_{VDDBAT} ≥ 10nF nom, C_{VDDREG} = 10nF nom[1)]
Current during flash write access	I_{FLASH_WRITE}			6	mA	T_{OP} = +25°C, V_{DD} = 3.0V
Current consumption during undervoltage	I_{UV}		62		µA	T_{OP} = 125°C, V_{DD} = 1.6V; Device in reset.

1) After internal voltage regulator start-up phase, due to internal switching events short, i.e. <<1µs, peak current pulses above 8mA can be generated. If these peaks shall be suppressed w.r.t. the battery, a C_{VDDBAT} of several hundred nF may be necessary.

1.3.12 LF Receiver Operating Range

Table 14 LF Receiver Operating Range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LF Carrier Frequency	f_{LF}	115		135	kHz	Sine wave, LF sensitivity levels are only valid for the specified carrier frequency range
LF Data Rate	DR_{LF}	3.8		4.2	kbit/s	
LF Data Rate Tolerance	TOL_{LF_DR}	-3		+3	%	
LF Frequency Detector Range	f_{DISCR_RANGE}	3			MHz	
LF Data Duty Cycle	DC_{LF}	45	50	55	%	

1.3.13 LF Receiver

Table 15 LF-Receiver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LF Input Differential Capacitance	C_{LF_DIFF}	2.5	3.9	10	pF	f_{LF} = 125kHz
LF Input differential Impedance	R_{LF_DIFF}	1			MΩ	f_{LF} = 125kHz, T_{OP} = -40°C to 90°C; AGC inactive
LF Input Differential Impedance, HT	$R_{LF\_DIFF\_HT}$	1-(T/°C - 90)/70			MOhm	f_{LF} = 125kHz, T_{OP} = 90°C to 125°C; AGC inactive
LF-Receiver Settling Time	$t_{ON\_SETTLING}$		3.0	3.9	ms	
Carrier Detector Filter Time	t_{CD}	700	1000	1300	µs	
LF Frequency Discriminator always accepted	f_{CD_DET}	112.5	125	137.5	kHz	Accepted LF frequency, in case LF carrier frequency discriminator is enabled
LF Frequency Discriminator always rejected low	$f_{CD\_NODET\_LOW}$	80			kHz	
LF Frequency Discriminator always rejected high	$f_{CD\_NODET\_HIGH}$			190	kHz	f_{LF} < 3MHz
Data Reception Preamble Time	$t_{SETTLING\_PRE}$	2			ms	Minimum duration of preamble for telegram reception

(table continues...)

Table 15 (continued) LF-Receiver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LF Carrier No Detect Level 2, RT	$S_{NODET\_CDM\_2\_RT}$	0.6			mVpp	T_{OP} = 0°C to +50°C
LF Carrier No Detect Level 2	$S_{NODET\_CDM\_2}$	0.5			mVpp	T_{OP} = -20°C to +90°C
LF Carrier No Detect Level 2, LT & HT	$S_{NODET\_CDM\_2\_LT\&HT}$	0.3			mVpp	T_{OP} = -40°C to -20°C and T_{OP} = +90°C to +125°C
LF Carrier Detect Level 2, RT	$S_{DET\_CDM\_2\_RT}$			2.15	mVpp	T_{OP} = 0°C to +50°C
LF Carrier Detect Level 2	$S_{DET\_CDM\_2}$			2.5	mVpp	T_{OP} = -20°C to +90°C
LF Carrier Detect Level 2, LT & HT	$S_{DET\_CDM\_2\_LT\&HT}$			3.0	mVpp	T_{OP} = -40°C to -20°C and T_{OP} = +90°C to +125°C
LF Data Reception No Detect Level 0, RT	$S_{NODET\_DRM\_0\_RT}$	0.6			mVpp	T_{OP} = 0°C to +50°C
LF Data Reception No Detect Level 0	$S_{NODET\_DRM\_0}$	0.5			mVpp	T_{OP} = -20°C to +90°C
LF Data Reception No Detect Level 0, LT & HT	$S_{NODET\_DRM\_0\_LT\&HT}$	0.3			mVpp	T_{OP} = -40°C to -20°C and T_{OP} = +90°C to +125°C
LF Data Reception Detect Level 0, RT	$S_{DET\_DRM\_0\_RT}$			2.15	mVpp	T_{OP} = 0°C to +50°C
LF Data Reception Detect Level 0	$S_{DET\_DRM\_0}$			2.5	mVpp	T_{OP} = -20°C to +90°C
LF Data Reception Detect Level 0, LT & HT	$S_{DET\_DRM\_0\_LT\&HT}$			3.0	mVpp	T_{OP} = -40°C to -20°C and T_{OP} = +90°C to +125°C
LF Receiver Dynamic Range	DYN_{LF}	75			dB	Defined at LF differential input pins.

1.3.14 RF Transmitter

The RF transmitter specification is valid at 50 Ω with an apropriate matching network between PAOUT pin and 50 Ω point.

Table 16 RF Transmitter

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RF Low TX Frequency	f_{TX_315}	314	315	316	MHz	
RF High TX Frequency	f_{TX_433}	433	433.92	435	MHz	

(table continues...)

Table 16 (continued) RF Transmitter

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
FSK deviation	f_{DEV_FSK}	35	80	100	kHz	peak to peak
Transmitter Data Rate	DR_{TX}	1		20	kbit/s	
Transmitter High Data Rate	DR_{TX_HIGH}	38.01	38.4	38.79	kBit/s	only for GFSK Modulation
RF Data Rate Tolerance	TOL_{DR}	-1		1	%	
RF Output Power at 50 Ohm, RT	$P_{RF50\Omega\_RT}$	4	5	6	dBm	V_{DD} = 2.5V to 3.6V, T_{op} = +25 to +60 °C
RF Output Power at 50 Ohm	$P_{RF50\Omega}$	3		7	dBm	T_{op} =-40 to 0 °C, V_{DD} = V_{TX_MIN} to 3.6V; T_{op} = +0 to +125 °C, V_{DD} = 2.5V to 3.6V
RF High Output Power at 50 Ohm	P_{RF_HIGH}	10			dBm	V_{DD} > 2.7V, T_{op} = 25°C [1)]
TX Modulation Duty Cycle	DC_{TX_DATA}	45	50	55	%	Valid for ASK and FSK
TX ASK Modulation Depth	MD_{TX_ASK}	90		100	%	Definition: $MD_{TX\_ASK} = (V_{High} - V_{Low})/V_{High}$
2nd Harmonic Attenuation	ATT_{2nd}	20			dBc	
Harmonics Attenuation	A_{TT_HAR}	35			dBc	Not valid for 2nd harmonic
Xtal Spurs Attenuation	ATT_{SP_XTAL}	50			dBc	
Attenuation of all other Spurs	ATT_{SP_OTHERS}	65			dBc	Below 4.4 GHz
Carrier Frequency Drift	C_{FDF_TX}	-10		10	ppm	Crystal tolerance not included. Valif for f_{TX} and f_{dev_FSK}.
Occupied bandwidth Korea (MIC 2007-63)	O_{BW_K}			180	kHz	f_{DEV_FSK} = 90 kHz p-p, DR_{TX} = 19200 bps; RBW = 10 KHz, VBW =Auto, Span = 750 KHz, Max Hold, Peak detector enabled, Sweep points=1000 "Sweep count" option disabled For GFSK or ASK.

(table continues...)

Table 16 (continued) RF Transmitter

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Occupied bandwidth Japan (ARIB STD-T93)	O_{BW_J}			400	kHz	f_{DEV_FSK} = 90 kHz p-p, DR_{TX} = 9600 bps; RBW =30 KHz, VBW =Auto, Span = 3500 KHz, Max Hold, Peak detector enabled, Sweep points=1000 "Sweep count" option disabled. For GFSK or ASK.
PLL lock time	t_{PLL_LOCK}			100	µs	

1) In order to achieve the high RF output power the following conditions are required: the voltage regulator at VDDPA is bypassed, all 16 PA stages are activated, and an appropriate antenna matching circuit is used. The compliance to regional RF regulations is in the responsibility of the integrator.

1.3.15 Crystal Oscillator

Table 17 Crystal Oscillator

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Crystal frequency	f_{XTAL}	25.920	26	26.080	MHz	
Crystal Oscillator Startup Time	t_{XTAL_START}			1	ms	
Crystal Oscillator Drive Current	I_{XTAL_DRIVE}	1.5			mA	

1.3.16 RC Oscillators

Table 18 RC Oscillators

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LP-RC Total Tolerance	TOL_{LPRC_TOT}	-30		+30	%	Nominal frequency is 2.2kHz
LP-RC Temperature Drift	T_{D_LPRC}	-0.075		+0.075	%/K	
MP-RC Total Tolerance	TOL_{MPRC_TOT}	-5		+5	%	Nominal frequency is 90 kHz
MP-RC Temperature Drift	T_{D_MPRC}	-0.05		+0.05	%/K	
HP-RC Total Tolerance	TOL_{HPRC_TOT}	-8		+8	%	Nominal frequency is 12 MHz

(table continues...)

Table 18 (continued) RC Oscillators

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HP-RC Temperature Drift	T_{D_HPRC}	-0.05		+0.05	%/K	

1.3.17 Timing

Table 19 Timing

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power on time	t_{INI}			10	ms	Time from V_{DD} exceeding V_{THR} until serial interface ready.
Mode Selection Time	t_{MODE_SEL}	2	2.8	4	s	
Normal mode delay time	t_{NM_DELAY}			110	us	Time after I2C command for normal mode sent until application code start.
Idle Resume Time	t_{RES_IDLE}	0.3		0.45	µs	
Stand-By Resume Time	t_{RES_STBY}	263	283	303	µs	Time from resume event to execution of application code
Power Down Wake-Up Time	t_{WU}			4	ms	Time from any Wake-Up event in Power Down to application code execution start.
Watchdog timer period	t_{WD}	0.7	1	1.3	s	
Fast Acquisition Time	t_{ACQ_FAST}			65	µs	Refers to acquisition of 4 raw samples plus hardware averaging.
LF OFF-Time Tolerance	TOL_{t_OFF}	-5		5	%	$t_{OFF} \geq 50$ ms [1)]
Short LF ON-Time Tolerance	$TOL_{T\_ON\_S}$	-1		1	ms	$T_{ON} < 50$ ms [1)]
Long LF ON-Time Tolerance	$TOL_{T\_ON\_L}$	-2		2	%	$T_{ON} \geq 50$ms [1)]

1) The tolerance is valid after calibration of the timer with FW and as long as temperature does not drift more than 10°C after calibration.

1.3.18 Resume and Wake-Up Charge

Table 20 Resume and Wake-Up charge

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Wake-up charge, RT	Q_{WAKEUP_RT}		0.62	0.8	µC	T_{OP} = +25°C, V_{DD} = 3.0V; From wake-up event in Power-Down to application code execution start.
Wake-up charge	Q_{WAKEUP}			1	µC	From wake-up event in Power-Down to application code execution start
Resume from Stand-By charge, RT	$Q_{RESUME\_S\_RT}$			0.13	µC	T_{OP} = +25°C, V_{DD} = 3.0V; From resume event in Stand-By to application code execution start.
Resume from Stand-By charge	Q_{RESUME_S}			0.16	µC	T_{OP} = +125°C, V_{DD} = 3.0V; From resume event in Stand-By to application code execution start.
LPM Start-Up charge, RT	$Q_{STARTUP\_LPM\_RT}$		0.09		µC	T_{OP} = +25°C, V_{DD} = 3.0V; From LPM postcounter elapsed until LPM measurement start
LPM Start-Up charge	$Q_{STARTUP\_LPM}$		0.1		µC	T_{OP} = +125°C, V_{DD} = 3.0V; From LPM postcounter elapsed until LPM measurement start.

2 Pin Description

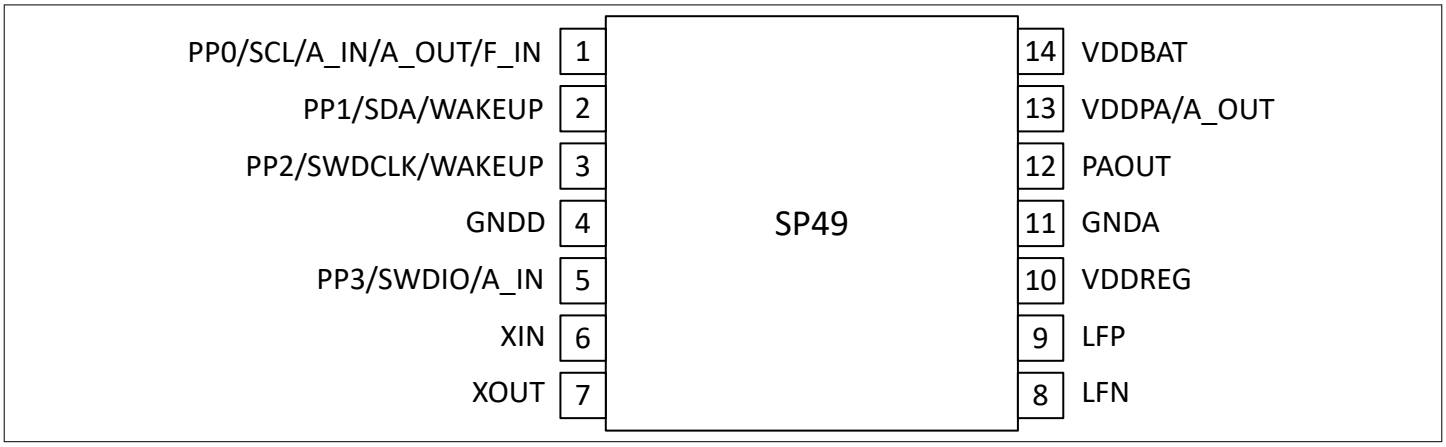

Figure 1 Pin Description

Table 21 Pin Description

Pin	Name	Description
1	PP0/SCL/A_IN/A_OUT / F_IN	General Purpose IO / I2C-SCL / Analog ADC Input /Analog Accelerometer or Pressure Sensor Output / External Reference Frequency Input
2	PP1/SDA/WAKEUP	General Purpose IO / I2C-SDA / External Wake-Up(*)
3	PP2/SWDCLK/WAKEUP	General Purpose IO / Serial Wire Debug Interface Clock/ External Wake-Up(*)
4	GNDD	Digital Ground
5	PP3 / SWDIO /A_IN	General Purpose IO / Serial Wire Debug Interface Input Output/ Analog ADC Input
6	XIN	Crystal Oscillator Input
7	XOUT	Crystal Oscillator Output
8	LFN	LF Receiver Input
9	LFP	LF Receiver Input
10	VDDREG	Internal Regulated Power Supply
11	GNDA	Analog and Power amplifier Ground
12	PAOUT	RF Power Amplifier Output
13	VDDPA/A_OUT	Regulated Power Supply for RF Power Amplifier / Analog Accelerometer or Pressure Output
14	VDDBAT	Power Supply

(*) Either PP1 **or** PP2 can be configured as external Wake-Up source.

3 Functional Description

3.1 Operating Modes

Apart from normal operating mode where the application code is executed the SP49 provides additional operating modes for debugging and programming. Program Mode is intended to be used at the customer's production line whereas Debug Mode is used for application code development.

Table 22 Operation modes

Operating mode	Device controlled by	Short Description	Entering method
Normal mode	Application code	Normal operating mode for execution of TPMS application software.	I2C command
Program mode	External I^2C Master	Used for programming application code, writing user configuration data and device locking. Additional I^2C commands available for diagnosis purposes, e.g. reading sensor measurement values.	I2C command
Debug mode	SWD interface	Used for application code development. Commands for RAM read/write, program counter manipulation, execute single step and run until breakpoint/interrupt are available. Device may also be programmed in Debug Mode.	Line reset sequence

After release from system reset the device waits for mode selection. Normal Mode or Program Mode are selected by a specific I^2C command at PP0/PP1. Debug Mode is entered by line reset sequence at PP2/PP3. If no valid mode selection information is received the device starts up in Normal Mode after a defined time-out. This time-out is called Mode Selection time (MST), see parameter t_{MS}.

The MST can be disabled by a certain voltage level applied at a selectable general purpose pin during Power On reset phase. If the MST is disabled the device immediately starts up with Normal Mode after reset release. In this case neither Debug Mode nor Program Mode can be entered.

The voltage level for disabling the MST is configurable and can be high or low. The pin for disabling the MST is selectable, it can be PP0, PP1, PP2, PP3. If no pin is selected the MST is always activated. The corresponding configuration information is located in the first line of the user flash memory.

3.2 Device States

Table 23 Device States

Device State	Description	Main purpose
Run State	CPU running	Application Code or Firmware execution
Idle State	CPU halted. Device is waiting for a resume event and immediate (t_{RES_IDLE}) code continuation. Device fully powered.	Used if software needs to wait a short time for a hardware event.
Stand-By	CPU halted. Device is waiting for a resume event and fast (t_{RES_STBY}) code continuation. Fewer circuits powered as in Idle. RAM powered.	Used together with the Sampling Timer, e.g. for RF Interframes or in wait states between subsequent measurements.
Power Down	Digital Core powered down. Lowest current consumption because only few circuits remain powered, mainly the Interval Timer and optionally the LF Receiver and Low Power Monitoring (LPM).	Power saving state during long time intervals where the device is waiting for a hardware Wake-Up event.

(table continues...)

Table 23 (continued) Device States

Device State	Description	Main purpose
Thermal Shutdown	Almost all circuits shut off apart from a temperature detector and the Interval Timer. Resume to Run State if temperature returns to normal operating range.	Device protection against overstress in case of ambient temperature out of operating range.

3.2.1 State Transitions

The diagram in Figure 2 below shows the possible state transitions in normal operating mode. The central device state is Run State because state transitions are only possible from and to Run State. Device states other than Run State are entered by application code control. Return to Run State is triggered by hardware event sources, for instance timer underflow flags and LF flags.

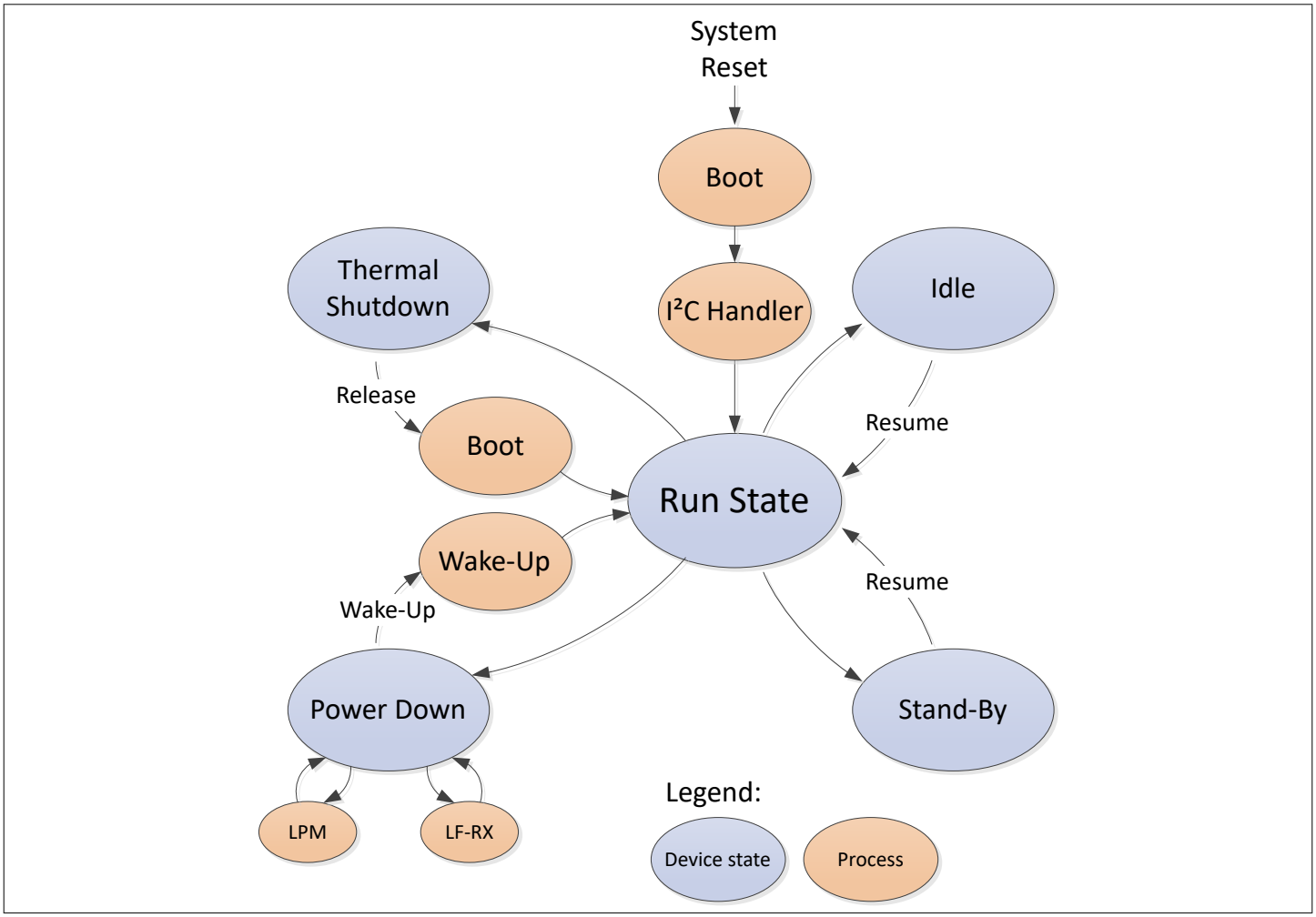

Figure 2 State transitions diagram

A resume event restores the CPU context and continues code execution right after the point where Stand-By or Idle was entered. After Wake-Up the code execution starts at the reset vector.

3.2.2 Thermal Shutdown

In order to avoid undefined device behavior outside the normal operating temperature range, the device provides the option to enter a Thermal Shutdown state.

Thermal Shutdown can be entered if either the ambient temperature rises above a defined hot threshold T_{HOT_E} or falls below a defined cold threshold T_{COLD_E}. Thermal Shutdown is fully under application code control and is not automatically entered.

The device remains in Thermal Shutdown until the ambient temperature goes back to normal operating range, i.e. when the temperature reaches a defined upper threshold T_{COLD_REL} or lower release threshold T_{HOT_REL}.

When Thermal Shutdown is released the device re-enters RUN state, and a dedicated flag is set to indicate this situation to the application.

There is a defined hysteresis between thresholds for entering end releasing Thermal Shutdown, see Figure 3 below.

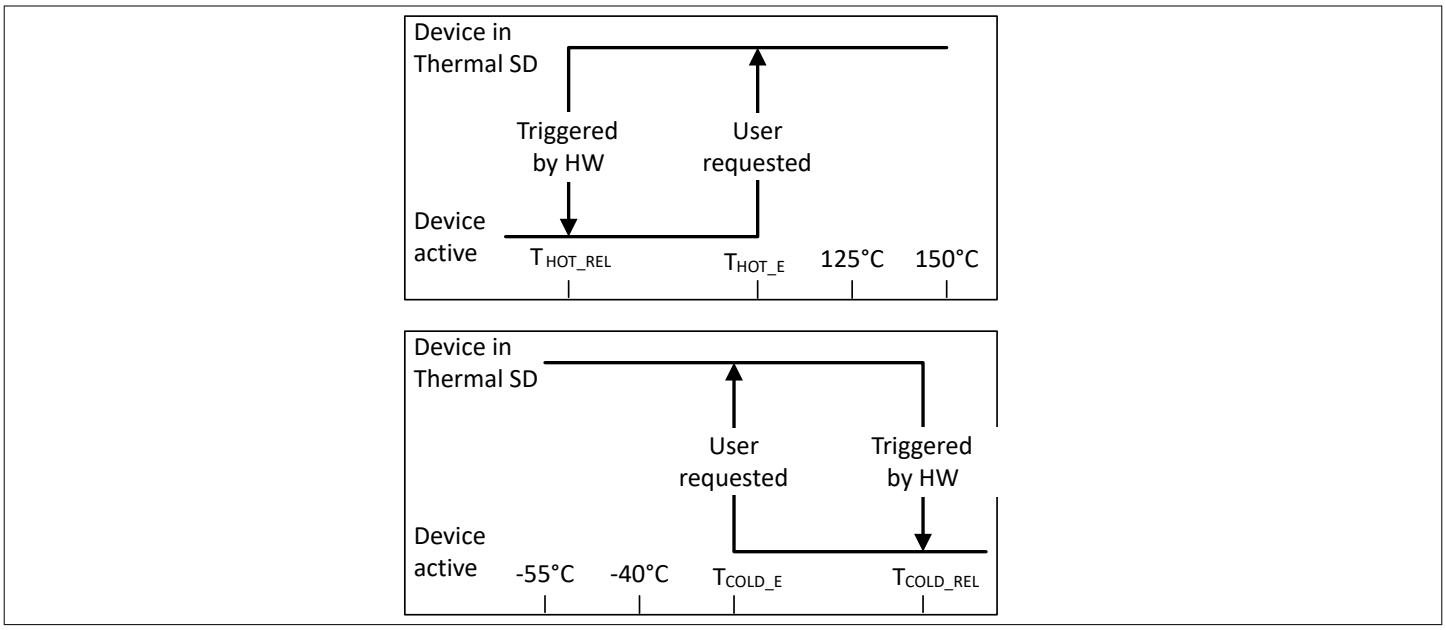

Figure 3 Thermal Shutdown Hysteresis

3.3 Block Diagram

The SP49 can be considered as a combination of three controllers plus peripherals which are specialized and optimized for TPMS application. In hierarchical order the controllers are the Wake-Up Controller the System Controller and the Core.

The Wake-Up Controller is always enabled and controls the device in Power Down. Here the major functions are Interval Timing, LF receiver control with the LF ON/OFF Timer and timing of the Low Power Monitoring (LPM).

The System Controller depends on the Wake-Up Controller and is only activated for special higher level tasks which can be performed without the Core. Important tasks are control of the Measurement Interface and the Power Domains as well as Sampling Timing.

The Core is based on an ARM® Cortex® M0+ MCU. It can only run if the appropriate power domain is enabled by the System Controller. The ARM® controller is used for execution of firmware and application software. The Core comprises a Watchdog Timer, a CRC unit, an I2C controller and a Debug Access Port (DAP). Furthermore four general purpose timers are implemented, two of which are reserved for FW, and two for application code.

The memory block consists of flash for application code and user data, ROM for firmware, RAM used by the ARM® controller and Special Function Registers (SFR) for hardware control. Part of the SFRs and RAM are implemented as retention memory which keep their content in all device states.

The specialized peripherals are the Measurement Interface, the RF Transmitter and the LF Receiver. The operation of these peripherals is supported by firmware functions. The RF transmitter is controlled by the MCU, however, part of the transmitter data processing is done by hardware like shifting bits from FIFO and bit encoding.

The power supply block provides the voltage for different power domains. The voltage domains are activated by the System Controller on demand, allowing lowest system current consumption.

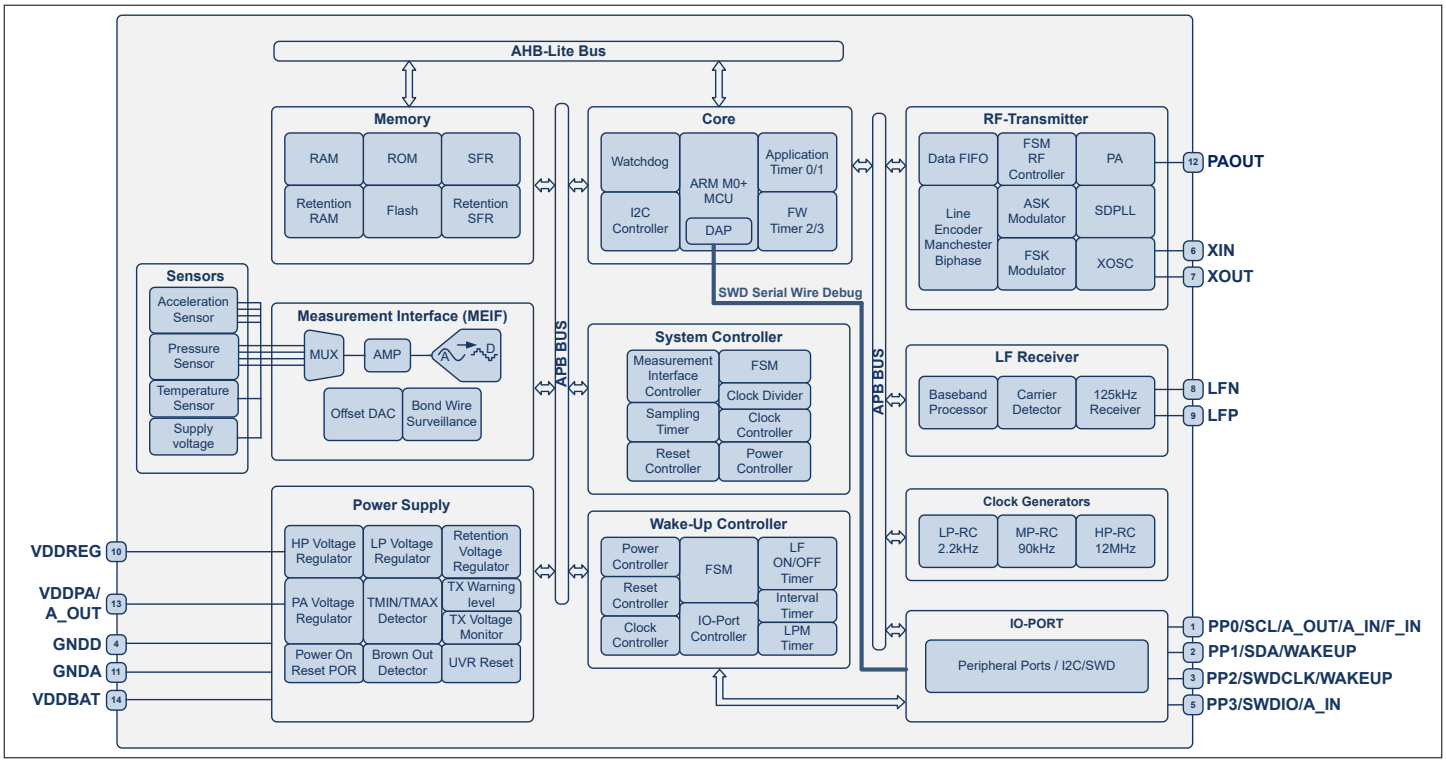

Figure 4 Block diagram

3.4 System Reset

In order to avoid device operation out of operating range or a persisting malfunction the device has a reset circuit. Reset may be triggered by various sources:

- Power On (POR)
- Under Voltage Detector, monitoring the VDDBAT voltage
- Brown Out Detector, monitoring the regulated 1.5V domain
- Flash error, i.e. reset if in a flash word a 2 bit error is detected (ECC2)
- Watchdog
- Software Reset

After reset release the application code is capable to determine the reset source by reading dedicated flags.

3.5 Sensor Measurements

The device allows measurement of the following physical quantities:

- Absolute Pressure
- Temperature
- Voltage at VDDBAT pin
- Acceleration perpendicular to the device's mounting plane

The integrated measurement interface comprises an ADC which is triggered by application software on demand. The resulting ADC raw reading can be compensated by firmware library functions which use individual calibration coefficients stored in manufacturer flash area. All calibration coefficients are secured by CRC values.

3.5.1 Accelerometer Low Pass Filter

The device provides a digital low pass filter for the accelerometer signal to mitigate signal noise and to avoid aliasing effects.

Application software can decide if this filter is used or not.

3.5.2 Analog Sensor Output

The device allows to route either the analog acceleration signal or the analog pressure signal from the measurement interface to either VDDPA pin or PP0 pin, configurable by software.

3.6 Digital Core

3.6.1 Microcontroller

The device includes a ARM® Cortex® M0+ low power microcontroller core which executes user application software and allows to use and configure the device.

3.6.2 GP Timer / Counter

The device includes two configurable 16 bit timers / counters for exclusive use by the application software. Amongst others both timers can be clocked from the following sources:

- The HP-RC (12 MHz) divided by 4
- The crystal oscillator divided by 8
- The MP-RC (90 kHz)
- The LP-RC (2.2 kHz) multiplied by 2

For both timers a clock pre-divider is implemented which allows a wide range of dividing ratios.

Both timers are able to operate in Run State and Idle State. When activated and when the programmed time interval has elapsed, each timer / counter immediately sets a flag, generates a resume event to the microcontroller, and (if configured accordingly) restarts counting automatically.

3.6.3 Watchdog Timer

The device has a Watchdog timer which is enabled after reset by default. The Watchdog timer uses a different clock than the CPU core and operates in Run State and Idle. In Stand-By state the watchdog timer is halted and keeps its value. It is not reset automatically after resume from Stand-By.

In Power Down state the Watchdog timer is disabled and has no effect. After Wake-Up from Power Down the Watchdog timer is reset automatically.

In Program mode, where the device is controlled by I2C, the firmware I2C handler resets the Watchdog. In Debug mode the Watchdog is inactive.

In case the Watchdog timer overflows a device reset is triggered. A dedicated Watchdog reset flag is set to notify the reset source to the application software after device restart.

3.6.4 Wake-Up and Resume Sources

Various sources are available to wake up or resume the device from a low power state:

- Interval Timer
- General Purpose Timer (Resume from Idle)
- Sampling Timer (Resume from Stand-By or Idle)
- LF Receiver
- Low Power Sensor Monitoring (LPM)
- Wake-Up pin (PP1 or PP2)
- Temperature detector for Wake-Up from Thermal Shutdown

When a CPU Wake-Up event happens during a low power state, an associated Wake-Up flag is set. If the event is not masked, a Wake-Up/Resume is generated, the device goes into Run-state, and the Wake-Up flag can be read by application code in order to identify the Wake-Up source. Each Wake-Up flag can be individually cleared by writing a "1" to it. There is no automatic clearing mechanism.

3.6.5 CPU Wake-Up and Resume Events

Table 24 Wake-Up/resume events

Event Type	Description of the event	Wake-Up / resume from states
Interval Timer	Interval timer (post-counter dedicated to CPU Wake-Up) expired	Power Down / Stand-By / Idle
LF Sync Pattern	LF Receiver is activated in Data Reception Mode (DRM) mode and a valid LF-Sync pattern is detected	Power Down / Stand-By / Idle
LF Pattern 0/1/2/3	LF Receiver is activated in DRM mode and a valid LF Wake-Up pattern is detected	Power Down / Stand-By / Idle
LF Carrier	LF Receiver is activated in Carrier Detection Mode (CDM) mode and a valid carrier is detected.	Power Down / Stand-By / Idle
LF End of Message	A complete LF frame has been received, i.e. a violation of Manchester coding is detected.	Power Down / Stand-By / Idle
LF buffer full	LF data buffer is full.	Power Down / Stand-By / Idle
Wake-Up pin	This event occurs each time an active low or high level (selectable) is detected on a Wake-Up pin.	Power Down / Stand-By / Idle
Thermal shutdown release	The device returns from Thermal Shutdown after temperature reaches the release threshold.	Thermal Shutdown
Timer 0/1	Timer / Counter 0 or 1 reaches underflow or overflow depending on user configuration.	IDLE
Sampling Timer	Sampling Timer reaches underflow or overflow depending on user configuration.	Stand-By / Idle
Low Power Monitoring	Low Power Monitoring has detected pressure / acceleration / temperature out of window.	Power Down

All events can be masked out by individual mask bits, except the Thermal Shutdown and the Interval Timer event, which are not maskable. When any other event is masked out, it does not generate a Wake-Up or Resume.

3.6.6 Debug Mode

The device has full debug capabilities including

- run until breakpoint (4 breakpoints)
- stop upon data watchpoint (2 watchpoints)
- single step
- read and write program counter
- read and write RAM and retention RAM and all customer SFRs

Furthermore the Debug Mode allows to

- read and write (program) all user flash sectors
- use all FW- and HW- functions and peripherals that are available in Normal Mode
- use all low power states and resume debugging when low power states are terminated
- set and keep break- and watchpoints during all low power states

3.6.7 Sampling Timer

The device includes a sampling timer which is operable in Run-, Idle- or Stand-By- State. The timer can be configured by FW function Lib_Calib_Sample_Timer. When the programmed sampling time has elapsed, the timer will set a dedicated event flag and generate a resume event. The timer automatically restarts after the programmed sampling time has elapsed. The sampling timer is clocked by the MP-RC clock (90 kHz) and is mainly intended to be used with Stand-By State where the GP timers are not functional.

3.6.8 Interval Timer

The device has a programmable low power Interval Timer (IT) which starts operating after reset release. It consists of a 9 bit long pre-counter, clocked by the LP-RC (2.2kHz), and a 12 bit long post-counter. The pre-counter is always running and generates the clock for the post-counter. The IT cannot be disabled and sets a Wake-Up flag when it elapses. This Wake-Up is not maskable in Normal Mode.

3.6.9 Low Power Monitoring

In order to increase battery life time the device provides a Low Power Monitoring (LPM) function which allows periodic interruption of the Power Down state for the acquisition and monitoring of pressure-, acceleration- and temperature-raw values without the execution of application code. The raw values are compared to upper and lower thresholds, respectively. If a raw value goes below the corresponding lower threshold or exceeds the corresponding upper threshold a device Wake-Up is generated.

Unlike in Run State, in LPM the measurements are always conducted without any self diagnosis check and without checking for ADC over- or underflow. This is because LPM is considered as Wake-Up source only. Consequently the LPM measurement results are not accessible by application code.

The behavior of the LPM is described in the following list and further illustrated in Figure 5:

1. The monitoring interval of each of the three physical quantities can be programmed individually. For this purpose three 10bit long LPM post-counters are implemented, for pressure-, temperature-, and acceleration-measurement, respectively. If the preload value of a certain LPM post-counter is set to zero the corresponding LPM measurement is deactivated. The LPM post-counters are clocked by the Interval Timer pre-counter. Hence LPM measurements and Interval Timer are synchronized.
2. When any of the individual intervals elapses a corresponding flag (LPMx_PEND) is set, indicating a pending LPM measurement. If the device is in Power Down, a transition to Run State takes place. However, instead of running application code a task scheduler is started which conducts measurements in a user programmable order (priority) in case multiple monitoring events take place at the same time. In all other device states the LPMx_PEND flags are set but the scheduler is not started and no measurements are executed.
3. Immediately after the measurement the result is compared with the corresponding thresholds. If a threshold is exceeded an LPM Wake-Up flag (LPMx_FLAG) is set and and a device Wake-Up is generated. Still pending measurements with lower priority are not executed.
4. The LPMx_FLAGs indicate to the application which physical quantity generated the Wake-Up. They must be cleared by application software.
5. The LPMx_PEND flags are cleared by FW after conducting the corresponding measurements. If a Wake-Up occurs before conducting all measurement the pending LPMx_PEND flags are not cleared. In this case the application SW can read and has to clear the LPMx_PEND flags.
6. Other Wake-Up events (if not masked) have a higher priority than LPM measurements, e.g. events triggered by LF receiver or the Interval Timer. However, such Wake-Ups do not interrupt an ongoing LPM task but wait until its completion. (The LPM task comprises the actual measurement acquisition, the comparison of the result with the thresholds and, if exceeded, the setting of the LPMx_FLAG.)
7. Note that the LF receiver can be operated in parallel with LPM.

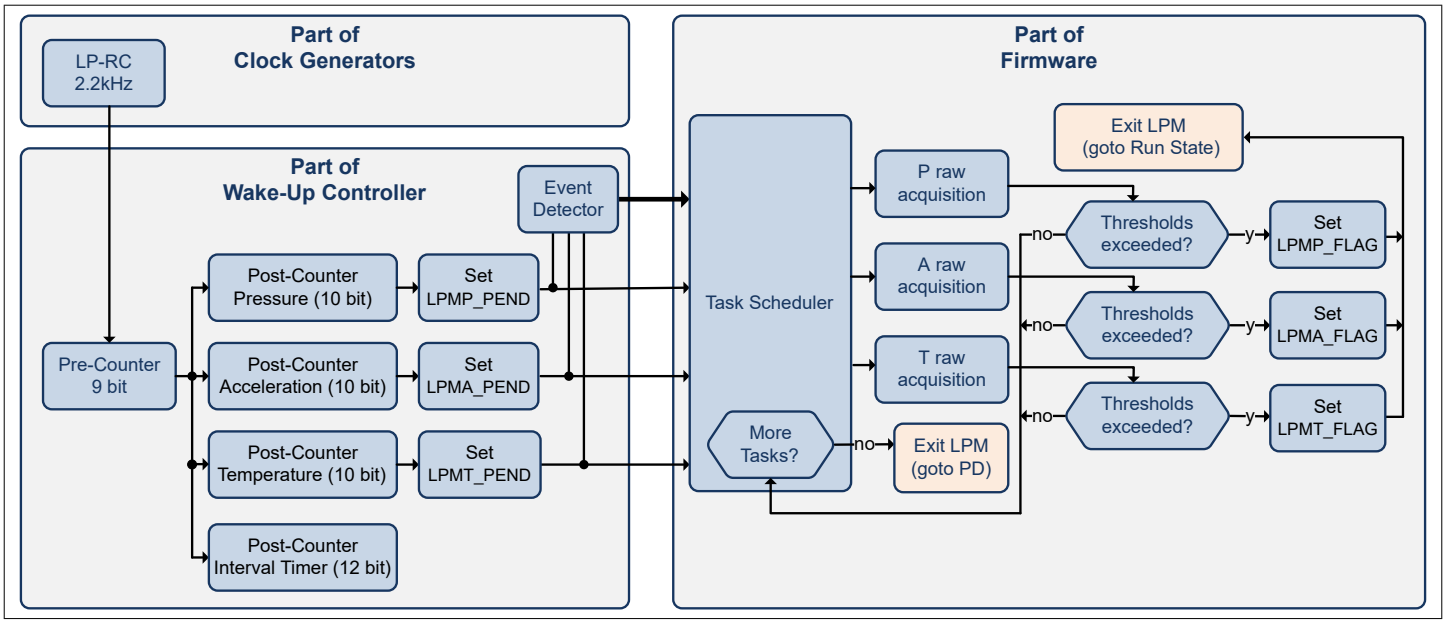

Figure 5 Flow of LPM event

3.7 User Flash Memory

The total user flash memory size is 19 kByte, separated into 8 physical sectors as shown in Figure 6 below. From low to high address the flash is organized in three types of logical sectors:

1. Boot sector (BS): 1 kByte to 7 kByte
2. (Multiple) user configuration sector(s) (UCS): 0 to 6 sectors of 1 kByte
3. User code sector: 12 kByte to 18 kByte

When allocating the flash blocks to the three sectors, only the following three restrictions apply:

- The first 1 kByte block is always a BS, but may be used for normal application code, too.
- The following 6 kByte can freely be allocated to the three logical sector types, in 1 kByte steps.
- The 12 kByte block is always allocated to the code sector.

A UCS always has 1 kByte. If more than 1 kByte user configuration memory is needed, several independent UCSs are configurable.

The first 1 kByte block contains the 32 byte long flash configuration line. These 32 Byte are not available for the Boot Sector. The flash configuration line is used to configure the pin settings for disabling the mode selection time, set the flash configuration and enable or disable the device protection.

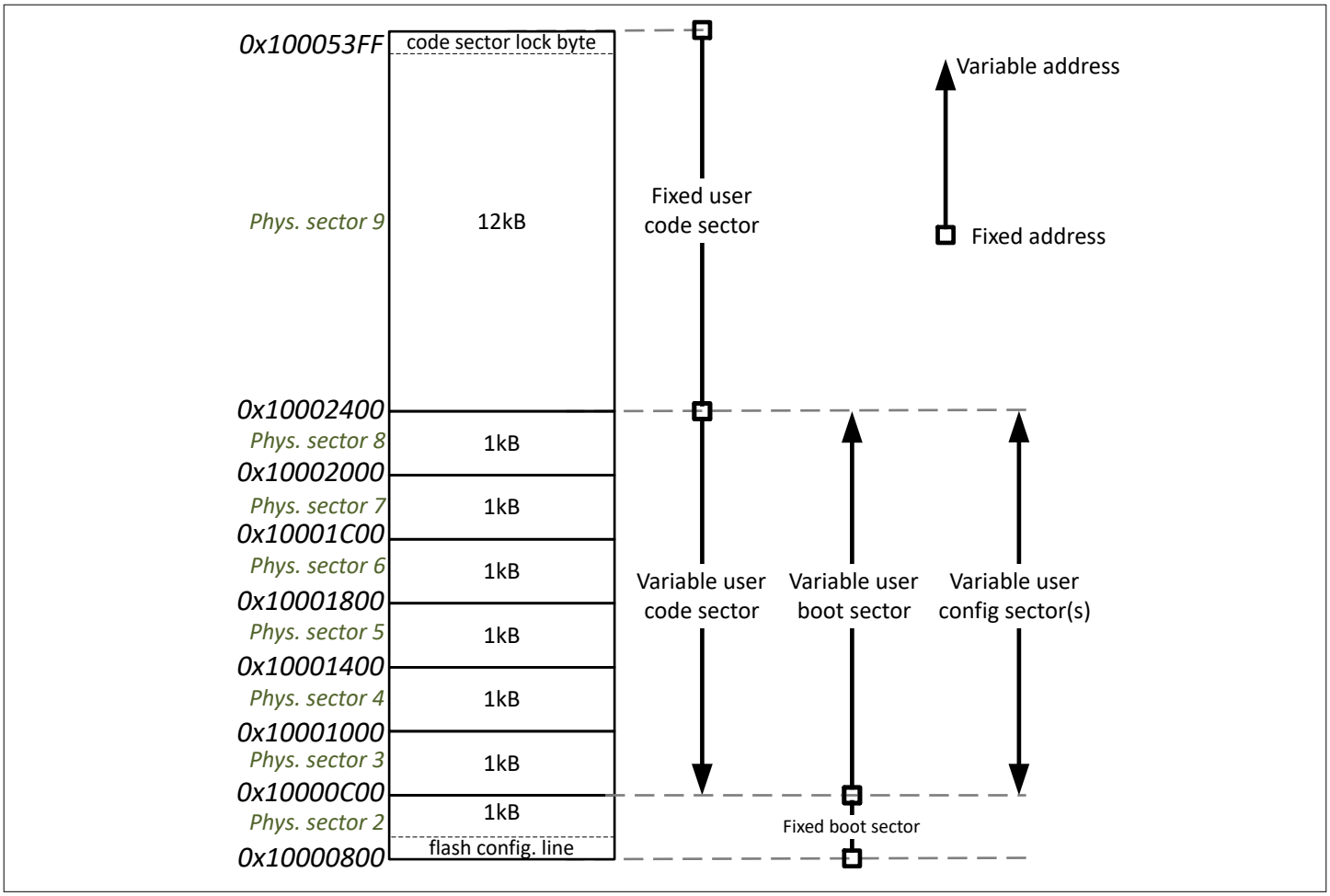

Figure 6 User Flash Memory

The default configuration shown in Figure 7 below applies if the flash configuration line of the user flash is blank or invalid.

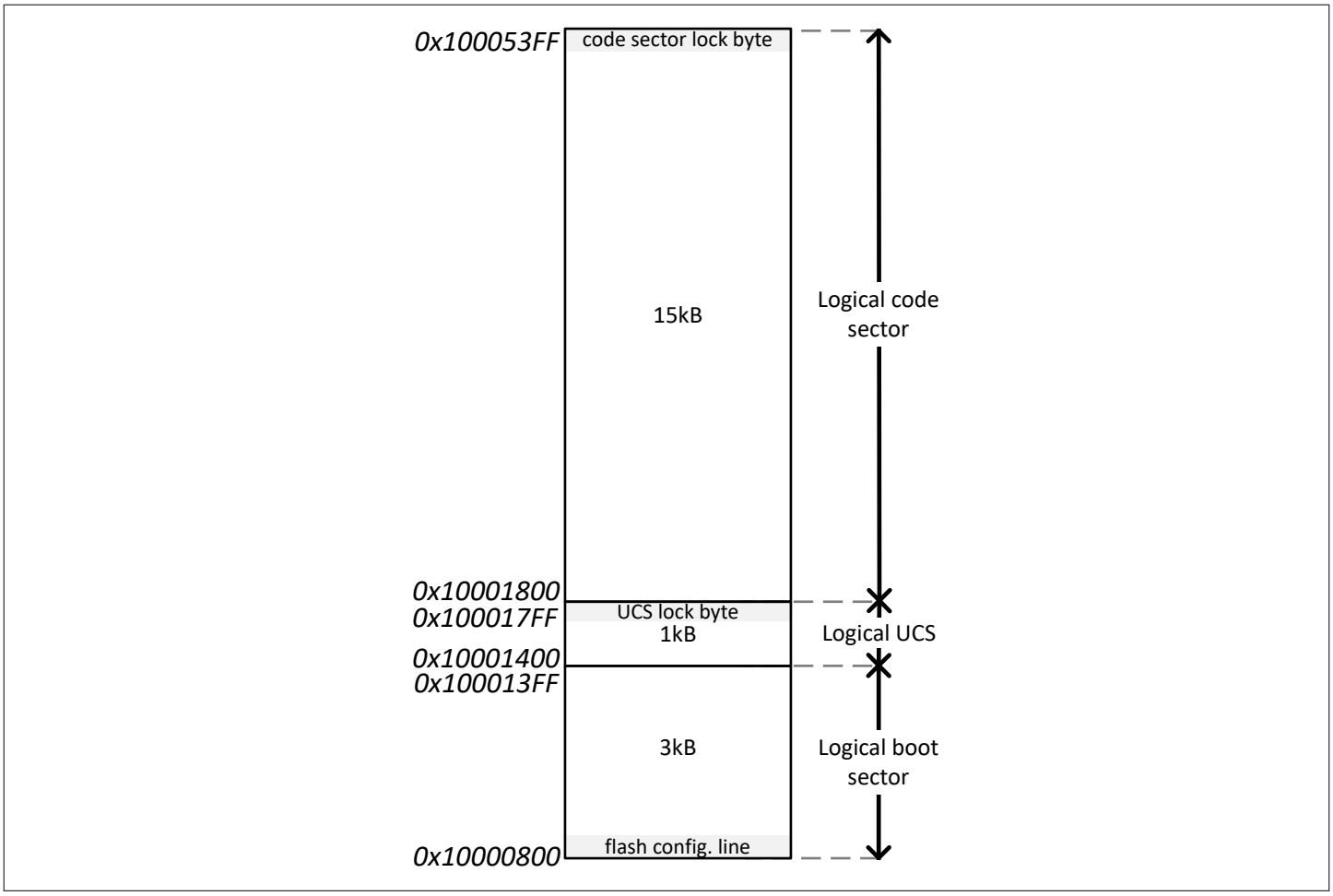

Figure 7 User Flash Default Configuration

3.7.1 Device Protection

The device has a mechanism for protection of IP, i.e. user code or any other user data. It can be activated by setting the last two bytes of the flash configuration line to 0x6969 and only be deactivated by completely erasing the user flash by a Program Mode command. The device protection becomes effective after reset.

The device behavior is shown in the following table.

Table 25 Device Protection

		Device protection activated			Device protection deactivated		
		read	**write**	**erase**	**read**	**write**	**erase**
Program Mode	**Boot sector**	no	no	all together	yes	yes	yes
Program Mode	**Code sector User config sector(s)**	no	no	all together	yes	LB depending	individually
Debug Mode	**Boot sector**	no debug mode available			yes	yes	yes
Debug Mode	**Code sector User config sector(s)**				yes	LB depending	individually
Normal Mode	**Boot sector**	yes	no	no	yes	no	no

(table continues...)

Table 25 (continued) Device Protection

		Device protection activated			Device protection deactivated		
Normal Mode	**Code sector**	yes	LB depending	yes	yes	LB depending	yes
Normal Mode	**User config sector(s)**	yes	LB depending	individually	yes	LB depending	individually

LB means the individual lock-byte of a logical user sector.

3.7.2 Lock Bytes

Each logical user sector, except the boot sector, has reserved two bytes for sector locking to prevent unintended write access to this sector. A locked sector may still be read or erased. Erasing a locked sector unlocks it after next device reset or Wake-Up. After setting the two lock bytes the locking becomes effective only after device reset or Wake-Up.

3.8 Peripherals

3.8.1 General purpose I/O

The device features four configurable general purpose I/O pins, named PP0 to PP3. Each I/O pin can be configured by application software via SFRs as follows:

- Output (push-pull)
- Input (tri-state)
- Input (with internal pull-up resistor)
- Input (with internal pull-down resistor)

When the device starts in normal mode after POR, all I/O pins are configured as input with pull-up by default.

I/O configuration is kept in all device states.

Either PP1 or PP2 can be configured as Wake-Up to allow device Wake-Up from an external source. The pin Wake-Up feature is automatically disabled during and after reset and can be enabled by application software.

PP0 and PP1 are shared with SCL/SDA of the I2C interface and PP2 and PP3 are shared with the SWD interface. For other shared functionalities of the PP pins see the pin description in Chapter 2.

3.8.2 Serial interfaces

The device features two on-chip serial synchronous interfaces for programming and debugging respectively. Each interface uses two pins, one for serial clock and one for serial data.

First a high-speed hardware master/slave I2C interface is included for programming or in-circuit testing via special commands. After POR release it is enabled by default in slave mode for receiving commands from an external master. In Normal Mode the I2C interface is disabled by default and may be configured as master in order to connect to external slave devices, e.g. external sensors.

The second interface is a standard SWD interface for debugging purposes and is enabled by default after POR release. The SWD interface allows device programming during debug session. Therefore it is possible to program and debug the device even if the I2C pins are used for other purposes in the application.

3.8.3 Analog Input

PP0 or PP3 can be configured as single ended analog input. The analog signal is directly routed to the integrated ADC which is used to sample the analog signal. No analog amplification or filtering is applied to the signal. See parametric section for specification of the analog input.

3.9 RAM and Registers

3.9.1 Retention RAM

The device contains a total of 256 bytes of retention RAM (Saved RAM). Therefrom 192 bytes are available for application code. 64 bytes are permanently reserved for the firmware.

3.9.2 Volatile RAM

The device contains 1 kbyte of volatile RAM, where a maximum of 512 bytes is used by the firmware library functions.

3.9.3 Special Function Registers

The hardware of the SP49 is controlled by Special Function Registers (SFRs). They are classified by internal and external SFRs. The external SFRs can be accessed by application code. They are described in the SP49 User Manual. The internal SFRs are only modified by the firmware. They are protected against write access from application code.

3.10 LF Receiver

The LF receiver is an independent circuit block that can run in all device states, apart from Thermal Shutdown. It is able to wake up/resume the device from any low power state upon LF carrier detection (CDM) or ASK modulated telegram reception (DRM). The receiver allows to decode a standard synchronization sequence and Inverted Manchester (A logical "zero" is coded as ASK high to ASK low transition, a logical "one" is coded as ASK low to ASK high transition) encoded data.

By default the LF receiver is disabled after POR and can be enabled and configured by application software. Once the LF receiver is enabled it continues operating regardless of the device state, except for Thermal Shutdown.

The LF receiver Wake-Up/Resume events are maskable, i.e. masked events will not wake up the device. During Run state LF receiver events do not have any effect on a running operation, regardless if they are masked or not.

3.10.1 LF Receiver Duty Cycle

In order to save energy the LF receiver can optionally be operated with a configurable duty cycle.

- During the ON-time the LF receiver is fully operable and can detect LF carriers (CDM) or LF telegrams (DRM).
- ON- and OFF-time can be configured via FW function (Lib_Calib_LF_OnOff_Timer).
- OFF-time and ON-time tolerances are specified by TOL_{t_OFF}, $TOL_{t\_ON\_s}$, and $TOL_{t\_ON\_l}$.
- The configured ON-time is effective ON-time, i.e. the LF receiver settling (see $t_{ON\_SETTLING}$) is not included in the selected ON-time and is considered automatically by the firmware.

3.10.2 LF Carrier Detection Mode (CDM)

In CDM up to three criteria are checked in order to proof signal validity:

1. Signal amplitude: Criterion is always enabled. It is fulfilled when the input signal is above a specified and configurable level.
2. Signal duration: Criterion is optional. It is fulfilled when the input signal is present for a specified period of time t_{CD}.
3. Signal frequency: Criterion is optional. It is fulfilled when the frequency of the input signal is within a specified range f_{CD_DET}, f_{CD_NODET}.

Optional criteria can be enabled and disabled by application software. As soon as all of the enabled criteria are fulfilled a maskable event flag is set by the LF-receiver. If not masked, the event wakes up /resumes the device to RUN state from any low power state

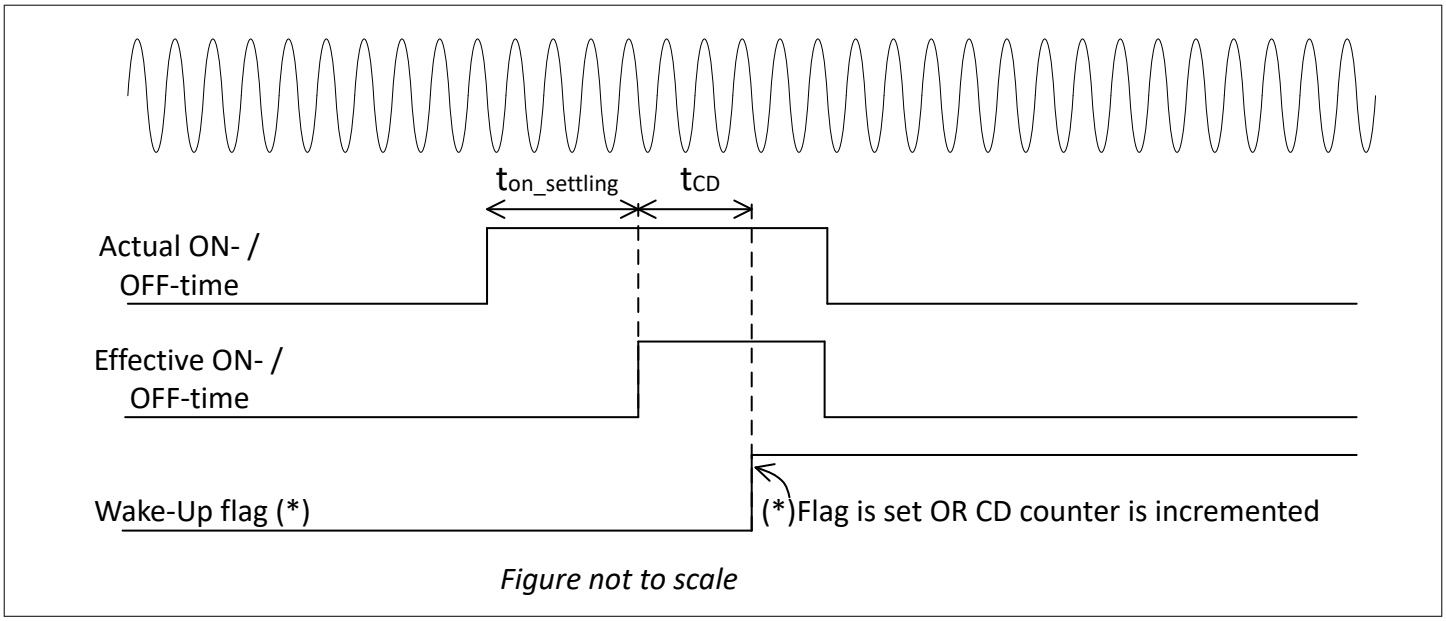

Figure 8 Timing diagram for carrier detection when LF receiver is operated with a duty cycle smaller than 1

3.10.3 Carrier Detect Counter

For detection of long carrier pulses which persist for several duty cycles a counter is provided which counts up once each ON-time if the selected CDM criteria are fulfilled. After successful carrier detection the LF receiver is switched off immediately for the remaining ON-time. If the counter reaches a configurable number of counts the LF receiver generates a wake-up/resume event. The maximum configurable number is 64. If during any ON-time no carrier is detected the counter is reset.

3.10.4 LF Data Reception Mode (DRM)

In DRM the LF receiver behaves as follows:

1. Each time the LF-receiver is turned on in Data Reception Mode the baseband processor is off and the receiver monitors the input signal amplitude. When the amplitude reaches a specified level the baseband processor is switched on.
2. With the baseband processor enabled the receiver starts scanning the input signal for a valid sync-pattern. When the receiver is duty cycled, the ON-time will be prolonged as soon as sync-pattern decoding has started. If the sync-pattern cannot be correctly detected the receiver switches off after a configurable timeout of nominal 4ms to 1020ms, programmable in 4ms steps.
3. After successful sync-pattern recognition the receiver will remain turned on until the end of the telegram, ignoring the actual ON-time. End of telegram is detected by a Manchester code violation.
4. The receiver sets an event flag after successful detection of the sync-pattern, the Wake-Up pattern, after a configurable number of received data bytes, and upon Manchester code violation, respectively.

3.10.5 LF Telegram

The device is capable to receive an amplitude modulated LF telegram assembled of four phases:

1. Preamble. It is a sequence of Manchester coded "zeros" and has a minimum length specified by $t_{SETTLING\_PRE}$. The preamble allows the receiver to settle its analog circuitry and correctly detect a valid signal amplitude.
2. Synchronization pattern. It synchronizes the receiver with the incoming bit stream.
3. Wake-Up pattern. It follows the sync-pattern seamlessly. It can consist of 8 or 16 Manchester encoded bits.
4. A variable number of Manchester encoded data bytes, following the wake-up pattern seamlessly.

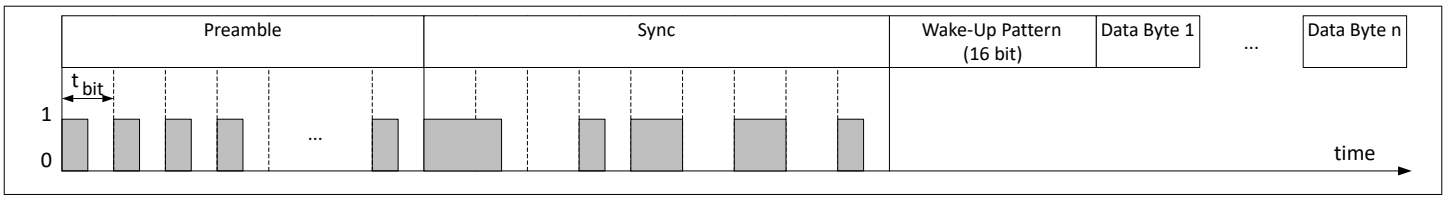

Figure 9 LF telegram

The shaded areas in Figure 9 represent the LF 125kHz carrier.

3.10.6 Wake-Up Patterns

The device offers four Manchester coded Wake-Up patterns with following options, configurable by application software separately for each pattern:

- Pattern enable/disable
- Pattern length of either 8 or 16 bits
- Pattern value

If all four Wake-Up patterns are disabled, the Wake-Up pattern phase is skipped and the baseband processor will, after successful detection of the synchronization pattern, continue with the decoding of data bytes.

For each pattern there is an individual event flag set upon pattern match. Each event flag can trigger a Wake-Up/ resume if not masked by application code.

A decoding error during Wake-Up pattern reception does not generate device Wake-Up / Resume.

3.10.7 Data Decoding and Storage

After decoding the Wake-Up pattern the receiver starts data decoding until a Manchester violation is detected. If Manchester violation is detected a dedicated event flag is set. The receiver autonomously stores the decoded data bytes in a ring buffer of 8 byte length. The receiver can be configured to set an event flag upon writing to a defined location of the byte-oriented ring buffer. This location is configurable by application software.

After Wake-Up/Resume the application code can identify which locations of the ring buffer have been loaded and can read the data.

For each location of the byte-oriented ring buffer there is a software readable flag in place which is set if the corresponding byte location is overwritten by the receiver before it is read by software.

3.10.8 Reception of LF Data Bits

The receiver is capable of receiving full nibbles, too. In case the LF-telegram ends with a nibble it is stored in the receive buffer and the flag LFDRXINFO.TOM is set.

For receiving single encoded bits, the user application can use the bits LFDRXINFO.LFBP, .LFDATA, .LFOV and .DECERR. Reception of single bits must be handled by application code, e.g. the receive buffer cannot be used in this case.

3.10.9 Toggle Mode

In Toggle Mode the receiver switches from ON-phase to ON-phase between DRM and CDM.

The application software can determine which mode is used for the first ON cycle after enabling the receiver.

If the LF receiver is continuously turned on it can still operate in Toggle Mode. In this case the toggle interval is determined by the ON-time setting.

3.11 RF Transmitter

3.11.1 Power Amplifier

The RF-TX Power Amplifier has a configurable number of transistor stages (1 to 16). A regulated and adjustable voltage for supplying the RF output stage is available, too. This allows to adjust RF output power by application software.

3.11.2 RF Modulation schemes

The device allows the user to choose between one of the following modulation schemes:

- ASK
- OOK
- FSK
- GFSK

The device allows changing of modulation scheme between consecutive frames, which are separated by the interframe interval. In case of changing between ASK/OOK and FSK/GFSK the ASK/OOK carrier frequency is the same as the FSK/GFSK center frequency and vice versa.

3.11.3 RF Burst and Inter-Frame Timing

RF data is typically transmitted in bursts of several frames. Between these bursts the device waits in Stand-By state. For timing of these inter-frame intervals the Sampling timer is intended.

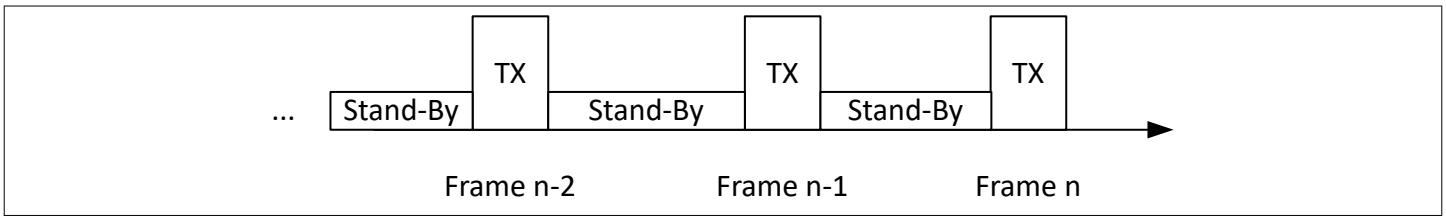

Figure 10 RF Burst and Inter-Frame Timing

3.11.4 RF Frame

Within a single frame the RF transmitter supports a payload of 8 to 256 bits and a payload repetition of up to 15 times. The payload can be encoded according to the following schemes:

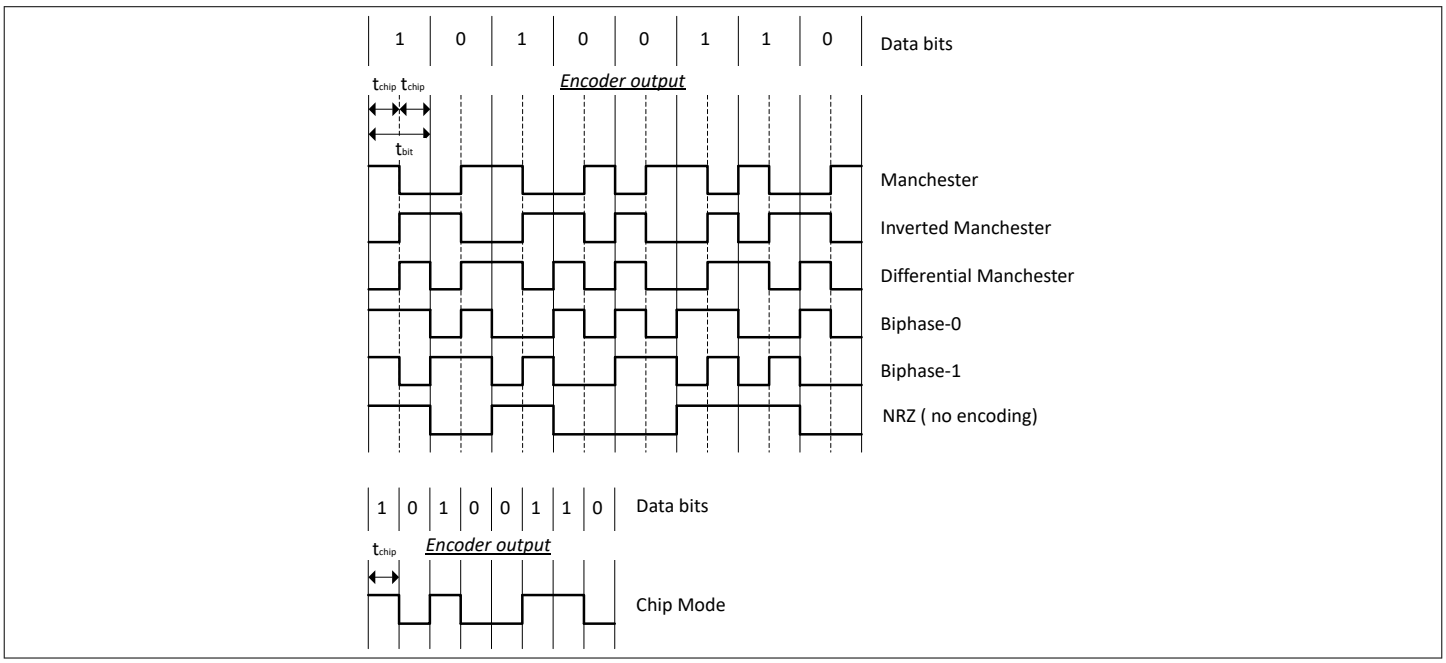

Figure 11 Possible encoding schemes for RF frames

Apart from "Chip Mode" for all other encoding schemes the encoder generates two chips from each data bit. Therefore the bitrate is half the chip-rate (or half the Baud rate), i.e. $t_{bit} = 2t_{chip}$.
In "Chip Mode" the bit-rate equals the chip-rate.

3.11.4.1 SOM and EOM

The RF transmitter supports Start of Message (SOM) and End of Message (EOM) pattern with a maximum length of 255 bit, respectively.

SOM is transmitted once at the beginning of each RF frame. The first payload bit follows without any delay.

EOM is transmitted once at the end of each RF frame. It follows the last payload bit without any delay.

For SOM and EOM the same encoding schemes as for the payload are available. The encoding can be configured independently from payload encoding.

The chip-rate for SOM, payload, and EOM is always the same and cannot be changed within one frame.

The modulation type (i.e. ASK or FSK) used to transmit the SOM and EOM patterns is the same as for the payload.

3.11.5 RF transmission abortion

Following errors are causing the immediate abortion of an ongoing RF transmission:

- PLL does not lock
- Crystal oscillator is instable or stops
- Battery voltage below V_{TX_MON} (optional)

In any of these cases the PA output is turned off immediately and then the device returns to application code execution. Dedicated status flags indicate to the application the reason for abortion.

3.11.6 RF Voltage Warning and Monitoring

During RF transmission the device optionally monitors the battery voltage and compares it to two fixed thresholds. If the voltage falls below the first threshold V_{TX_MIN} a warning flag is set. It can be read after completed RF transmission in application code. If the battery voltage falls below the second threshold V_{TX_MON} the RF power amplifier is immediately shut off in order to avoid device reset since V_{TX_MON} is above the Under Voltage reset threshold V_{UVR_A}.

Although the three mentioned thresholds are close, the relation $V_{TX\_MIN} > V_{TX\_MON} > V_{UVR\_A}$ is given by design.

The Warning and Monitoring feature can only be enabled together.

4 Application Circuit

The specification of SP49 is valid under the condition that the external circuitry complies to the limits specified in the table below.

Typical values are recommendations based on a reference design and have to be adapted by the module integrator according to the application requirements and selected module components (e.g. crystal, antenna,...). Adaptations of the external circuitry are in the responsibility of the module Integrator.

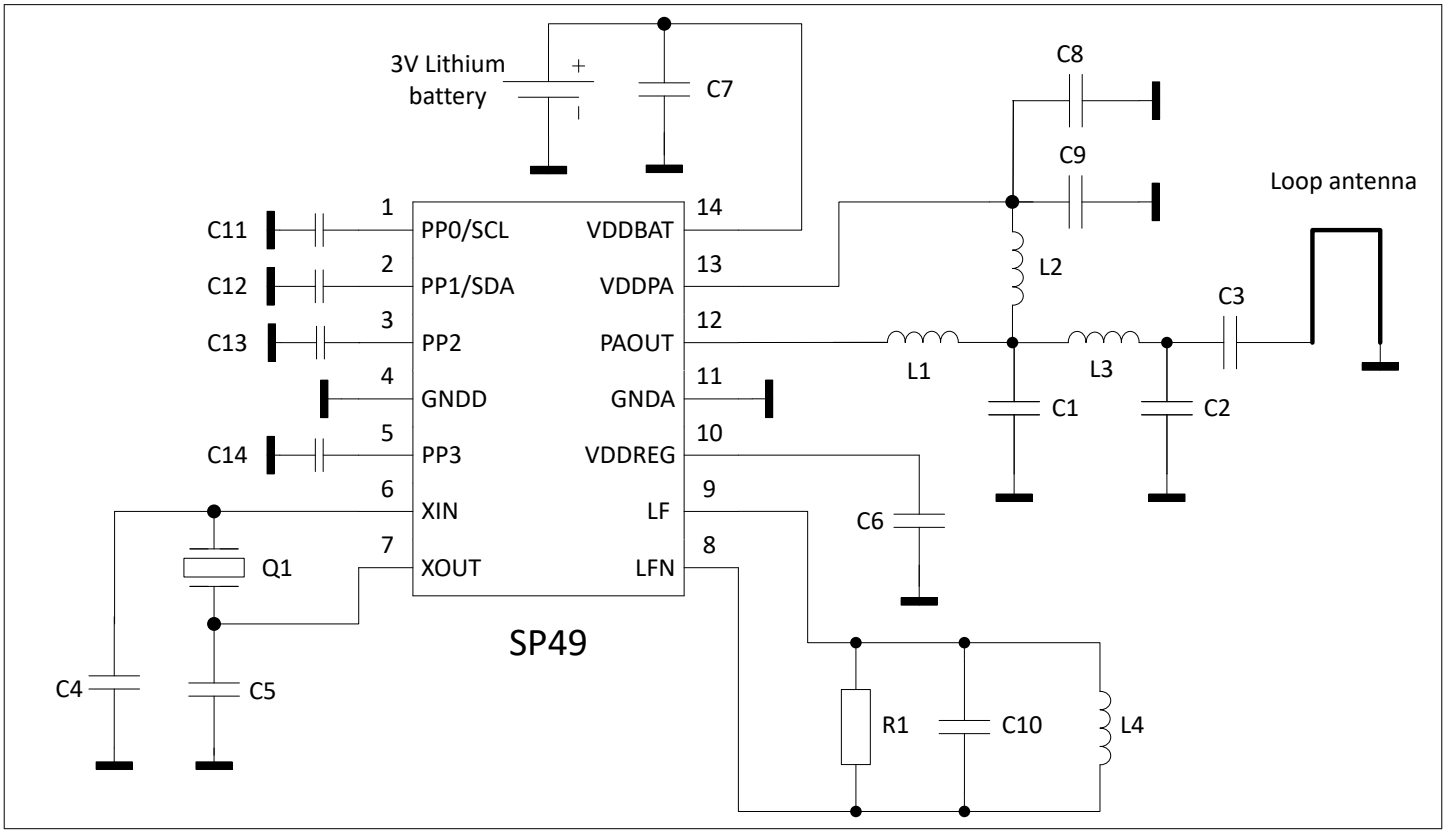

Figure 12 Application circuit

Table 26 Application Circuit Components

Unit	Min	Nom	Max	Unit	Comment
C1, C2, C3, L1, L2, L3	-	-	-	-	These components are forming the matching network. The values depend on antenna impedance and required RF power
C4		16		pF	These values are taking pin capacitances into account and are valid for a crystal that requires 10 pF load capacitance.
C5		16		pF	
C6	7	10	13	nF	Place as close as possible to the pin
C7		10		nF	
C8	7	10	13	nF	If pin 13 is used as analog output (A_OUT) C8 should be omitted.
C9		100		pF	A capacitor with a minimum impedance at RF center frequency should be chosen. The value for this optimal capacitor depends on capacitor material, size etc. Please refer to manufacturer documentation. C9 is not needed if pin 13 is used as analog output.
C10		1.5		nF	Value depends on L4

(table continues...)

Table 26 (continued) Application Circuit Components

Unit	Min	Nom	Max	Unit	Comment
C11		10		pF	Optional capacitors, only used if EMC performance, which depends on PCB layout, needs to be improved. Typically not needed if PPx pins are not connected. If used, place as close as possible to the pins.
C12		10		pF	
C13		10		pF	
C14		10		pF	
L4		1.1		mH	Value depends on coil type
R1		41		kOhm	With the herein stated values for R1, C10 and L4 the Q-factor of the LF- antenna circuit is 6.2. However, application may require another Q-factor. Hence the LF antenna circuit is understood as example.
Q1		26.000		MHz	

5 Self Diagnosis Checks

The device incorporates a number of self diagnosis features which can be triggered by the user.

1. Accelerometer breakage check (so called RD check).
2. Bonding wire check for testing the wiring between MEMS chip and electronics chip.
3. Signal path check. Here the analog signal path plus the ADC are tested by applying test voltages instead of the actual sensor signals.
4. RC oscillator check where the 2.2 kHz, the 90 kHz, and the 12 MHz clock are compared to the crystal clock.

All checks are executed by firmware library functions which can be called by application code.

6 Package Information

The package type is PG-DSOSP-14-84, it is a special development for TPMS application. The green package fulfills the solder condition for Pb-free assembly. The moisture sensitivity is MSL 1, the solder profile is according to JEDEC-J-STD-020D, with a peak temperature of 250°C.

6.1 Package Drawing

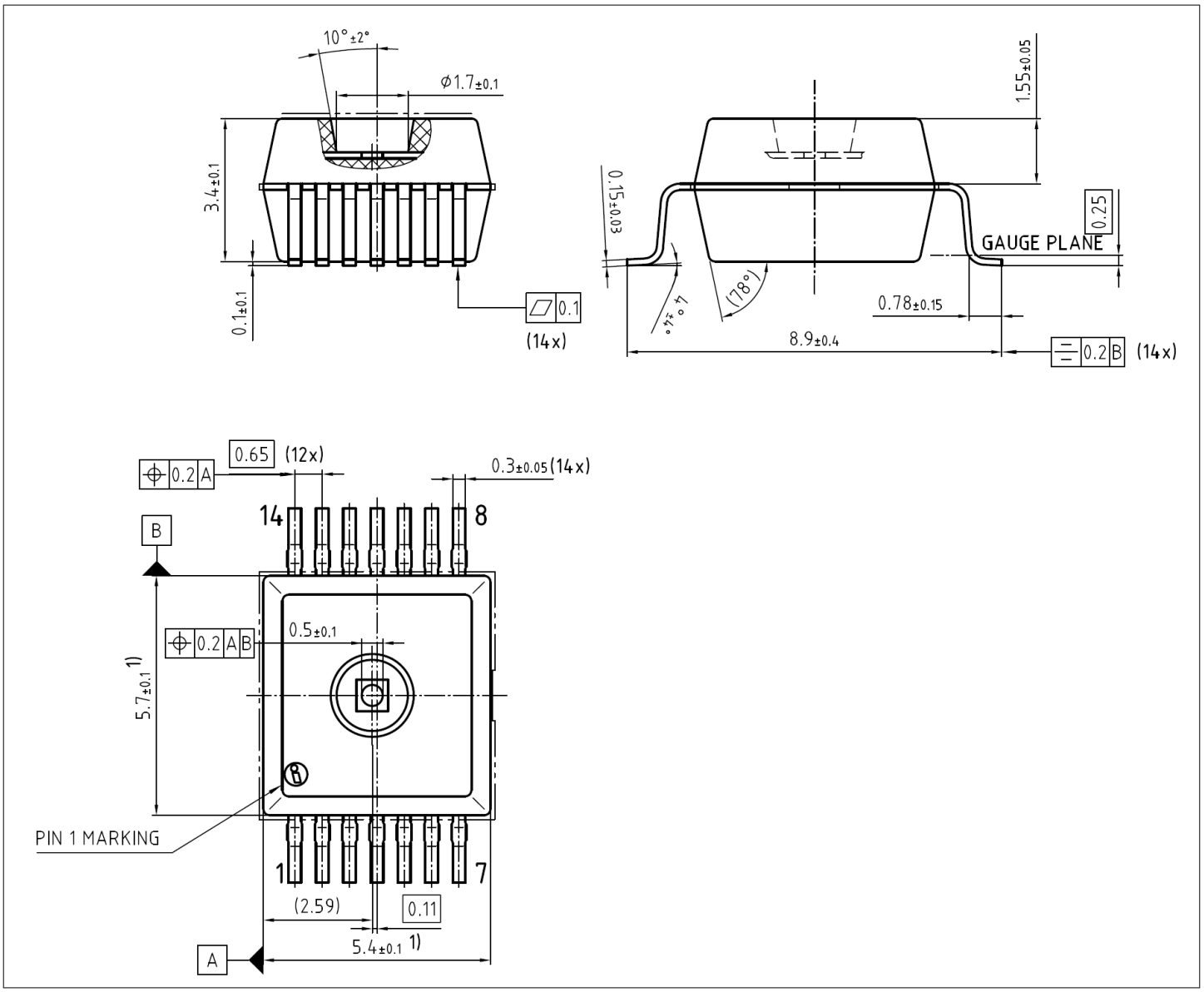

Figure 13

6.2 Package Marking

The laser marking consists of four fields:

- 11 digit Lot Code
- 5 digit Date Code, always starting with G followed by 2 digit year code and 2 digit week code, where YY is the production year minus 2000 and WW is the calendar week.
- 5 digit Product Identifier, where x depends on the product variant.
- Pin 1 marking

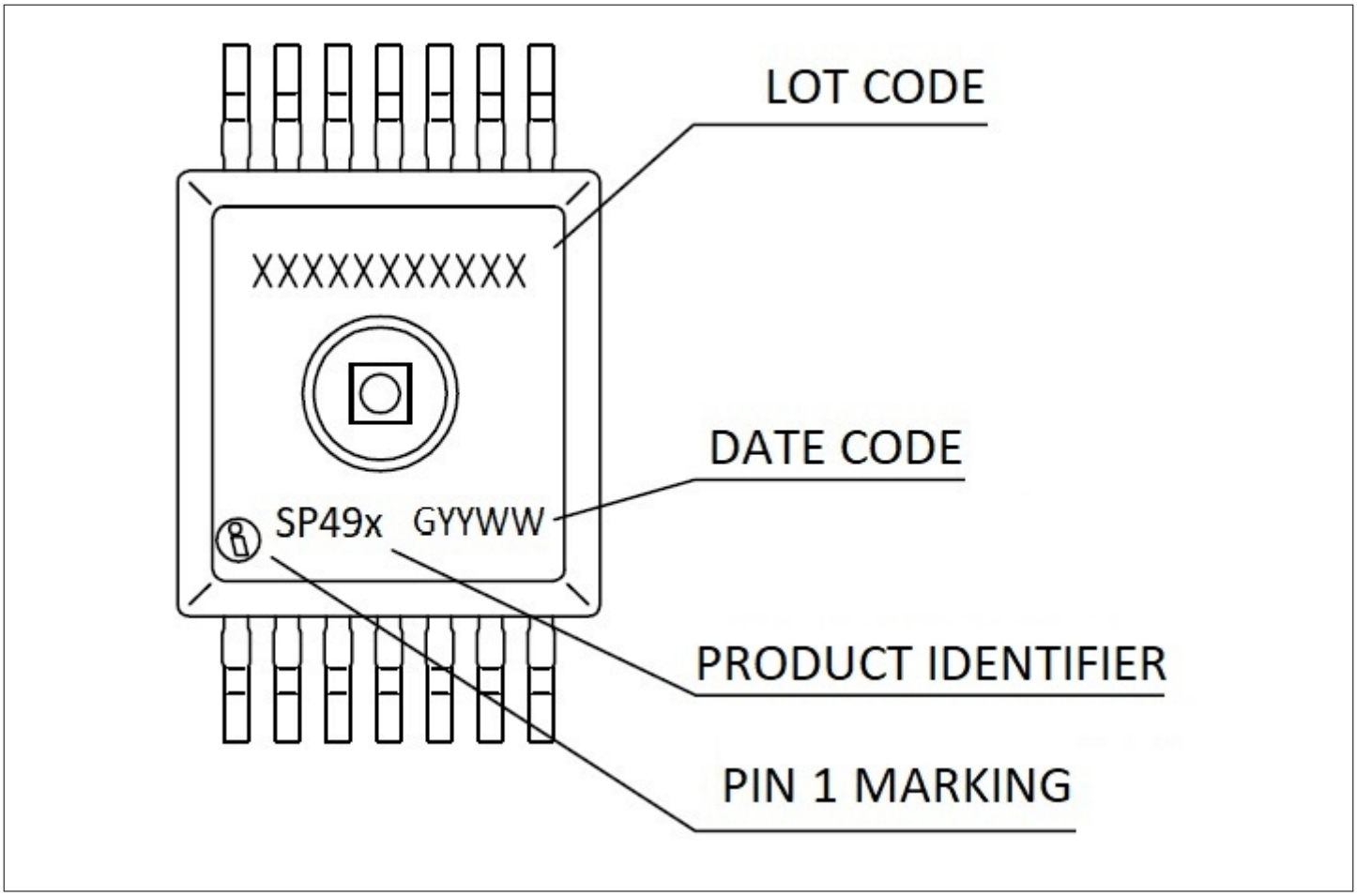

Figure 14 Package Marking

7 Device Identification

The device has an electronically readable 4 byte Serial Number. This Serial Number will be restarted after the maximally possible number is reached. Note that not every possible Serial Number may occur.

An additional electronically customer readable Product Code allows Infineon the unambiguous identification of the product and the specification variant.

8 Revision History

Table 27 Revision History

Document version	Date of release	Description of changes
1.0	2024-04-10	Initial version

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