Single-Event Burnout and Avalanche Characteristics of Power DMOSFETs

Sandra Liu, *Member, IEEE*, Milton Boden, *Member, IEEE*, Dev Alok Girdhar, *Senior Member, IEEE*, and Jeffrey L. Titus, *Senior Member, IEEE*

***Abstract*—Analyses of quasi-stationary avalanche simulations on radiation-hardened power MOSFETs suggest that the single-event burnout (SEB) failure is determined by the device's avalanche characteristics and confirm SEB failure mechanism is due to the turn-on of parasitic bipolar transistor. The heavy ion beam is only acting as a trigger. Simulation results on various 600 V and 250 V radiation-hardened power MOSFETs from International Rectifier are compared to an extensive set of single event effect test results and prove quasi-stationary avalanche simulation is capable of evaluating and predicting SEB susceptibility.**

***Index Terms*—Avalanche simulations, buffer layer, heavy ion beam, MOSFET, power DMOSFET, quasi-stationary, R6, SEB, single-event burnout.**

I. Introduction

Single-event burnout (SEB) can be triggered by the passing of a heavy ion through a MOSFET when biased in its off state [1]. It is believed that the transient current generated by the heavy ion activates (turns on) the parasitic bipolar transistor inherent to the MOSFET structure, where the $n+$ source region acts like the emitter, the p-body region acts like the base, and the epitaxial layer acts like the collector (see Fig. 1 for a typical cross sectional representation). A regenerative feedback mechanism then causes the collector current to sufficiently increase triggering the onset of second breakdown, which ultimately causes catastrophic device failure. In 1985, Wrobel *et al.* explained epitaxial burnout with the concept of current-induced avalanche (CIA) based upon burnout observations during dose rate tests of bipolar transistors and VDMOSFETs. They explained in detail how the maximum electric field shifted to the N-N++ interface under high current density leading to avalanche based on Poisson's equation [2].

It is good that we understand the SEB failure mechanisms. It would be more desirable to be able to do SEE simulations and predict device performances. Johnson *et al.* provided an excellent review on the techniques used for modeling single-event effects (SEE) in power MOSFETs before 1996 [3]. They explained, in detail, the analytical, semi-analytical and numerical simulation models, summarizing representative simulation results for each approach. Dodd provided an overview on physics-based simulations of single-event effects [4]. However, none of those simulations provided results that were predictive and they did not totally explain the failure mechanism. To date, many researchers have attempted to simulate the dynamic SEE failure mode [5]–[7]. Some have specifically focused on better understanding of the heavy ion beams. One researcher, in particular, Edmonds, has dedicated a tremendous effort in understanding, explaining, and defining the ion track (i.e., the charge deposition and subsequent charge collection) [8].

The difficulties in achieving accurate or very meaningful SEE simulation results with the inclusion of an ion track are due to lack of: 1) proper ion track definition and 2) valid or practical simulation models available (e.g., charge generation and transport). Current simulation models are not capable in defining an accurate ion track and its charge transport.

Recent extensive SEE test results on International Rectifier's (IR), proto-type R6 600 V, n-channel MOSFETs have shown that SEB, if present, occurred without regards to choice of ion or its energy [9]. For SEE tests of those proto-type R6 600 V devices, Krypton and Xenon with 25 $\mathrm{MeV\cdot amu^{-1}}$ setup were used, providing many different LET values from 20 to 63.4 $\mathrm{MeV\cdot cm^{2}\cdot mg^{-1}}$, when their beam energy was varied from 163 MeV to 2954 MeV. Forty-eight devices were characterized to SEB failure. SEB failure occurred at approximately the same drain voltage of 580 V regardless of the ion or its energy. Since the SEB mechanism appears to be independent of the deposited charge (LET and depth) but strongly dependent upon a fixed value of drain bias suggests that some inherent device characteristic determines the SEB failure threshold voltage. This paper presents a straightforward quasi-stationary avalanche simulation approach to explain the avalanche characteristics of power MOSFETs, the role of the heavy ion beam in the SEB test, the triggering and failure mechanism of SEB, and the comparisons of simulation results verses SEB test results showing quasi-stationary avalanche simulation can be a very useful tool in evaluating, predicting power DMOSFETs' SEB susceptibility.

II. Typical Quasi-Stationary Avalanche Curve of a Power Mosfet

The quasi-stationary avalanche simulation was performed using TCAD simulation tools from Synopsys [10]. Devices simulated are proto-type, R6, 600 V, n-channel MOSFETs manufactured by IR. The R6 process uses a stripe-cell design. Simulations were performed on MOSFETs with a single or dual epitaxial layer (first grown epitaxial layer often referred to as buffer layer). Using the TCAD process simulation tool, DIOS, we generated the structures based upon actual design and process details. A full cell was simulated incorporating the

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S. Liu, M. Boden, and D. A. Girdhar are with the International Rectifier Corporation, El Segundo CA 90245 USA (e-mail: sliu1@irf.com; mboden1@irf.com; dalok1@irf.com).

J. L. Titus is with the NAVSEA Crane Division, Crane IN 47522 USA (e-mail: jtitus@atd.crane.navy.mil).

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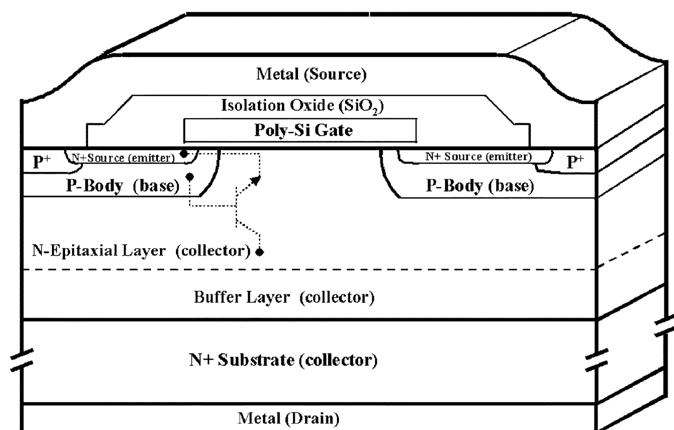

Fig. 1. Cross-sectional representation of a vertical power MOSFET (not drawn to scale) where the n+ source acts like the emitter, p-body acts like the base and the epitaxial layer acts like the collector of the inherent parasitic bipolar transistor.

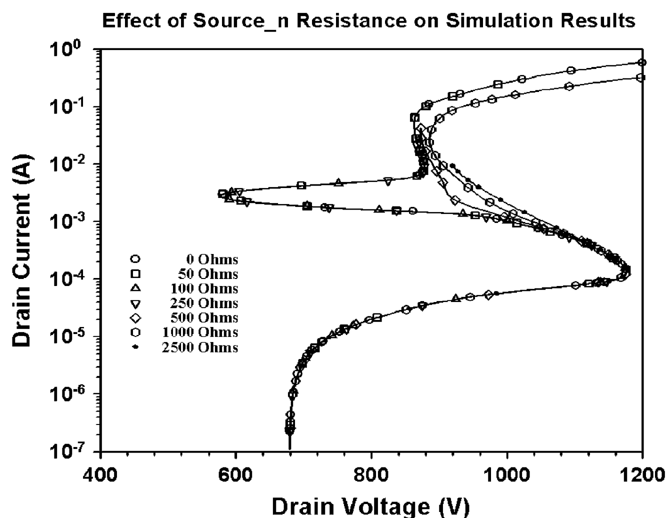

Fig. 2. Quasi-stationary avalanche curves of a power DMOSFET using different source_n resistor values with source_p resistor value kept at 2500 Ω.

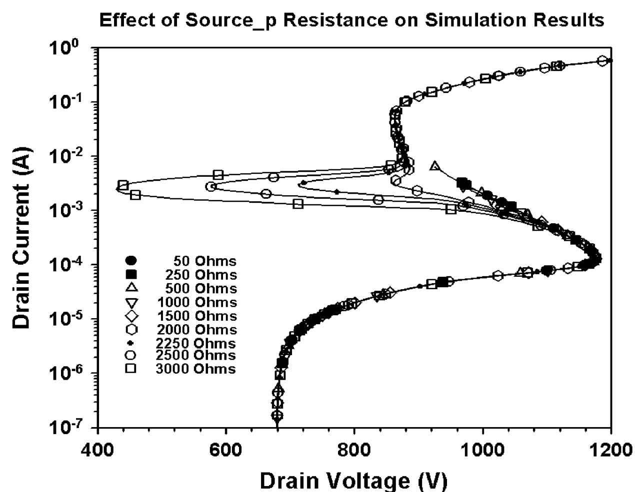

Fig. 3. Quasi-stationary avalanche curves of a power DMOSFET using different source_p resistor values with source_n resistor value kept at 250 Ω.

full thickness of the epitaxial layer, buffer if used, and partial highly doped substrate. Meshing was optimized manually using the Mdraw tool. Metal contacts were added to the gate, drain and source regions. For simulation purposes, the source contact was divided into two separate contacts: a) contact to the P-Body (base) region referenced herein as the source_p and b) contact to the N+ source (emitter) region referenced herein as the source_n. The source electrode was split to independently monitor current flow through the P-body region (mostly hole current) and N+ source region (mostly electron current). In addition, this provided the freedom to specify a different contact resistance between the metal/P-body contact and the metal/N+ source contact. The source contact resistance, especially the source_p resistance, strongly influences the simulation results and its convergence. Fig. 2 shows how the simulation results change with source_n resistor values, while Fig. 3 shows the effects of source_p resistor values.

Fig. 2 shows the quasi-stationary avalanche simulation curves with the source_n resistor value varied from 0 to 2500 Ω, while the source_p resistor value was kept at 2500 Ω. Results show that when the source_n resistor value is higher than 500 Ω, second breakdown was not observed. This is easily explained in that when the source dose is low, it makes the source contact resistance high reducing the parasitic bipolar transistor gain. When the source_n resistor value is set at 250 Ω, second breakdown is present and for source_n resistor values below 250 Ω, the second breakdown voltage does not change.

Fig. 3 shows the quasi-stationary avalanche simulation curves with the source_p resistor value varied from 50 to 3000 Ω, while the source_n resistor value was kept at 250 Ω. Convergence problems were encountered when the source_p resistor was below 1500 Ω. Second breakdown was observed when the source_p resistor was increased to 2000 Ω and above. The second breakdown value decreases with increased source_p resistor value.

When comparing the above simulated second breakdown voltages with actual SEB test results, we found the resistor values of 2500 Ω for the source_p and 250 Ω for the source_n best fits our test results. When different sets of resistor values were selected (source_p resistor greater than 2500 Ω and source_n resistor lower than 250 Ω), different simulated second breakdown voltages were derived, but the trends remained the same. The purpose of our current effort is mainly to seek a way to simulate and predict the relative susceptibility of single event burnout of radiation-hardened power MOSFET for device optimization in the new product development. All the avalanche simulations discussed later in this paper used a 2500-Ω resistor for the source_p contact and a 250-Ohm resistor for the source_n contact. Simulation results proved to be predictive.

The avalanche simulation code defines the input/output files, the contacts and their resistance, the physics models, math, and two quasi-stationary steps to bring the drain voltage and current to their desired values. The simulations were performed at room temperature. Thermal effects were not considered at this point. Graphical representations of the current are based upon the simulated output of a single cell, which is the full cell pitch width times 1.0 μm in thickness.

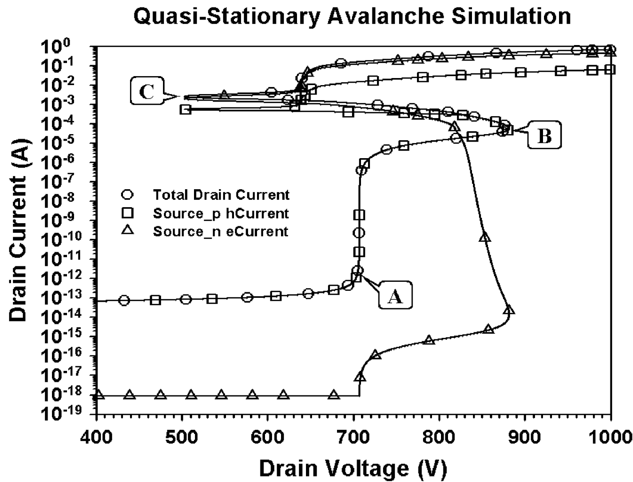

Fig. 4. Quasi-stationary avalanche curve of a power DMOSFET using singleepitaxial layer (Device #1), where Point A reflects the onset of avalanche breakdown, Point B reflects the bipolar turn on, and Point C is the onset of secondary breakdown.

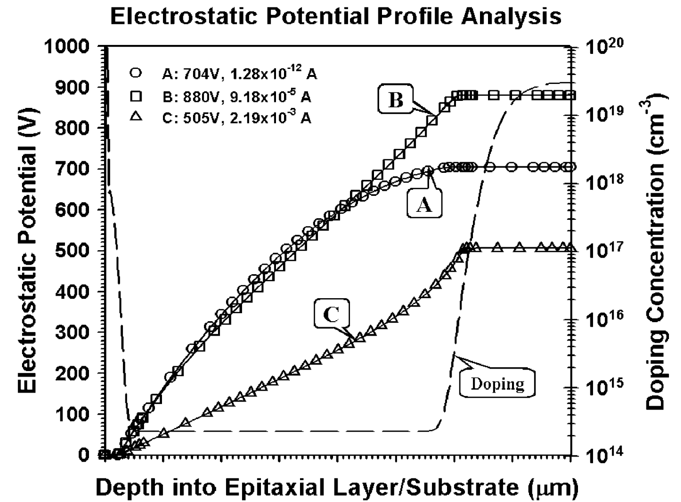

Fig. 5. Electrostatic potential profiles of the three critical points A, B and C along with the doping concentration profile as a function of depth of a simulated power MOSFET utilizing a single epitaxial layer (Device #1).

Fig. 4 is a typical quasi-stationary avalanche curve obtained for a full MOSFET cell with a single epitaxial layer (referenced herein as Device #1). The drain voltage was first incremented to 600 V, followed by an increase in drain current to a very large value (>1.0 A). The curve using circle symbols represents the total drain current as a function of drain voltage. The total drain current is comprised of the hole current flowing from the source_p region (curve using square symbols) and of the electron current flowing from the source_n region (curve using triangle symbols). When the drain voltage reaches approximately 704 V, Device #1 enters normal avalanche breakdown. Above this voltage, the total drain current increases very quickly from its initial value of 1.28×10^{-13} A to approximately 2.56×10^{-6} A without a significant increase in drain voltage. From 2.55×10^{-6} A to 9.18×10^{-5} A, Device #1 supports higher drain voltages from 706 to 874 V, because there are sufficient electrons in the depletion region to change the electric field profile from triangular to rectangular. Before avalanche breakdown, the total source current was essentially the hole current from the source_p region and the contribution of the electron current from the source_n region was minimal until avalanche breakdown at 704 V. Once Device #1 entered avalanche breakdown, the electron current from the source_n region increased from 1.28×10^{-18} A at 704 V to 1.28×10^{-14} A at 874 V. From this point on, the electron current in the source region increases exponentially, indicating that the parasitic bipolar is turned on. Once turned on, the parasitic bipolar transistor would amplify any current entering the base region (i.e., any increase in base current causes more electrons to be injected from the emitter into the base region). Above this point, Device #1 enters a negative resistance regime; electron current from the source_n region supersedes the hole current from the source_p region, initiating a positive feedback mechanism. When the current is increased further, the internal voltage supported by Device #1 begins to decrease. When the drain current reaches 2.19×10^{-3} A, the onset of second breakdown occurs at a drain voltage of 505 V.

Three important points can be identified from the avalanche curve of Device #1: (Point A) $V_{DS} = 704$ V, $I_{DS} = 1.28 \times 10^{-12}$A; (Point B) $V_{DS} = 874$ V, $I_{DS} = 9.18 \times 10^{-5}$ A; and (Point C) $V_{DS} = 505$ V, $I_{DS} = 2.19 \times 10^{-3}$ A. Point A reflects when the device begins the onset of avalanche breakdown. The simulated device supports the rated voltage under low current conditions. Point B reflects when the parasitic bipolar transistor turns on. Point C reflects when the device begins the onset of secondary breakdown. To design a rugged MOSFET, it is preferred to have both high bipolar turn-on current and high secondary breakdown voltage on the avalanche simulation curve.

Figs. 5 and 6 show the simulated electrostatic potential profile and the electric field distribution, respectively, for Device #1, as a function of depth (zero reflects the silicon surface) for conditions at points A (designated with circles), B (designated with squares), and C (designated with triangles). The doping concentration profile is also provided (dash line). The electrostatic potential profile, electric field distribution, and doping profile were obtained perpendicular to the die surface, along the edge of the poly gate, through the source, body, and drift (epitaxial) region, and all the way into substrate.

In Fig. 5, the electrostatic potentials of 704 V for Point A (onset of avalanche breakdown), 874 V for Point B (turn on of the parasitic bipolar transistor), and 505 V for Point C (onset of second breakdown) are each supported by the lower doped epitaxial layer. For Point A, the electrostatic potential is not evenly distributed across the drift region, while for Point B it is evenly distributed. When the drain current is increased beyond Point B, the voltage supported by the epitaxial layer begins to decrease.

In Fig. 6, the maximum electric fields for points A, B and C were 2.35×10^5, 2.35×10^5, and 2.24×10^5 V·cm^{-1}, respectively. For Point A (onset of avalanche breakdown) and Point B (onset of bipolar turn on), the maximum electric field occurred at the base-drift (base-collector) junction. However, under avalanche breakdown (Point A), the electric field decreases linearly across the drift region to a minimum of 3×10^2 V·cm^{-1} at the epitaxial-substrate interface (a triangular shape). Under a

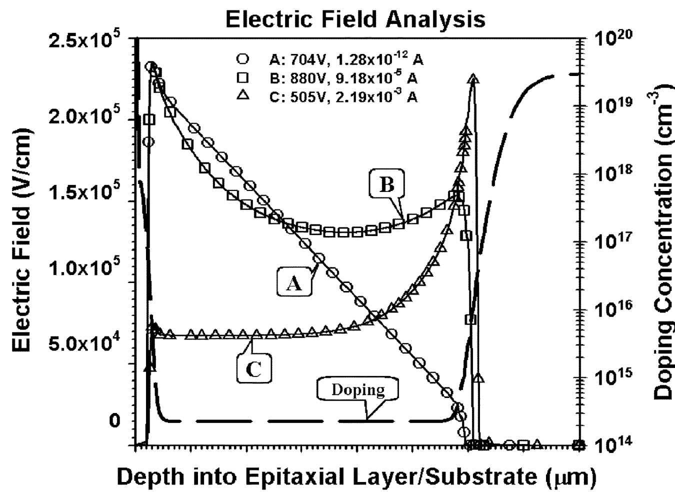

Fig. 6. Electric field distributions of points A, B and C and doping concentration as a function of depth of a simulated power MOSFET utilizing a single epitaxial layer (Device #1).

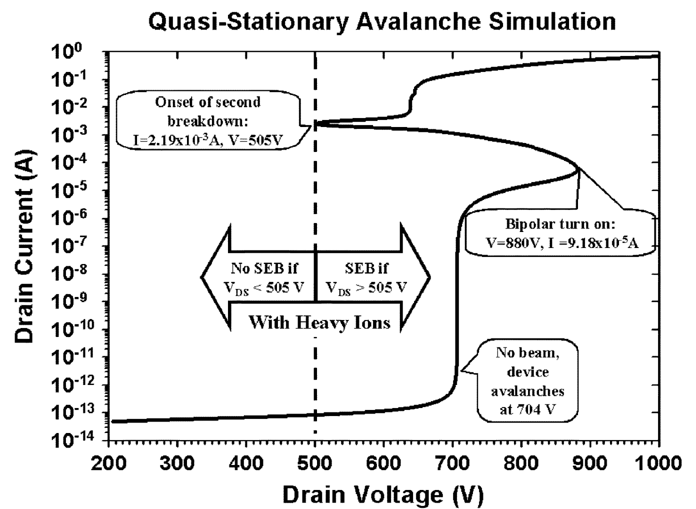

Fig. 7. Illustration of relationship between avalanche characteristics and SEB of Device #1 (single epitaxial layer). Under heavy ion irradiation, SEB can occur if drain voltage exceeds 505 V.

bipolar turn on condition (Point B), the electric field decreases non-linearly to a minimum of 1.3×10^5 V·cm^{-1}, which occurs within the epitaxial layer, then increases non-linearly to its second peak of 1.5×10^5 V·cm^{-1} at the epitaxial-substrate interface (a rectangular shape). For Point C (onset of second breakdown), the maximum electric field shifted from the base-drift junction to the drift-substrate interface. The electric field across the majority of the epitaxial layer is relatively low and constant at 6.8×10^4 V·cm^{-1} but rapidly increases to its peak value of 2.24×10^5 V·cm^{-1} at the epitaxial-substrate interface.

The above simulation results clearly explain the avalanche characteristics of a typical power MOSFET incorporating a single epitaxial layer. It also provides a good evaluation of device ruggedness in terms of how easily the parasitic bipolar turns on and at what voltage second breakdown occurs.

III. SEB Test Setup and Role of Heavy Ion

For the SEB test setup, the desired test sample was positioned into the beam path and was checked with its full rated gate bias to ensure device integrity. With no bias on the gate (V_{GS} of zero) and initial starting drain bias, the beam shutter was opened, and heavy ion irradiation initiated. During exposure, the leakage currents on both the drain and gate were monitored. When the preset beam fluence was reached, the beam was automatically shuttered stopping the heavy ion exposure run. The preset fluence was typically set at 3×10^5 cm^{-2}. Upon completion of the run, the bias was removed and the device was tested again with the full rated gate voltage. The drain bias was then increased to the next test condition and the irradiation sequence repeated. This continued until the device failed. The flux was typically set at 10^4 p·cm^{-2}·s^{-1}, but varied during each run.

Fig. 7 illustrates the relationship between the avalanche curve characteristics and SEB. This illustration uses the simulated avalanche curve of Device #1, a single epitaxial layer device. When at low current level or there is no ion beam, Device #1 would reach static equilibrium with drain biases up to its regular avalanche voltage of 704 V, survive transient voltage spikes up to 880 V, if the current does not exceed 9.18×10^{-5} A, or will survive transient current spikes as high as 2.19×10^{-3} A, if the drain bias is less than 505 V. The two latter conditions assume that the transient time is short enough to prevent second breakdown and/or catastrophic failure. When subjected to a destructive heavy ion beam (resulting in sufficiently high current level), Device #1 would survive with drain biases less than 505 V since the voltage is below that required for second breakdown or bipolar turn on voltages. However, Device #1 would fail with drain biases greater than 505 V since the voltage is above that required for second breakdown placing Device #1 into a negative resistance regime, turning the parasitic bipolar on, causing Device #1 to catastrophically fail.

In this illustration, it is assumed that sufficient electron-hole pairs are introduced into the system from the ion strike to trigger Device #1 into this negative resistance regime. Or if the initial amount of electron-hole pairs were not sufficient enough to generate high transient current density turning the bipolar transistor on (maybe in the case with low LET value beams), the initial electron-hole pairs induced from the heavy ion strike are immediately separated, accelerated and multiplied under high field conditions. These accelerated electron-hole pairs generate a sufficient amount of electron-hole pairs along their path resulting in a transient current level sufficient to induce failure. One thing needs to be emphasized here is that the high current density alone will not cause the device to failure. The high current density has to be in combination with a drain bias higher than the second breakdown voltage, which would place the device into the negative resistance regime, where the bipolar is turned on.

When the drain bias was set at or above the critical secondary breakdown voltage (as determined from simulation) and during heavy ion exposure, the device under test did not immediately fail each time the beam shutter was opened activating the heavy ion exposure sequence. This observation along with the fact that the device survives a heavy ion strike under drain biases below the critical secondary breakdown voltage means: 1) the

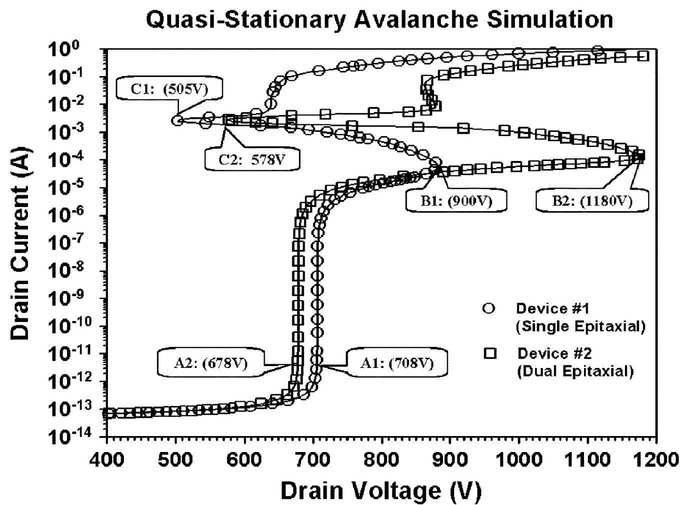

Fig. 8. Quasi-stationary avalanche curves from simulations of Device #1 (single epitaxial layer) and Device #2 (dual epitaxial layers). A comparison of the two devices shows an improvement of 72 volts in secondary breakdown voltage along with a significant improvement in the bipolar turn-on voltage.

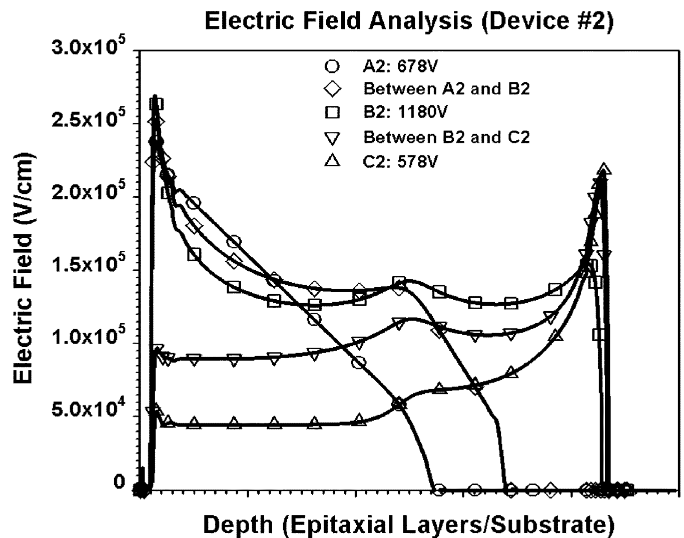

Fig. 9. Electric field distributions of Device #2 (dual epi layers) at various points. This can be compared to Device #1 (single epi) shown in Fig. 3.

ion beam alone does not damage the part; 2) the transient current generated directly from the heavy ion does not turn on the parasitic bipolar transistor; 3) the position of the ion strike is important; and 4) the SEB failure is triggered by a set of combinations of high transient current and applied drain bias.

Given this, it is reasonable to assume that the role of the heavy ion beam in SEB test is to alter the high electric field equilibrium by introducing electron-hole pairs into the system to check the device's capability of absorbing extra charges while the device is reverse biased at its rated voltage. If the device were designed in a way be able to handle these extra charges, then it would most likely survive heavy ion irradiation resulting in an SEE hardened product. By doing quasi-stationary avalanche simulations, designers can evaluate and even predict the device's SEB performance, while optimizing other performance parameters like breakdown voltage and on-state resistance.

IV. Simulation Versus Experimental Results

A. Single Epi Versus Dual Epi

Buffer layers (a second epitaxial layer) have been introduced into the development of newer generation radiation hardened power MOSFETs (e.g., IR's R6 process), since it was proven that MOSFETs incorporating a buffer layer exhibit better SEB performance (i.e., the device is capable of withstanding higher drain voltages for a given ion) [11], [12]. Fig. 8 shows a comparison of quasi-stationary avalanche curves of Device #1 (single epitaxial layer) and Device #2 (dual epitaxial layers). The total epi resistance of Device #1 and Device #2 were designed to be similar. All other design and process parameters were identical. Simulation results show approximately a 72 V improvement in the device's secondary breakdown voltage when a buffer layer was used. In addition, the buffer layer increases the device's bipolar turn on voltage from approximately 900 to 1180 V and increased bipolar turn on current from 7.54×10^{-5} A to 1.64×10^{-4} A. The predicted secondary breakdown voltage improved from 505 V for Device #1 to 578 V for Device #2.

Fig. 9 shows the simulated electric field distributions for Device #2 (dual epitaxial layers) for regular avalanche breakdown (Point A), onset of bipolar turn on (Point B), and the onset of second breakdown (Point C) and two more points in between. These electric field distributions can be easily compared to the electric field distributions of a single epitaxial layer device shown in Fig. 6. At low current levels (at or below regular avalanche currents), the electric field distributions between a device using a single epitaxial layer and one that uses dual epitaxial layers are almost identical. However, at higher currents (currents approaching bipolar turn on), the electric field of Device #2 extends into the first epi layer (buffer layer) allowing the device to support higher electrostatic potentials.

Processed samples of Device #2 were taken to Texas A&M and evaluated for SEB using Krypton and Xenon at many different beam energies. For those tests, the gate bias was fixed at zero volts. Fig. 10 provides a summary of the passing and failing drain voltages for SEB. All the tested devices failed between 570 and 590 V, regardless of the ion or ion energy selected. Detailed test results are summarized in [9].

Quasi-stationary avalanche simulations confirmed that dual epi (an epitaxial layer plus a buffer layer), improved the SEB performance (an increase in drain voltage before the occurrence of SEB) by increasing the device's secondary breakdown voltage. Moreover, the simulations show that increasing the top epitaxial layer thickness (without incorporating a second epitaxial layer) does not provide the added performance benefits when compared to its equivalent device counterpart with dual epitaxial layers.

B. Source Dose

The SEB failure mechanism has long been identified and verified here as the turn on of the parasitic bipolar transistor. Therefore, any design or process considerations that would lead to suppression of the bipolar gain should improve the device's SEB performance. One such approach is to reduce the emitter doping

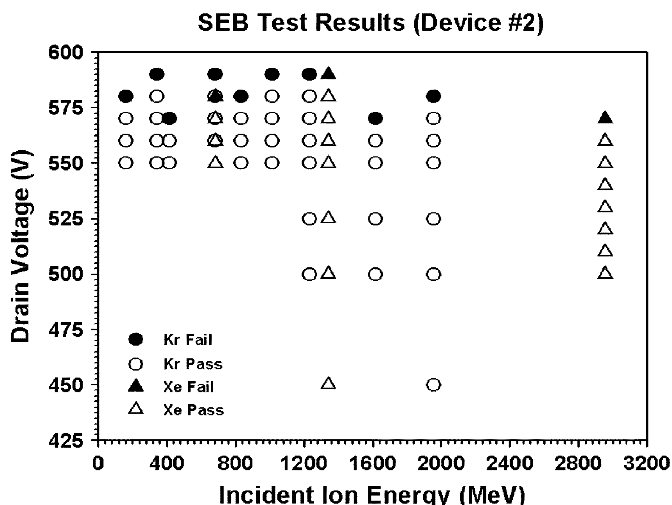

Fig. 10. SEB test results of Device #2 using Kr and Xe. All devices failed for SEB between 570 V and 590 V as simulation indicated.

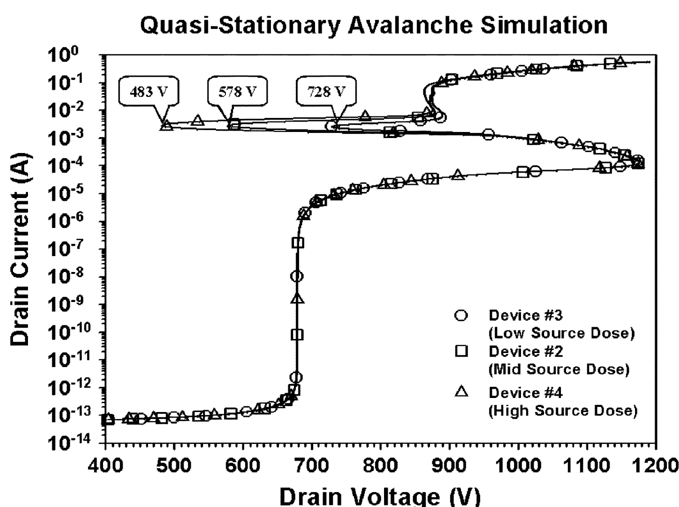

Fig. 11. Quasi-stationary avalanche curves of three different MOSFETs with buffer layers. Each device uses a different source dose (Device #2 is the baseline device, Device #3 has a 33% less dose, and Device #4 has a 67 increase in dose).

concentration causing a reduction in the emitter injection efficiency, hence a reduction in the parasitic bipolar gain.

Fig. 11 shows the quasi-stationary avalanche simulation curves for three structures with different source doses (i.e., different emitter doping concentrations). Device #3 used a 33% lower source dose than that used in Device #2, while Device #4 used a 67% higher source dose. These three devices all used a buffer layer and all other design and process parameters were kept identical (except, of course, the source doping). The simulation results indicate that the secondary breakdown voltages for Device #2, #3 and #4 are 578, 728, and 483 V, respectively. In other words, Device #3 should exhibit better SEB performance (no SEB for drain voltages up to 728 V) when compared to Device #2 (no SEB for drain voltages up to 578 V) and Device #4 (no SEB for drain voltages up to 483 V). Changing the source dose did not affect the device's cell breakdown voltage of 678 V nor did it change the bipolar turn on voltage of 1180 V.

However, if the source dose is reduced too much it will increase the source contact resistance and in turn increase the device's total on-resistance, which is not desirable. Device #3 used a 33% lower source dose than Device #2—the change in on-resistance was minimal ($<1\%$). Device #4 used a 67% higher source dose than Device #2; the on-resistance changed by 34%. Another important parameter that is affected by source dose is the threshold voltage. The threshold voltage increased substantially when the source dose was reduced by 33%. Process modifications were needed to bring the threshold voltage back to its original target. When optimizing the device's SEB performance, we need to be careful not to compromise the device's electrical performance by using a lower source dose than necessary.

Processed samples of Device #3 were taken to Texas A&M and evaluated for SEB using Xenon at several different beam energies. Fig. 12 presents the outcome of those tests. Devices with the lower source dose passed heavy ion irradiation to rated drain voltages of 600 V. However, all samples failed between 620 V and 630 V due to termination avalanche breakdown. Though the

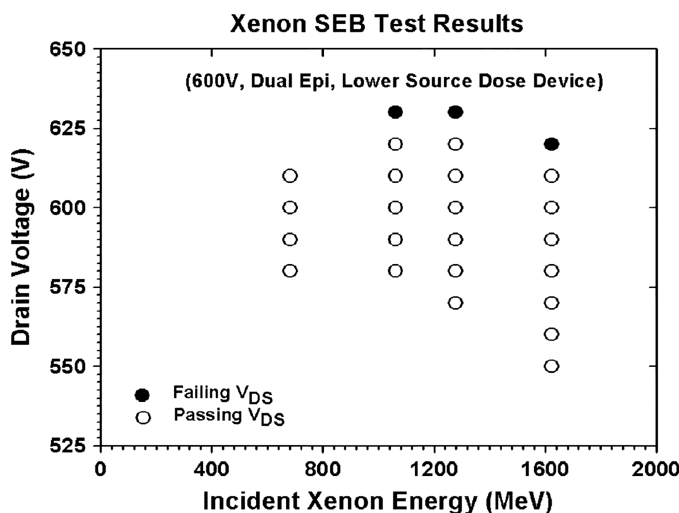

Fig. 12. SEB test results of Device #3, which uses a lower source dose, at different Xenon energies. Devices passed 600 V as simulation suggested. Indicated failures reflect termination breakdown.

simulated avalanche breakdown of the cell structure is 678 V, the ultimate breakdown voltage of this device is determined by the termination breakdown voltage. The average termination breakdown voltage of tested samples of Device #3 is 640 V, preventing the collection of SEB data above this voltage. The explanation for this 10 to 20 V reduction of termination breakdown under ion beam irradiation needs further investigation.

C. IR R6 250 VN

Fig. 13 is the simulated avalanche characteristics of the R6 250 VN device. The avalanche curves show that regular avalanche breakdown is 267 V (Point A), that the bipolar turn on voltage is 501 V (Point B), and that the onset of second breakdown is 384 V (Point C). Since the voltage for second breakdown is much higher than the voltage for regular avalanche breakdown, this device during SEE testing should

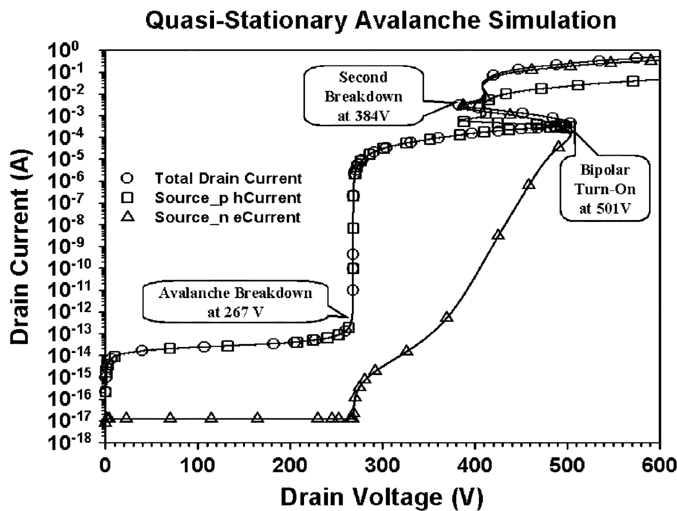

Fig. 13. Quasi-stationary avalanche curve of an IR R6 250 VN MOSFET showing that the second breakdown voltage is significantly higher than the normal avalanche breakdown voltage.

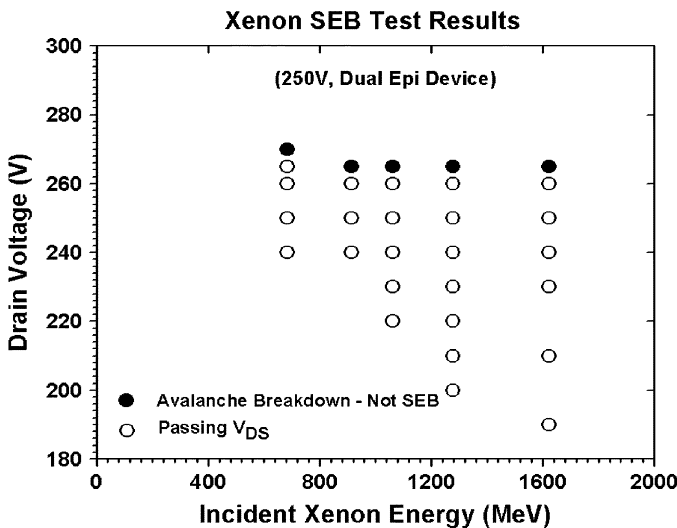

Fig. 14. SEB test results of IR R6 250VN rad-hard MOSFET, which uses a dual epitaxial layer, at different Xenon energies.

fail from regular avalanche breakdown before it fails from SEB, which was the case when devices were exposed to xenon. In addition, the avalanche curve indicates that the parasitic bipolar is suppressed until the source_n electron current reaches 1.64×10^{-4} A.

The SEE test results for the IR R6 250 VN rad-hard MOSFET using xenon at six different beam energies are reproduced in Fig. 14, [9]. All samples tested either failed due to regular avalanche breakdown or failed due to SEGR under a higher gate bias. No SEB failures were observed.

V. Conclusion

Quasi-stationary avalanche simulations confirm that 1) SEB is due to the turn on of the parasitic bipolar transistor; 2) SEB can be determined from the device's avalanche characteristics and the secondary breakdown voltage on the avalanche curve is directly related to power MOSFET's SEB threshold voltage; 3) the SEB trigger is not due to the heavy ion strike alone but a combination of high electric field along with the injection of electron-hole pairs from the heavy ion strike. Simulation results with different epitaxial materials and source doses agree with test results. Quasi-stationary avalanche simulation is capable of predicting SEB failure susceptibility and will be a valuable tool in future device development to meet radiation hardness requirements.

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