AURIX™ TC27x errata sheet

Marking/Step: ES-DC, DC

10500AERRA

About this document

Scope and purpose

This document describes the deviations of the device from the current user documentation, to support the assessment of the effects of these deviations on your custom hardware and software implementations.

Please take note of the following information:

- This errata sheet applies to all temperature and frequency versions and to all memory size variants, unless explicitly noted otherwise. For a derivative synopsis, see the latest datasheet or user manual
- Multiple device variants are covered in this one document. If an issue is related to a particular module, and this module is not specified for a specific device variant, then the issue does not apply to that device variant
  - For example, issues with the identifier "EMEM" (extension memory) do not apply to devices for which no extension memory is specified ("EMEM" is used only as a generic example and may not be a feature of the device that this document covers)
- Devices marked with EES or ES are engineering samples which may not be completely tested in all functional and electrical characteristics and are therefore only suitable for evaluation
  - The specific test conditions for EES and ES are documented in a separate status sheet
- Some of the errata have workarounds which may be supported by the tool vendors. Some corresponding compiler switches may need to be set. Please refer to the respective documentation of your compiler
- To understand the effect of issues relating to the on-chip debug system, please refer to the respective debug tool vendor documentation

Table 1 Current documentation

TC27x D-Step User's Manual	V2.2	2014-12
TC270/TC275/TC277 DC-Step Data Sheet	V1.2	2019-04
TriCore™ TC1.6P & TC1.6E: • Core Architecture • Instruction Set	 V1.0D10 V1.0D15	 2012-02 2013-07
OCDS User's Manual (distribution under NDA, only relevant for tool development not for application development)	V2.9.1	2014-11-24

Newer versions replace older versions, unless specifically stated otherwise.

Please always refer to the corresponding documentation for this device available in the category 'Documents' at www.infineon.com/AURIX™ and www.myInfineon.com.

Conventions used in this document

Each erratum identifier follows the pattern [Module]_[Arch].[Type][Number]:

- [Module] = subsystem, peripheral, or function affected by the erratum
- [Arch] = microcontroller architecture where the erratum was initially detected
  - AI = Architecture Independent
  - TC = TriCore™
- [Type] = category of deviation
  - [none] = Functional deviation

About this document

  - P = Parametric deviation
  - H = Application hint
- [Number] = ascending sequential number within the three previous fields

  ***Note**:* *[Number] As this sequence is used over several derivatives, including already solved deviations, gaps can occur inside this numbering sequence*

Table of contents

1 Errata overview

List of errata referenced in this document.

Table 2 Functional deviations

Issue title	Change	Page
[ADC_AI.016] No Channel Interrupt in Fast Compare Mode with GLOBRES		21
[ADC_TC.068] Effect of VAGND Cross Coupling on Conversion Result		21
[ASCLIN_TC.004] SLSO in SPI mode still active after module disable		24
[ASCLIN_TC.005] Unjustified collision detection error in half-duplex SPI mode		24
[ASCLIN_TC.006] Unjustified response timeout in LIN slave mode		25
[ASCLIN_TC.007] Break Detected in LIN Frames in Soft Suspend mode		25
[ASCLIN_TC.008] Response timeout in LIN Mode in case of header only		25
[ASCLIN_TC.009] RFL flag set in Buffer Mode when Receive FIFO Inlet is disabled		25
[ASCLIN_TC.010] Flush of TXFIFO leads to frame transmission		26
[BROM_TC.008] Sporadic Power-on Reset after Wake-up from Standby Mode		26
[CPU_TC.123] Data Corruption possible when CPU GPR accesses made via SRI slave with CPU running		26
[CPU_TC.127] Pending Interrupt Priority Number PIPN in Register ICR		27
[CPU_TC.131] Performance issue when MADD or MSUB instructions use E0 or D0 register as accumulator		27
[CPU_TC.132] Unexpected PSW values used upon Fast Interrupt entry		28
[DAP_TC.002] DAP client_blockread has Performance issue in Specific Operation Modes		29
[DAP_TC.003] DAP CRC32 definition and algorithm		29
[DAP_TC.004] DAP client_blockwrite telegram with CRC6 and CRC32 protection options		30
[DAP_TC.005] DAP client_read: dirty bit feature of Cerberus' Triggered Transfer Mode		31
[DAP_TC.006] CRC6 error in telegram following a get_CRCdown telegram prevents reset of CRC32 calculator		31
[DAP_TC.009] CRC6 error in client_blockwrite telegram		32
[DMA_TC.015] DMA Double Buffering: No Timestamp Support		32
[DMA_TC.016] Byte and Half-word Write Accesses to specific Registers not supported		32
[DMA_TC.017] Pattern Detection Double Interrupt Trigger when INTCT = 11_B		33
[DMA_TC.018] FPI timeout can cause pipelined register reads to break		33
[DMA_TC.019] CBS Accesses with Large SPB:SRI Clock Ratios Configured		33
[DMA_TC.020] DMA Conditional Linked List: Circular Buffer Enabled		34
[DMA_TC.021] Combined Software/Hardware Controlled Mode Spurious Errors		34
[DMA_TC.022] Conditional Linked List: Bus Error		34

(table continues...)

Table 2 (continued) Functional deviations

Issue title	Change	Page
[DMA_TC.024] Suspend Request coincident with Channel Activation		35
[DMA_TC.025] Conditional Linked List: new non-CLL mode TCS load can corrupt SDCRC RAM write		35
[DMA_TC.026] Linked List: Failed TCS load can trigger wrap interrupt		35
[DMA_TC.028] Transaction Request Lost (TRL) Interrupt Service Request Behaviour		35
[DMA_TC.031] CHCSR.ICH can be incorrectly set after pattern match		36
[DMA_TC.034] DMA Timestamp and Destination Circular Buffer		36
[DMA_TC.035] Last DMA Transaction in a Linked List triggers a DMA Daisy Chain		37
[DMA_TC.036] Linked List: SADR/DADR can be overwritten when loading a non-LL TCS		37
[DMA_TC.037] Conditional Linked List: Bit TSR.CH not cleared for a CLL transaction upon pattern match		38
[DMA_TC.038] Linked List: SIT interrupt when SIT bit set in newly loaded TCS		38
[DMA_TC.039] Read Data CRC		38
[DMA_TC.040] DMA Linked Lists: Intermittent Clearing of Hardware Transaction Request Enable with mixed mode Transaction Control Sets		38
[DMA_TC.041] DMA Circular Buffer Wrap Interrupt		39
[DMA_TC.042] DMA Interrupt from Channel reported before Completion of DMA Transaction		40
[DMA_TC.043] DMA Write Move Data Corruption for non 32-byte Aligned Cacheable Source Address		40
[DMA_TC.044] Clock Switch after SPB Error Reported results in Spurious SRI Error		40
[DMA_TC.045] DMA Reconfigures DMA Channels Lockup		41
[DMA_TC.046] Shadow Operation Read Only Mode		41
[DMA_TC.048] DMARAM Internal ECC Error		41
[DMA_TC.049] Bus Error Reported During LL TCS Load		42
[DMA_TC.050] Clearing CHCSR.FROZEN during Double Buffering		42
[DMA_TC.051] DMARAM Alarm		42
[DMA_TC.052] SER and DER During Linked List Operations		43
[DMA_TC.053] TS16_ERR Type of Error Reporting Unreliable		43
[DMA_TC.054] DMA Channel Halt Acknowledge Unreliable		43
[DMA_TC.055] ICU to DMA Interface in Sleep Mode		44
[DMA_TC.056] TSR and SUSENR Access Protection Unreliable		44
[DMA_TC.058] Linked List Load Transaction Control Set (TCS) Integrity Error		45
[DMA_TC.061] DMA Double Buffering Operations		46
[DMA_TC.062] Termination of DMA Transaction for Pattern Match		47

(table continues...)

1 Errata overview

Table 2 (continued) Functional deviations

Issue title	Change	Page
[DMA_TC.063] DMA Timestamp Destination Address		47
[DMA_TC.064] DMA Daisy Chain Request		48
[DMA_TC.065] DMA Move Concurrent Bus Accesses		48
[DMA_TC.066] DMA double buffering operations - Update address pointer		48
[DSADC_TC.011] Modulator Coupling Option no longer supported		49
[DSADC_TC.012] Common Mode Hold Voltage Not Applied During Calibration		49
[DSADC_TC.013] Common Mode Voltage Selection		49
[DTS_TC.001] Temperature Sensor Formula		50
[ETH_AI.003] Overflow Status bits of Missed Frame and Buffer Overflow counters get cleared without a Read operation		50
[ETH_TC.004] DMA Access to Reserved/Protected Resources: FPI Error Response not correctly evaluated		51
[FLASH_TC.052] Use of Write Page Once command		51
[FlexRay_AI.087] After reception of a valid sync frame followed by a valid non-sync frame in the same static slot the received sync frame may be ignored		52
[FlexRay_AI.088] A sequence of received WUS may generate redundant SIR.WUPA/B events		52
[FlexRay_AI.089] Rate correction set to zero in case of SyncCalcResult=MISSING_TERM		53
[FlexRay_AI.090] Flag SFS.MRCS is set erroneously although at least one valid sync frame pair is received		53
[FlexRay_AI.091] Incorrect rate and / or offset correction value if second Secondary Time Reference Point (STRP) coincides with the action point after detection of a valid frame		54
[FlexRay_AI.092] Initial rate correction value of an integrating node is zero if pMicroInitialOffsetA,B = 0x00		54
[FlexRay_AI.093] Acceptance of start-up frames received after reception of more than gSyncNodeMax sync frames		55
[FlexRay_AI.094] Sync frame overflow flag EIR.SFO may be set if slot counter is greater than 1024		55
[FlexRay_AI.095] Register RCV displays wrong value		55
[FlexRay_AI.096] Noise following a dynamic frame that delays idle detection may fail to stop slot		56
[FlexRay_AI.097] Loop back mode operates only at 10 MBit/s		56
[FlexRay_AI.099] Erroneous cycle offset during start-up after abort of start-up or normal operation		57
[FlexRay_AI.100] First WUS following received valid WUP may be ignored		57
[FlexRay_AI.101] READY command accepted in READY state		58

(table continues...)

Table 2 (continued) Functional deviations

Issue title	Change	Page
[FlexRay_AI.102] Slot status vPOC!SlotMode is reset immediately when entering HALT state		58
[FlexRay_AI.103] Received messages not stored in Message RAM when in Loop Back Mode		58
[FlexRay_AI.104] Missing start-up frame in cycle 0 at coldstart after FREEZE or READY command		59
[FlexRay_AI.105] RAM select signals of IBF1/IBF2 and OBF1/OBF2 in RAM test mode		59
[FlexRay_AI.106] Data transfer overrun for message transfers Message RAM to Output Buffer (OBF) or from Input Buffer (IBF) to Message RAM		60
[GTM_AI.139] ATOM SOMC mode: forced update does not activate comparison		62
[GTM_AI.140] ATOM SOMC mode: a write access to ATOM_CH_CTRL sets WRF if CCU0 compare match already occurred but CCU1 compare match open		63
[GTM_AI.141] TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TIEM, TPWM, TIPM, TPIM, TGPS		63
[GTM_AI.142] TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TBCM		64
[GTM_AI.143] GTM_TOP level: AEI pipelined write to GTM_BRIDGE_MODE register directly after setting aei_reset='0' can result in blocking of AEI configuration interface		65
[GTM_AI.146] ATOM SOMC mode: compare match does not clear WR_REQ		65
[GTM_AI.150] TIM: Valid edge after Timeout		65
[GTM_AI.152] DPLL: THVAL value not immediately available at inactive trigger slope		66
[GTM_AI.153] TIM: Incorrect data captured to CNTS register when TIM channel operates in mode TPWM or TPIM and CNTS_SEL = 1 and selected CMU_CLK ≠ sys_clk		66
[GTM_AI.154] TOM: Incorrect duty cycle in PCM mode (bit reversed mode)		67
[GTM_AI.158] DPLL: Reset of pcm1/pcm2 bits in relation to an interrupt		67
[GTM_AI.161] DPLL MTI/TORI-IRQ's are not activated when low_res='1' and ts0_hrt='1'; MSI/SORI-IRQ's are not activated when low_res='1' and ts0_hrs='1'		68
[GTM_AI.162] DPLL: Input signal (active edge) which is ignored by PVT-check occurring at a gap in the profile or a lost input signal causes that the MTI_IRQ is not activated		68
[GTM_AI.163] TIM: timeout signaled when TDU unit is reenabled		69
[GTM_AI.164] TIM: capturing of data into TIM[i]_CH[x]_CNTS with setting CNTS_SEL=1 not functional in TPWM and TPIM mode		69
[GTM_AI.166] DPLL: The content of registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext is added independently of the state of DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status to the pointers apt_2b/aps_1c2		70
[GTM_AI.167] ATOM SOMP mode: for RST_CCU0=1 and ARU_EN=1, if CN0 reaches CM0 an update of the register SRx is requested		70

(table continues...)

Table 2 (continued) Functional deviations

Issue title	Change	Page
[GTM_AI.168] DPLL: CPU read / write accesses to RAM2 in competition to DPLL accesses to RAM2 may lead to wrong SYN_T data read by DPLL		71
[GTM_AI.169] DPLL: no TORI/SORI interrupt in case low_res = 1 AND ts0_hrt/s = 0		72
[GTM_AI.170] DPLL: Action calculation: requested action not always calculated immediately		72
[GTM_AI.172] TIM: overflow bit in TIM ARU data not set; signal level bit in ARU data has opposite value		73
[GTM_AI.173] DPLL: new PMT data not received		73
[GTM_AI.174] DPLL: PMT result not sent to ARU		74
[GTM_AI.178] MCS: Evaluation of CAT bit after blocking ARU instruction		75
[GTM_AI.181] TIM: Incorrect signal level bit ECNT[0] in mode TIEM, TPWM, TIPM, TPIM, TGPS		75
[GTM_AI.202] (A)TOM: no CCU1 interrupt in case of CM1=0 or 1 and RST_CCU0=1		76
[GTM_AI.204] TIM: incorrect signal level on TIM_MODE change if TIM channel is disabled		76
[GTM_AI.205] TIM: unexpected CNTS register update in TPWM OSM mode		77
[GTM_AI.208] DPLL: Start of sub-increment generation and action calculation delayed by one input event if PCM1/2 bits are set and DPLL_STATUS.FTD = '0'		77
[GTM_AI.209] TOM/ATOM: no update of CM0/CM1/CLK_SRC via trigger signal from preceding instance if selected CMU_CLKx is not SYS_CLK		78
[GTM_AI.210] ATOM: data loss in SOMS one-shot mode if ARU is enabled and the period of the selected CMU_CLKx is greater than ARU-cycle-time/2		78
[GTM_AI.212] F2A: stream data register will not be deleted after disabling stream		79
[GTM_AI.215] FIFO: read pointer will be incremented in ring buffer mode on empty FIFO channel with read access from AFD_CHx_BUF_ACC		79
[GTM_AI.218] DPLL: PWI-IRQ permanently activated		79
[GTM_AI.219] DPLL: Wrong internal pointer calculation in case of backwards direction can lead to wrong PMT calculation results (PMT in PAST)		80
[GTM_AI.220] DPLL: PVT check is deactivated in case of direction change; Behaviour implemented but not documented in specification so far		80
[GTM_AI.221] DPLL: Possible inconsistency of internal pointers and parameter NUTE/NUSE when NUTE/NUSE modified in dedicated time window		81
[GTM_AI.222] DPLL: TAXI-irq not deactivated for THMA=0		81
[GTM_AI.223] DPLL: discontinuities in the sub increments when DPLL_NUTC/S.FST/FSS=1; set to full scale		82
[GTM_AI.247] DPLL: Input event not served after DPLL_CTRL_1.DEN is activated		82
[GTM_AI.250] DPLL: DPLL_STATUS.BWD1/2 not reset after DPLL_CTRL_1.DEN = 1->0->1, when DPLL_CTRL_0 has been written some time before		83

(table continues...)

Table 2 (continued) Functional deviations

Issue title	Change	Page
[GTM_AI.260] TOM/ATOM: Async. update in SOMP mode with CM1=0 and selected CMU clock unequal sys_clk not functional		83
[GTM_AI.270] (A)TOM: output signal is postponed one period for the values CM0=1 and CM1>CM0 if CN0 is reset by the trigger of a preceding channel (RST_CCU0=1)		84
[GTM_AI.271] DPLL: No DCGI-irq after direction change and DPLL_CTRL_0 has been written		84
[GTM_AI.272] DPLL: No update of DPLL_RAM1b.PSTC after direction change and DPLL_CTRL_0 has been written		85
[GTM_AI.278] FIFO: Restoring of F2A (ARU to FIFO interface) read access to FIFO after GTM_HALT condition not functional		86
[GTM_AI.292] DPLL: pulse correction at direction change incompletely for DPLL_CTRL_1.SMC='1'		87
[GTM_AI.300] DPLL: Change to forward operation when DPLL_THMI is set to zero does not work correctly		87
[GTM_AI.301] DPLL: Reset of DPLL_STATUS.BWD1=1 by disabling the DPLL does not cause the direction to change from backward to forward in any case		88
[GTM_AI.302] DPLL: Pulse generation ongoing for DPLL_CTRL_1.DMO=1 (continuous mode) if DPLL_CTRL_1.sge1/2=0		88
[GTM_AI.306] DPLL: DPLL_NUTC.syn_t_old, DPLL_NUSC.syn_s_old not updated according specification		89
[GTM_AI.317] DPLL: DPLL_STATUS.LOCK1/2 is set incorrectly when direction change, unexpected missing trigger/state or trigger/state out of range occurs		90
[GTM_AI.320] ATOM: Unexpected restart of a SOMS oneshot cycle while ATOM[i]_CH[x]_CM0 is zero		91
[GTM_AI.323] DPLL: Registers DPLL_NUTC.SYN_T and DPLL_NUSC.SYN_S are updated by the profile (ADT_T.NT/ADT_S.NS) before the DPLL is synchronized (DPLL_STATUS.SYT/S=0)		92
[GTM_AI.326] TIM: ARU bit ACB[0] (signal level) incorrect in case a second ARU request occurs while the actual request is just acknowledged		92
[GTM_AI.336] GTM Bus Bridge: Incorrect AEI access execution in case the previous AEI access was aborted with the access timeout abort function		93
[GTM_AI.340] TOM/ATOM: Generation of TRIG_CCU0/TRIG_CCU1 trigger signals skipped in initial phase of A/TOM SOMP one-shot mode		93
[GTM_AI.342] DPLL: Unwanted direction change when switching to emergency mode during active phase of TRIGGER input signal		94
[GTM_AI.346] ATOM SOMS mode: Shift cycle is not executed correctly in case the reload condition is deactivated with ATOM[i]_AGC_GLB_CTRL.UPEN = 0		95
[GTM_AI.348] DPLL: Correction of missing pulses delayed after start of pulse generation		96

(table continues...)

Table 2 (continued) Functional deviations

Issue title	Change	Page
[GTM_AI.349] TOM-SPE: OSM-Pulse width triggered by SPE_NIPD for selected CMU_FXCLK not correct		96
[GTM_AI.350] TOM-SPE: Update of SPE[i]_OUT_CTRL triggered by SPE_NIPD not working for a delay value 1 in TOM[i]_CH[x]_CM1		97
[GTM_AI.351] MAP: Disable of input lines by MAP_CTRL register not implemented for input signals TSPP0 TIM0_CHx(48) (x=0..2) and TSPP1 TIM0_CHx(48) (x=3..5)		97
[GTM_AI.353] SPEC-ATOM: Specification of the smallest possible PWM period in SOMP mode wrong, when ARU_EN=1		98
[GTM_AI.361] IRQ: Missing pulse in single-pulse interrupt mode on simultaneous interrupt and clear event		99
[GTM_AI.380] (A)TOM: potentially wrong output signal in case of RST_CCU0=1 and CM0=1 on triggered channel in SOMP mode		100
[GTM_AI.398] DPLL: Incorrect DPLL_THVAL calculation leading to a false direction decision in case tbu_ts0 wraps around		100
[GTM_AI.408] (A)TOM-RTL: Missing edge on output signal (A)TOM_OUT when CN0 is reset with force update event		101
[GTM_AI.410] GTM_AEI: The AEI bridge might not execute an accepted write transaction	New	102
[GTM_AI.419] TIM: Potentially wrong capture values		102
[GTM_AI.421] GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in pipeline mode can lead to violation of pipeline protocol		103
[GTM_AI.422] DPLL: Wrong DPLL_RDT_S_ACT/DPLL_RDT_T_ACT value in case of overflow correction		104
[GTM_AI.429] TIM: Missing glitch detection interrupt event		104
[GTM_AI.430] TIM: Unexpected increment of filter counter		105
[GTM_AI.431] TIM: Glitch detection interrupt event of filter is not a single cycle pulse		106
[GTM_AI.450] DPLL: Stored time stamp values do not consider filter delays		106
[GTM_AI.451] DPLL: Wrong measured position stamps in RAM		107
[GTM_AI.456] DPLL: No action calculation		107
[GTM_AI.458] DPLL: Missing TOR interrupt and status flag		108
[GTM_AI.462] (A)TOM: Missing CCU0TC_IRQ interrupt signal		108
[GTM_AI.463] DPLL: DPLL_PVT not cleared after direction change		109
[GTM_AI.474] DPLL: DPLL_PSTC, DPLL_PSSC erroneously modified		109
[GTM_AI.475] DPLL: Incorrect values of DPLL_RCDT_TX, DPLL_RCDT_SX		110
[GTM_AI.477] DPLL: DPLL_DCGI interrupt not triggered		110
[GTM_AI.478] DPLL: Incorrect calculation of DPLL_THVAL, DPLL_THVAL2		111

(table continues...)

Table 2 (continued) Functional deviations

Issue title	Change	Page
[GTM_AI.487] GTM_AEI: Changing BRIDGE_MODE[2:0] in pipeline mode can lead to violation of pipeline protocol		111
[GTM_AI.488] GTM_AEI: Turning off BRIDGE_MODE.MSK_WR_RSP in asynchronous mode might lead to following transactions being corrupted		112
[GTM_AI.492] DPLL: Wrong value of DPLL_INC_CNT1.INC_CNT1 upon switching to normal mode		112
[GTM_AI.507] DPLL: Irregular pulse generation and wrong PMT results	New	113
[GTM_AI.516] SPE-RTL: IRQ raised on disabled inputs	New	114
[GTM_AI.517] (A)TOM: Missing edge on output signal (A)TOM_OUT	New	114
[GTM_AI.522] (A)TOM: Edge at output signal (A)TOM_OUT does not occur	New	115
[GTM_TC.010] Effects of GTM Resets		115
[GTM_TC.012] Read Access Control by Register ODA		116
[HSCT_TC.007] RX_FIFO overflow interrupt		117
[HSCT_TC.009] Sleep mode not to be used		117
[HSCT_TC.010] Master Mode Interface Test Mode not working		117
[HSCT_TC.014] HSCT PLL lock loss error during the start-up of PLL	New	117
[I2C_TC.001] I2C FIFO data buffer does not support double buffering		118
[I2C_TC.003] Limits on selectable INC and DEC values		119
[I2C_TC.004] High speed mode: SCL clock ratio 1:2		119
[I2C_TC.005] Hold Time Start violation in Multi-Master Mode		120
[IOM_TC.002] Missed or spurious IOM events when pulse length exceeds Event Window counter range		120
[IOM_TC.003] Unexpected Event upon Kernel Reset		120
[IOM_TC.004] Write to IOM register space when IOM_CLC.RMC > 1		120
[MSC_TC.012] Increased Jitter for Data Frame Transmission in Repetition Mode with ABRA		121
[MSC_TC.013] Missing Chip Select for Command Frame with Length zero		122
[MSC_TC.014] Upstream Timeout Interrupt cannot be issued at Service Request Output SR4		122
[MSC_TC.015] Emergency Stop not effective at Injected Bit Positions in Downstream Frame		122
[MTU_TC.005] Access to MCx_ECCD and MCx_ETRRi while MBIST disabled		123
[MTU_TC.011] MBIST Bitmap not working for w0 - r1		123
[MTU_TC.012] Security of CPU cache memories during runtime is limited		124
[MTU_TC.016] Wrong Address(es) Tracked in Registers ETRRx of TC1.6E CPU0 PSPR and DSPR		124

(table continues...)

1 Errata overview

Table 2 (continued) Functional deviations

Issue title	Change	Page
[MultiCAN_TC.041] Clock used in Bit Timing Mode	New	128
[OCDS_TC.038] Disconnecting a debugger without device reset (“hot detach”) may require reading of OCS registers		128
[OCDS_TC.040] DAP turn_off to JTAG telegram not working properly		128
[OCDS_TC.042] OTGS capture registers can miss single clock cycle triggers		129
[OCDS_TC.043] Read-Modify-Write Bus Transactions to Cerberus Registers		129
[PADS_TC.012] Pull-ups activate on specific analog inputs upon PORST		130
[PLL_ERAY_TC.001] PLL_ERAY Initialization after Cold Power-up or Wake-up from Standby mode		130
[PLL_TC.005] PLL Initialization after Cold Power-up or Wake-up from Standby mode		130
[PLL_TC.007] PLL Loss of lock when oscillator shaper is used		131
[PMC_TC.004] Field SDFREQSPRD in register EVRSDCTRL1 – Documentation update		132
[PORTS_TC.002] Behavior of P21 Port Pins upon Power-on Reset		132
[PSI5_TC.005] Incorrect read pointer upon two consecutive RDFn read operations if two or more channels are configured		133
[QSPI_TC.006] Baud rate error detection in slave mode (error indication in current frame)		133
[QSPI_TC.017] Slave: Reset when receiving an unexpected number of bits		134
[RESET_TC.005] Indication of Power Fail Events in SCU_RSTSTAT		134
[SCU_TC.034] $\overline{\text{TESTMODE}}$ pin shall be held at static high level during LBIST		134
[SMU_TC.006] OCDS Trigger Bus OTGB during Application Reset		134
[SMU_TC.007] Size and Position of Field ACNT in Register SMU_AFCNT		135
[SMU_TC.008] Behavior of Action Counter ACNT		135
[SMU_TC.010] Transfer to SMU_AD register not triggered correctly		136
[SMU_TC.012] Unexpected alarms when registers FSP or RTC are written		136

Table 3 Parametric deviations

Issue title	Change	Page
[ADC_TC.P011] Leakage current for ADC reference pins VAREF, VAGND		138
[FlexRay_TC.P002] Pad Configuration for E-Ray Parameters		141
[IDD_TC.H001] IPC Limits used in Production Test for IDD Max Power Pattern		142
[IPA2_TC.P001] Pull-up/-down current for A2 pad - Documentation update		142
[KOVA_TC.P001] Increased overload coupling factor (KOVAP, KOVAN) for specific analog pins		142
[PADS_TC.P002] Restrictions for P00.1 .. P00.12 if V_{DDM} is lower than V_{EXT}		143

(table continues...)

Table 3 (continued) Parametric deviations

Issue title	Change	Page
[PADS_TC.P003] Input Frequency f_{IN} for Class S Pads		143
[PADS_TC.P006] P21.6/P21.7 Pull-up Reset Behavior		143
[PADS_TC.P009] Bonding of VGATE1P on Bare Die Variants		144
[QSPI_TC.P001] Master Mode timing for MPss output pads (5 V) - Documentation update		145
[RTH_TC.H001] Thermal characteristics of the package - Footnote update for LF-BGA-292-6 package		145
[VDDPPA_TC.H001] Voltage to ensure defined pad states - Footnote update		146

Table 4 Application hints

Issue title	Change	Page
[ADC_AI.H003] Injected conversion may be performed with sample time of aborted conversion		147
[ADC_TC.H012] DSADC/VADC Connections to VAREF1/2, VAGND1/2		147
[ADC_TC.H014] VADC Start-up Calibration		148
[ADC_TC.H015] Conversion Time with Broken Wire Detection		148
[ADC_TC.H016] P02 Output Driver Setting for External Multiplexer Control		149
[ADC_TC.H019] G6ARBCNT Connection to GTM		149
[ADC_TC.H020] Minimum/Maximum Detection Compares 12 Bits Only		150
[ADC_TC.H022] Sample Time Control - Formula		150
[ADC_TC.H024] Documentation: Filter control only in registers GxRCR7/GxRCR15		150
[ADC_TC.H038] Multiplexer Diagnostics Connection - Documentation update		151
[ASCLIN_TC.H001] Bit field FRAMECON.IDLE in LIN slave tasks		151
[ASCLIN_TC.H003] Behavior of LIN Autobaud Detection Error Flag		151
[ASCLIN_TC.H004] Changing the Transmit FIFO Inlet Width / Receive FIFO Outlet Width		151
[ASCLIN_TC.H005] Collision detection error reported twice in LIN slave mode		152
[ASCLIN_TC.H006] Sample point position when using three samples per bit		153
[ASCLIN_TC.H008] SPI master timing – Additional information to Data Sheet characteristics		153
[BCU_TC.H001] HSM Transaction Information not captured		154
[BoardDesign_TC.H001] Common board design for PD and ED in QFP packages		154
[BROM_TC.H003] Information related to Register FLASH0_PROCOND		154
[BROM_TC.H009] Re-enabling lockstep via BMHD		155
[BROM_TC.H010] Interpretation of value UNIQUE_CHIP_ID_32BIT		155
[BROM_TC.H019] CRC32 ethernet polynomial - Footnote correction		155

(table continues...)

Table 4 (continued) Application hints

Issue title	Change	Page
[CCU6_AI.H001] Update of Register MCMOUT		155
[CCU6_AI.H002] Description of Bit RWHE in Register ISR		156
[CCU6_AI.H003] Bit TRPCTR.TRPM2 in Manual Mode - Documentation Update		156
[CCU_TC.H001] Clock Monitor Check Limit Values		156
[CCU_TC.H002] Oscillator Gain Selection via OSCCON.GAINSEL		157
[CCU_TC.H005] References to f_{PLL2}, f_{PLL2_ERAY} and K3 Divider in User's Manual		158
[CCU_TC.H006] Clock Monitor Support - Documentation Update		158
[CCU_TC.H007] Oscillator Watchdog Trigger Conditions for ALM3[0]		159
[CCU_TC.H010] Oscillator Mode control in register OSCCON - Documentation Update		159
[CPU_TC.H006] Store Buffering in TC1.6/P/E Processors		159
[CPU_TC.H008] Instruction Memory Range Limitations		161
[CPU_TC.H009] Details on CPU Clock Control		161
[CPU_TC.H010] External Accesses to CPU Local Memory may delay CPU Execution Progress		162
[CPU_TC.H012] Behavior of bit-wise operations on certain peripheral register bits which need to be written back with the same value		162
[CPU_TC.H014] ACCEN* Protection for Write Access to Safety Protection Registers - Documentation Update		164
[CPU_TC.H015] Register Access Modes for Safety Protection Registers - Documentation Update		164
[CPU_TC.H017] MSUB.Q does not match MUL.Q+SUB - Documentation Update		164
[CPU_TC.H019] Semaphore handling for shared memory resources		165
[CPU_TC.H021] Resource update failure despite correct SW synchronization upon retried FPI write transactions by CAN and E-Ray modules		167
[DAP_TC.H002] DAP client_blockread in Combination with TGIP and all Parcels with CRC6		168
[DAP_TC.H003] Not acknowledged DAP telegrams in noisy environments		168
[DMA_TC.H002] Bit CHCSRz.BUFFER can be toggled when not in Double Buffer Mode		168
[DMA_TC.H003] Spurious Error Interrupt Service Requests after Transaction Lost Event in Double Buffer Mode		169
[DMA_TC.H004] Transaction Request Lost upon software trigger with pattern match		169
[DMA_TC.H005] Linked List Transfer leading to loading of non-Linked List TCS causes corruption		169
[DMA_TC.H006] Clearing of HTRE when DMA channel is configured for Single Mode		169
[DMA_TC.H007] Selecting the Priority for DMA Channels		170
[DMA_TC.H008] Transaction Request State		171

(table continues...)

Table 4 (continued) Application hints

Issue title	Change	Page
[DMA_TC.H009] Resetting Bits ICH and IPM in register CHCSRz		171
[DMA_TC.H010] Calculation of DMA Address Checksum for DMA read moves to Cacheable Addresses		171
[DMA_TC.H011] DMA_ADICRz.SHCT - Reserved Values		172
[DMA_TC.H012] TCS Update in Halt State		172
[DMA_TC.H013] MExSR.WS and MExSR.RS Status Bits		172
[DMA_TC.H014] DMARAM Error Interrupt Service Request		172
[DMA_TC.H015] DMARAM Address Integrity Errors		173
[DMA_TC.H016] DMARAM ECC Error Disable		173
[DMA_TC.H017] DMA Channel Request Control - Documentation Update		173
[DSADC_TC.H002] Influence of Temperature on DC Offset Error EDOFF (calibrated)		173
[DSADC_TC.H003] FIR Filters not reset when Integration starts		174
[DSADC_TC.H004] Full-scale Values produced by On-chip Modulator		174
[DSADC_TC.H005] Data Strobe Setting for On-chip Modulator		175
[DSADC_TC.H006] Avoiding Intermediate States		175
[DSADC_TC.H007] Dithering Control		176
[DSADC_TC.H008] DSADC Gain Calibration Procedure		176
[DSADC_TC.H009] DSADC digital connections		176
[DSADC_TC.H010] Support for synchronous use of two or more DSADC channels		177
[DTS_TC.H001] Update of Bit DTSSTAT.BUSY		177
[ENDINIT_TC.H001] Endinit Protection for Registers KRST0, KRST1, KRSTCLR		178
[ETH_AI.H001] Sequence for Switching between MII and RMII Mode		178
[ETH_TC.H001] ETHMDIO on P21.1 not to be used for productive systems		178
[ETH_TC.H002] Minimum operation frequency for Ethernet MAC		179
[ETH_TC.H003] Interrupt Generation by Wake-up or Magic Packet Frames		179
[ETH_TC.H004] Ethernet MAC Clock Control – Documentation update		179
[FLASH_TC.H007] Advice for using Suspend and Resume		179
[FLASH_TC.H008] Understanding Flash Retention/Endurance Figures in the Data Sheet		180
[FLASH_TC.H009] PFlash Operations Concurrent to DF1 Operations		181
[FLASH_TC.H022] Flash Wait State configuration		181
[FlexRay_AI.H004] Only the first message can be received in External Loop Back mode		182
[FlexRay_AI.H005] Initialization of internal RAMs requires one eray_bclk cycle more		182
[FlexRay_AI.H006] Transmission in ATM/Loopback mode		182

(table continues...)

Table 4 (continued) Application hints

Issue title	Change	Page
[FlexRay_AI.H007] Reporting of coding errors via TEST1.CERA/B		182
[FlexRay_AI.H009] Return from test mode operation		183
[FlexRay_AI.H011] Behavior of interrupt flags in FlexRay™ Protocol Controller (E-Ray)		183
[FlexRay_TC.H002] Initialization of E-Ray RAMs		183
[FlexRay_TC.H004] Bit WRECC in register TEST2 has no function		185
[FlexRay_TC.H005] E-Ray OTGB2 trigger set active even if disabled		185
[FPI_TC.H002] Write access to register ACCEN1		186
[GPT12_TC.H001] Timer T5 Run Bit T5R - Documentation Correction		186
[GPT12_TC.H002] Bits TxUD and TxUDE in incremental interface mode - Additional information		186
[GTM_AI.H473] SPEC-FIFO: Wrong description of FIFO flush operation		187
[GTM_AI.H481] SPEC-TIM: Wrong description for TBCM mode		188
[GTM_AI.H497] SPEC-SPE wiring in figure is wrong		189
[GTM_AI.H502] SPEC-DPLL input selection for SUB_INC1 is incomplete		189
[GTM_AI.H519] SPEC-(A)TOM: Misleading description of Continuous Counting Up Mode	New	190
[GTM_AI.H803] SPEC-(A)TOM: Missing priority information for register update	New	191
[GTM_TC.H003] Typo: GTM Chapters “Multi Channel Sequencer (MCS)” and “Memory Configuration (MCFG)” sometimes use “MSC” instead of “MCS”		191
[GTM_TC.H004] Correction to Bit Fields GTM_TIMi_IN_SRC.VAL_x		192
[GTM_TC.H005] External Capture in TIM Pulse Integration Mode (TPIM)		192
[GTM_TC.H007] GTM to CAN Timer Triggers		193
[GTM_TC.H008] Correction to Figure “SPE to TOM Connections”		194
[GTM_TC.H011] First CM0 updates in case of SR0=1 and (A)TOM used as Triggered Channel		194
[GTM_TC.H014] Synchronous Bridge Mode Restrictions		194
[GTM_TC.H015] Register TIMi_CHx_CTRL - Correction to Register Image		195
[GTM_TC.H016] Evaluating DSADC Signals SAULx/SBLLx		195
[GTM_TC.H017] Bit DXINCON.24 (DSS10) - Documentation Correction		196
[GTM_TC.H020] GTM can cause unintended bus errors after enabling when SPB or GTM frequency is very low		196
[HSCT_TC.H003] Functionality of bit TX_PWDPD		196
[HSCT_TC.H005] Access to reserved address 0xF009 0060 when $f_{SPB} = f_{SRI}$		196
[HSCT_TC.H007] HSSL Integrated Phase Noise		197
[HSCT_TC.H008] Details on PLL Lock-in Time		198

(table continues...)

Table 4 (continued) Application hints

Issue title	Change	Page
[HSCT_TC.H010] Interface control command timing on the LVDS ports		198
[I2C_TC.H001] I2C Module Behavior in OCDS Suspend Mode		199
[I2C_TC.H002] Initialization of INC/DEC values in Slave mode		200
[I2C_TC.H003] DMA Channel Configuration		201
[I2C_TC.H004] Transfers of more than 32 Bytes		201
[I2C_TC.H005] FIFO Data is lost during Transaction RX->TX		201
[I2C_TC.H008] Handling of RX FIFO Overflow in Slave Mode		202
[IOM_TC.H001] How to clear the IOM_LAMEWCm register		202
[IOM_TC.H002] IOM Clock Control		202
[IOM_TC.H003] Configuration of LAMCFG.IVW and LAMEWS.THR		203
[IOM_TC.H004] Behavior of LAMEWCn.CNT when LAMEWSn.THR is 0		204
[IOM_TC.H006] ACCEN* Protection for Write Access to IOM Registers		204
[IOM_TC.H007] Write Access to FPCESR		205
[LBIST_TC.H004] Update reset behavior of LBISTCTRL2 register - Additional information		205
[LMU_TC.H002] On-the-fly BBB:SRI clock ratio switching		205
[LMU_TC.H003] Function of Bit MEMCON.PMIC (Protection Bit for Memory Integrity Control Bit)		206
[MSC_TC.H010] Configuration of SCU.EMSR for the EMGSTOPMSC Signal		206
[MSC_TC.H011] Effect of kernel reset on MSC0_FCLP when selected in Event Trigger Logic		207
[MSC_TC.H012] Handling the overflow interrupt of the ABRA block		207
[MSC_TC.H013] Empty Data Frames not supported with ABRA		207
[MTU_TC.H003] AURIX™ Memory Tests using the MTU		207
[MTU_TC.H004] Handling the Error Tracking Registers ETRR		208
[MTU_TC.H005] Handling SRAM Alarms		208
[MTU_TC.H006] Alarm Propagation to SMU via Error Flags in MCx_ECCD		209
[MTU_TC.H007] Reset Values of Bit ECCS.TRE		210
[MTU_TC.H009] Reset Value for Register ECCD		210
[MTU_TC.H010] Register MCONTROL - Bit Field Res4		212
[MTU_TC.H011] Access Protection for Memory Control Registers		212
[MTU_TC.H012] Kernel Reset triggers Reset of MBIST Registers		213
[MTU_TC.H014] Access to SRAM while MTU operations are underway		213
[MultiCAN_AI.H005] TxD Pulse upon short disable request		213

(table continues...)

Table 4 (continued) Application hints

Issue title	Change	Page
[MultiCAN_AI.H006] Time stamp influenced by resynchronization		214
[MultiCAN_AI.H007] Alert Interrupt Behavior in case of Bus-Off		214
[MultiCAN_TC.H003] Message may be discarded before transmission in STT mode		214
[MultiCAN_TC.H004] Double remote request		215
[MultiCAN_TC.H007] Oscillating CAN Bus may Disable the CAN Interface		215
[MultiCAN_TC.H008] Changes due to CAN FD protocol ISO 11898-1:2015		215
[MultiCAN_TC.H009] Limitation on Secondary Sample Point (SSP) Position (ISO CAN FD nodes only)		218
[MultiCAN_TC.H010] Limitation on maximum SJW Range for CAN FD Data Phase (ISO CAN FD nodes only)		219
[MultiCAN_TC.H011] Transmitter Delay Compensation Behaviour (CAN FD only)		220
[MultiCAN_TC.H012] Delayed time triggered transmission of frames		220
[OCDS_TC.H012] Minimum Hold Time for Inputs OCDS_TGIx		220
[OCDS_TC.H019] System or Application Reset while OCDS and lockstep monitoring are enabled		221
[PACKAGE_TC.H006] Exposed pad dimensions and package outlines for QFP packages - Updates to TC27x Data Sheet		221
[PADS_TC.H001] Hysteresis Inactive Function		222
[PADS_TC.H002] Write Access to Register PMSWCR0 when HWCFG[6] = 0		223
[PADS_TC.H005] Input function ETHRXCLKA on P11.12 – Additional information		223
[PLL_ERAY_TC.H002] Correction in Figure “PLL_ERAY Block Diagram”		223
[PMC_TC.H001] Check for permanent Overvoltage during Power-up		223
[PMC_TC.H002] Description of Register PMSWSTAT		224
[PMS_TC.H002] Sensitivity to supply voltage ripple during start-up		224
[PMS_TC.H008] Interaction of interrupt and power management system - Additional information		226
[PMU_TC.H002] Impact of Application Reset on register FLASH0_FCON		227
[PORTS_TC.H006] Using P33.8 while SMU is disabled		228
[PORTS_TC.H008] Emergency Stop for LVDS TX Pads in LVDS Mode		228
[PORTS_TC.H013] Port 22 Pad Driver Mode 0 Register - Documentation Update		229
[PORTS_TC.H016] Oscillating signal may enable DXCPL and reconfigure the functionality of the port pins P14.0 and P14.1		229
[PSI5_TC.H001] No communication error in case of payload length mismatch		229
[QSPI_TC.H005] Stopping Transmission in Continuous Mode		229
[QSPI_TC.H006] Corrections to Figures “QSPI - Frequency Domains” and “Phase Duration Control, Overview”		230

(table continues...)

Table 4 (continued) Application hints

Issue title	Change	Page
[QSPI_TC.H007] RXFIFO Overflow Bit Behavior in Slave Mode		230
[QSPI_TC.H008] Details of the baud rate and phase duration control - Documentation update		231
[QSPI_TC.H009] Dummy frame required after changing SCLK polarity and phase in three wire mode		231
[QSPI_TC.H011] Missing information on SLSI misplaced inactivation enable error	New	231
[RESET_TC.H002] Unexpected SMU Reset Indication in SCU_RSTSTAT		232
[RESET_TC.H003] Usage of the Prolongation Feature for ESR0 as Reset Indicator Output		232
[SCU_TC.H009] LBIST Influence on Pad Behavior		233
[SCU_TC.H013] Correction to Register References in Chapter “Watchdog Timers”		233
[SCU_TC.H014] Reset Value of Bit Field IOCR.PC1 - Control for Pin $\overline{\text{ESR1}}$		233
[SCU_TC.H027] Bit field INP0 and INP1 in register EICRi - Documentation correction		234
[SCU_TC.H028] ERU configuration changes may lead to ERU reactions	New	235
[SCU_TC.H029] Non-master CPUs can wake-up unexpectedly when exiting from sleep mode	New	235
[SENT_TC.H002] SENT Nibble Tolerance		236
[SENT_TC.H003] First Write Access to Registers FDR and TPD after ENDINIT Status Change		236
[SENT_TC.H004] Short Serial Message - Figure Correction		237
[SENT_TC.H009] Unexpected NNI error behavior	New	238
[SMU_TC.H001] Write all bit-fields of SMU_PCTL with one write access		238
[SMU_TC.H004] Alarm Mapping related to ALM3[9] in ALM3 Group		238
[SMU_TC.H005] Correction to Figure “SMU Register Map”		238
[SMU_TC.H006] Description of Bit EFRST in Register SMU_AGC		239
[SMU_TC.H007] SPB Bus Control Unit (SBCU) Alarm Signalling to SMU		239
[SMU_TC.H010] Clearing individual SMU flags: use only 32-bit writes		239
[SMU_TC.H013] Increased Fault Detection for SMU Bus Interface (SMU_CLC Register)		240
[SMU_TC.H014] Unintended short pulse on FSP pins in Time switching or Dual-rail mode		240
[SRI_TC.H001] Using LDMST and SWAPMSK.W instructions on SRI mapped peripheral registers (range 0xF800 0000-0xFFFF FFFF)		241
[STM_TC.H001] Effect of kernel reset on interrupt outputs STMIR0/1		241
[STM_TC.H002] Access Protection for STM Control Registers		241
[STM_TC.H003] Suspend control for STMx - Documentation Update		242
[STM_TC.H004] Access to STM registers while STMDIV = 0		242

(table continues...)

1 Errata overview

Table 4 (continued) Application hints

Issue title	Change	Page
[TC27xDC_TC.H001] Revision history for datasheet TC27xDC_DS_v12		242

2 Functional deviations

2.1 [ADC_AI.016] No Channel Interrupt in Fast Compare Mode with GLOBRES

Description

In fast compare mode, the compare value is taken from bit-field RESULT of the selected result register and the result of the comparison is stored in the respective bit FCR.

A channel event can be generated when the input becomes higher or lower than the compare value.

In case the global result register GLOBRES is selected, the comparison is executed correctly, the target bit is stored correctly, source events and result events are generated, but a channel event is not generated.

Workaround

If channel events are required, choose a local result register GxRESy for the operation of the fast compare channel.

2.2 [ADC_TC.068] Effect of VAGND Cross Coupling on Conversion Result

Description

Due the implementation of the clock dividers as fractional dividers, a statistical phase shift of one f_{VADC} clock can occur between the operation of different converter groups. If the last f_{VADC} clock of the sample phase of a converter group Gx coincides with the first f_{VADC} clock of a conversion step of (one or more) other converter groups Gy, the Total Unadjusted Error (TUE) of the conversion result of Gx is increased due to cross coupling via VAGND.

Effects

- For TC29x and TC27x, the TUE is increased up to ± 80 LSB_{12}
- For TC26x, TC23x, TC22x, and TC21x, the TUE is increased up to ± 25 LSB_{12}

Workarounds - Introduction

***Note**:*

- *Workaround 1..3 may be used with any device step*
- *Workaround 4 can only be used with TC21x, TC22x, TC23x ≥ step AB, TC26x ≥ step BB, TC27x ≥ step DB, TC29x ≥ step BB.*

  For TC29x ≥ step BB, workaround 4 is the preferred workaround for this device, since for Workaround 1 in particular increased error limits would have to be accepted for high temperature / high pin-count variants.

Workaround 1

Synchronize the trigger events of different converter groups as follows:

Workaround 1: Implementation details for TC27x and TC29x

- Operate the arbiters and the analog parts of the VADC at the same clock frequency, i.e. select the divider factors DIVA and DIVD in register GLOBCFG such that $f_{ADCD} = f_{ADCI}$ for all converter groups:
  - For $f_{VADC} = f_{SPB} = 100$ MHz, reduce f_{ADCD} to 25 MHz (with DIVD = 3), and increase f_{ADCI} to 25 MHz (with DIVA = 3). Depending on supply/reference voltage and junction temperature T_J, this will result in the increased error limits shown in Table 5 (for TC27x in all package variants and for TC297 devices

in BGA-292 package) and Table 6 (for TC298/9 devices in BGA-416/516 package and TC290 bare die variants) below

- Otherwise, to achieve $f_{ADCD} = f_{ADCI} = 20$ MHz with the error limits specified in the Data Sheet, $f_{VADC} = f_{SPB}$ must be reduced to 80 MHz

- Enlarge the length of an arbitration round to a minimum of 16 arbitration slots (i.e. bit field GxARBCFG.ARBRND ≥ 2 for any x)
- Select the conversion time (including sample time) of the longest conversion of any group Gx to be shorter than two arbitration rounds. This ensures that all converters are idle when the arbiters have determined the next conversion request
- Synchronize the digital and the analog clock by switching off/on the Module Disable Request bit, i.e. set CLC.DISR = 1_B and then CLC.DISR = 0_B
- Initiate the start-up calibration by setting bit GLOBCFG.SUCAL = 1_B (mandatory after switching off/on VADC clocks via CLC.DISR)

Table 5 TC27x (all packages) and TC297 (in BGA-292 package): Increased VADC Error Limits for f_{ADCI} = 25 MHz, 12-Bit Resolution

Total Unadjusted Error TUE	DNL Error EA_{DNL}	INL Error EA_{INL}	RMS Noise EN_{RMS}	Unit	Condition	
					VAREF/VDDM	T_J
4.4	3.5	3.5	0.95	LSB	*5V ± 10%*	≤ 150°C
5.7	3.5	3.5	0.95			> 150°C
10	12	12	1.5	LSB	3.3 V ± 10 %	≤ 125°C
14	14	16	1.5			*125°C* < T_J ≤ 150°C
This workaround is not recommended for T_J > 150°C and VAREF/VDDM = 3.3 V ± 10 %						> 150°C

Table 6 TC298/9 in BGA-416/516 Package and TC290 bare die: Increased VADC Error Limits for f_{ADCI} = 25 MHz, 12-Bit Resolution

Total Unadjusted Error TUE	DNL Error EA_{DNL}	INL Error EA_{INL}	RMS Noise EN_{RMS}	Unit	Condition	
					VAREF/VDDM	T_J
6.4	6.0	5.4	0.95	LSB	*5V ± 10%*	≤ 150°C
8.4	7.9	7.1	0.95			> 150°C
10	12	12	1.5	LSB	3.3 V ± 10 %	≤ 125°C
14	14	16	1.5			*125°C* < T_J ≤ 150°C
This workaround is not recommended for T_J > 150°C and VAREF/VDDM = 3.3 V ± 10 %						> 150°C

***Note**: For error types (offset, gain, ..) not listed in the table above see corresponding values specified in the Data Sheet for f_{ADCI} = 20 MHz.*

***Note**: For available combinations of package type and temperature range see the corresponding AURIX™ TC2x Variants Data Sheet Addendum.*

Workaround 1: Implementation details for TC26x and TC23x, TC22x, TC21x

- Operate the arbiters and the analog parts of the VADC at the same clock frequency, i.e. select the divider factors DIVA and DIVD in register GLOBCFG such that $f_{ADCD} = f_{ADCI}$ for all converter groups:
  - Note: As $f_{ADCD} = f_{VADC}/4$ with the maximum divider (DIVD = 3), this implies that $f_{VADC} = f_{SPB}$ must be limited to 80 MHz to achieve $f_{ADCD} = f_{ADCI}$ with the error limits specified for f_{ADCI} = 20 MHz in the Data Sheet
- Enlarge the length of an arbitration round to a minimum of 16 arbitration slots (i.e. bit field GxARBCFG.ARBRND ≥ 2 for any x)
- Select the conversion time (including sample time) of the longest conversion of any group Gx to be shorter than two arbitration rounds. This ensures that all converters are idle when the arbiters have determined the next conversion request
- Synchronize the digital and the analog clock by switching off/on the Module Disable Request bit, i.e. set CLC.DISR = 1_B and then CLC.DISR = 0_B
- Initiate the start-up calibration by setting bit GLOBCFG.SUCAL = 1_B (mandatory after switching off/on VADC clocks via CLC.DISR)

Workaround 2

Ensure that conversions never overlap for any two converter groups Gx and Gy.

This may be achieved under software control, or by exclusively using the VADC background request source.

For this workaround, no restrictions apply on clock and arbitration round settings.

Workaround 3

Use the converters within a synchronization group in master/slave configuration, such that they are synchronized for parallel sampling, triggered by one common master. In this case, the cross coupling effect will not occur as long as only one synchronization group is performing conversions.

For devices that support more than one synchronization group, operate the synchronization groups in an interleaving manner.

For this workaround, no restrictions apply on clock and arbitration round settings.

Workaround 4

To avoid the cross coupling effect, this device step (see “Workarounds - Introduction” above) supports selection of signal CCU6061_TRIG1 to synchronize the start of the converter groups to a raster of $1/f_{ADCI}$ (e.g. $5/f_{SPB}$ = 50 ns @f_{SPB} = 100 MHz and f_{ADCI} = 20 MHz, or $4/f_{SPB}$ = 64 ns @f_{SPB} = 62.5 MHz and f_{ADCI} = 12.5 MHz). The resulting jitter (delay from trigger to start of conversion) is thus limited to max. $1/f_{ADCI}$.

For this workaround, either CCU60_T13 or CCU61_T13 is configured (reserved) to provide the synchronization signal. The selection is performed via bit field TRIG1SEL in register CCU60_MOSEL:

- TRIG1SEL = 000_B: signal CCU60_COUT63 from CCU60_T13 is selected
- TRIG1SEL = 001_B: signal CCU61_COUT63 from CCU61_T13 is selected

The synchronization signal is enabled inside the VADC module by setting bit GLOBCFG.DCMSB = 1_B. The default function of this bit (DCMSB = 0_B: one clock cycle for MSB conversion step) is hardwired and thus stays unaffected.

The following examples describe the initialization of CCU60 or CCU61, respectively, to provide a 20 MHz synchronization signal @f_{SPB} = 100 MHz:

Example for CCU60 initialization

```
CCU60_CLC = 0x0;          // enable CCU60 kernel
CCU60_T13PR = 0x4;        // 4+1 clock periods with ..
CCU60_CC63SR = 0x1;       // duty cycle 40 ns low / 10 ns high
CCU60_PSLR |= 0x0080;     // passive state level of COUT63 = 1
CCU60_MODCTR |= 0x8000;   // ECT13O = 1 enables T13 output (CC63ST -> COUT63)
CCU60_TCTR4 |= 0x4200;    // set bit T13STR and T13RS to enable shadow transfer and start T13
CCU60_MOSEL &= 0x1C7;     // CCU6061_TRIG1 is CCU60_COUT63
```

Example for CCU61 initialization

***Note**: In case an application only uses kernel CCU61, ensure that kernel CCU60 is also clocked until register CCU60_MOSEL is configured.*

```
CCU61_CLC = 0x0;          // enable CCU61 kernel
CCU60_CLC = 0x0;          // ensure CCU60 kernel is clocked until CCU60_MOSEL is configured
CCU61_T13PR = 0x4;        // 4+1 clock periods with ..
CCU61_CC63SR = 0x1;       // duty cycle 40 ns low / 10 ns high
CCU61_PSLR |= 0x0080;     // passive state level of COUT63 = 1
CCU61_MODCTR |= 0x8000;   // ECT13O = 1 enables T13 output (CC63ST -> COUT63)
CCU61_TCTR4 |= 0x4200;    // set bit T13STR and T13RS to enable shadow transfer and start T13
CCU60_MOSEL |= 0x8;       // CCU6061_TRIG1 is CCU61_COUT63
```

2.3 [ASCLIN_TC.004] SLSO in SPI mode still active after module disable

Description

It is expected that in SPI mode, after module disable, the Slave Select Output signal SLSO should be in idle state according to configuration of Slave Polarity in Synchronous mode (IOCR.SPOL).

However, in this design step, when the module is disabled, the Slave Select Output signal SLSO is always 0 (low) independent of IOCR.SPOL, i.e., it is still active even when IOCR.SPOL = 1_B.

Workaround

Before disabling the ASCLIN module, set SLSO to the desired level in the corresponding Port control registers.

2.4 [ASCLIN_TC.005] Unjustified collision detection error in half-duplex SPI mode

Description

In Half Duplex SPI mode, when collision detection is enabled and the number of stop bits in SPI frame is configured as any value from 1 to 7 in FRAMECON.STOP, a Collision Error (FLAGS.CE) is triggered during the trailing phase (i.e., during stop bits), although RX and TX signal are identical.

Workaround

In half-duplex SPI mode, set FRAMECON.STOP = 0 if trailing phase is irrelevant, or ignore/disable collision error if FRAMECON.STOP > 0.

2.5 [ASCLIN_TC.006] Unjustified response timeout in LIN slave mode

Description

When ASCLIN is configured as LIN slave and Response timeout is configured as DATCON.RM = 1_B, Response timeout is triggered even when an incomplete LIN Header frame is received. The timeout counter runs further after Header timeout detection without reset and triggers Response Timeout when it reaches the Response Timeout Threshold value defined by DATCON.RESPONSE.

Workaround

Ignore the Response Timeout which comes directly after a Header Timeout has occurred and before the next break is detected.

2.6 [ASCLIN_TC.007] Break Detected in LIN Frames in Soft Suspend mode

Description

When ASCLIN has entered Soft Suspend mode (OCS.SUS = 0x2), it still detects a Break Field in LIN frames and triggers an interrupt if enabled (FLAGSENABLE.BDE = 1_B).

Workaround

Ignore a detected break event when the module has been soft-suspended (for example set FLAGSENABLE.BDE = 0_B when using soft suspend mode).

2.7 [ASCLIN_TC.008] Response timeout in LIN Mode in case of header only

Description

In LIN (Master/Slave) mode, when Header Only (DATCON.HO = 1_B) is configured, Response timeout could occur even though no Response frame is expected.

Workaround

To avoid the unwanted interrupt, disable the interrupt on Response Timeout by FLAGSENABLE.RTE = 0_B whenever Header Only (DATCON.HO = 1_B) is configured.

2.8 [ASCLIN_TC.009] RFL flag set in Buffer Mode when Receive FIFO Inlet is disabled

Description

When RXFIFO is configured in Buffer Mode (RXFIFOCON.BUF = 1_B) and Receive FIFO Inlet is disabled (RXFIFOCON.ENI = 0_B), the receive FIFO level flag is set (FLAGS.RFL = 1_B) even though RXFIFO is not filled with new incoming data.

Workaround

To avoid the unwanted Receive FIFO Level interrupt, disable it by setting FLAGSENABLE.RFLE = 0_B whenever Receive FIFO Inlet is disabled (RXFIFOCON.ENI = 0_B),

2.9 [ASCLIN_TC.010] Flush of TXFIFO leads to frame transmission

Description

When the TXFIFO is flushed (TXFIFIOCON.FLUSH = 1_B), it triggers transmission of a frame in the following corner case:

- Starting condition:
  - TXFIFO is not empty and TXFIFOCON.ENO = 0_B
- Triggering condition:
  - Write to TXFIFOCON with both TXFIFOCON.FLUSH = 1_B and TXFIFOCON.ENO = 1_B

Workaround

Do not flush TXFIFO and change bit TXFIFOCON.ENO from 0_B to 1_B in one single write to TXFIFOCON if TXFIFO is not empty.

2.10 [BROM_TC.008] Sporadic Power-on Reset after Wake-up from Standby Mode

Description

On a wake-up from Standby mode, the Standby RAM redundancy installation procedure is executed. In case there is a sporadic Power-on reset in a time window between 600 µs - 1 ms after Standby mode wake-up, it can happen that the application data stored in specific Standby RAM cells are overwritten.

***Note**: This effect can occur only on devices where non-zero data are stored in CPU0 DSPR at locations D000 2000$_H$ to D000 203F$_H$ by the Startup Software (SSW) after cold power-on.*

For TC26x and TC27x B-step, see for example section "Entering Standby Mode .." in the PMC chapter within chapter "System Control Units" of the corresponding User's Manual.

For all other TC2xx devices, see for example section "Preparation before to enter Stand-by mode" in the BootROM chapter of the corresponding User's Manual.

Only CPU0 DSPR Standby RAM is affected, EMEM in ADAS or ED devices is not affected.

Workarounds

1. Calculate CRC over critical Standby RAM data and store result before Standby mode entry. On a consequent wake-up, CRC of the critical data shall be carried out. The CRC is a general recommended measure for improved robustness of Standby RAM handling.

Or / and

2. Keep a copy of the critical data at a second location in Standby RAM. On wake-up, compare data from both locations to ascertain their integrity

2.11 [CPU_TC.123] Data Corruption possible when CPU GPR accesses made via SRI slave with CPU running

Description

Data corruption may occur when another master accesses a TriCore CPU's General Purpose Registers (GPRs) via its SRI slave port whilst the CPU is running (i.e. not Idle, Halted or Suspended). The TriCore GPRs are A0-A15 and D0-D15. The scenarios in which data corruption may occur are different for the TC1.6P and TC1.6E processors as described below.

TC1.6P - Data corruption may occur when one of the CPU GPRs is **written** via the SRI slave port whilst the CPU is running. Both AGPR and DGPR writes may be affected.

TC1.6E - Data corruption may occur when one of the CPU Address GPRs (A0-A15) is **read** via the SRI slave port whilst the CPU is running. However, data corruption can only occur when the slave AGPR read interacts with the execution of a specific form of store instruction. The store instructions affected by this issue are ST.A and ST.DA, where the address register to be stored is modified by the addressing mode of the store instruction. For example:

```
ST.A [+A0], A0
```

However, such store instructions are architecturally undefined and should not be being used. In the case of this errata all data written to memory by this store instruction may be corrupted.

Workaround

Writes to a CPU's GPRs via its SRI slave port must never be performed whilst the CPU is running. If it is necessary for an external master to write to a CPU's GPR then that CPU must first be placed in Idle, Halt or Suspend mode.

If it is necessary for an external master to read a TC1.6E CPU's AGPR whilst that CPU is running then store instructions of the form above (where any source register is modified by the addressing mode of the store instruction) are not allowed.

2.12 [CPU_TC.127] Pending Interrupt Priority Number PIPN in Register ICR

Description

In the TriCore™ Architecture Manual, it is described for the Pending Interrupt Priority Number ICR.PIPN that it is reset to 0x0 in case there is no request pending.

However, the AURIX™ hardware implementation behaves differently, as the value of PIPN is not changed after the interrupt is serviced in case there is no further request pending.

2.13 [CPU_TC.131] Performance issue when MADD or MSUB instructions use E0 or D0 register as accumulator

Description

***Note**: Consider the following notes for TC26x, TC27x, TC29x:*

- ***TC26x**: In TC26x devices, this problem only affects the TC1.6P processor (CPU1). The TC1.6E processor (CPU0) is not affected by this problem.*
- ***TC27x**: In TC27x devices, this problem only affects the TC1.6P processors (CPU1 and CPU2). The TC1.6E processor (CPU0) is not affected by this problem.*
- ***TC29x**: In TC29x devices, this problem affects the TC1.6P processors (CPU0, CPU1, and CPU2).*

Under certain conditions, when a Multiply (MULx.y) or Multiply-Accumulate (MAC) instruction is followed by a MAC instruction which uses the result of the first instruction as its accumulator input, a performance reduction may occur if the accumulator uses the E0 or D0 register. The accumulator input is that to which the multiplication result is added to (in the case of MADDx.y), or subtracted from (in the case MSUBx.y), in a MAC instruction.

All MAC instructions MADDx.y, MSUBx.y are affected except those that operate on Floating-Point operands (MADD.F, MSUB.F).

The problem occurs where there is a single cycle bubble, or an instruction not writing a result, between these dependent instructions in the Integer Pipeline (IP). When this problem occurs the dependent MAC instruction will take 1 additional cycle to complete execution. If this sequence is in a loop, the additional cycle will be added to every iteration of the loop.

Example

```
maddm.h e0, e0, d3, d5ul ; MUL/MAC writing E0 as result
ld.d e8, [a5] ; Load instruction causing IP bubble
maddm.h e0, e0, d6, d8ul ; MAC using E0 as accumulator.
                    ; Should be delayed by 1 cycle due to
                    ; dependency to result of previous LD.D,
                    ; but is delayed for 2 cycles
```

***Note**: If there are 2 or more IP instructions, or a single IP instruction writing a result, between the MAC and the previous MUL/MAC, then this issue does not occur.*

Workaround

Since the issue only affects D0 or E0, it is recommended that to ensure the best performance of an affected sequence as the above example, D0 or E0 is replaced with another register (D1-D15 or E2-E14).

2.14 [CPU_TC.132] Unexpected PSW values used upon Fast Interrupt entry

Description

Under certain conditions, unexpected PSW values may be used during the first instructions of an interrupt handler, if the interrupt has been taken as a fast interrupt. For a description of fast interrupts, see the “CPU Implementation-Specific Features” section of the relevant User’s Manual.

When the problem occurs, the first instructions of the interrupt handler may be executed using the PSW state from the end of the previous exception handler, rather than that which is being loaded by the fast interrupt entry sequence. The TC1.6E, TC1.6P and TC1.6.2P processors are all affected by this problem as follows:

- TC1.6E (in TC21x..TC27x):
  - Only the first instruction of the ISR is affected
- TC1.6P (in TC26x..TC29x), TC1.6.2P (in TC3xx):
  - Up to 4 instructions at the start of the ISR may be affected.
  - However, if the following pre-condition is not met, then there is no issue for these processor variants:

    A11 must point to the first instruction of the fast interrupt handler at the end of the previous exception handler, i.e. the return value from the previous exception must be pointing to the very first instruction of the new interrupt handler. Note that this case should not occur normally, unless software updates the A11 register to a value corresponding to the start of an interrupt handler

Workaround 1

When the PSW fields PSW.PRS, PSW. S, PSW.IO or PSW.GW need to be changed in an exception handler, the change should be wrapped in a function call.

```
_exception_handler:
  CALL _common_handler
  RFE

_common_handler:
  MOV.U d0, #0x0380
  MTCR #(PSW), d0 // PSW.IO updated to User-0 mode
  ...
  RET
```

Note that this workaround assumes SYSCON.TS == SYSCON.IS such that the workaround functions correctly for both traps and interrupts. If this is not the case it is possible for bus accesses to use an incorrect master Tag ID, potentially resulting in an access to be incorrectly allowed, or an unexpected alarm to be generated. In this case it should be ensured that for all interrupt handlers the potentially affected instructions do not produce bus accesses.

Workaround 2

Do not use any instructions dependent upon PSW settings (for example BISR or ENABLE, dependent on PSW.IO) as the first instruction of an ISR in TC1.6E, or as one of the first 4 instructions in an ISR for TC1.6P or TC1.6.2P.

***Note**: The workarounds need to be applied in TC1.6P and TC1.6.2P only in case software modifies the A11 register in an exception handler, as described in the pre-conditions above.*

2.15 [DAP_TC.002] DAP client_blockread has Performance issue in Specific Operation Modes

Description

For achieving the highest block read bandwidth, the following word is already read chip internally while a word is transmitted on DAP. This read ahead is under certain conditions disabled in the case that the “All parcels with CRC6” bit is set in the telegram. In this case the distance between the reply parcels becomes significantly longer, due to the missing read ahead. This effect occurs also in Wide Mode.

The data values in the parcels are always correct, it is just a performance issue.

Workaround

Don’t use the “All parcels with CRC6” option, use “Read CRCup” instead.

This mode is anyway better in terms of performance for larger blocks (no CRC6 overhead for each parcel) and data protection (32 bit CRC). For a few words, the impact of this performance issue might be tolerable. For the first word a read ahead is not possible anyway.

2.16 [DAP_TC.003] DAP CRC32 definition and algorithm

Description

The DAP CRC32 algorithm is different from the IEEE 802.3 Ethernet CRC.

Workaround

Use the following (VHDL) algorithm for each incoming data bit. The CRC32 value is initialized with all ones. In Wide Mode the function is called for both DAP data bits in each DAP0 clock cycle.

```
subtype  crc32_t is std_ulogic_vector(31 downto 0);
function calc_crc32_f(crc_now : crc32_t;
                      bit_new : std_ulogic)
                     return crc32_t is
  variable crc : crc32_t;
begin
  crc(31 downto 1) := crc_now(30 downto 0);
  crc(0)  := bit_new xor crc_now(31);
  crc(1)  := bit_new xor crc_now(0)  xor crc_now(31);
  crc(2)  := bit_new xor crc_now(1)  xor crc_now(31);
  crc(4)  := bit_new xor crc_now(3)  xor crc_now(31);
  crc(5)  := bit_new xor crc_now(4)  xor crc_now(31);
  crc(7)  := bit_new xor crc_now(6)  xor crc_now(31);
  crc(8)  := bit_new xor crc_now(7)  xor crc_now(31);
  crc(10) := bit_new xor crc_now(9)  xor crc_now(31);
  crc(11) := bit_new xor crc_now(10) xor crc_now(31);
  crc(12) := bit_new xor crc_now(11) xor crc_now(31);
  crc(16) := bit_new xor crc_now(15) xor crc_now(31);
  crc(22) := bit_new xor crc_now(21) xor crc_now(31);
  crc(23) := bit_new xor crc_now(22) xor crc_now(31);
  crc(26) := bit_new xor crc_now(25) xor crc_now(31);
  return crc;
end calc_crc32_f;
```

2.17 [DAP_TC.004] DAP client_blockwrite telegram with CRC6 and CRC32 protection options

Description

***Note**: This problem is only relevant for tool development, not for application development.*

When issuing a DAP client_blockwrite telegram from the tool to the device several CRC protection options are available, namely CRC6 and CRC32.

Expected Behavior

- For CRC6 the expected behavior is:
  - (1) A CRC6 will be appended to the reply of only the last parcel of the telegram
  - (2) An optional CRC6 can be appended to the devices “single startbit response” by setting DAPISC.RC6
- For CRC32 the expected behavior is:
  - (3) The telegram can optionally send the CRCdown value as the last parcel

Actual Implementation

- For the actual implementation the CRC6 slightly differs as follows:
  - (1) The CRC6 of the last parcel will be erroneous if DAPISC.RC6 is set or if the CRCdown option is enabled
  - (2) If DAPISC.RC6 = 1_B, an unintentional CRC6 will be appended to the device response of parcels which are not the last parcel
- For the actual implementation the CRC32 option slightly differs as follows:
  - (3) If also the CRC6option is set, the CRCdown option will not return the correct CRCdown value

Workaround for (3)

Workaround for (3) is not to use the CRCdown feature of the client_blockwrite telegram, but to use the dedicated get_CRCdown telegram.

2.18 [DAP_TC.005] DAP client_read: dirty bit feature of Cerberus' Triggered Transfer Mode

Description

***Note**: This problem is only relevant for tool development, not for application development.*

The DAP telegram client_read reads a certain number of bits from an IOclient (for example Cerberus). The parameter k can be selected to be zero, which is supposed to activate reading of 32 bits plus dirty bit.

However, in the current implementation, the dirty bit feature does not work correctly.

It is recommended not to use this dirty bit feature, meaning the number k should not evaluate to "0".

2.19 [DAP_TC.006] CRC6 error in telegram following a get_CRCdown telegram prevents reset of CRC32 calculator

Description

***Note**: This problem is only relevant for tool development, not for application development.*

If a CRC6 error occurs in the telegram following a get_CRCdown telegram the AURIX™ internal CRC32 calculator does not get reset, as is the expected behavior for get_CRCdown.

This effect can lead to unexpected CRC32 values for the next get_CRCdown telegram. This corresponds to the perception of the tool that there has been a CRC32 error, even if the data was transmitted correctly.

Workaround 1

Accept extra traffic for a required retransmission : In this case the tool could see a CRC32 error which is not based on a wrong transmission, but on the missing reset of the AURIX™ internal CRC32 calculator. This would trigger the retransmission of correctly sent data.

Workaround 2

Check for no-reply after a get_CRCdown telegram : If the tool does not receive an answer for the telegram following a get_CRCdown, it needs to re-send the get_CRCdown telegram and ignore the data.

2.20 [DAP_TC.009] CRC6 error in client_blockwrite telegram

Description

***Note**: This problem is only relevant for tool development, not for application development.*

If a CRC6 error happens in a client_blockwrite telegram, the DAP module will not execute the write and the tool will run into timeout according to the DAP protocol.
But in this case a following client_blockwrite (with start address) will be ignored by the DAP module.

Workaround

If the tool is running into a timeout after a client_blockwrite telegram it should transmit a dummy client_blockread telegram (for example len=0, arbitrary address) which will clean up the DAP client_blockwrite function.

2.21 [DMA_TC.015] DMA Double Buffering: No Timestamp Support

Description

When a DMA channel is configured for DMA Double Buffering, and flow control (or appendage of time stamp) is selected, i.e. DMA_ADICRz.STAMP $= 1_B$, the Move Engine may lock up.

Workaround

When a DMA channel is configured for DMA Double Buffering then flow control (or appendage of time stamp) should not be selected, i.e. bit DMA_ADICRz.STAMP must be = 0_B.

2.22 [DMA_TC.016] Byte and Half-word Write Accesses to specific Registers not supported

Description

***Note**: This erratum might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.*

Byte and half-word write accesses via the SPB (System Peripheral Bus) to the Regfile and Request Control logic are not supported.
This affects the following registers:

- DMA_OTSS (OCDS Trigger Set Select)
- DMA_ERRINTR (Error Interrupt)
- DMA_PRR0 (Pattern Read Register 0)
- DMA_PRR1 (Pattern Read Register 1)
- DMA_MODEy (Hardware Resource Mode)
- DMA_HRRz (Hardware Resource Partition)
- DMA_SUSENRz (Channel Suspend Enable)
- DMA_TSRz (Transaction State)

Workaround

Make sure only 32-bit word data is written to the registers listed above by selecting the appropriate data types.

2.23 [DMA_TC.017] Pattern Detection Double Interrupt Trigger when INTCT = 11_B

Description

A DMA channel z is configured for pattern detection by programming the DMA_CHCFGRz.PATSEL to reference a data value set in one of the pattern read registers DMA_PRR0 or DMA_PRR1. If DMA_ADICRz.INTCT = 11_B then DMA channel z will generate a channel interrupt trigger and set CHSRz.ICH each time TCOUNT is decremented.

If a pattern match is detected then a channel interrupt trigger will be correctly generated but a second channel interrupt trigger will be generated when TCOUNT decrements. The second interrupt trigger is a bug and should not occur.

If the DMA channel z interrupt trigger is directed via the Interrupt Router to generate a DMA hardware request to another DMA channel then the second interrupt trigger may result in a Transaction Request Lost event.

Workaround

Workaround is to ignore the generation of the Transaction Request Lost event:

- Either disable the generation of error interrupt service requests by setting ADICRz.ETRL = 0_B
- Or if the error interrupt service request is enabled, check all error status bits. If only the TRL bit for DMA channel x (pattern detection channel) is set then clear TRL and continue normal DMA operation

2.24 [DMA_TC.018] FPI timeout can cause pipelined register reads to break

Description

Due to a problem in the FPI slave interface (SIF) to the System Peripheral Bus (SPB) in the DMA module, a register access which is pipelined behind an access which is timed-out may terminate early and return the wrong data to the bus.

The scenario for this problem to occur is as follows:

1. An FPI read transaction is performed which takes a long time in the data phase. Pipelined behind this is a register access to DMA or Cerberus
2. The first transaction is timed out, and in the same cycle the register access is taken by the SIF

Workaround

Timeout indicates a severe problem, meaning that something took unexpectedly long. In the event of an FPI timeout on the SPB, an error routine should be run to determine the error, and perform a system reset.

2.25 [DMA_TC.019] CBS Accesses with Large SPB:SRI Clock Ratios Configured

Description

When operating in debug mode and a large SPB:SRI clock ratio is configured then Cerberus accesses to the SRI address space may be unreliable and result in the Cerberus hanging.

Workaround

Limit the SPB:SRI clock ratio to 1:1, 2:1, 3:1 or 4:1, and do not perform Cerberus accesses to the SRI address space while switching the SPB:SRI clock ratio.

2.26 [DMA_TC.020] DMA Conditional Linked List: Circular Buffer Enabled

Description

When a DMA channel is configured for Conditional Linked List (i.e. ADICRz.SHCT = 1111_B) and circular buffer operation (i.e. ADICRz.SCBE = 1_B OR ADICRx.DCBE = 1_B) then if the source and destination addresses are not set to wrap boundaries then the behavior will not be as intended, for example the wrap bits CHCSRz.WRPS and CHCESRz.WRPD may be spuriously set.

Workaround

If a DMA channel is configured for Conditional Linked List and circular buffers are enabled then the user must set the source and destination addresses to wrap boundaries.

2.27 [DMA_TC.021] Combined Software/Hardware Controlled Mode Spurious Errors

Description

A DMA channel is configured for combined software/hardware controlled mode. If the Move Engine is servicing a DMA channel software request and a DMA channel hardware trigger is received then a Transaction Request Lost event is set. When the Move Engine completes the current DMA access the TSRz.CH bit is not cleared. The DMA channel will continue to request channel arbitration as the CH bit is set. If the DMA channel wins arbitration then the Move Engine will continue to service the DMA channel.

In summary, 2 DMA requests (software and hardware) have resulted in 2 X DMA transfers and 1 X Transaction Request Lost (i.e. 3 X DMA actions for 2 X DMA triggers) i.e. a spurious error is generated.

Workaround

If a DMA channel is configured for combined software/hardware mode then increased attention must be paid to de-conflict the triggering of DMA channels from the servicing of DMA requests. The workaround will remove the source of spurious errors.

2.28 [DMA_TC.022] Conditional Linked List: Bus Error

Description

When a DMA channel is configured for Conditional Linked List (i.e. ADICRz.SHCT = 1111_B) then if a bus error is reported then:

- If there is a pattern match then the number of DMA moves subsequently executed may not be as intended
- If there is an error during the loading of a new Transaction Control Set then the DMA channel does not clear the TSRz.CH bit and begins the next DMA transaction with an erroneous Transaction Control Set

Workaround

If a DMA channel is configured for Conditional Linked List then the user must enable the error interrupt service request. On receiving notification of an error interrupt service request the user must read the Move Engine Error Status Registers to confirm that no bus errors were reported:

- If DMA_ERRSRx.DER = 0_B and DMA_ERRSRx.SER = 0_B then no bus errors reported
- If a bus error is reported then check the last error channel DMA_ERRSRx.LEC
- If DMA_ERRSRx.DLLER = 1_B then there was an error during the loading of a new Transaction Control Set

2.29 [DMA_TC.024] Suspend Request coincident with Channel Activation

Description

If DMA channel z is suspend enabled (SUSENRz.SUSEN = 1_B) and the DMA receives a suspend request then if during the same clock cycle the DMA channel becomes active in a Move Engine, the following effects will occur:

- SUSACRz.SUSAC is set for a cycle and then cleared
- A DMA transfer is performed for DMA channel z
- SUSACRz.SUSAC is set again on completion of the DMA transfer and the DMA channel is finally suspended

Workaround

When polling SUSACRz.SUSAC in software, additionally check whether DMA channel z is active in a Move Engine x by reading bit-field MExSR.CH.

2.30 [DMA_TC.025] Conditional Linked List: new non-CLL mode TCS load can corrupt SDCRC RAM write

Description

When a Conditional Linked List (CLL) transaction is running and gets a CLL pattern match, this will stop the running transaction and cause a transaction control set (TCS) load.

In case the new TCS load is set up so that it is not in CLL mode, then the SDCRC value of the new TCS may get corrupted.

Workaround

Avoid selection of non-CLL mode in the TCS loaded after a CLL pattern match.

2.31 [DMA_TC.026] Linked List: Failed TCS load can trigger wrap interrupt

Description

When a Transaction Control Set (TCS) linked list load is performed, and an error is received during the load process, this terminates the load. A DMA linked list error is indicated by the error status flag ERRSRx.DLLER.

If the DADR address left in the register matches the destination wrap boundary, this results in the issuing of a destination wrap interrupt in case the destination wrap interrupt enable is set. Hence a failed TCS load has triggered an interrupt.

***Note**: This only happens for destination interrupts. Logic is already in place to exclude source interrupts.*

Workaround

An error interrupt for the DMA linked list error is triggered by the status flag ERRSRx.DLLER if enabled by EERx.ELER. Therefore the destination wrap buffer interrupt can be ignored in this case.

2.32 [DMA_TC.028] Transaction Request Lost (TRL) Interrupt Service Request Behaviour

Description

The DMA channel TRL error interrupt service request is a DMA safety measure signalling a lost DMA request to the system. For each DMA channel TRL event, the DMA may trigger one or more error interrupt service requests.

The application software should include a DMA error handler to resolve all DMA errors including TRL.

Workaround

None.

2.33 [DMA_TC.031] CHCSR.ICH can be incorrectly set after pattern match

Description

If a pattern match is seen during a transaction, the transaction is halted for the current active channel. The move engine zeroes its internal move counter, and holds the transfer count status MEx_CHCSR_TCOUNT at the last value. However, the MEx_CHCSR.ICH bit will still be set indicating a TCOUNT decrement.

Workaround

As there is a pattern match, a DMA channel pattern match interrupt service request will be generated. The pattern match interrupt routine can service the interrupt and clear the status bits including ICH.

2.34 [DMA_TC.034] DMA Timestamp and Destination Circular Buffer

Description

The DMA must not write a DMA timestamp at an address that overwrites DMA move data stored at a DMA destination address. If the DMA channel is configured for linear DMA destination address generation (DMA channel ADICRz.DCBE = 0_B), the DMA appends the DMA timestamp to the end of a DMA transaction (i.e. beyond the last DMA write move data).

If the DMA channel is configured for destination circular buffer (DMA channel ADICRz.DCBE = 1_B), there are three use cases:

- **Use Case 1:** the size of the DMA transaction **equals** the size of the destination circular buffer. If the DMA writes the last DMA write move data at the last address in the destination circular buffer, the DMA correctly writes the DMA timestamp beyond the destination circular buffer
- **Use Case 2:** the size of the DMA transaction is **less than** the size of the destination circular buffer. If the DMA writes the last DMA write move data NOT at the last address in the destination circular buffer, the DMA writes the DMA timestamp inside the destination circular buffer. Erroneously, the DMA may store the DMA timestamp at an address that overwrites DMA write move data
- **Use Case 3:** the size of the DMA transaction is **greater than** the size of the destination circular buffer. After the DMA destination address has wrapped, the DMA will overwrite DMA write move data with fresh DMA write move data

***Note**: DMA Timestamp works as specified when using only source circular buffer.*

Workaround 1

If a DMA channel is configured

- for destination circular buffering (ADICRz.DCBE = 1_B) AND
- the appendage of a DMA timestamp (ADICRz.STAMP =1_B), AND
- the size of the DMA transaction (defined by CFCFGRz.TREL) **equals** the size of the destination circular buffer (defined by ADICRz.CBLD)

the DMA shall append the DMA timestamp beyond the destination circular buffer if

- For increment of DMA destination address (ADICRz.INCD = 1_B), the initial DMA destination address is at the bottom of the destination circular buffer
- For decrement of DMA destination address (ADICRz.INCD = 0_B), the initial DMA destination address is at the top of the destination circular buffer

Workaround 2

If DMA channel z is configured

- for destination circular buffering (ADICRz.DCBE = 1_B) AND
- increment of DMA destination address (ADICRz.INCD = 1_B) AND
- the appendage of a DMA timestamp (ADICRz.STAMP = 1_B) AND
- the size of the DMA transaction (defined by CFCFGRz.TREL) is **less than** the size of the destination circular buffer (defined by ADICRz.CBLD)

the DMA shall append the DMA timestamp to the DMA write move data if the following DMA channel parameters are configured:

- ADICRz.DMF = 001_B (address offset is 2 x CHCFGRz.CHDW) AND
- CHCFGRz.CHDW = 010_B (32-bit data width for moves, SDTW)

In all other DMA destination circular buffer use cases, the DMA channel shall be configured to disable the appendage of DMA timestamp (ADICRz.STAMP = 0_B).

2.35 [DMA_TC.035] Last DMA Transaction in a Linked List triggers a DMA Daisy Chain

Description

DMA Channels can be daisy chained by setting the bit CHCFGRz.PRSEL = 1_B. When a higher priority DMA channel z completes a DMA transaction then it will initiate a DMA transaction on the next lower priority DMA channel z-1 by setting the access pending bit TSRz-1.CH.

However, if the current transaction was the last one in a linked list, and PRSEL is set to daisy chain, TSRz-1.CH of the next lower channel z-1 is set just after the TCS (transaction control set) load, that is, before the last transaction of the linked list has even started. Therefore the last TCS is not executed by the Linked List.

Workaround

Do not use Daisy Chain with Linked Lists (i.e. if ADICRz.SHCT[3:2] = 11_B then CHCFGRz.PRSEL = 0_B).

If the use case needs to trigger a further TCS in the next lower DMA channel then the trigger should be routed via the Interrupt Router.

2.36 [DMA_TC.036] Linked List: SADR/DADR can be overwritten when loading a non-LL TCS

Description

If a Linked List (LL) loads in a non-LL Transaction Control Set (TCS) which has a shadow mode selected (ADICRz.SHCT = 0001_B or 0010_B or 0100_B or 0101_B), during the write-back it can overwrite the contents of SADR/DADR in the newly loaded TCS before the DMA transaction has been run.

Workaround

Do not use shadow address modes with DMA Conditional Linked List.

***Note**: The Application Note AP32245 "DMA Linked List" will highlight that shadow address modes are not required.*

2.37 [DMA_TC.037] Conditional Linked List: Bit TSR.CH not cleared for a CLL transaction upon pattern match

Description

When a Conditional Linked List (CLL) pattern match is found, the transaction ends. TSR.CH should be cleared, and set later during write-back of the Transaction Control Set (TCS) if the newly loaded TCS is auto-starting (i.e. CHCSRz.SCH = 1_B).

Due to an internal problem TSR.CH is not cleared in this case.

Workaround

There is no workaround.

The assessment is that a DMA CLL transaction that does not get a match will transition to the next DMA transaction. The CH bit will be cleared.

2.38 [DMA_TC.038] Linked List: SIT interrupt when SIT bit set in newly loaded TCS

Description

The Set Interrupt Trigger (SIT) bit is a means of generating a DMA channel interrupt service request via software. It is a debug feature that allows to trigger the Interrupt Router, without configuring the DMA channel and executing a DMA transaction.

When a new Transaction Control Set (TCS) is loaded in linked list mode, and the SIT bit in the new TCS being loaded is set in the value written to register CHCSRz, a channel interrupt trigger will be activated.

Therefore, the SIT bit should always be set to 0_B when using linked lists.

***Note**: The latest versions of the documentation are/will be updated to reflect this.*

2.39 [DMA_TC.039] Read Data CRC

Description

The Read Data CRC (RDCRC) calculates an IEEE 802.3 ethernet CRC32 checksum as DMA moves read data through the DMA. The DMA implementation of the algorithm does not zero extend the read data for SDTB (8-bit) and SDTH (16-bit) accesses resulting in the calculation of a wrong checksum value.

The RDCRC must only be used with STDW (32-bit), SDTD (64-bit), BTR2 (128-bit) and BTR4 (256-bit) access sizes. It must be noted that SDTD, BTR2 and BTR4 are only supported for SRI-source to SRI-destination transactions.

2.40 [DMA_TC.040] DMA Linked Lists: Intermittent Clearing of Hardware Transaction Request Enable with mixed mode Transaction Control Sets

Description

When a DMA channel is configured for linked list operation, if a Transaction Control Set (TCS) is configured for Continuous Mode (DMA_CHCFGRz.CHMODE = 1_B) and the next TCS is configured for Single Mode (DMA_CHCFGRz.CHMODE = 0_B) then DMA_TSRz.HTRE may be intermittently cleared disabling the servicing of DMA hardware requests.

Workaround

If a DMA channel is configured for linked list operation then all application DMA transactions must be configured for Continuous Mode (DMA_CHCFGRz.CHMODE = 1_B). If there is a need for the application to clear the Hardware Transaction Request Enable (DMA_TSRz.HTRE = 0_B) then two additional dummy DMA transactions should be serviced by the DMA in the linked list:

- Dummy Transaction 1:

  The TCS is configured as a linked list TCS (DMA_ADICRz.SHCT = 0xC, 0xD or 0xE) in Single Mode (DMA_CHCFGRz.CHMODE = 0) and auto start (DMA_CHCSRz.SCH = 1_B). The TCS should configure a single DMA move to read a word from memory in order to write DMA_TSRz.DCH = 1_B and disable subsequent DMA hardware requests
- Dummy Transaction 2:

  The TCS is configured for normal shadow control mode (DMA_ADICRz.SHCT = 0000_B) and Single Mode. A dummy DMA move is performed

2.41 [DMA_TC.041] DMA Circular Buffer Wrap Interrupt

Description

If a DMA channel is configured for source circular buffer operation (ADICRz.SCBE = 1_B), the DMA shall correctly calculate the DMA source addresses. When the DMA source address wraps, the DMA is unreliable in updating the wrap source buffer status (CHCSRz.WRPS). If the wrap source buffer interrupt is enabled (ADICRz.WRPSE = 1_B), the DMA is unreliable in triggering a source wrap buffer interrupt.

If a DMA channel is configured for destination circular buffer operation (ADICRz.DCBE = 1_B), the DMA shall correctly calculate the DMA destination addresses. When the DMA destination address wraps, the DMA is unreliable in updating the wrap destination buffer status (CHCSRz.WRPD). If the wrap destination buffer interrupt is enabled (ADICRz.WRPDE = 1_B), the DMA is unreliable in triggering a destination wrap buffer interrupt.

Workaround

The source wrap buffer interrupt shall be disabled (ADICRz.WRPSE =0_B).

The destination wrap buffer interrupt shall be disabled (ADICRz.WRPDE =0_B).

If a DMA channel is configured for circular buffer operation (ADICRz.SCBE = 1_B or ADICRz.DCBE = 1_B), the DMA channel shall be configured as follows:

- The size of the DMA transaction shall equal the size of the circular buffer
- If a source circular buffer is configured (ADICRz.SCBE = 1_B), the initial DMA source address shall be the start address of the source circular buffer
- If a destination circular buffer is configured (ADICRz.DCBE = 1_B), the initial DMA destination address shall be the start address of the destination circular buffer
- The DMA channel interrupt control shall be configured to trigger an interrupt on completion of the DMA transaction (DMA_ADICRz.INTCT = 10_B and DMA_ADICRz.IRDV = 0000_B)

If a DMA channel is configured for both source circular buffer operation (ADICRz.SCBE = 1_B) AND destination circular buffer operation (ADICRz.DCBE = 1_B), the size of the source circular buffer shall equal the size of the destination circular buffer.

2.42 [DMA_TC.042] DMA Interrupt from Channel reported before Completion of DMA Transaction

Description

The Interrupt from Channel (ICH) status bit should be set on completion of a DMA transaction. If the DMA channel is configured to append a DMA Timestamp then validation have discovered that the ICH bit is set before the DMA timestamp has been written.

Workaround 1

On receipt of a DMA channel interrupt service request software shall poll the Move Engine (ME) Status Register(s) to confirm the DMA channel is no longer active.

1. Check active DMA channel in ME SR
2. Check Write Status in ME SR

If these fields in both ME are no longer the DMA channel that triggered the DMA channel interrupt service request then the DMA transaction has completed.

Workaround 2

To avoid polling the Move Engine status, the user may use a DMA linked list to execute the following DMA transactions:

- DMA transaction 1:
  - move operation (DMA timestamp shall not be selected)
- DMA transaction 2:
  - single 32-bit DMA move to copy DMA timestamp from DMA TIME register to next 32-bit aligned destination after DMA transaction 1

2.43 [DMA_TC.043] DMA Write Move Data Corruption for non 32-byte Aligned Cacheable Source Address

Description

If the DMA channel TCS selects a 256-bit channel data width and a non 32-byte aligned source address then the beat order of the DMA write move will be different for DMA read moves to cacheable (segments 8 and 9) and non-cacheable (segments A and B) source addresses. The effect is data corruption for accesses to cacheable addresses.

Workarounds

1. Use 32-byte aligned source addresses for DMA read move to cacheable addresses (segments 8 and 9)
2. Use non-cacheable source addresses (segments A and B)

2.44 [DMA_TC.044] Clock Switch after SPB Error Reported results in Spurious SRI Error

Description

If an SPB error is reported, and then immediately the SRI:SPB clock ratio is changed, then if the next DMA read move is to an SRI source address a spurious error may be reported.

Workaround

1. The system shall not change the SRI:SPB clock ratio while the DMA is active
2. The DMA error handler should monitor the reporting of SPB and SRI errors after a clock switch

2.45 [DMA_TC.045] DMA Reconfigures DMA Channels Lockup

Description

If two or more DMA channels are used to re-configure other DMA channels (i.e. perform a DMA write move to DMA address space) the DMA may lock up if the re-configuration DMA channels are assigned to different DMA hardware resource partitions.

The effect of the DMA lock up is to lock up other SPB master interfaces which attempt a write access to DMA address space.

Workaround

All DMA channels used to re-configure other DMA channels shall be assigned to the same hardware resource partition in their corresponding DMA Channel Hardware Resource Registers HRRz.

2.46 [DMA_TC.046] Shadow Operation Read Only Mode

Description

If a DMA channel is configured for Source Address Buffering Read Only (ADICR.SHCT = 0001_B) or Destination Address Buffering Read Only (ADICR.SHCT = 0010_B), the DMA is unreliable when performing a shadow address update. In these modes, the SADR/DADR registers may get directly updated (instead of SHADR) in the middle of a transaction, potentially resulting in a DMA data transfer corruption.

Workaround

The DMA channel configuration for Read Only Modes (SHCT = 0001_B or SHCT = 0010_B) must not be used.

Instead, to update the SADR/DADR in the middle of a transaction, use the corresponding Direct Write Mode for Source Address Buffering (ADICR.SHCT = 0101_B) or Destination Address Buffering (ADICR.SHCT = 0110_B), and write the new address to the SHADR register.

2.47 [DMA_TC.048] DMARAM Internal ECC Error

Description

If the DMA detects an integrity error when loading a TCS from DMARAM,

- The DMA shall
  - set DMA_MEMCON.INTERR
  - trigger an alarm to the SMU
  - record the DMA channel number in DMA_ERRSRx.LEC
  - set the error status bit DMA_ERRSRx.RAMER
- The DMA shall **not** execute the DMA transaction

Erroneously,

- The DMA will not record the DMA channel number in DMA_ERRSRx
- The DMA will execute the DMA transaction

Workaround

None.

2.48 [DMA_TC.049] Bus Error Reported During LL TCS Load

Description

If a DMA channel is configured for Linked List (LL) operation AND a bus error is reported during the load of a new Transaction Control Set (TCS), the DMA shall set the DMA_ERRSRx.DLLER status bit (Move Engine x DMA Linked List Error).

Erroneously, the DMA additionally sets the DMA_ERRSRx.SER status bit (Move Engine x Source Error).

Workaround

None.

2.49 [DMA_TC.050] Clearing CHCSR.FROZEN during Double Buffering

Description

If a DMA channel is configured for one of the following Double Buffering operations:

- 1001_B Double Source Buffering Automatic Hardware and Software Switch
- 1011_B Double Destination Buffering Automatic Hardware and Software Switch

AND the active buffer fills/empties before software has cleared the DMA channel CHCSRz.FROZEN bit, the DMA shall overflow/underflow the active buffer.

Erroneously, the DMA will not trigger a Transaction Request Lost (TRL) error.

Workaround

Software shall clear DMA channel CHCSRz.FROZEN before the active buffer overflows/underflows.

2.50 [DMA_TC.051] DMARAM Alarm

Description

A DMARAM alarm is reported for the following error conditions:

- Internal ECC error:
  - if the DMARAM signals an ECC error, the DMA shall set MEMCON.INTERR and trigger a DMARAM alarm
- SPB read access:
  - if the DMARAM signals an ECC error, the DMA shall set MEMCON.DATAERR and trigger a DMARAM alarm
- SPB write access:
  - if the DMARAM signals an ECC error during the read phase of an internal Read Modify Write, the DMA shall set MEMCON.RMWERR and trigger a DMARAM alarm

Erroneously, the DMA additionally sets the following bits:

- SPB read access:
  - if the DMARAM signals an ECC error, the DMA sets MEMCON.INTERR
- SPB write access:
  - if the DMARAM signals an ECC error, the DMA sets MEMCON.INTERR
- ME loads Transaction Control Set:
  - if the DMARAM signals an ECC error, the DMA sets MEMCON.DATAERR

Workaround

None.

2.51 [DMA_TC.052] SER and DER During Linked List Operations

Description

Software may configure a DMA channel for one of the DMA linked list operations:

- DMA linked list
  - (DMA channel DMA_ADICRz.SHCT = 1100_B)
- Accumulated linked list
  - (DMA channel DMA_ADICRz.SHCT = 1101_B)
- Safe linked list
  - (DMA channel DMA_ADICRz.SHCT = 1110_B)
- Conditional linked list
  - (DMA channel DMA_ADICRz.SHCT = 1111_B)

If the DMA is servicing a DMA request for a DMA channel configured for one of the linked list operations and the DMA indicates a Source Error (SER) (i.e. DMA_ERRSRx.SER = 1_B) or a Destination Error (DER) (i.e. DMA_ERRSRx.DER = 1_B), the DMA completes the current DMA transaction. If the DMA channel is configured for conditional linked list, the DMA disables pattern matching for each DMA read move reporting a SER. When the DMA completes the current DMA transaction, the DMA stops servicing the linked list operation and the DMA will not load the next transaction control set to allow debug of the current DMA transaction.

Erroneously, upon a SER or DER, the DMA does not reliably stop the linked list operation (when it should) on completion of the current DMA transaction.

If the Move Engine is configured to enable DMA error interrupt service request for SER (DMA_EERx.ESER =1_B) and for DER (DMA_EERx.EDER = 1_B), the DMA triggers a DMA error interrupt service request.

The application software should include a DMA error handler to resolve all DMA errors including SER and DER.

Workaround

None.

2.52 [DMA_TC.053] TS16_ERR Type of Error Reporting Unreliable

Description

During debugging, the error trigger set (TS16_ERR) may be used to identify the type of DMA error and the number of the DMA channel. After TS16_ERR reports an error the error type bits (ME0SE, ME0DE, ME1SE and ME1DE) are not cleared. If TS16_ERR reports a subsequent error, the type of error reporting is unreliable.

Workaround

After TS16_ERR reports an error, the error type bits must be cleared.

2.53 [DMA_TC.054] DMA Channel Halt Acknowledge Unreliable

Description

Software may halt a DMA channel by writing to the halt request bit (TSRz.HLTREQ = 1_B). When a DMA channel enters the halt state, the DMA reports DMA channel halt acknowledge (TSRz.HLTACK = 1_B).

The reporting of DMA channel halt acknowledge is unreliable when software sets the TSRz.HLTREQ bit just as channel z is about to be scheduled to a move engine. In this case, the DMA may report a DMA channel is halted when the DMA channel is active in a move engine.

Workaround

If the DMA reports a DMA channel is halted, the software should check the DMA channel is not active in a move engine by monitoring the active channel in the move engine status register(s).

2.54 [DMA_TC.055] ICU to DMA Interface in Sleep Mode

Description

The Interrupt Router triggers DMA hardware requests via the ICU interface. If the DMA is in sleep mode, the DMA will not acknowledge DMA hardware requests. The effect is to lock up the ICU to DMA interface.

Workaround

The application must disable the triggering of DMA hardware requests before placing the DMA in sleep mode.

2.55 [DMA_TC.056] TSR and SUSENR Access Protection Unreliable

Description

The DMA access protection is part of a system wide access protection scheme to restrict write accesses to DMA registers to individual on-chip bus masters.

If the application software configures DMA freedom from interference measures (i.e. when any on-chip bus master write to the DMA is prohibited by a DMA access enable setting), then on-chip bus master writes to the DMA channel TSR and SUSENR registers are unreliable and may result in the following effects:

1. Safety Related Effects

- 1.1. An illegal write access to a DMA channel TSR register will succeed with no indication

The safety related effects (in point 1.1) relate to the DMA channel reset, halt and hardware request control functions in the TSR register. The most severe safety effect is that a DMA operation may be lost.

Workaround (for 1.1)

If the application software implements temporal monitoring of DMA transactions (for example using DMA timestamp) to detect lost DMA operations, the application software will detect the effect of the illegal access to DMA channel TSR register.

2. Non Safety Related Effects

- 2.1. An illegal write access to a DMA channel SUSENR register may succeed with no indication.
  - Impact of 2.1: The SUSENR register is a debug only register. No impact is foreseen during a normal application
- 2.2. A legal write access to a DMA channel TSR register may fail with an indication - this means unexpected bus errors may be triggered when accessing TSR registers
- 2.3. A legal write access to a DMA channel SUSENR register may fail with an indication - this means unexpected bus errors may be triggered when accessing SUSENR registers.
  - Impact of 2.2 & 2.3: Unexpected SPB bus errors and hence CPU traps and SPB error alarms may occur during application run

Workaround (for 2.2 & 2.3)

If the system implements DMA freedom from interference measures, then the Impact of 2.2 & 2.3 will occur, and cause unexpected SPB bus errors and hence CPU traps and SPB error alarms when writing to TSR and SUSENR registers.

In order to work around this problem, the application software shall implement all of the following steps:

- W1: Before an intended write access to a DMA channel TSR or SUSENR register, perform an additional preceding write access to a DMA channel Transaction Control Set (TCS) register of the same DMA channel.
  - TCS registers include the DMA channel RDCRC, SDCRC, SADR, DADR, SHADR, ADICR, CHCSR and CHCFGR registers
- W2: Ensure that this additional preceding write access to a DMA channel TCS register has no real effect. Recommendation: Simply read and write back the RDCRCR register
- W3: Perform the write access to the DMA channel TSR register

Ensure that no other on-chip bus master can access any DMA register of a different resource partition between steps W2 and W3 in the workaround above.

Example Code Snippet

To update TSR register of DMA channel 25 with value:

1. Uint32 temp = DMA_RDCRCR25.U;
2. DMA_ RDCRCR25.U = temp;
3. DMA_TSR25.U = value;

2.56 [DMA_TC.058] Linked List Load Transaction Control Set (TCS) Integrity Error

Description

If DMA channel z is configured for one of the following linked list operations:

- DMA Linked List
  - (DMA channel ADICRz.SHCT = 1100_B)
- Accumulated Linked List
  - (DMA channel ADICRz.SHCT = 1101_B)
- Safe Linked List
  - (DMA channel ADICRz.SHCT = 1110_B)
- Conditional Linked List
  - (DMA channel ADICRz.SHCT = 1111_B)

Then on completion of a DMA transaction a new TCS is loaded into DMA channel z from the on-chip bus.

The DMA ignores data integrity errors in the new TCS:

- The DMA does not trigger an alarm to the SMU
- The DMA does not store any DMA error status
- The DMA may execute a corrupted DMA transaction

Detection of most corrupted DMA transactions is provided by the DMA safety mechanisms as follows:

- Use of the DMA address checksum to detect address generation faults
- Use of the DMA timestamp[1)] to detect temporal faults

Workaround

None.

1 Conditional Linked List does not support the appendage of timestamps (ADICRz.STAMP = 0_B).

2.57 [DMA_TC.061] DMA Double Buffering Operations

Description

***Note**:* *This erratum DMA_TC.061 (DMA Double Buffering Operations) substitutes the following errata text modules*

- *DMA_TC.029 (DMA Double Buffering Overflow),*
- *DMA_TC.047 (DMA Double Buffering Buffer Switch), and*
- *DMA_TC.057 (Double Buffering Overflow Causes Other Channel Corruption)*

included in previous TC2xx errata sheet releases.

Software may configure a DMA channel for one of the DMA double buffering operations:

- DMA Double Source Buffering Software Switch Only
  - (DMA channel DMA_ADICRz.SHCT = 1000_B)
- DMA Double Source Buffering Automatic Hardware and Software Switch
  - (DMA channel DMA_ADICRz.SHCT = 1001_B)
- DMA Double Destination Buffering Software Switch Only
  - (DMA channel DMA_ADICRz.SHCT = 1010_B)
- DMA Double Destination Buffering Automatic Hardware and Software Switch
  - (DMA channel DMA_ADICRz.SHCT = 1011_B)

If the DMA is servicing a DMA request for a DMA channel configured for one of the double buffering operations AND the software executes a Software Buffer Switch operation (DMA_CHCSRz.SWB = 1_B), the DMA will not perform the buffer switch reliably.

The following sections provide recommendations for the implementation of DMA double buffering operations.

Supported DMA double buffering operations

As a consequence, the software should configure for a limited number of DMA double buffering operations:

- DMA Double Source Buffering Automatic Hardware Switch
  - (DMA channel DMA_ADICRz.SHCT = 1001_B)
- DMA Double Destination Buffering Automatic Hardware Switch
  - (DMA channel DMA_ADICRz.SHCT = 1011_B)

The software must

- NOT perform a Software Buffer Switch (DMA_CHCSRz.SWB = 0_B)
- NOT set the frozen bit (DMA_CHCSRz.FROZEN = 1_B)

DMA channel ETRL configuration

The software must set the Enable Transaction Request Lost (ETRL) bit (DMA_ADICRz.ETRL = 1_B) to prevent the DMA locking up during a DMA double buffering operation.

DMA channel monitoring

The software should configure the DMA to trigger a DMA channel interrupt service request when the DMA empties (source buffering) or fills (destination buffering) a buffer on the completion of a DMA transaction. The software must service the DMA channel interrupt service requests. As soon as the software has analysed a buffer, the software must clear the frozen bit (DMA_CHCSRz.FROZEN = 0_B) and re-initialise the buffer address pointer.

DMA channel underflow or overflow

If the software fails to analyse a frozen buffer before the next DMA channel interrupt service request, the DMA channel will underflow (source buffering) or overflow (destination buffering) on receiving the next DMA request. Erroneously, the DMA will not trigger a DMA error interrupt service request.

As soon as the CPU receives a DMA channel interrupt service request, the software must check for an underflow or overflow by monitoring the DMA transaction count. If the software reads a zero transaction count (DMA_CHCSRz.TCOUNT = 0_D), the DMA channel is in an underflow or overflow state.

DMA channel interference

Erroneously a DMA channel underflow or overflow may cause the setting of the TRL flag and the clearing of a DMA request in one or more other DMA channels (note: dependent on the scheduling of DMA channels around this DMA request). The DMA channel interference is independent of resource partition assignment.

DMA channel reset

If the software detects a DMA channel underflow or overflow, the software must apply a DMA channel reset to all used DMA channels. On completion of the DMA channel reset, the software must re-configure all used DMA channels.

Alternatively, the software may apply an application reset.

Workaround

None.

2.58 [DMA_TC.062] Termination of DMA Transaction for Pattern Match

Description

If a DMA channel is configured for pattern detection and the DMA detects a pattern match, the DMA should terminate the DMA transaction. The DMA should provide the software with the capability to use the DMA channel status to identify the transfer number of the DMA move data.

Erroneously, the DMA may decrement 1 from the TCOUNT value making identification of the DMA move data unreliable.

Workaround

None.

2.59 [DMA_TC.063] DMA Timestamp Destination Address

Description

If software configures a DMA channel

- for increment of DMA destination address (DMA_ADICRz.INCD = 1_B) AND
- to append a DMA timestamp (DMA_ADICRz.STAMP = 1_B);

and the intended write address of the DMA timestamp is in a different 32 Kbyte page to the last DMA destination address to write DMA move data, the DMA erroneously calculates the DMA timestamp write address. The DMA writes the DMA timestamp to an incorrect address inside the same 32 Kbyte page as the last DMA destination address.

Workaround

The last DMA destination address and the write address of the DMA timestamp shall exist in the same 32 Kbyte page (i.e. and shall not cross the 32 Kbyte page boundary).

2.60 [DMA_TC.064] DMA Daisy Chain Request

Description

If software configures a DMA channel for one of the following DMA operations:

- DMA Pattern Detection
  - (DMA channel DMA_CHCFGRz.PATSEL[1:0] != 00_B)
- DMA Double Source Buffering Software Switch Only
  - (DMA channel DMA_ADICRz.SHCT = 1000_B)
- DMA Double Source Buffering Automatic Hardware and Software Switch
  - (DMA channel DMA_ADICRz.SHCT = 1001_B)
- DMA Double Destination Buffering Software Switch Only
  - (DMA channel DMA_ADICRz.SHCT = 1010_B)
- DMA Double Destination Buffering Automatic Hardware and Software Switch
  - (DMA channel DMA_ADICRz.SHCT = 1011_B)
- DMA linked list
  - (DMA channel DMA_ADICRz.SHCT = 1100_B)
- Accumulated linked list
  - (DMA channel DMA_ADICRz.SHCT = 1101_B)
- Safe linked list
  - (DMA channel DMA_ADICRz.SHCT = 1110_B)
- Conditional linked list
  - (DMA channel ADICRz.SHCT = 1111_B)

the software must not select daisy chain (DMA channel CHCFGRz.PRSEL = 0_B).

2.61 [DMA_TC.065] DMA Move Concurrent Bus Accesses

Description

The highest number DMA channel always wins arbitration to shared DMA resources (Move Engine and DMA on-chip bus master interfaces). The configuration of the DMA priority (DMA_CHCFGRx.DMAPRIO) has no effect on internal DMA arbitration.

The DMA priority is used by the System Peripheral Bus (SPB) controller to arbitrate between requests from all the SPB master interfaces.

Workaround

None.

2.62 [DMA_TC.066] DMA double buffering operations - Update address pointer

Description

Software may configure a DMA channel for one of the DMA double buffering operations:

- DMA Double Source Buffering Software Switch Only
  - (DMA channel DMA_ADICRz.SHCT = 1000_B)
- DMA Double Source Buffering Automatic Hardware and Software Switch
  - (DMA channel DMA_ADICRz.SHCT = 1001_B)

- DMA Double Destination Buffering Software Switch Only
  - (DMA channel DMA_ADICRz.SHCT = 1010_B)
- DMA Double Destination Buffering Automatic Hardware and Software Switch
  - (DMA channel DMA_ADICRz.SHCT = 1011_B)

If the software updates a buffer address pointer by BYTE or HALF-WORD writes, the resulting value of the address pointer is corrupted.

Workaround

If the software updates a buffer address pointer, the software should only use a 32-bit WORD access.

2.63 [DSADC_TC.011] Modulator Coupling Option no longer supported

Description

The modulator coupling feature (two adjacent 3rd-order modulators can optionally be combined to operate as a 4th-order modulator and a 2nd-order modulator) is no longer supported in this device step.

Therefore, only the default setting DICFGx.DSRC = 0000_B must be used.

***Note**: The DSADC parameter specification of the Data Sheet is achieved with the internal modulators operating in the default 3rd-order configuration (DICFGx.DSRC = 0000_B). The User's Manual will be adapted accordingly.*

2.64 [DSADC_TC.012] Common Mode Hold Voltage Not Applied During Calibration

Description

The common mode hold voltage V_{CMH} can be applied to a pin while this pin is not connected to the standard common mode voltage V_{CM}. This is the case while the input pin is not selected by the analog input multiplexer (MODCFGx.INMUX, if available for the respective channel) or while the modulator is switched off.

During calibration the modulator is connected to internal signal sources (MODCFGx.INCFG*), i.e. not to the pin.

In this case neither V_{CM} nor V_{CMH} are connected to the pin.

The voltage provided to passive sensors may, therefore, decrease for a short while (i.e. during the calibration time).

Workaround

None.

2.65 [DSADC_TC.013] Common Mode Voltage Selection

Description

The common mode voltage V_{CM} depends on the configuration of bit-field MODCFGx.CMVS and on the supply voltage range selected by bit GLOBCFG.LOSUP.

The divider factors and resulting values of V_{CM} for V_{AREF} = 3.3 V listed in the description of CMVS in register MODCFGx in the DSADC chapter of the User's Manual are incorrect. The corrected description is shown in the following Table 7.

Table 7 Corrected Description of Bit Field CMVS in Register MODCFGx

Field	Bits	Type	Description
CMVS	[25:24]	rw	**Common Mode Voltage Selection** Defines the common mode voltage V_{CM} for the input buffers of a twin-modulator. V_{CM} depends on CMVS and on the selected supply voltage range (GLOBCFG.LOSUP). 00_B $V_{CM} = V_{AREF} / 3.0 \mid 2.0$ (for LOSUP = 0 | 1) V_{CM} = 1.67 V for V_{AREF} = 5.0 V | 3.3 V 01_B $V_{CM} = V_{AREF} / 2.27 \mid 1.5$ (for LOSUP = 0 | 1) V_{CM} = 2.21 V for V_{AREF} = 5.0 V | 3.3 V 10_B $V_{CM} = V_{AREF} / 2.0 \mid 1.32$ (for LOSUP = 0 | 1) V_{CM} = 2.5 V for V_{AREF} = 5.0 V | 3.3 V 11_B Reserved ***Note**: For most applications $V_{CM} = V_{AREF} / 2.0$ will be the optimum (see Section "Common Mode Voltage" in User's Manual, chapter DSADC)*

This means that $V_{CM} = V_{AREF} / 2.0$ is selected by CMVS = 10_B when LOSUP = 0_B, and by CMVS = 00_B when LOSUP = 1_B.

***Note**: The description of bit-field VCMHS for the Common Mode **Hold** Voltage Selection in register GLOBVCMH2 in the User's Manual is correct, i.e. $V_{CMH} = V_{DDM} / 2.0$ is selected by VCMHS = 00_B.*

2.66 [DTS_TC.001] Temperature Sensor Formula

Description

The formula documented in older Data Sheet versions may result in an increased temperature error when calculating the junction temperature Tj of the device from a DTS temperature measurement.

To properly calculate the temperature measured by the DTS in [°C] from the RESULT bit-field of register SCU_DTSSTAT, it is recommended to use the following formulas depending on the contents of bit-field SCU_DTSCON[30:29]:

- While bit-field SCU_DTSCON[30:29] = 00_B: Tj = (RESULT - 607_D) / 2.13
- While bit-field SCU_DTSCON[30:29] = 01_B: Tj = (RESULT - 646_D) / 2.11

Bit field SCU_DTSCON[30:29] can only deliver one of the two values (00_B, 01_B) listed above (constant for a given device).

Make sure the application software does not modify the values installed during device start-up in register SCU_DTSCON.

***Note**: The description in the Data Sheet will be updated appropriately.*

2.67 [ETH_AI.003] Overflow Status bits of Missed Frame and Buffer Overflow counters get cleared without a Read operation

Description

The DMA maintains two counters to track the number of frames missed because of the following:

- Rx Descriptor not being available
- Rx FIFO overflow during reception

The Missed Frame and Buffer Overflow Counter register indicates the current value of the missed frames and FIFO overflow frame counters. This register also has the Overflow status bits (Bit 16 and Bit 28) which indicate whether the rollover occurred for respective counter. These bits are set when respective counter rolls over. These bits should remain high until this register is read.

However, erroneously, when the counter rollover occurs second time after the status bit is set, the respective status bit is reset to zero.

Effects

The application may incorrectly detect that the rollover did not occur since the last read operation.

Workaround

The application should read the Missed Frame and Buffer Overflow Counter register periodically (or after the Overflow or Rollover status bits are set) such that the counter rollover does not occur twice between read operations.

2.68 [ETH_TC.004] DMA Access to Reserved/Protected Resources: FPI Error Response not correctly evaluated

Description

The ETH module includes a configurable DMA function to support the ETH Rx/Tx data transfers from/to system memory resources. The ETH DMA function accesses the system memory resources via the on-chip bus system (SPB/SRI). If the ETH DMA is accessing reserved system address ranges or protected resources (for example protected via system MPU/ACCEN register), the ETH DMA transactions via the on-chip bus system will be finished on the on-chip bus with an Error Acknowledge.

Depending on the target address, the first transaction with an Error Acknowledge will be captured by the BCU_FPI (SPB Bus Control Unit) and/or by the XBAR_SRI. An interrupt can be generated by BCU_FPI / XBAR_SRI if the related SRN is enabled, and an Alarm is signalled to the SMU.

However, the ETH DMA will not be stopped by an Error Acknowledge. It will ignore the Error Acknowledge (i.e. bits FBI and EB in register ETH_STATUS are not set).

In this situation the ETH RX data transferred by the DMA to an invalid internal address will be lost, ETH will go on with invalid TX data.

2.69 [FLASH_TC.052] Use of Write Page Once command

Description

When applying a Write Page Once (WPO) command to a pre-programmed or incompletely erased PFlash location, the WPO command will fail as expected, with both EVER (Erase Verify Error) and PVER (Program Verify Error) error flags being raised.

For an EVER failure in the WPO command, the read bias conditions on the NVM cells for the subsequent read operations will be incorrect. The incorrect bias conditions at the NVM cell terminals may lead to single-bit or multi-bit errors in the PFlash. Only zeroes (erased cells) will be affected by this phenomenon.

The physical content of the flash cells is not damaged by the incorrect read bias conditions, or by the WPO command failure.

***Note**: As per the safety manual's Architecture for Management of Faults [SM_AURIX_PMU_3], it is assumed that the WPO command is not used during application run time.*

Workaround

The incorrect NVM read bias conditions can be fully recovered by performing one of the following actions immediately after the WPO failure:

- Request Flash module sleep mode and wake-up immediately after the WPO failure:
  - Request Sleep mode by setting bit FCON.SLEEP = 1_B
  - Poll the Flash Sleep Mode status bit FSR.SLM to make sure that the Flash is in sleep mode
  - Initiate wake-up by clearing FCON.SLEEP = 0_B
  - Poll status bit FSR.SLM to make sure that the flash is in normal state again

***Note**: For more details about AURIX™ power-down modes, please refer to Application Note "AURIX™ standby power mode" (AP32332).*

- Perform System Reset immediately after the WPO failure

2.70 [FlexRay_AI.087] After reception of a valid sync frame followed by a valid non-sync frame in the same static slot the received sync frame may be ignored

Description

If in a static slot of an even cycle a valid sync frame followed by a valid non-sync frame is received, and the frame valid detection (prt_frame_decoded_on_X) of the DEC process occurs one sclk after valid frame detection of FSP process (fsp_val_syncfr_chx), the sync frame is not taken into account by the CSP process (devte_xxs_reg).

Scope

The erratum is limited to the case where more than one valid frame is received in a static slot of an even cycle.

Effects

In the described case the sync frame is not considered by the CSP process. This may lead to a SyncCalcResult of MISSIMG_TERM (error flag SFS.MRCS set). As a result the POC state may switch to NORMAL_PASSIVE or HALT or the Start-up procedure is aborted.

Workaround

Avoid static slot configurations long enough to receive two valid frames.

2.71 [FlexRay_AI.088] A sequence of received WUS may generate redundant SIR.WUPA/B events

Description

If a sequence of wake-up symbols (WUS) is received, all separated by appropriate idle phases, a valid wake-up pattern (WUP) should be detected after every second WUS.The E-Ray detects a valid wake-up pattern after the second WUS and then after each following WUS.

Scope

The erratum is limited to the case where the application program frequently resets the appropriate SIR.WUPA/B bits.

Effects

In the described case there are more SIR.WUPA/B events seen than expected.

Workaround

Ignore redundant SIR.WUPA/B events.

2.72 [FlexRay_AI.089] Rate correction set to zero in case of SyncCalcResult=MISSING_TERM

Description

In case a node receives too few sync frames for rate correction calculation and signals a SyncCalcResult of MISSING_TERM, the rate correction value is set to zero instead of to the last calculated value.

Scope

The erratum is limited to the case of receiving too few sync frames for rate correction calculation (SyncCalcResult=MISSING_TERM in an odd cycle).

Effects

In the described case a rate correction value of zero is applied in NORMAL_ACTIVE / NORMAL_PASSIVE state instead of the last rate correction value calculated in NORMAL_ACTIVE state. This may lead to a desynchronisation of the node although it may stay in NORMAL_ACTIVE state (depending on gMaxWithoutClockCorrectionPassive) and decreases the probability to re-enter NORMAL_ACTIVE state if it has switched to NORMAL_PASSIVE (pAllowHaltDueToclock=false).

Workaround

It is recommended to set gMaxWithoutClockCorrectionPassive to 1. If missing sync frames cause the node to enter NORMAL_PASSIVE state, use higher level application software to leave this state and to initiate a re-integration into the cluster. HALT state can also be used instead of NORMAL_PASSIVE state by setting pAllowHaltDueToClock to true.

2.73 [FlexRay_AI.090] Flag SFS.MRCS is set erroneously although at least one valid sync frame pair is received

Description

If in an odd cycle 2c+1 after reception of a sync frame in slot n the total number of different sync frames per double cycle has exceeded gSyncNodeMax and the node receives in slot n+1 a sync frame that matches with a sync frame received in the even cycle 2c, the sync frame pair is not taken into account by CSP process. This may cause the flags SFS.MRCS and EIR.CCF to be set erroneously.

Scope

The erratum is limited to the case of a faulty cluster configuration where different sets of sync frames are transmitted in even and odd cycles and the total number of different sync frames is greater than gSyncNodeMax.

Effects

In the described case the error interrupt flag EIR.CCF is set and the node may enter either the POC state NORMAL_PASSIVE or HALT.

Workaround

Correct configuration of gSyncNodeMax.

2.74 [FlexRay_AI.091] Incorrect rate and / or offset correction value if second Secondary Time Reference Point (STRP) coincides with the action point after detection of a valid frame

Description

If a valid sync frame is received before the action point and additionally noise or a second frame leads to a STRP coinciding with the action point, an incorrect deviation value of zero is used for further calculations of rate and/or offset correction values.

Scope

The erratum is limited to configurations with an action point offset greater than the static frame length.

Effects

In the described case a deviation value of zero is used for further calculations of rate and/or offset correction values. This may lead to an incorrect rate and / or offset correction of the node.

Workaround

Configure action point offset smaller than static frame length.

2.75 [FlexRay_AI.092] Initial rate correction value of an integrating node is zero if pMicroInitialOffsetA,B = 0x00

Description

The initial rate correction value as calculated in figure 8-8 of protocol spec v2.1 is zero if parameter pMicroInitialOffsetA,B was configured to be zero.

Scope

The erratum is limited to the case where pMicroInitialOffsetA,B is configured to zero.

Effects

Starting with an initial rate correction value of zero leads to an adjustment of the rate correction earliest 3 cycles later (see figure 7-10 of protocol spec v2.1). In a worst case scenario, if the whole cluster is drifting away too fast, the integrating node would not be able to follow and therefore abort integration.

Workaround

Avoid configurations with pMicroInitialOffsetA,B equal to zero. If the related configuration constraint of the protocol specification results in pMicroInitialOffsetA,B equal to zero, configure it to one instead. This will lead to a correct initial rate correction value, it will delay the start-up of the node by only one micro tick.

2.76 [FlexRay_AI.093] Acceptance of start-up frames received after reception of more than gSyncNodeMax sync frames

Description

If a node receives in an even cycle a start-up frame after it has received more than gSyncNodeMax sync frames, this start-up frame is added erroneously by process CSP to the number of valid start-up frames (zStartupNodes). The faulty number of start-up frames is delivered to the process POC. As a consequence this node may integrate erroneously to the running cluster because it assumes that it has received the required number of start-up frames.

Scope

The erratum is limited to the case of more than gSyncNodeMax sync frames.

Effects

In the described case a node may erroneously integrate successfully into a running cluster.

Workaround

Use frame schedules where all start-up frames are placed in the first static slots. gSyncNodeMax should be configured to be greater than or equal to the number of sync frames in the cluster.

2.77 [FlexRay_AI.094] Sync frame overflow flag EIR.SFO may be set if slot counter is greater than 1024

Description

If in the static segment the number of transmitted and received sync frames reaches gSyncNodeMax and the slot counter in the dynamic segment reaches the value cStaticSlotIDMax + gSyncNodeMax = 1023 + gSyncNodeMax, the sync frame overflow flag EIR.SFO is set erroneously.

Scope

The erratum is limited to configurations where the number of transmitted and received sync frames equals to gSyncNodeMax and the number of static slots plus the number of dynamic slots is greater or equal than 1023 + gSyncNodeMax.

Effects

In the described case the sync frame overflow flag EIR.SFO is set erroneously. This has no effect to the POC state.

Workaround

Configure gSyncNodeMax to number of transmitted and received sync frames plus one or avoid configurations where the total of static and dynamic slots is greater than cStaticSlotIDMax.

2.78 [FlexRay_AI.095] Register RCV displays wrong value

Description

If the calculated rate correction value is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping], vRateCorrection of the CSP process is set to zero. In this case register RCV should be updated with this value. Erroneously RCV.RCV[11:0] holds the calculated value in the range [-pClusterDriftDamping .. +pClusterDriftDamping] instead of zero.

Scope

The erratum is limited to the case where the calculated rate correction value is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping].

Effects

The displayed rate correction value RCV.RCV[11:0] is in the range of [-pClusterDriftDamping .. +pClusterDriftDamping] instead of zero. The error of the displayed value is limited to the range of [-pClusterDriftDamping .. +pClusterDriftDamping]. For rate correction in the next double cycle always the correct value of zero is used.

Workaround

A value of RCV.RCV[11:0] in the range of [-pClusterDriftDamping .. +pClusterDriftDamping] has to be interpreted as zero.

2.79 [FlexRay_AI.096] Noise following a dynamic frame that delays idle detection may fail to stop slot

Description

If (in case of noise) the time between 'potential idle start on X' and 'CHIRP on X' (see Protocol Spec. v2.1, Figure 5-21) is greater than gdDynamicSlotIdlePhase, the E-Ray will not remain for the remainder of the current dynamic segment in the state 'wait for the end of dynamic slot rx'. Instead, the E-Ray continues slot counting. This may enable the node to further transmissions in the current dynamic segment.

Scope

The erratum is limited to noise that is seen only locally and that is detected in the time window between the end of a dynamic frame's DTS and idle detection ('CHIRP on X').

Effects

In the described case the faulty node may not stop slot counting and may continue to transmit dynamic frames. This may lead to a frame collision in the current dynamic segment.

Workaround

None

2.80 [FlexRay_AI.097] Loop back mode operates only at 10 MBit/s

Description

The looped back data is falsified at the two lower baud rates of 5 and 2.5 MBit/s.

Scope

The erratum is limited to test cases where loop back is used with the baud rate prescaler (PRTC1.BRP[1:0]) configured to 5 or 2.5 MBit/s.

Effects

The loop back self test is only possible at the highest baud rate.

Workaround

Run loop back tests with 10 MBit/s (PRTC1.BRP[1:0] = 00_B).

2.81 [FlexRay_AI.099] Erroneous cycle offset during start-up after abort of start-up or normal operation

Description

An abort of start-up or normal operation by a READY command near the macro tick border may lead to the effect that the state INITIALIZE_SCHEDULE is one macro tick too short during the first following integration attempt. This leads to an early cycle start in state INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK.

As a result the integrating node calculates a cycle offset of one macro tick at the end of the first even/odd cycle pair in the states INTEGRATION_COLDSTART_CHECK or INTEGRATION_CONSISTENCY_CHECK and tries to correct this offset.

If the node is able to correct the offset of one macro tick (pOffsetCorrectionOut >> gdMacrotick), the node enters NORMAL_ACTIVE with the first start-up attempt.

If the node is not able to correct the offset error because pOffsetCorrectionOut is too small (pOffsetCorrectionOut ≤ gdMacrotick), the node enters ABORT_STARTUP and is ready to try start-up again. The next (second) start-up attempt is not effected by this erratum.

Scope

The erratum is limited to applications where READY command is used to leave STARTUP, NORMAL_ACTIVE, or NORMAL_PASSIVE state.

Effects

In the described case the integrating node tries to correct an erroneous cycle offset of one macro tick during start-up.

Workaround

With a configuration of pOffsetCorrectionOut >> gdMacrotick • (1+cClockDeviationMax) the node will be able to correct the offset and therefore also be able to successfully integrate.

2.82 [FlexRay_AI.100] First WUS following received valid WUP may be ignored

Description

When the protocol engine is in state WAKEUP_LISTEN and receives a valid wake-up pattern (WUP), it transfers into state READY and updates the wake-up status vector CCSV.WSV[2:0] as well as the status interrupt flags SIR.WST and SIR.WUPA/B . If the received wake-up pattern continues, the protocol engine may ignore the first wake-up symbol (WUS) following the state transition and signals the next SIR.WUPA/B at the third instead of the second WUS.

Scope

The erratum is limited to the reception of redundant wake-up patterns.

Effects

Delayed setting of status interrupt flags SIR.WUPA/B for redundant wake-up patterns.

Workaround

None

2.83 [FlexRay_AI.101] READY command accepted in READY state

Description

The E-Ray module does not ignore a READY command while in READY state.

Scope

The erratum is limited to the READY state.

Effects

Flag CCSV.CSI is set. Cold starting needs to be enabled by POC command ALLOW_COLDSTART (SUCC1.CMD = 1001_B).

Workaround

None

2.84 [FlexRay_AI.102] Slot status vPOC!SlotMode is reset immediately when entering HALT state

Description

When the protocol engine is in the states NORMAL_ACTIVE or NORMAL_PASSIVE, a HALT or FREEZE command issued by the Host resets vPOC!SlotMode immediately to SINGLE slot mode (CCSV.SLM[1:0] = 00_B). According to the FlexRay protocol specification, the slot mode should not be reset to SINGLE slot mode before the following state transition from HALT to DEFAULT_CONFIG state.

Scope

The erratum is limited to the HALT state.

Effects

The slot status vPOC!SlotMode is reset to SINGLE when entering HALT state.

Workaround

None

2.85 [FlexRay_AI.103] Received messages not stored in Message RAM when in Loop Back Mode

Description

After a FREEZE or HALT command has been asserted in NORMAL_ACTIVE state, and if state LOOP_BACK is then entered by transition from HALT state via DEF_CONFIG and CONFIG, it may happen that acceptance filtering for received messages is not started, and therefore these messages are not stored in the respective receive buffer in the Message RAM.

Scope

The erratum is limited to the case where Loop Back Mode is entered after NORMAL_ACTIVE state was left by FREEZE or HALT command.

Effects

Received messages are not stored in Message RAM because acceptance filtering is not started.

Workaround

Leave HALT state by hardware reset.

2.86 [FlexRay_AI.104] Missing start-up frame in cycle 0 at coldstart after FREEZE or READY command

Description

When the E-Ray is restarted as leading coldstarter after it has been stopped by FREEZE or READY command, it may happen, depending on the internal state of the module, that the E-Ray does not transmit its start-up frame in cycle 0. Only E-Ray configurations with start-up frames configured for slots 1 to 7 are affected by this behavior.

Scope

The erratum is limited to the case when a coldstart is initialized after the E-Ray has been stopped by FREEZE or READY command. Coldstart after hardware reset is not affected.

Effects

During coldstart it may happen that no start-up frame is sent in cycle 0 after entering COLDSTART_COLLISION_RESOLUTION state from COLDSTART_LISTEN state.

The next coldstart attempt is no longer affected. Coldstart sequence is lengthened but coldstart of FlexRay system is not prohibited by this behavior.

Workaround

Use a static slot greater or equal 8 for the start-up/sync message.

2.87 [FlexRay_AI.105] RAM select signals of IBF1/IBF2 and OBF1/OBF2 in RAM test mode

Description

When accessing Input Buffer RAM 1, 2 (IBF1, 2) or Output Buffer RAM 1, 2 (OBF1, 2) in RAM test mode, the following behavior can be observed when entering RAM test mode after hardware reset.

- Read or write access to IBF2:
  - In this case also IBF1 RAM select eray_ibf1_cen is activated initiating a read access of the addressed IBF1 RAM word. The data read from IBF1 is evaluated by the respective parity checker.
- Read or write access to OBF1:
  - In this case also OBF2 RAM select eray_obf2_cen is activated initiating a read access of the addressed OBF2 RAM word. The data read from OBF2 is evaluated by the respective parity checker.

If the parity logic of the erroneously selected IBF1 resp. OBF2 detects a parity error, bit MHDS.PIBF resp. MHDS.POBF in the E-Ray Message Handler Status register is set although the addressed IBF2 resp. OBF1 had

not error. The logic for setting MHDS.PIBF / MHDS.POBF does not distinguish between set conditions from IBF1 or IBF2 resp. OBF1 or OBF2.

Due to the IBF / OBF swap mechanism as described in section 5.11.2 in the E-Ray Specification, the inverted behavior with respect to IBF1, 2 and OBF1, 2 can be observed depending on the IBF / OBF access history.

Scope

The erratum is limited to the case when IBF1, 2 or OBF1, 2 are accessed in RAM test mode. The problem does not occur when the E-Ray is in normal operation mode.

Effects

When reading or writing IBF1, 2 / OBF1, 2 in RAM test mode, it may happen, that the parity logic of IBF1, 2 / OBF1, 2 signals a parity error.

Workaround

For RAM testing after hardware reset, the Input / Output Buffer RAMs have to be first written and then read in the following order: IBF1 before IBF2 and OBF2 before OBF1

2.88 [FlexRay_AI.106] Data transfer overrun for message transfers Message RAM to Output Buffer (OBF) or from Input Buffer (IBF) to Message RAM

Description

The problem occurs under the following conditions:

1) A received message is transferred from the Transient Buffer RAM (TBF) to the message buffer that has its data pointer pointing to the first word of the Message RAM's Data Partition located directly after the last header word of the Header Partition of the Last Configured Buffer as defined by MRC.LCB

2) The Host triggers a transfer from / to the Last Configured Buffer in the Message RAM with a specific time relation to the start of the TBF transfer described under 1)

Under these conditions the following transfers triggered by the Host may be affected:

a) Message buffer transfer from Message RAM to OBF

When the message buffer has its payload configured to maximum length (PLC = 127), the OBF word on address 00h (payload data bytes 0 to 3) is overwritten with unexpected data at the end of the transfer.

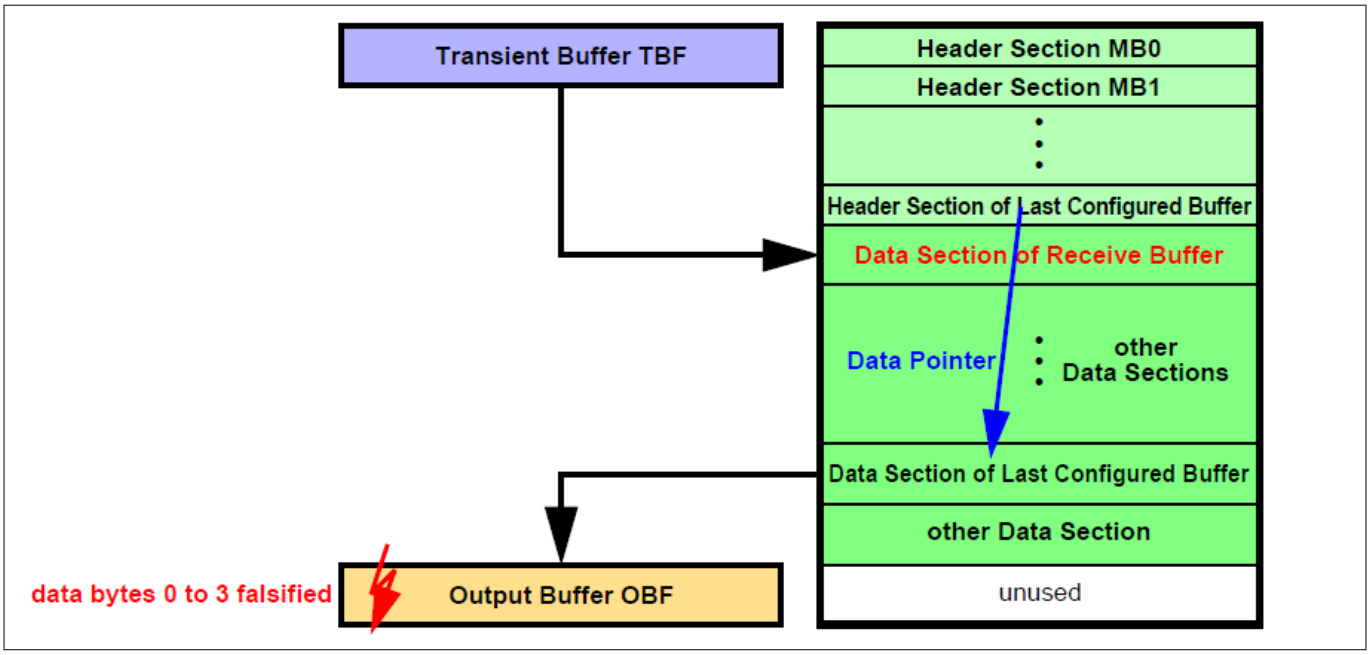

Figure 1 Message buffer transfer from Message RAM to OBF

b) Message buffer transfer from IBF to Message RAM

After the Data Section of the selected message buffer in the Message RAM has been written, one additional write access overwrites the following word in the Message RAM which might be the first word of the next Data Section.

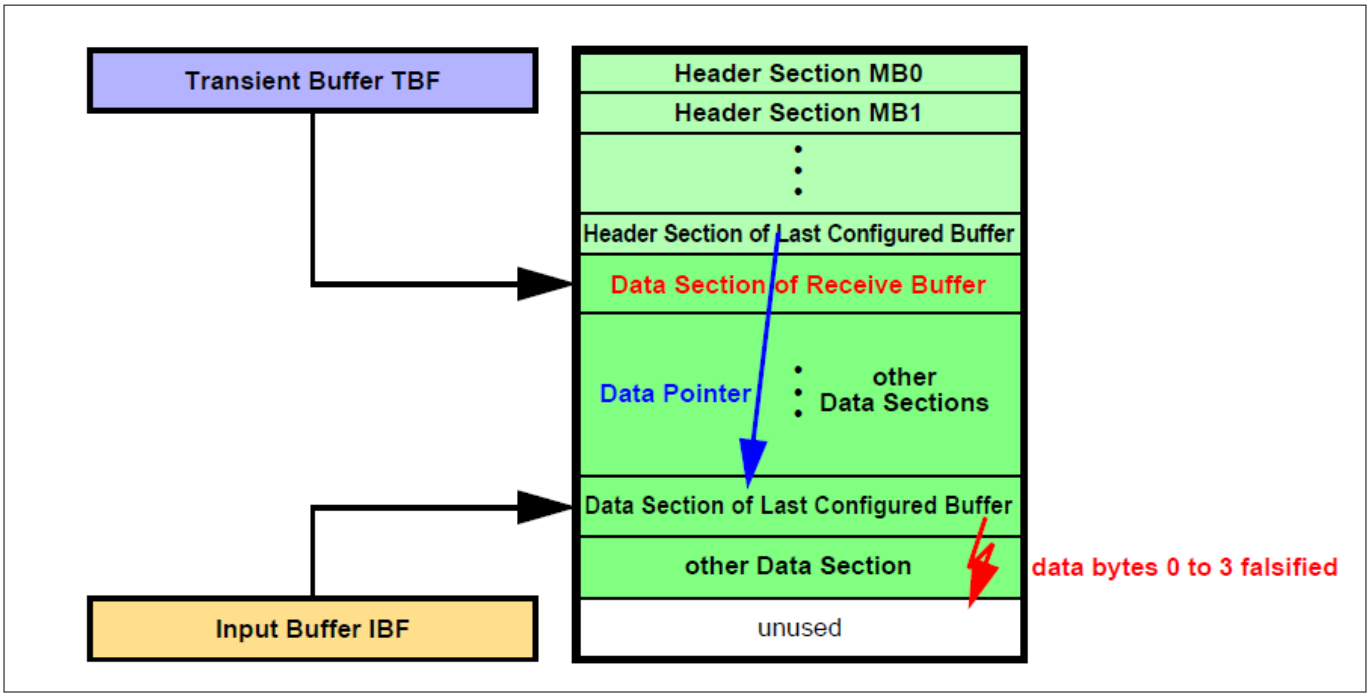

Figure 2 Message buffer transfer from IBF to Message RAM

Scope

The erratum is limited to the case when (see Figure 3 “Bad Case”):

1) The first Data Section in the Data Partition is assigned to a receive buffer (incl. FIFO buffers)

AND

2) The Data Partition in the Message RAM starts directly after the Header Partition (no unused Message RAM word in between)

Effects

a) When a message is transferred from the Last Configured Buffer in the Message RAM to the OBF and PLC = 127 it may happen, that at the end of the transfer the OBF word on address 00h (payload data bytes 0 to 3) is overwritten with unexpected data (see Figure 1)

b) When a message is transferred from IBF to the Last Configured Buffer in the Message RAM, it may happen, that at the end of the transfer of the Data Section one additional write access overwrites the following word, which may be the first word of another message's Data Section in the Message RAM (see Figure 2)

Workaround 1

Leave at least one unused word in the Message RAM between Header Section and Data Section.

Workaround 2

Ensure that the Data Section directly following the Header Partition is assigned to a transmit buffer.

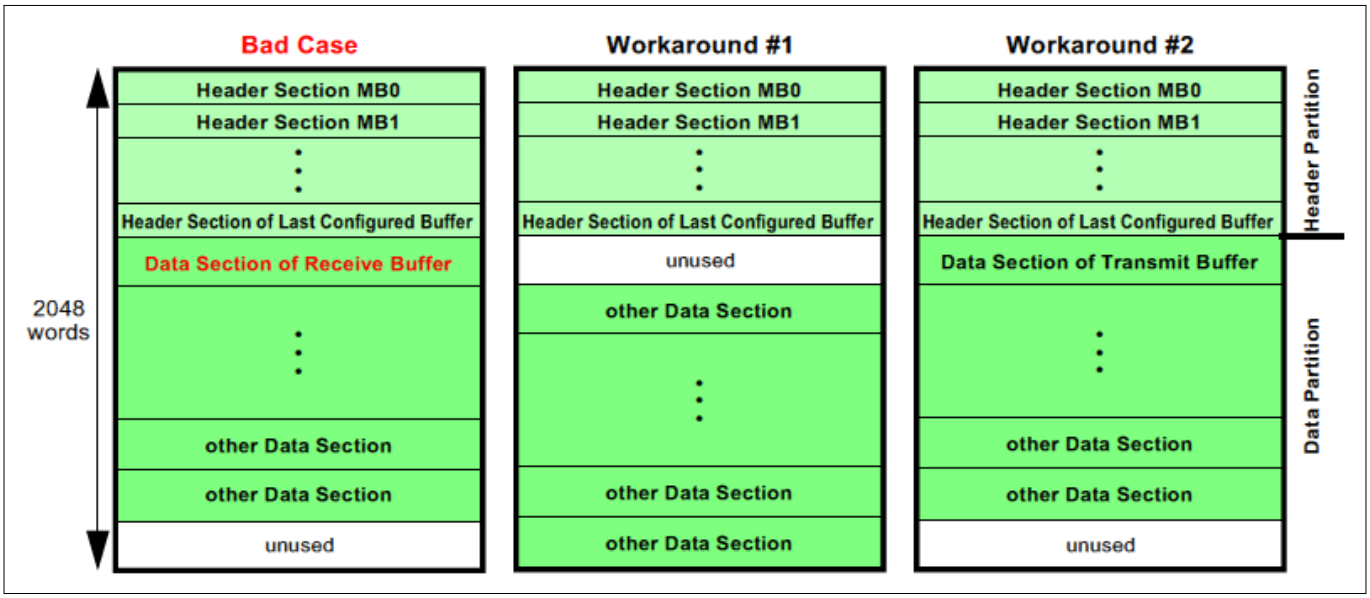

Figure 3 Message RAM configurations

2.89 [GTM_AI.139] ATOM SOMC mode: forced update does not activate comparison

Description

Under following configuration:

- ATOM SOMC mode
- ARU_EN=1
- no comparison active (bit DV in register ATOM[i]_CH[x]_STAT = 0)

If in this case a late update is tried by first setting WR_REQ (see register ATOM[i]_CH[x]_CTRL), then updating SRx register and maybe ACB control bits in register ATOM[i]_CH[x]_CTRL and finally updating the CMx register via a forced update, the register CMx are updated correctly but no new comparison is activated.

The ACBO bits are erroneously not cleared.

The ARU read request is canceled because of WR_REQ=1.

Scope

ATOM SOMC mode.

Effects

In the described case, the ARU read request is canceled but no new comparison with new CMx register values is activated.

The system may stick in waiting for late update event to happen.

The ACBO bits are erroneously not cleared.

Workaround

After the forced update write additionally by CPU the new desired value of CM0 or CM1 to corresponding work register CM0 or CM1 to activate comparison and to reset ACBO bits.

2.90 [GTM_AI.140] ATOM SOMC mode: a write access to ATOM_CH_CTRL sets WRF if CCU0 compare match already occurred but CCU1 compare match open

Description

Under following configuration:

- ATOM SOMC mode
- ARU_EN=1

For compare strategy 'serve last', if after CCU0 compare match and before CCCU1 compare match a write access to register ATOM_CH_CTRL is done, WRF bit is set independent of written bit WR_REQ.

Scope

ATOM SOMC mode.

Effects

In the described case the WRF flag may be set erroneously.

Workaround

If ATOM[i]_CH[x]_CTRL is written without the intention to set WR_REQ while there may be a comparison active on this channel x, reset afterwards erroneously set WRF flag by writing a '1' to WRF bit of register ATOM[i]_CH[x]_STAT.

2.91 [GTM_AI.141] TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TIEM, TPWM, TIPM, TPIM, TGPS

Description

In case of a TIM channel capture event issued by a rising edge at TIM[i]_CH[x]_FOUT the capturing of the TIM[i]_CH[x]_ECNT register to the TIM[i]_CH[x]_GPRi register is incorrect. The captured value will be ECNT_REG+2; bit 0 (signal level) will be 0. The correct operation would be to capture ECNT_REG+1; bit 1 (signal level) would be 1.

Scope

TIM.

***Note**: The effects described below related to the ARU do not apply to TC23x .. TC21x devices (no ARU is implemented).*

Effects

a) Inconsistency of ARU signal level bit and bit[0] of ARU word which shows the captured ECNT.

b) Reading of TIM[i]_CH[x]_GPRi shows inconsistency when comparing bits [31:24] to [7:0]. At the point in time of capture event the bits [31:24] contain the correct value and are subject to be changed with new incoming edge.

Workaround

a) When using captured data via ARU routing the correct data can be reconstructed by:

IF ARU_SIGNAL_LEVEL ==1 AND ARU_DATA[0] == 0 THEN ARU_DATA = ARU_DATA -1;

b) When reading TIM[i]_CH[x]_GPRi by configuration interface the data can be corrected as long as there is no GPR overflow and no new edge by:

IF TIM[i]_CH[x]_GPRi[24] == 1 AND TIM[i]_CH[x]_GPRi[0] == 0 THEN TIM[i]_CH[x]_GPRi[23:0] = TIM[i]_CH[x]_GPRi[23:0] -1

2.92 [GTM_AI.142] TIM: Incorrect data captured to GPR registers and routed via ARU when EGPRi_SEL,GPRi_SEL= 100 in TIM channel mode TBCM

Description

In case of a TIM channel capture event issued by an input pattern match to condition TIM[i]_CH[x]_CNTS the capturing of the TIM[i]_CH[x]_ECNT register to the TIM[i]_CH[x]_GPRi register can be incorrect. Starting at t=0 with counter value ECNT_REG(t=0), the captured values of two consecutive edges can be ECNT_REG(t=0)+2 followed by ECNT_REG(t=0)+2 instead of ECNT_REG(t=0)+1 followed by ECNT_REG(t=0)+2.

Scope

TIM.

***Note**: The effects described below related to the ARU do not apply to TC23x .. TC21x devices (no ARU is implemented).*

Effects

a) In 2 following ARU transfers the ARU word which shows the captured ECNT do not increment by 1.

b) Reading of TIM[i]_CH[x]_GPRi shows inconsistency between [31:24] and [7:0]

Workaround

a) Ignore captured data via ARU and build with MCS independent counter which increments on each ARU transfer.

b) When reading TIM[i]_CH[x]_GPRi by configuration interface use only TIM[i]_CH[x]_GPRi[31:24] as EDGE counter; don't use TIM[i]_CH[x]_GPRi[23:0].

2.93 [GTM_AI.143] GTM_TOP level: AEI pipelined write to GTM_BRIDGE_MODE register directly after setting aei_reset='0' can result in blocking of AEI configuration interface

Description

If the GTM bus bridge is reset with aei_reset= '0' (this means reset by application or module/kernel reset) and the next AEI transfer is a write command to GTM_BRIDGE_MODE register the AEI configuration interface can be blocked.

Scope

AEI pipelined protocol.

Effects

GTM Bus interface does not issue aei_ready which could lead to bus timeout of the serving bus master.

Workaround

Ensure that after setting aei_reset to inactive state (this means after resetting the GTM by application or module/kernel reset) the next command must be a read to any other register except GTM_BRIDGE_MODE. Issue desired write to GTM_BRIDGE_MODE register afterwards.

2.94 [GTM_AI.146] ATOM SOMC mode: compare match does not clear WR_REQ

Description

If an ATOM channel is operating in SOMC mode, ARU is enabled and, initiated by setting WR_REQ=1, a late update of CM0/CM1 register and/or compare strategy (i.e. ACB[4..0]) was successfully done, then, after final compare match the WR_REQ bit should be reset.

This is erroneously not done.

Scope

ATOM SOMC mode.

Effects

In the described case the bit WR_REQ is not reset. As a result no new ARU read request is set up after final compare match.

Workaround

Reset WR_REQ by software after late update (after forced update).

2.95 [GTM_AI.150] TIM: Valid edge after Timeout

Description

Assume that a TIM timeout event triggers an ARU write request with timeout information ACB2=1 and ACB1=0. If this request is acknowledged by the ARU while a new valid edge occurs, the valid edge is neither signalized by setting the bits ACB2=1 and ACB1=1 within the acknowledged transfer nor by setting up a new subsequent ARU write request for the new valid edge with ACB2=0 and ACB1=0.

Scope

TIM timeout detection in combination with ARU transfers.

Effects

If a valid edge occurs after a timeout event, the valid edge is not signalized reliably via the ACB bits over the ARU.

Workaround

The workaround for this issue requires an additional plausibility check within the MCS or CPU via FIFO:

1. Always store the received data ARUDATA(47:0)n and ACB0n in temporary variables
2. If an ARU transfer with ACB2n+1=1 and ACB1n+1=0 is received also check the following:
   If ACB0n+1 ≠ ACB0n OR ARUDATA(47:0)n+1 ≠ ARUDATA(47:0)n then a timeout with subsequent valid edge has occurred, which means ACB1 must be corrected to 1

2.96 [GTM_AI.152] DPLL: THVAL value not immediately available at inactive trigger slope

Description

According to the specification chapter x.16.8.6[2] it is specified that “for each invalid trigger slope....store this value to THVAL”. The value THVAL is calculated correctly but this value is stored into the THVAL memory location with every new active edge of the trigger signal.

Scope

DPLL storage of value THVAL into memory.

Effects

The value THVAL is not available in the memory at the specified point in time.

Workaround

If the THVAL value is needed immediately with the inactive trigger edge it is necessary to calculate the THVAL value by an TIM_CHO/1 to obtain the active and inactive slopes in input event mode. With this timestamps the CPU is able to calculate the time span within the CPU.

2.97 [GTM_AI.153] TIM: Incorrect data captured to CNTS register when TIM channel operates in mode TPWM or TPIM and CNTS_SEL = 1 and selected CMU_CLK ≠ sys_clk

Description

In case of CNTS_SEL = 1 and TIM_MODE = TPWM or TPIM in the CNTS_REG register the value of TBU_TS0 shall be captured. This does not happen when the selected CMU_CLK ≠ sys_clk.

Scope

TIM.

2 Section “Scheduling of the Calculation”, Table “State description of the State Machine”

Effects

Unexpected values in CNTS_REG.

Workaround

Setup the TIM channel to operate on a CMU_CLK (Divider =1) which is identical to sys_clk. Please notice that the measurement with TIM_CNT has resolution of sys_clk.

2.98 [GTM_AI.154] TOM: Incorrect duty cycle in PCM mode (bit reversed mode)

Description

The generated duty cycle on the TOM output in PCM mode is always one smaller than the configured value in the CM1 register. So if the value 1 is configured, a duty cycle of 0% will be generated. Configuring the max value (0xFFFF) in the CM1 register results in a duty cycle of max-1. Expected is 100% duty cycle in this case. A zero in CM1 register results in 100% duty cycle.

Scope

TOM.

Effects

Unexpected duty cycle in PCM mode.

Workaround

Configure always the value for the expected duty cycle in the CM1 register with expected duty cycle + 1.

To get 0% duty cycle, value 1 has to be configured. To get 100% duty cycle, 0 has to be configured to CM1 register while CM0 is always configured with max. value of 0xFFFF. Configuring CM0=0x1000 and CM1=0xFFFF will also get a duty cycle of 100%.

2.99 [GTM_AI.158] DPLL: Reset of pcm1/pcm2 bits in relation to an interrupt

Description

The PCM1/2 bits are reset after the correction values MPVAL1/2 are used to calculate the number of sub_incs for the next increment and to calculate the add_in values. See specification chapter x.16.8.6[3)] (States 5, 25). The problem is that the PCM1 bit is transferred with an active edge into the dedicated shadow registers, but cleared some time later. If the PCM1/2 bits are written by the CPU in between the point of time of the transfer to the shadow register and the point of time were the PCM1/2 bits are cleared, the bits are cleared and never used. This is not what one should expect from a properly defined user interface and to prevent additional expenditure to calculate the correct point of time for writing the PCM1/2 bits.

From application point of view the desired behavior is that the PCM1/2 bits are cleared when transferred to their shadow registers (not in state 5, 25). The proposed workaround would fit to this described modification.

Scope

DPLL.

3 Section “Scheduling of the Calculation”, table “State description of the State Machine”

Effects

When the PCM1/2 bits are written in the critical timeframe the bits are cleared before they are used.

Workaround

The point of time when the PCM1/2 bits are written by the CPU must be around 750 system clocks after the TASI interrupt. This time could be derived by a GTM resource like an ATOM channel.

2.100 [GTM_AI.161] DPLL MTI/TORI-IRQ's are not activated when low_res='1' and ts0_hrt='1'; MSI/SORI-IRQ's are not activated when low_res='1' and ts0_hrs='1'

Description

The DPLL Interrupts MTI/TORI are not raised when the DPLL is configured with low_res='1' and ts0_hrt='1' when the upper three bits of the tbu_ts0 are not equal to “000”.

The DPLL Interrupts MSI/SORI are not raised when the DPLL is configured with low_res='1' and ts0_hrs='1' when the upper three bits of the tbu_ts0 are not equal to “000”.

Scope

DPLL in mode low_res='1' and tso_hrt='1' ts0_hrs='1'.

Effects

When this effect is activated by the configuration and when the upper tbu_ts0 bits are not equal to “000” the interrupts MTI/TORI or MSI/SORI are not activated. A consequence of this is that the lock1/2 bits and the mti/msi flags in the DPLL_STATUS register are not operating correctly.

Workaround

Don't use the configuration low_res='1' and ts0_hrt='1'.

The signals are working correctly for the configurations low_res='0' and low_res='1' and ts0_hrt/s='0'.

2.101 [GTM_AI.162] DPLL: Input signal (active edge) which is ignored by PVT-check occurring at a gap in the profile or a lost input signal causes that the MTI_IRQ is not activated

Description

The DPLL interrupt MTI_IRQ is not raised when:

- a) during a gap in the profile an active input signal edge is ignored by the PVT check
- b) the input signal is getting lost after an active input signal edge is ignored by the PVT check

Scope

DPLL.

Effects

For the gap where the described situation occurs the MTI interrupt is not activated. In this moment the lock1/2 signals are unaffected. The possible problem is that in case of monitoring the DPLL synchronization for example with the use of the MTI_IRQ in a gap such monitoring may report a synchronization problem which is not real.

A lost input signal can not be detected because no interrupt will be generated.

Workaround

The violated PVT check is reported by the activation of the PWI interrupt. This interrupt can be used to check if a gap condition in the profile or a lost input signal has occurred. This information can be used to correct the wrong information out of the DPLL.

2.102 [GTM_AI.163] TIM: timeout signaled when TDU unit is reenabled

Description

In the following situation an undesired timeout event is signaled:

After stopping the TDU the TO_CNT bit-field will have an arbitrary value TO_CNT0 <= TOV0 bit-field. Assume TOV will be reconfigured to value TOV1 with TOV1 <= TO_CNT0. If the TDU will be enabled again by writing to TOCTRL a value !=0 and at the same time the TCS selected CMU_CLK has an active edge an unintended timeout is signaled. This results due to the fact that for one clock cycle TO_CNT0 >= TOV1.

Scope

TIM.

Effects

Unexpected timeout event when TIM TDU is enabled.

Workaround

If TDU unit has to be reenabled with a TOV value TOV1 which is less than the previous one in use TOV0 (2 alternatives are available):

a) Wait with disabling TDU until condition TOV1 > TO_CNT is fulfilled. Configure TOV with TOV1 reenable TDU Unit.

b) Disable TDU; if TOV1 <= TO_CNT write TOV with FF_H; enable TDU unit; reconfigure TOV to desired value TOV1.

2.103 [GTM_AI.164] TIM: capturing of data into TIM[i]_CH[x]_CNTS with setting CNTS_SEL=1 not functional in TPWM and TPIM mode

Description

If CNTS_SEL=1 is selected and a new input edge is signaled by the TIM Filter unit while the selected CMU_CLK has no rising edge the register TIM[i]_CH[x]_CNTS will capture data TIM[i]_CH[x]_CNT instead of TBU_TS0.

Scope

TIM.

Effects

Captured data in TIM[i]_CH[x]_CNTS is not as expected.

Workaround

a) Select with CLK_SEL a CMU_CLK which is identical to sys_clk (clock divider=1 applied in CMU channel and for global fractional divider).

b) Use TIEM mode to capture TBU_TS0 for rising and falling input edges.

c) PWM mode: Use CNTS_SEL=0 with CMU_CLK source selected as in use for TBU_TS0 counting. Capture with EGPR0_SEL=0, GPR0_SEL=0 in GPR0_REG TBU_TS0 and with EGPR1_SEL=0, GPR1_SEL= 3 in GPR1_REG CNT. Calculate the desired timestamp with GPR0_REG - GPR1_REG + CNTS_REG.

2.104 [GTM_AI.166] DPLL: The content of registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext is added independently of the state of DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status to the pointers apt_2b/aps_1c2

Description

If during synchronization the registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext are loaded with non-zero values they are added to the pointers apt_2b/aps_1c2 independently from the status of the control bits DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status. Correctly this should happen only when the control signals DPLL_apt_sync.APT_2b_status or DPLL_aps_sync.APS_1c2_status are set to “1”.

Scope

DPLL.

Effects

Wrong status of pointers apt_2b or aps_1c2 after synchronization has been executed.

Workaround

If the pointers apt_2b/aps_1c2 should remain unchanged after synchronization the registers DPLL_apt_sync.APT_2b_ext and DPLL_aps_sync.APS_1c2_ext must be set to zero before synchronization is performed.

2.105 [GTM_AI.167] ATOM SOMP mode: for RST_CCU0=1 and ARU_EN=1, if CN0 reaches CM0 an update of the register SRx is requested

Description

For the configuration ATOM SOMP mode, ARU_EN=1, RST_CCU0=1 an update of SR0/SR1 register via ARU is requested erroneously any time CN0 reaches CM0.

Because of RST_CCU0=1, if CN0 reaches CM0, CN0 is not reset but counting until it is reset be the trigger of a preceding channel. Therefore, it may not be the end of a period if CN0 reaches CM0.

The expected point in time for a new ARU read request to update the shadow register SR0/SR1 would be the trigger to reset CN0 which triggers also the update of CM0/CM1 with the value of SR0/SR1.

Scope

ATOM SOMP mode.

Effects

For the described configuration, the ATOM channel requests and updates the SR0/SR1 register not only after the update of CM0/CM1.

Depending on time between CM0 of this channel and the value of CN0 in case of reset by the trigger, the SR0/SR1 register may be updated two times between two triggers to reset CN0.

In case of ARU_EN=1, means the update of SR0/SR1 is requested via ARU, if CM0 is greater than the end value of CN0 before it is reset by trigger, no further update via ARU is requested because CN0 never reaches CM0.

Workaround

1. If new data via ARU is provided by FIFO, avoid for ATOM SOMP mode the combination of configuration ARU_EN=1 and RST_CCU0=1
2. If new data is provided by MCS, ensure by MCS that only one time per period new data for SR0/SR1 register can be read. This can be reached by starting the 'master period' which triggers the reset of CN0 on a time base value and provide to the MCS the start value and the period. Then, the MCS can calculate a time for providing new ARU data

2.106 [GTM_AI.168] DPLL: CPU read / write accesses to RAM2 in competition to DPLL accesses to RAM2 may lead to wrong SYN_T data read by DPLL

Description

If at a dedicated point in time during sub increment calculation the DPLL TRIGGER processing unit reads a profile value out of RAM2 and in competition a second read/write operation is scheduled on the RAM2 via CPU/DMA interface, there is a dedicated state and signal constellation that leads to the effect that the RAM2 output data belonging to the CPU/DMA access is used as read data for the internal TRIGGER processing unit. This can lead to a wrong internal syn_t, syn_t_old value leading to a desynchronization of the DPLL. The desynchronization can be detected if the missing trigger interrupt (MTI-irq) is activated together with a suitable parameter TOV.

Scope

DPLL.

Effects

DPLL TRIGGER processing unit reads out from RAM2 wrong syn_t, syn_t_old data. As a result sub increment calculations of the DPLL are wrong.

This leads to loss of synchronization. Further observations are corrupted data in the TSF_T data field of RAM2 as a consequence of the desynchronization.

Workaround

The application SW has to avoid any access (CPU or DMA) to DPLL RAM2 in the time window starting with the active TRIGGER edge and ending with the TASI interrupt.

Workaround 1

Synchronization of CPU/DMA accesses to phases where DPLL is not accessing RAM2.

This can be reached by synchronizing DPLL RAM2 accesses to TRIGGER signal using the TASI interrupt and checking continuously if the RAM2 access is finished before next active TRIGGER edge.

As an alternative for TASI interrupt one can start with the TIM0_CH0 active edge interrupt an ATOM pulse (SOMP mode, one shot mode) of the length 200 SYS_CLK periods. With the CCU1 interrupt of the ATOM channel the critical phase of DPLL internal RAM2 accesses is finished and now the CPU/DMA can access DPLL RAM2.

Workaround 2

Asynchronous CPU/DMA accesses to phases where DPLL is not accessing RAM2.

This can be achieved by using MCS to calculate and set flags that indicate the uncritical phase of DPLL RAM2 accesses.

2.107 [GTM_AI.169] DPLL: no TORI/SORI interrupt in case low_res = 1 AND ts0_hrt/s = 0

Description

If the described configuration is chosen there is no TORI/SORI interrupt raised at all.

Scope

DPLL.

Effects

The TORI/SORI interrupt is not coming in that configuration.

Workaround

For the configuration low_res=1 and ts0_hrt/s = 0 use TOM or ATOM to generate an interrupt on time out of TRIGGER/STATE:

With every TRIGGER/STATE edge adapt (A)TOM period to current speed and reset CN0. If CN0 is not reset by next TRIGGER/STATE event, (A)TOM raises an edge interrupt at the end of the period.

2.108 [GTM_AI.170] DPLL: Action calculation: requested action not always calculated immediately

Description

If the action calculation by DPLL was interrupted due to a new input event it may happen that with the next TRIGGER/STATE input event, after sub increment calculation is finished, the action calculation starts again at the same internal action number which has been interrupted before. If in between new action data arrives where the action number is above the currently calculated action this new action data is only calculated after the next input event. The reason for that behavior is that if action calculation was interrupted the action calculation starts with the internal action address which was stored at the end of the event cycle before. New PMT data for action with higher action number are not recognized. The action calculation stops if the action number zero is reached.

Generally: The calculation of sub increments and PMT cannot be done in parallel due to resource sharing. This leads to the behavior that PMT calculation is interrupted if a new input event (TRIGGER/STATE) occurs.

When DPLL is doing the action calculations the DPLL has exclusive access rights to RAM1a which contains the PMT request values. Then the DPLL cannot accept new PMT requests via ARU.

Scope

DPLL.

Effects

Requested actions are not calculated regularly with every tooth (as long as they are not in the past).

Workaround

Request actions which are not “past” so far with every new tooth. The synchronization of the MCS task to TIM input event can be done by routing the TIM edge capture event value via ARU to MCS.

Then, if new PMT data is arriving after the action number has reached the value zero, the action is calculated immediately starting with the highest action number again.

As a workaround one can request the action calculation tooth by tooth until action runs into past. An additionally PMT request can be placed earlier after new input event (TRIGGER/STATE) while DPLL is doing sub increment calculations because then RAM1a can be handled exclusively for updating PMT requests via ARU.

Generally it is recommended to sent PMT requests at least 3 teeth before action has to be executed. This ensures that even under presence of the erratum the MCS, ATOM are getting calculated action results at least from a calculation of the action in an input event cycle before.

2.109 [GTM_AI.172] TIM: overflow bit in TIM ARU data not set; signal level bit in ARU data has opposite value

Description

Relevant mode TIEM with ISL=1 and ARU_EN=1.

In case of 2 input signal changes with distance smaller than ARU routing time the overflow Bit ACB1 might not be set.

The erroneous behavior occurs, if an edge (first_level) starts an ARU transfer and one system clock before the ARU request is serviced the input signal changes (! first_level). In this case the overflow bit ACB1 is not set (keeps ACB1=0), and the signal level bit ACB0 will be incorrect ACB0= first_level.

Note that the irq_notify(3) bit (gpr_overflow) is set correctly.

Scope

TIM.

Effects

The overflow information in the ARU ACB1 bit is not set, ARU ACB0 signal level incorrect.

Workaround A

Ensure with TIM filter that input signal changes smaller than ARU Routing Time will be removed. Configure FLT_FE/FLT_RE with filter delay which is greater than ARU Routing time.

Workaround B

Select ECNT or CNT to be transferred in ARU_DATA. Next is shown a pseudo code which can be used as a workaround:

```
Last_CNT = -1
For each ARU_DATA
 If ARU_DATA(ACB1) ==0
  If Last_CNT != -1
   If Last_CNT+1 != ARU_DATA(CNT)
    Message(Hit on ERRATA: Detected overflow condition)
   ARU_DATA(ACB1) = 1
  ARU_DATA(ACB0) = not ARU_DATA(ACB0)
 else
  Message(No signal level present yet, cannot apply workaround)

Last_CNT = ARU_DATA(CNT)
```

2.110 [GTM_AI.173] DPLL: new PMT data not received

Description

The root cause of the problem in a dedicated constellation of time is an action calculation with the result “past” although a pending data transfer to the DPLL via ARU with new input data on the same PMT channel cannot be

executed. So the data transfer of the new action data starts after the action calculation so that first the action is finished for example with the result past before the new input data can be used.

When the DPLL receives PMT requests after a new input slope, only that requests can be considered, which are transferred during a simple ARU routing cycle. The DPLL blocks new PMT requests when there is a time of about 200 ns since the last PMT request is passed. New PMT requests are only accepted after the calculation of the pending action calculations are performed. This calculation starts in step 13 (33) of the state machine, about 10 µs after the input event and ends depending on the number x of actions to be calculated x*3.7 µs later. After this time a single new PMT request is accepted, but there is no possibility to stop an action calculation with an update of data. The “old” value is always calculated.

Scope

DPLL.

Effects

PMT result calculated on “older” PMT input data because a pending data transfer with newer input data to the DPLL cannot be executed.

Workaround

When the calculated action is transmitted to the MCS check, if there is a ARU transfer with new data of this action was blocked by the ARU, because the DPLL was not ready to receive new data within these increment. Also in the case the ARU transfer was just performed, the corresponding action contains only the “old” PMT requirements. Ignore this action value and wait for the new value which appears about 3.7 µs after the PMT requirement update was transmitted.

New action values relating to new PMT requests are considered in the states 18 to 20 (38 to 40) of the state machine. Typically one PMTR update is transmitted and then corresponding action is calculated until a new PMTR is accepted (when not transmitted in a block with directly succeeding ARU transmissions).

2.111 [GTM_AI.174] DPLL: PMT result not sent to ARU

Description

The root cause for the problem is that before reaching a dedicated state of the DPLL there is a gap in time in which the DPLL.act_n(i) bit of an action is reset before the act_n_shd_reg signal (shadow register) is set to “1” which starts the transfer of the output data via ARU. If in this gap a new input event is arriving the act_n(i) and the internal state controller changes to the processing of this new input event the signal act_n_shd(i) is not set and so there is no request for transmitting the output data to the ARU placed. This leads to the situation in which an action calculation is finished without transferring the data via the ARU. PMT calculations were the result is not “PAST” are not affected by this issue. The time frame in which a incoming input signal is causing the misbehavior is about 25 system clock cycles.

Scope

DPLL.

Effects

The results of a PMT calculation are not transferred to their target. This can only happen if the result of the PMT is “PAST”.

Workaround

In general a workaround has to take into account that a message ending in “past” is going to have the issue when during action calculation at a dedicated point of time a new input event occurs.

For the MCS program it is therefore necessary that the MCS program is reading the PMT data from DPLL via non blocking ARU reads to prevent that the MCS program is blocked. Additionally, the MCS program should make

inside the loop that is doing the non-blocking ARU reads a plausibility check if the requested action is 'out of time' or 'out of angle'.

The MCS can read at any time from TBU the time base tbu_ts0 and the angle from tbu_ts1/tbu_ts2. This information should be used to determine if there is a requested action pending or out of date. If the MCS program did not get back a result in the expected time window, it could either request the old value again or, if the requested event is in the past, request a new value.

Additionally the TIM0 interrupt could be routed to the MCS to check if an active edge occurred. In this case all actions which delivered a result so far must not be checked again independently if their result was “PAST” or not.

If the PMT is used such that the PMT result is transferred directly from the DPLL to the ATOM, there should be a default assignment to the ATOM which is not in PAST to make sure that, even if the DPLL fails to sent the PMT result to the ATOM, the ATOM is not missing an event completely.

2.112 [GTM_AI.178] MCS: Evaluation of CAT bit after blocking ARU instruction

Description

The specification for the instructions ARD, AWR, ARDI, and AWRI claims that the CAT bit can be evaluated by the MCS program in order to check if the last ARU transfer was successful (CAT=0) or cancelled by Software (CAT=1). However, since the CAT bit can be set directly by Software to cancel an ARU transfer at any time the bit does not reflect the status information reliably. Bad case: If the CPU software is setting CAT between the time of ARU data arrival and evaluation of CAT bit.

Scope

MCS.

Effects

If the mechanism for cancelling blocking ARU transfers by CPU is used the MCS may signalize an aborted ARU transfer by a set CAT bit although the transfer has finished successfully.

Workaround

If the mechanism for cancelling blocking ARU transfers by CPU is used and data consistency by ARU transfers is important, a possible workaround may check the consistency by inspection of the transferred data (for example checking for linear increment of ECNT for data transfers from TIM to MCS).

2.113 [GTM_AI.181] TIM: Incorrect signal level bit ECNT[0] in mode TIEM, TPWM, TIPM, TPIM, TGPS

Description

In case of re-enabling a previously disabled TIM channel the bit ECNT[0] might not reflect the actual signal level of the corresponding input TIM[i]_CH[x]_FOUT until the next input edge occurs. This situation can only occur if between disabling and re-enabling the ECNT register is not read.

Scope

TIM.

Effects

Inconsistency of input signal level with ECNT bit[0].

Workaround

- After disabling the TIM channel, ensure that the ECNT register is read at least once and afterwards the TIM channel can be re-enabled
- Before re-enabling a TIM channel, issue a TIM channel reset and reconfigure the TIM channel control registers

2.114 [GTM_AI.202] (A)TOM: no CCU1 interrupt in case of CM1=0 or 1 and RST_CCU0=1

Description

In case of channel x has configuration of RST_CCU0=1 (i.e. CN0 is reset by trigger input) and CN0 counts from 0 to MAX:

- if CM1=0, CM0>0 -> no CCU1 interrupt is generated
- if CM1=1, CM0=MAX+1 -> only one time a CCU1 interrupt is generated

Scope

TOM / ATOM SOMP mode.

Effects

For the described configuration no CCU1 interrupt is generated.

Workaround

Use for triggering channel y (i.e. the channel that triggers on channel x the reset of counter CN0) the configuration of CM0=MAX, CM1=1.

In case of duty cycle configuration of CM1=0 and CM0>0 on channel x use instead of CCU1 interrupt on channel x the CCU0 interrupt of triggering channel y.

In case of duty cycle configuration of CM1=1 and CM0=MAX+1 on channel x use instead of CCU1 interrupt on channel x the CCU1 interrupt of triggering channel y.

2.115 [GTM_AI.204] TIM: incorrect signal level on TIM_MODE change if TIM channel is disabled

Description

If TIM_EN=0 and TIM_MODE=”100” (TBCM) and corresponding channel input signal is high any write of TIM_MODE!=”100” while TIM_EN=0 will not update the signal level bit ECNT[0]. Expected operation is that ECNT[0] will be set to the actual channel input value on TIM_MODE change.

Scope

TIM.

Effects

Unexpected signal level.

Workaround

Never set unnecessary TIM_MODE=”100” followed by TIM_MODE!=”100” while TIM_EN=0.

2.116 [GTM_AI.205] TIM: unexpected CNTS register update in TPWM OSM mode

Description

If OSM=1 and TIM_MODE=”000” (TPWM) an active edge defined by DSL will stop the measurement. In case of an inactive edge following after 1 GTM system clock cycle the active edge the CNTS register will be reset unexpected.

Scope

TIM.

Effects

Unexpected CNTS register content.

Workaround

a) Use CMU clock in TIM channel with frequency lesser than system clock.

b) Enable filter and configure filter parameter in a way that two consecutive edges will never occur with distance of GTM system clock.

2.117 [GTM_AI.208] DPLL: Start of sub-increment generation and action calculation delayed by one input event if PCM1/2 bits are set and DPLL_STATUS.FTD = '0'

Description

The DPLL is delaying the start of sub-increment generation and the action calculation by one input event cycle if the DPLL starts after activation (DPLL_CTRL1.DEN= 0 ->1) when the flag DPLL_STATUS.FTD = '0'. In these situations and when additionally PCM1/2 was activated just before or remains (DPLL_CTRL1.PCM1/2 = '1') the sub-increment generation is starting delayed by one input event cycle.

This results in a wrong state of the TBU_TS1 angle clock. The start of action calculation (PMT) could be delayed by one input event cycle as well.

Scope

DPLL.

Effects

Delayed start of sub-increment generation and action calculation (PMT) by one input event.

Workaround

The issue can happen only when the DPLL starts after activation (DPLL_CTRL1.DEN= 0 ->1) when the Flag DPLL_STATUS.FTD = '0'. In these situations and when additionally PCM1/2 was activated just before (DPLL_CTRL1.PCM1/2 = '1') the DPLL_CTRL1.PCM1/2 bits must be set to '0' before the DPLL is activated again.

2.118 [GTM_AI.209] TOM/ATOM: no update of CM0/CM1/CLK_SRC via trigger signal from preceding instance if selected CMU_CLKx is not SYS_CLK

Description

The trigger signal between (A)TOM instances (for example signal TOM_TRIG_[i]) is registered between each TOM and between each 2nd ATOM and with this delayed by one SYS_CLK period to break long combinational path.

For each register in the trigger path between (A)TOM instance i and the succeeding (A)TOM instance i+1, this trigger from instance i does not trigger the update of register CM0, CM1 and CLK_SRC with content of SR0, SR1 and CLK_SRC_SR if the triggered channel of instance i+1 is not running with a selected CMU_CLKx = SYS_CLK.

Scope

TOM/ATOM.

Effects

In the described configuration no update of CM0, CM1 and CLK_SRC is done although the update is enabled by register TOM[i]_TGC[y]_GLB_CTRL / ATOM[i]_AGC_GLB_CTRL.

Workaround

For each register in trigger path between (A)TOM instance i and (A)TOM instance i+1, the channel of instance i+1 that should be triggered has to use a clock of period identical to SYS_CLK period.

A second workaround could be to set up on instance i+1 a redundant channel to trigger other channel of instance i+1 like it was set up on instance i to trigger other channel. Then, start both instances synchronously by using the TBU time base comparator of AGC/TGCx unit (i.e. the ATOM[i]_AGC_ATC_TB / TOM[i]_TGC[y]_ACT_TB register).

2.119 [GTM_AI.210] ATOM: data loss in SOMS one-shot mode if ARU is enabled and the period of the selected CMU_CLKx is greater than ARU-cycle-time/2

Description

ATOM in SOMS one-shot mode starts to request new data from ARU with ARU_EN = 1. If new data is delivered by ARU and stored into SR0/1 register, the data will be transferred to CM0/1 register and the ATOM starts to shift with next selected CMU_CLKx. In parallel ATOM requests immediately new data from ARU. If ARU will deliver next data before the first bit of the first data is shifted out which means before the next CMU_CLKx takes place, the data will be stored into SR0/1 register but it will not be marked as valid (bit DV not set) and therefore it will be ignored.

Scope

ATOM.

Effects

Delivered data from ARU is not marked as valid (bit DV not set) and will be ignored.

Workaround

It has to be ensured, that the time between delivering of two new data from ARU is greater than CMU_CLKx periods. This can be reached by delivering the data by MCS instead of by FIFO.

The issue can only occur if the ARU roundtrip time is greater than 2 CMU_CLKx periods.

2.120 [GTM_AI.212] F2A: stream data register will not be deleted after disabling stream

Description

Disabling a data stream inside the F2A will not delete existing valid data inside F2A. So after re-enabling the disabled stream, F2A will deliver the old data - independent of the configured data transfer direction.

Scope

F2A.

Effects

Delivering unexpected data by F2A after stream enable.

Workaround

Before enabling a data stream, the F2A has to be emptied. After disabling the stream, the ARU read address has to be set to reset value 0x1FE (always empty address). Then the F2A stream has to be configured into the direction ARU to FIFO. After this the stream can be enabled, so that old data will be transported into FIFO. At last the FIFO channel should be flushed.

2.121 [GTM_AI.215] FIFO: read pointer will be incremented in ring buffer mode on empty FIFO channel with read access from AFD_CHx_BUF_ACC

Description

If an empty FIFO channel x is configured into ring buffer mode an then a read access to AFD_CH[x]_BUF_ACC is executed, the read pointer of this FIFO channel x will be incremented.

Scope

FIFO.

Effects

FIFO channel delivers undefined data to ARU.

Workaround

There are 2 possibilities to avoid this erratum:

1. Do not execute a read access to AFD_CH[x]_BUF_ACC after setting the corresponding FIFO channel into ring buffer mode while the FIFO channel is empty.
   In general there are no real application to read a FIFO channel from CPU side (AFD_CH[x]_BUF_ACC) while the FIFO channel is in ring buffer mode
2. Do not set a FIFO channel into ring buffer mode while the FIFO channel is empty. First fill the FIFO channel and afterwards configure them into ring buffer mode

2.122 [GTM_AI.218] DPLL: PWI-IRQ permanently activated

Description

When the DPLL is activated (DPLL_CTRL_1.den= '1') and after that
a) the register DPLL_CTRL_0 is written and

b) the STATE input signals (emergency mode) is activated,
it happens that after the activation of the PWI-IRQ (active input signal event is rejected by negative PVT check) the PWI-IRQ is again and again activated.

Scope

DPLL after reactivation.

Effects

PWI-IRQ permanently activated.

Workaround

The issue can happen only when the DPLL starts after activation (DPLL_CTRL1.DEN= 0 ->1) when the control register DPLL_CTRL_0 is written after that. If this is prevented the issue will not occur.

2.123 [GTM_AI.219] DPLL: Wrong internal pointer calculation in case of backwards direction can lead to wrong PMT calculation results (PMT in PAST)

Description

A DPLL internal pointer register is calculated wrong in backwards direction. In this case the PMT calculations leading to wrong results for example PMT in “past”. This can only happen in backwards direction.

Scope

PMT computation of GTM/DPLL in backwards direction.

Effects

Wrong PMT computation results by DPLL when DPLL is operating in backwards direction.

Workaround

Combustion engine:
a) don't use PMT calculation in backwards direction.
or
b) If PMT calculations needed even in backwards direction the PMT results must be sent from DPLL to MCS to verify that PMT result is not erroneously in PAST before sent to ATOM.

2.124 [GTM_AI.220] DPLL: PVT check is deactivated in case of direction change; Behaviour implemented but not documented in specification so far

Description

The behaviour that the parameter PVT is set to zero after a direction change has occurred is implemented but so far not described in the specification in an adequate manner.

Scope

DPLL-PVT parameter.

Effects

Described and implemented behaviour not documented in specification.

2.125 [GTM_AI.221] DPLL: Possible inconsistency of internal pointers and parameter NUTE/NUSE when NUTE/NUSE modified in dedicated time window

Description

The parameters NUTE/NUSE are DPLL internally used to modify pointers as well as to decide which data to be used for doing the prediction of the next increment or the selection of the algorithm of PMT calculation to be used. After a new input signal reaches the DPLL either on TRIGGR or STATE processing unit the internal pointers are updated shortly after the TASI/SASI-irq's.

If the NUTE/NUSE parameter is changed after that point of time the pointers are not updated until the next input event such that the described inconsistency may occur. This inconsistency may lead to the use of wrong data which can corrupt the results of the increment prediction and the frequency calculation as well as the calculation of PMT.

Scope

DPLL increment prediction and PMT calculation.

Effects

This inconsistency may lead to the use of wrong data which can corrupt the results of the increment prediction and the frequency calculation as well as the calculation of PMT.

Workaround

Modification of NUSE/NUTE, VTN/VSN parameters must be done in uncritical time windows:

a) after new input signal (TIM0_CH0_irq) before TASI/SASI-irq.

b) after PMT calculation has finished for a dedicated increment: for example number of active PMT (n) that small THVAL > 10µs +n*3µs; In this case the parameters NUTE/VTN may be modified after the TISI irq.

2.126 [GTM_AI.222] DPLL: TAXI-irq not deactivated for THMA=0

Description

TAXI-irq not deactivated for THMA=0; The internal interrupt signal is not set correctly such that the notify bit of the DPLL_IRQ_NOTIFY.TAXI bit can only be reset if the taxi-irq is internally deactivated with a next input event which does not cause an activation of this interrupt.

Scope

DPLL-TAXI-irq.

Effects

TAXI-irq is activated even if parameter THMA set to zero.

Workaround

Use DPLL_IRQ_EN to deactivate TAXI-irq if not needed.

2.127 [GTM_AI.223] DPLL: discontinuities in the sub increments when DPLL_NUTC/S.FST/FSS=1; set to full scale

Description

When the physical deviations are used (DPLL_CTRL_1.AMT/AMS=1) or higher accelerations are happening and at the same time NUTE/FST, NUSE/FSS are set to full scale it happens that the sub increment generation is showing irregular behaviour. This means that the pulse generator frequency is not calculated correctly which ends up in either too fast or too slow generated micro ticks.

Scope

DPLL sub increments.

Effects

Not well distributed sub increments in between two teeth.

Workaround

Don't use DPLL in “full scale” mode, when NUTE/NUSE is set to maximum and FST/FSS is set to one, when stronger accelerations exist or physical deviation with significant deviation is used.

It is possible as well that for the phase of acceleration or the place in the profile, when a physical deviation is relevant for equation DPLL-2c, DPLL_2c1 or DPLL-7c, DPLL-7c1 that just the control bit DPLL_FST/FSS is set to '0'. In this case the error calculation EDT_T, MEDT_T must be observed and checked if not getting too high. If so, this value can be modified via CPU.

2.128 [GTM_AI.247] DPLL: Input event not served after DPLL_CTRL_1.DEN is activated

Description

After the DPLL is enabled by setting DPLL_CTRL_1.DEN = 0 --> 1 there is a time frame in which a new input signal either TRIGGER (i.e. Crank) or STATE (i.e. Cam) is not recognized and not stored.

After power on reset or DPLL software reset this timeframe is about 140 clock cycles.

When the DPLL is enabled after the module was disabled the timeframe is 20 clock cycles for a STATE signal and about 45 clock cycles for a TRIGGER input signal. In case of the TRIGGER input signal the time window can be longer if there are accesses to memory RAM1b in parallel.

Each RAM1b access will lengthen the time window by 10 clock cycles.

Scope

DPLL

Effects

Input events on TRIGGER/STATE input not served, and synchronization process can take longer.

Workaround

a) Input event will be neglected, DPLL calculations will start with one event delayed.

b) Reenabling of DPLL during operation: Within the time frame after the DPLL is enabled the TIM inputs must be observed if an input event has arrived. To adopt the angle clock the missing pulses must be repeated by the PCM1/2 mechanism.

c) Reenabling of DPLL during operation: Within the time frame after the DPLL is enabled the TIM inputs must be observed if an input event has arrived. Repeat the missing event/pulses by insertion of a TIM input event by writing to configuration register TIM0_IN_SRC.

2.129 [GTM_AI.250] DPLL: DPLL_STATUS.BWD1/2 not reset after DPLL_CTRL_1.DEN = 1->0->1, when DPLL_CTRL_0 has been written some time before

Description

If the DPLL is disabled and enabled again it happens that the DPLL_STATUS.BWD1/2 flags are not reset.

There are 2 conditions in which the DPLL is disabled for a too short timeframe.

a) If no active input signal is processed in the DPLL at reenabling within a timeframe smaller than ~1,2 µs (@100 MHz GTM clk frequency or 120 system clock cycles) after the register DPLL_CTRL_0 has been written.

b) If an active input signal is processed in the DPLL at reenabling within a timeframe smaller than 8,6 µs (@100 MHz GTM clk frequency or 860 system clock cycles) after the register DPLL_CTRL_0 has been written.

Scope

DPLL

Effects

Incorrect status of DPLL_STATUS.BWD1/2 and wrong angle clock because of opposite direction dependent calculation

Workaround

When the DPLL is disabled there should be at least

a) a time of 1,2 µs or 120 system clock cycles until the DPLL is enabled again (DPLL_CTRL_1.DEN = 1), when no active input signal is processed/expected in this situation.

b) a time of 8,6 µs or 860 system clock cycles until the DPLL is enabled again (DPLL_CTRL_1.DEN = 1), when an active input signal is processed or expected in this situation.

2.130 [GTM_AI.260] TOM/ATOM: Async. update in SOMP mode with CM1=0 and selected CMU clock unequal sys_clk not functional

Description

***Note**: In **TC23x/TC22x/TC21x** devices, this problem relates to the following scenario in TOM: Async. update with CM1=0 and selected CMU_FXCLK unequal to sys_clk not functional.*

An asynchronous update of the duty cycle by writing value 0 to CM1 register while a CMU clock unequal sys_clk is selected is not working. It is expected that the output signal level is set immediately to inactive level but it will remain at actual level.

Scope

TOM/ATOM.

Effects

The output signal level is not set to inactive level. It will remain at actual level.

Workaround

Writing value 1 instead of 0 to CM1 register will set the output to inactive level in the actual generated PWM period.

If the duty cycle duration should be zero also for the following period, the user has to take care, that the CM1 register is loaded with a 0 at the beginning of the next PWM period.

Otherwise, if the content of register CM1 remains at 1, a peak of one clock cycle with the selected CMU clock will be observed, with the next PWM period.

2.131 [GTM_AI.270] (A)TOM: output signal is postponed one period for the values CM0=1 and CM1>CM0 if CN0 is reset by the trigger of a preceding channel (RST_CCU0=1)

Description

If counter CN0 is reset by the trigger of a preceding channel (bit RST_CCU0 of register TOM[i]_CH[x]_CTRL/ ATOM[i]_CH[x]_CTRL is set), then the value of CM0 defines the signal edge to SL (signal level), whereas CM1 defines the edge to !SL (inverted signal level).

If - in this case - the value 1 is configured for the output edge to SL (CM0=1) and CM1 is configured to greater than CM0 (CM1>CM0) the expected output edge will be postponed by one period.

Scope

TOM, ATOM SOMP mode

Effects

The expected output edge will be postponed by one period.

Workaround

Instead of configuring CM0=1 it is also possible to configure CM1=1 and to invert SL to get the expected edge at counter value 1 (CN0=1).

2.132 [GTM_AI.271] DPLL: No DCGI-irq after direction change and DPLL_CTRL_0 has been written

Description

If the DPLL is running in normal mode and a direction change is detected after the register dpll_ctrl_0 has been written the DCGI-Interrupt does not occur for following direction changes until both a TRIGGER and a STATE input signal has been arrived at the DPLL inputs.

Scope

DPLL

Effects

DCGI-irq does not occur.

Workaround 1

Don't write to DPLL_CTRL_0 until both an active TRIGGER, STATE input signal has occurred in case of an direction change within this time frame.

How to prevent this, under need of changes of:

- a) Need to deactivate Trigger/state input signal (replacing changes on DPLL_CTRL_0.SEN, DPLL_CTRL_0.TEN):
  - Switch according TIM input channels receiving the TRIGGER/STATE input signal by:
  - Modification of TIM[i]_CH[x]_IN:SRC.MODE[i]=”10”, VAL[i]
- b) Need to change from normal mode to emergency mode by change of DPLL_CTRL_0.RMO:
  - If this is necessary the write operation to DPLL_CTRL_0 cannot be prevented
- c) Changes of DPLL_CTRL_0.TNU, SNU. MLT:
  - Such changes should not be necessary, if not the write operation to DPLL_CTRL_0 cannot be prevented
- d) Changes of Adaption modes TRIGGER, STATE (replacing changes of DPLL_CTRL_0.AMT, AMS):
  - Activate/Deactivate AMT, AMS after power up, activate mode by writing adapt data to RAM1c PD(ADT_S) and or RAM2 PD(ADT_T)
- e) Changes of Input Delay TRIGGER,STATE (replacing changes of DPLL_CTRL_0.IDT, IDS):
  - Activate/Deactivate TIM[i]_CH[x]_CTRL.FLT_EN to enable or disable filter input data within the dedicated TIM input channel
- f) Changes of DPLL_CTRL_0.IFP:
  - If such changes are necessary the write operation to DPLL_CTRL_0 cannot be prevented

If Workaround 1 is not doable:

Workaround 2

After writing to DPLL_CTRL_0: Check for direction change by evaluating the register DPLL_STATUS.BWD1 when an inactive edge occurred on TRIGGER (TISI-irq) until both an active TRIGGER, STATE input signal has occurred.

The pulse corrections and pointer modifications of the direction change are operated correctly!

2.133 [GTM_AI.272] DPLL: No update of DPLL_RAM1b.PSTC after direction change and DPLL_CTRL_0 has been written

Description

If the DPLL is running in normal mode and a direction change is detected after the register dpll_ctrl_0 has been written the DPLL_RAM1b.PSTC value is not updated for the following active input signal and keeps the difference for the following input signals.

Scope

DPLL

Effects

Incorrect PSTC value, incorrect PMT/action results. At he tooth with the incorrect PSTC only it can be observed that the subincrements are generated at highest speed.

Workaround 1

Don't write to DPLL_CTRL_0 until both an active TRIGGER, STATE input signal has occurred in case of an direction change within this time frame.

How to prevent this, under need of changes of:

- a) Need to deactivate Trigger/state input signal (replacing changes on DPLL_CTRL_0.SEN, DPLL_CTRL_0.TEN):
  - Switch according TIM input channels receiving the TRIGGER/STATE input signal by:
  - Modification of TIM[i]_CH[x]_IN:SRC.MODE[i]=”10”, VAL[i]

- b) Need to change from normal mode to emergency mode by change of DPLL_CTRL_0.RMO:
  - If this is necessary the write operation to DPLL_CTRL_0 cannot be prevented
- c) Changes of DPLL_CTRL_0.TNU, SNU. MLT:
  - Such changes should not be necessary, if not the write operation to DPLL_CTRL_0 cannot be prevented
- d) Changes of Adaption modes TRIGGER, STATE (replacing changes of DPLL_CTRL_0.AMT, AMS):
  - Activate/Deactivate AMT, AMS after power up, activate mode by writing adapt data to RAM1c PD(ADT_S) and or RAM2 PD(ADT_T)
- e) Changes of Input Delay TRIGGER,STATE (replacing changes of DPLL_CTRL_0.IDT, IDS):
  - Activate/Deactivate TIM[i]_CH[x]_CTRL.FLT_EN to enable or disable filter input data within the dedicated TIM input channel
- f) Changes of DPLL_CTRL_0.IFP:
  - If such changes are necessary the write operation to DPLL_CTRL_0 cannot be prevented

If Workaround 1 is not doable:

Workaround 2

In this case (direction change after DPLL_CTRL_0 has been written before both a TRIGGER and STATE input event has occurred) the PSTC value has to be corrected via CPU access from outside the DPLL.

To achieve this the calculation PSTC_new=PSTC_old +/- nmb_t_tar (+ forward(dir1=0); - backward(dir1=0)) has to be performed and stored to RAM1b.PSTC earlier as 1000 system clock cycles after the active input event, or 850 system clock cycles after the TASI-irq has occurred.

The PSTC value is internally of the DPLL used for PMT calculations. If no PMT calculation is ongoing in the tooth after direction change and the PSTC value is not needed in GTM external processes the described timing constraint for the PSTC correction can be relaxed until before the next PMT calculations are requested or the PSTC value is needed otherwise.

2.134 [GTM_AI.278] FIFO: Restoring of F2A (ARU to FIFO interface) read access to FIFO after GTM_HALT condition not functional

Description

GTM_HALT is activated while the submodule F2A is executing a read access to a FIFO channel buffer.

Then the F2A read access has to be stopped and restored after GTM_HALT is deactivated.

The restoring of the F2A read access will hand back false data to F2A.

Scope

FIFO

Effects

False data are read from FIFO.

Workaround

No workaround available.

2.135 [GTM_AI.292] DPLL: pulse correction at direction change incompletely for DPLL_CTRL_1.SMC='1'

Description

Under the assumption of DPLL_CTRL_1.SMC=1 the pulse correction at direction change is done incompletely such that some pulses may be not placed immediately after the direction change. Because the status of the register DPLL_INC_CNT1/2 for automatic end mode (DPLL_CTRL_1.DMO = 0) is correct the pulses can be placed for the next active input signal event.

Scope

DPLL

Effects

Under the assumption of DPLL_CTRL_1.SMC=1 the pulse correction at direction change is done incompletely such that some pulses may be not placed immediately after the direction change.

Workaround

No action, wait for repeating missed pulses in automatic end mode at the next active input event.

2.136 [GTM_AI.300] DPLL: Change to forward operation when DPLL_THMI is set to zero does not work correctly

Description

If direction control is set up via the TRIGGER input signal (DPLL_CTRL_1.IDDS=0, DPLL_CTRL_1.SMC=0) and DPLL_THMI is set to zero the direction does not change to forward (BWD1=0) when the current direction is backward (BWD1=1). Instead, when DPLL_THMI=0, the direction set latest is hold.

Scope

DPLL

Effects

DPLL direction does not change to forward (BWD1=0) if DPLL_THMI is set to 0. The current status of the direction is hold that means in case of BWD1=0 the direction will stay in forward (BWD1=0), in case of BWD1=1 the direction stays at backward (BWD1=1).

Workaround

- DPLL_CTRL_1.IDDS=0:
  - If the DPLL is operating in forward direction (BWD1=0) the direction can be kept by setting DPLL_THMI=0
  - If the DPLL is operating in backward direction the direction can be switched to forward by setting the DPLL_THMI value to the biggest possible value DPLL_THMI=0x00FFFF. This should set the direction back to forward
- Use different mechanism of direction control DPLL_CTRL_1.IDDS=1:
  - In this case the direction can be controlled by setting the TIM0_IN6 input signal of the GTM when MAP_CTRL.TSEL=0

In both cases the direction evaluation is done with the inactive edge of the TRIGGER input signal. The TRIGGER input signal must be active even in emergency mode to handle the direction changes correctly. If the TRIGGER input signal is not in a usable condition the necessary input signal sequence can be generated by a direct

modification of the input signal of TIM0_CH0 with the use of TIM[0]_IN_SRC.MAKE_0/VAL_0 and TIM[0]_CH[0]_ECTRL.USE_LUT (GTM v3.1.5 additionally).

2.137 [GTM_AI.301] DPLL: Reset of DPLL_STATUS.BWD1=1 by disabling the DPLL does not cause the direction to change from backward to forward in any case

Description

The issue occurs when the DPLL is operating in normal mode (DPLL_CTRL_0.RMO=0, DPLL_CTRL_1.SMC=0) and the direction of the trigger signal is evaluated in the mode DPLL_CTRL_1.IDDS=0 (input direction is detected comparing the THMI value with the duration between active and inactive slope of TRIGGER). If in this configuration a direction change happens on the trigger signal which is not plausible, because the direction change happens due to for example a disturbed signal, the direction change performed by the DPLL should be removed.

The direction in which the DPLL is operating can be read out by the status register DPLL_STATUS.BWD1. To disable the DPLL by setting DPLL_CTRL_1.DEN = 1->0->1 is resetting the BWD1 bit but this does not remove the direction change in every case and the BWD1 bit could be set to the unwanted direction again. The issue occurs when the DPLL has not received an active input signal on the STATE input such that DPLL_STATUS.fsd=0 before the DPLL is disabled (den=1->0->1) and switched to emergency mode (DPLL_CTRL_1.RMO=1). The issue does not occur if the DPLL is in the status of DPLL_STATUS.fsd=1 or if the DPLL is not switched to emergency mode (DPLL_CTRL_1.RMO=0) after the DPLL has been disabled/enabled.

Scope

DPLL

Effects

DPLL internal direction remains in current direction while DPLL_STATUS.BWD1 bit is reflecting it's reset value during a toggle sequence (1->0->1) of the DPLL enable bit DPLL_CTRL_1.DEN. At the end of the toggle sequence the BWD1 bit returns to the state of the current internal direction.

Workaround

If the issue occurs under the described conditions the wrong direction could be corrected by:

1. Adding an additional input signal (active edge followed by inactive edge while not exceeding the THMI limit) to the trigger input which switches the DPLL back to forward direction
2. Switching to the direction control mode DPLL_CTRL_1.IDDS=1 and to control the direction by setting the GTM input signal TIM0_IN6 to for example zero (forward direction). For combustion engine operation and MAP_CTRL.TSEL=0 the TDIR/SDIR signals can be used to control the direction with the TIM0_IN6 input signal. This TIM0_IN6 signal must be set directly on the GTM input pin by the mechanisms provided by the semiconductor supplier who integrated the GTM. This mechanism is bound to the resource of the TIM0_IN6 input channel

2.138 [GTM_AI.302] DPLL: Pulse generation ongoing for DPLL_CTRL_1.DMO=1 (continuous mode) if DPLL_CTRL_1.sge1/2=0

Description

In continuous mode (DPLL_CTRL_1.DMO=1) the pulse generation cannot be switched off by setting DPLL_CTRL_1.SGE1/2=0. The pulse generation is ongoing independently from the chosen mode (DPLL_CTRL_0.RMO, DPLL_CTRL_1.SMC).

Scope

DPLL

Effects

Pulse generator cannot be switched off by setting DPLL_CTRL_1.SGE1=0.

Workaround

Set number of pulses to DPLL_CNT_NUM1/2 =0 to suppress pulse generation for DPLL_CTRL_1.DMO=1.

2.139 [GTM_AI.306] DPLL: DPLL_NUTC.syn_t_old, DPLL_NUSC.syn_s_old not updated according specification

Description

The DPLL specification defines for DPLL_NUTC.WSYN=1 that an update of register DPLL_NUTC allows writing of the bits DPLL_NUTC.syn_t while DPLL_NUTC.syn_t_old inherits the previous value of DPLL_NUTC_syn_t.

Differing from the specified behavior the actual hardware does not update the value of DPLL_NUTC.syn_t_old with the previous value of DPLL_NUTC.syn_t but instead updates DPLL_NUTC.syn_t_old according to the corresponding bits of the write operation executed by the CPU.

The DPLL specification defines for DPLL_NUTC.WSYN=1 that an update of register DPLL_NUSC allows writing of the bits DPLL_NUSC.syn_s while DPLL_NUSC.syn_s_old inherits the previous value of DPLL_NUSC_syn_s.

Differing from the specified behavior the actual hardware does not update the value of DPLL_NUSC.syn_s_old with the previous value of DPLL_NUSC.syn_s but instead updates DPLL_NUSC.syn_s_old according to the corresponding bits of the write operation executed by the CPU.

Scope

DPLL

Effects

The registers bits DPLL_NUTC.syn_t_old are not updated with the previous value of DPLL_NUTC_syn_t but by the bits of the input data word.

The registers bits DPLL_NUSC.syn_s_old are not updated with the previous value of DPLL_NUSC_syn_s but by the bits of the input data word.

Workaround

If the update of syn_t/s_old shall be done like described in the specification the register DPLL_NU(T/S)C.syn_t/s must be read first, then the DPLL_NU(T/S)C.syn_(t/s) can be used to modify the bits which are written to DPLL_NU(T/S)C.syn_(t/s)_old.

As the current behavior of DPLL_NUT/SC.syn_s/t_old is in use by and can be advantageous for certain applications, there is no intend to change the current hardware behavior at this point in time. Instead a specification update to align the specification with the current hardware behavior is planned for future GTM generations.

2.140 [GTM_AI.317] DPLL: DPLL_STATUS.LOCK1/2 is set incorrectly when direction change, unexpected missing trigger/state or trigger/state out of range occurs

Extended Title

- When DPLL_CTRL_0.RMO=0 and DPLL_CTRL_1.SMC=0:
  - DPLL_STATUS.LOCK1 is set incorrectly when direction change, unexpected missing trigger or trigger out of range occurs
- When DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0:
  - DPLL_STATUS.LOCK1 is set incorrectly when direction change, unexpected missing state or state out of range occurs
- When DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=1:
  - DPLL_STATUS.LOCK2 is set incorrectly when direction change, unexpected missing state or state out of range occurs

Description

DPLL_CTRL_0.RMO=0 and DPLL_CTRL_1.SMC=0:

When DPLL_STATUS.LOCK1=0 and a direction change, an input signal with unexpected missing trigger occurs or if a trigger out of range event occurs the DPLL_STATUS.LOCK1 flag is set after two subsequent missing trigger interrupts have happened.

The correct behaviour is that DPLL_STATUS.LOCK1 is set after two subsequent missing trigger interrupts in either the same direction or without an unexpected missing trigger (missing trigger interrupt and DPLL_STATUS.ITN=1) interrupt or a trigger out of range interrupt occurs in between.

DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0:

When DPLL_STATUS.LOCK1=0 and a direction change, an input signal with unexpected missing state occurs or if a state out of range event occurs the DPLL_STATUS.LOCK1 flag is set after two subsequent missing state interrupts have happened.

The correct behaviour is that DPLL_STATUS.LOCK1 is set after two subsequent missing state interrupts in either the same direction or without an unexpected missing state (missing state interrupt and DPLL_STATUS.ISN=1) interrupt or a state out of range interrupt occurs in between.

DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=1:

When DPLL_STATUS.LOCK2=0 and a direction change, an input signal with unexpected missing state occurs or if a state out of range event occurs the DPLL_STATUS.LOCK2 flag is set after two subsequent missing state interrupts have happened.

The correct behaviour is that DPLL_STATUS.LOCK2 is set after two subsequent missing state interrupts in either the same direction or without an unexpected missing state (missing state interrupt and DPLL_STATUS.ISN=1) interrupt or a state out of range interrupt occurs in between.

Scope

DPLL

Effects

For DPLL_CTRL_0.RMO=0 AND DPLL_CTRL_1.SMC=0:

DPLL_STATUS.LOCK1 status flag is operating incorrectly.

If the DPLL_STATUS.LOCK1 flag is set incorrectly the DPLL_STATUS.itn flag could be set if additionally an unexpected missing trigger event would occur.

For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=0:

DPLL_STATUS.LOCK1 status flag is operating incorrectly.

If the DPLL_STATUS.LOCK1 flag is set incorrectly the DPLL_STATUS.isn flag could be set if additionally an unexpected missing state event would occur.

For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=1:

DPLL_STATUS.LOCK2 status flag is operating incorrectly.

If the DPLL_STATUS.LOCK2 flag is set incorrectly the DPLL_STATUS.isn flag could be set if additionally an unexpected missing state event would occur.

Workaround

For DPLL_CTRL_0.RMO=0 AND DPLL_CTRL_1.SMC=0:

When DPLL_STATUS.LOCK1= 0 the status of unexpected missing trigger, direction change and trigger out of range must be monitored to make the decision if DPLL_STATUS.LOCK1 is set correctly or not. For this reason either the interrupts DPLL_IRQ_NOTIFY.MTI, CDTI, TORI or the signals DPLL_STATUS.BWD1, ITN, TOR should be evaluated.

For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=0:

When DPLL_STATUS.LOCK1= 0 the status of unexpected missing state, direction change and state out of range must be monitored to make the decision if DPLL_STATUS.LOCK1 is set correctly or not. For this reason either the interrupts DPLL_IRQ_NOTIFY.MSI, CDSI, SORI or the signals DPLL_STATUS.BWD1/, ISN, SOR should be evaluated.

For DPLL_CTRL_0.RMO=1 AND DPLL_CTRL_1.SMC=1:

When DPLL_STATUS.LOCK2=0 the status of unexpected missing state, direction change and state out of range must be monitored to make the decision if DPLL_STATUS.LOCK2 is set correctly or not. For this reason either the interrupts DPLL_IRQ_NOTIFY.MSI, CDSI, SORI or the signals DPLL_STATUS.BWD2, ISN, SOR should be evaluated.

2.141 [GTM_AI.320] ATOM: Unexpected restart of a SOMS oneshot cycle while ATOM[i]_CH[x]_CM0 is zero

Description

If ATOM is set to SOMS oneshot mode (bit-field MODE of ATOM[i]_CH[x]_CTRL is set to 0b11 and bit-field OSM in register ATOM[i]_CH[x]_CTRL is set) a oneshot cycle is started immediately by writing a value unequal to zero to ATOM[i]_CH[x]_SR0 register while the value of ATOM[i]_CH[x]_CM0 register is zero.

Scope

ATOM

Effects

Restarting of a oneshot cycle starts immediately while ATOM[i]_CH[x]_CM0 is zero and a write access to ATOM[i]_CH[x]_SR0 is executed with a value unequal to zero.

Workaround

Avoid value 0 in ATOM[i]_CH[x]_CM0 register if SOMS oneshot mode is enabled (bit-field OSM in register ATOM[i]_CH[x]_CTRL).

2.142 [GTM_AI.323] DPLL: Registers DPLL_NUTC.SYN_T and DPLL_NUSC.SYN_S are updated by the profile (ADT_T.NT/ADT_S.NS) before the DPLL is synchronized (DPLL_STATUS.SYT/S=0)

Description

The registers DPLL_NUTC.SYN_T and DPLL_NUSC.SYN_S as well as the corresponding *_OLD registers are updated unexpectedly by the profile (ADT_T.NT/ADT_S.NS) before the DPLL is synchronized (DPLL_STATUS.SYT/S=0).

This is not a problem for the calculation of the number of pulses (nmb_t/s,..), due to the fact that the correct value of SYN_T/S for the internal use is determined by the signal DPLL_STATUS.SYT/S. The microtick generation of the DPLL is not affected by this bug.

This problem is only relevant if the SYN_T/S values are read from other consumers than the DPLL.

Scope

DPLL

Effects

When the DPLL is enabled and before the DPLL is synchronized (by writing to the relevant pointers (DPLL_APT_2c/DPLL_APS_1C3) the DPLL_NUTC.SYN_T/DPLL_NUSC.SYN_S registers are unexpectedly updated by the profile.

Because the SYN_T_OLD and SYN_S_OLD registers are updated by SYN_T, SYN_S they are affected as well.

The DPLL internal processes of calculation of the number of microticks for the next increment is not affected by that bug.

Workaround

When DPLL_NUTC.SYN_T/_OLD, DPLL_NUSC_SYN_S/_OLD values are needed outside the DPLL it must be checked that the DPLL is already synchronized (DPLL_STATUS.SYT/SYS). When the relevant DPLL channel (TRIGGER/STATE) is not synchronized yet the SYN_T/S values should be taken into account as “1”.

2.143 [GTM_AI.326] TIM: ARU bit ACB[0] (signal level) incorrect in case a second ARU request occurs while the actual request is just acknowledged

Description

An issued ARU request will be served at least after the ARU round trip time.

If one GTM clock cycle before the ARU request is acknowledged a new capture event occurs (overflow condition due to for example input change) the bit ACB[0] will not show the new value.

The overflow bit ACB[1] and the ARU data words selected by (E)GPRy_SEL) will show the correct behavior, only the ACB[0] will show the previous state.

Scope

TIM, ARU transfers

Effects

ARU bit ACB[0] not consistent with data transferred in ARU data words.

Workaround 1

Ensure that events which trigger a ARU request occur with a greater timely distance than the ARU round trip time.

Workaround 2

Use the signal level information embedded in the ARU data words (selectable by ECNT/TIM_INP_VAL).
This data will show the correct signal level.

2.144 [GTM_AI.336] GTM Bus Bridge: Incorrect AEI access execution in case the previous AEI access was aborted with the access timeout abort function

Description

In case the GTM internal AEI access timeout abort function is in use (GTM_CTRL.TO_VAL != 0 and GTM_CTRL.TO_MODE=1), a following AEI access can be corrupted:

a) A write access might not be executed (register/ memory not written to the specified value)

b) A read access can return random data (read value does not reflect the content of the addressed register / memory).

Hint: As a timeout based abort of a GTM register access is assumed to be an error scenario, the internal state of the GTM might be exposed. To ensure the proper behavior after such a severe incident, the GTM IP should be re-initialized as part of a recovery action on system level.

Scope

CPU interface accesses

Effects

Read access returns random data.
Write access does not change the content of the target address.

Workaround

Do not use the AEI access abort mode, use the observe mode instead (Set GTM_CTRL.TO_MODE=0).
Enable additionally the timeout observe IRQ by setting GTM_IRQ_EN.AEI_TO_XPT_IRQ=1 to invoke higher level recovery mechanisms for GTM re-initialization.
(e.g. abort the pending access to the GTM and re-initialize the GTM_IP from hardware reset).

2.145 [GTM_AI.340] TOM/ATOM: Generation of TRIG_CCU0/TRIG_CCU1 trigger signals skipped in initial phase of A/TOM SOMP one-shot mode

Description

Configuration in use:

- A/TOM[i]_CH[x]_CTRL.OSM=1
- A/TOM[i]_CH[x]_CTRL.OSM_TRIG=0
- A/TOM[i]_CH[x]_CTRL.UDMODE=00
- ATOM[i]_CH[x]_CTRL.MODE=10

Expected behavior

The generation of one-shot pulses in A/TOM can be initiated by a write to CN0. In this case the pulse generation comprises of an initial phase where the signal level at A/TOM output is inactive followed by a pulse. The duration of the initial phase can be controlled by the written value of CN0, where the duration is defined by CM0-CN0. After the counter CN0 reaches the value of CM0-1, the pulse starts with its active edge, CN0 is reset, and starts counting again. When CN0 reaches CM1-1, the inactive edge of the pulse occurs. Due to the fact, that the capture compare units CCU0 and CCU1 compare also in the initial phase of the pulse generation, the trigger conditions for these comparators apply also in this initial phase. Thus, the TRIG_CCU0 and TRIG_CCU1 signals also occur in the initial phase of the one-shot pulse. When these trigger signals are enabled in the A/TOM[i]_CH[x]_IRQ_EN, an interrupt signal is generated by A/TOM on the CCU0TC and CCU1TC trigger conditions and the corresponding A/TOM[i]_CH[x]_IRQ_NOTIFY bits are set.

Observed behavior

For certain start values of CN0 and dependent on the history of pulse generation, the trigger signals TRIG_CCU0 and TRIG_CCU1 are skipped. As a consequence, this can led to missing interrupts CCU0TC and CCU1TC on behalf of their missing trigger signals TRIG_CCU0 and TRIG_CCU1.

For the first pulse generation after enabling the channel, all trigger signals TRIG_CCU0 and TRIG_CCU1 appear as expected and described in the section expected behavior. If the channel stays enabled and a new value CN0 is written to trigger a subsequent one-shot pulse, the TRIG_CCU0/TRIG_CCU1 triggers in the initial phases of subsequent one-shot pulses are skipped under the following conditions:

- For TRIG_CCU0 trigger: if the one-shot pulse is started by writing a value to CN0 greater or equal to CM0-1
- For TRIG_CCU1 trigger: if the one-shot pulse is started by writing a value to CN0 greater or equal to CM1-1

Scope

TOM/ATOM

Effects

Missing TRIG_CCU0 and TRIG_CCU1 trigger signals in initial phase of subsequent pulses in A/TOM one-shot mode, when one shot-mode is started with writing to CN0 values greater equal CM0-1 or CM1-1.

Workaround 1

Disabling, resetting (channel reset), re-enabling and initializing of the channel between each one-shot pulse will ensure the correct behavior of CCU0TC and CCU1TC interrupt source.

Workaround 2

Starting a new one-shot pulse by writing twice the counter CN0 whereas the first value, which is written to CN0 should be zero followed by the value which defines the length of the initial phase.

Be aware that in this case, the total length of the initial phase until the pulse is started, is influenced by the time between the two write accesses to CN0.

2.146 [GTM_AI.342] DPLL: Unwanted direction change when switching to emergency mode during active phase of TRIGGER input signal

Description

When the DPLL is configured to DPLL_CTRL_1.IDDS=0 and the DPLL is switched to DPLL_CTRL_0.RMO=1 during the active phase of the TRIGGER input signal (timeframe between active and inactive input signal slope) and the TRIGGER input signal is causing a direction change, the direction status (DPLL_STATUS.BWD1) switches back to the former direction when the switch to emergency mode (RMO=1) is executed.

Scope

DPLL

Effects

By changing into the emergency mode the active direction is wrong.

Workaround

Don't change DPLL_CTRL_0.RMO when TRIGGER input signal is between active and inactive slope of input signal. A necessary switch to DPLL_CTRL_0.RMO=1/0 should be done only when the direction (DPLL_STATUS.BWD1) remains in a correct state.

Hint : If the direction change is caused by a disturbed or incorrect input signal the direction change can be recovered by using the ATOM-TIM loopback to generate an additional input signal to the DPLL. This input signal sets back the direction indication within the DPLL to the correct value.

2.147 [GTM_AI.346] ATOM SOMS mode: Shift cycle is not executed correctly in case the reload condition is deactivated with ATOM[i]_AGC_GLB_CTRL.UPEN = 0

Description

ATOM is configured to SOMS continuous mode by setting the following configuration bit-fields:

- ATOM[i]_CH[x]_CTRL.MODE=11
- ATOM[i]_CH[x]_CTRL.OSM=0
- ATOM[i]_CH[x]_CTRL.ARU_EN=0
- ATOM[i]_AGC_GLB_CTRL.UPEN[x]=0b00

Expected behaviour

After the counter CN0 reaches CM0, no reload cycle is executed due to the configuration of UPEN=0b00.
Instead of a reload cycle a shift cycle has to be executed to ensure an continuous shifting.

Observed behaviour

Neither a reload cycle nor a shift cycle is executed when the counter CN0 reaches CM0. The shifting stops and the shift register CM1 as well as the output ATOM[i]_CH[x]_OUT stays unexpectedly stable for two shift clock cycles whereas the counter CN0 continuously counting further on.

Scope

ATOM

Effects

After the counter CN0 reaches CM0 the output stays stable for two shift clock cycles before the next shift will be executed.

Workaround

Increase the number of bits that have to be shifted out inside CM0 register to the maximum value of 23 to ensure an continuous shifting of all bits of the shift register CM1.

2.148 [GTM_AI.348] DPLL: Correction of missing pulses delayed after start of pulse generation

Description

The described erratum occurs in the DPLL configuration DPLL_CTRL_1.DMO=0 (Automatic end mode) and DPLL_CTRL_1.COA=0 (Fast pulse correction). When after the start of pulse generation (DPLL_CTRL_1.SGE1/2=0-->1) not all pulses scheduled could be generated, repeating the pulses at fast speed is not executed at the second TRIGGER/STATE input event.

Scope

DPLL

Effects

When the pulse generation has been started by setting DPLL_CTRL_1.SGE1/2 and not all scheduled pulses could be generated there is no fast pulse correction after the second active input signal. Beyond that the DPLL internal pulse counter DPLL_ICNT1/2 is incremented correctly so that no pulse is getting lost. After the third input event the pulse correction is working as specified.

Workaround 1

DPLL must be in direct load mode (DPLL_CTRL_1.DLM1/2 =1). Set DPLL_ADD_IN_LD1/2.ADD_IN_LD1/2=0 for the first two increments after the DPLL pulse generation has been started by DPLL_CTRL_1.SGE1/2=1 (all GTM Versions)

Workaround 2

Do nothing: If there is no need to do the pulse correction for the second input signal after start of pulse generation. With the third input signal the pulse correction is starting to work.

Workaround 3

***Note**: Workaround 3 is applicable for all GTM versions used in TC3xx devices. It is not applicable for TC2xx devices.*

Use pulse correction mechanism triggered by DPLL_CTRL_1.PCM1/2:

- Set DPLL_MPVAL1/2.MPVAL1/2 to the desired number of pulses which has to be sent out fast
- Set DPLL_CTRL_11.PCMF1/2=1 AND DPLL_CTRL_11.PCMF1/2_INCCNT_B=1
- Trigger the fast pulses by setting DPLL_CTRL_1.PCM1/2=1

2.149 [GTM_AI.349] TOM-SPE: OSM-Pulse width triggered by SPE_NIPD for selected CMU_FXCLK not correct

Description

The SPE_NIPD signal is used to reset TOM_CH_CN0 and to generate a one-shot pulse. When the CMU_FXCLK of the corresponding TOM_CH is set to a value unequal to 0, there are two effects observed:

1. the first pulse triggered by SPE_NIPD is generated with the CMU_FXCLK(0), while any subsequent pulses are generated with the configured CMU_FXCLK;
2. the pulses generated with the correct CMU_FXCLK show no determinism. Some pulses end with CCU_TRIG1, some with CCU_TRIG0

Scope

TOM, SPE

Effects

The OSM-Pulse width triggered by SPE_NIPD are not correct.

Workaround

Use SYS_CLK by selecting CMU_FXCLK(0) instead of a value unequal to zero for CMU_FXCLK.

To reach the same pulse width on the output signal, the value for the period (TOM[i]_CH[x]_CM0.CM0) and duty cycle (TOM[i]_CH[x]_CM1.CM1) has to be scaled due to the relationship between SYS_CLK and the needed CMU_FXCLK.

2.150 [GTM_AI.350] TOM-SPE: Update of SPE[i]_OUT_CTRL triggered by SPE_NIPD not working for a delay value 1 in TOM[i]_CH[x]_CM1

Description

When configured in one-shot mode some TOM channels can initiate a delayed change of register SPE_OUT_CTRL. The delay can be configured in TOM[i]_CH[x]_CM1 register of the corresponding TOM channel.

Expected behaviour

The SPE_OUT_CTRL register changed its content after a delay of CMU_FXCLK cycles which are configured in the TOM channel. For CM1=0, no update is expected, for CM1=1, the update is expected with the next CMU_FXCLK, for CM1=2, a delay of two CMU_FXCLK clock cycles is expected.

Observed behaviour

For CM1=1, there is no change of SPE_OUT_CTRL at all, independent of CMU_FXCLK.

Scope

TOM, SPE

Effects

The update of SPE_OUT_CTRL register is not executed.

Workaround

Use SYS_CLK by selecting CMU_FXCLK(0) instead of a value unequal to zero for CMU_FXCLK.

To get the trigger signal from TOM for the delayed update at the same time, the value for the period (TOM[i]_CH[x]_CM0.CM0) and duty cycle (TOM[i]_CH[x]_CM1.CM1) has to be scaled due to the relationship between SYS_CLK and the needed CMU_FXCLK.

2.151 [GTM_AI.351] MAP: Disable of input lines by MAP_CTRL register not implemented for input signals TSPP0 TIM0_CHx(48) (x=0..2) and TSPP1 TIM0_CHx(48) (x=3..5)

Description

The Control bits TSPP0_I0V, TSPP0_I1V, TSPP0_I2V, TSPP1_I0V, TSPP1_I1V, TSPP1_I2V of register MAP_CTRL are not operating as specified. The specified gating functions of the input signals TIM0_CH0(48), TIM0_CH1(48), TIM0_CH2(48) of TSPP0 submodule and the input signals TIM0_CH3(48), TIM0_CH4(48), TIM0_CH5(48) of TSPP1 submodule are not implemented, hence the input signals cannot be disabled.

Scope

MAP

Effects

The specified disable function of the input signals TIM0_CH0(48), TIM0_CH1(48), TIM0_CH2(48) of TSPP0 submodule and the input signals TIM0_CH3(48), TIM0_CH4(48), TIM0_CH5(48) of TSPP1 submodule are not implemented, hence the input signals cannot be disabled.

Workaround

The combined TRIGGER or STATE output signals to the DPLL module can be disabled by using the control signals DPLL_CTRL_0.TEN(TRIGGER, TSPP0) and DPLL_CTRL_0.SEN (STATE, TSPP1).

No workaround exists for switching off the level input signals of the TSPP0 and TSPP1 submodules individually.

2.152 [GTM_AI.353] SPEC-ATOM: Specification of the smallest possible PWM period in SOMP mode wrong, when ARU_EN=1

Description

Configuration in use:

- ATOM[i]_CH[x]_CTRL.MODE=0b10 (SOMP)
- ATOM[i]_CH[x]_CTRL.ARU_EN=1
- ATOM[i]_AGC_GLB_CTRL.UPEN_CTRLx=1

Functionality

When ATOM[i]_CH[x]_CTRL.ARU_EN=1 and ATOM[i]_AGC_GLB_CTRL.UPEN_CTRLx=1 the PWM period and duty cycle (PWM characteristic) can be reloaded via ARU in SOMP mode. The ATOM generates a PWM on the operation registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1 while the new values received via ARU are stored in the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1.

Reloading of the ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1 registers with the values from ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 takes place, when the old PWM period expires (ATOM[i]_CH[x]_CN0.CN0 reaches ATOM[i]_CH[x]_CM0.CM0 in up counter mode or ATOM[i]_CH[x]_CN0.CN0 reaches 0 in up/down counter mode).

Therefore, it is important, that the new PWM characteristic is available in the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 before ATOM[i]_CH[x]_CN0.CN0 reaches ATOM[i]_CH[x]_CM0.CM0 (up counter mode) or 0 (up/down counter mode).

Problem description

The GTM-IP specification defines as minimal possible PWM period, where the PWM characteristic can be reloaded in a predictable manner so that new data is always available in time at the ATOM channel, to be the ARU round trip time of the specific microcontroller device. This is not correct, because the data needs two additional ARU clock cycles to flow through the ARU from a source to the ATOM channel plus one clock cycle for loading the value from the shadow registers ATOM[i]_CH[x]_SR0.SR0 and ATOM[i]_CH[x]_SR1.SR1 to the registers ATOM[i]_CH[x]_CM0.CM0 and ATOM[i]_CH[x]_CM1.CM1.

When the PWM period is smaller than the ARU round trip time plus three ARU clock cycles, the PWM output is not correct.

Scope

SPEC-ATOM

Effects

When the ATOM channel operates in SOMP mode and receives updates of PWM period and/or duty cycle via ARU, new PWM period and/or duty cycle values get lost, when the PWM Period is smaller than the ARU round trip time plus one or two ARU clock cycles for the given microcontroller device the PWM Period runs on.

Recommendation for TC2xx

The PWM period has to be larger than ARU round trip time + 3 ARU clock cycles.

Recommendation for TC3xx

The PWM period has to be larger than ARU round trip time + 3 ARU clock cycles. Alternatively use ARU dynamic routing, or reduce the value of ARU_CADDR_END to a value, which fits the PWM period. So, PWM period greater than ARU_CADDR_END + 1 + 3 ARU clock cycles.

2.153 [GTM_AI.361] IRQ: Missing pulse in single-pulse interrupt mode on simultaneous interrupt and clear event

Description

In single-pulse interrupt mode ([MODULE]_IRQ_MODE = 0b11) only the first interrupt event of the interrupt bits of the interrupt notify register inside this module generates a pulse on the output signal IRQ_line, if the associated interrupt is enabled ([MODULE]_IRQ_EN=1). All further interrupt events have no effect on the output signal IRQ_line until all enabled interrupts are cleared, except when an interrupt and a clear event (HW_clear or a SW_clear) occur at the same time.

Expected behaviour

On simultaneous occurrence of an interrupt and clear event, a pulse on the output signal IRQ_line is generated.

Observed behaviour

If the associated notify register bit of the interrupt event is not set and another bit of the same notify register is set and this interrupt is enabled, no pulse on the output signal IRQ_line is generated.

All modules ([MODULE]) are affected by this ERRATUM, which are able to generate interrupts and which have multiple interrupt sources which are ORed to the output. Not affected are the modules DPLL and ARU.

Scope

IRQ

Effects

Missing pulse on interrupt signal IRQ_line.

All modules, which deliver an interrupt signal and have more than one internal interrupt source which are ORed are affected. The only exceptions are the modules ARU and DPLL.

Workaround

On a SW clear prevent HW clear events and read the interrupt notify register to check on new interrupts without a received interrupt pulse on IRQ_line. In this case repeat the SW clear step to enable interrupt generation again.

When disabling the HW clear is not an option refrain from using the single-pulse interrupt mode.

2.154 [GTM_AI.380] (A)TOM: potentially wrong output signal in case of RST_CCU0=1 and CM0=1 on triggered channel in SOMP mode

Description

When the reset of (A)TOM_CHx_CN0 of a TOM or ATOM channel is triggered by a preceding channel or assigned TIM module (RST_CCU0=1) and the ATOM channel is configured in SOMP mode, the CM0 value defines the edge to SL and CM1 defines the edge to !SL.

Expected behavior

When SR0 is configured to '1', and CM0 is updated with SR0=1 on trigger signal coming from previous channel, an edge to SL is expected, when CN0=CM0=1.

Observed behavior

When CM0 is updated synchronously from SR0 for the next period, and CM0>1 at the actual period, no edge to SL is generated when CM0=CN0=1 for the first period after CM0=1 becomes active (was updated to CM0=1 from SR0).

Scope

TOM, ATOM

Effects

For the configuration RST_CCU0=1 and CM0=1, CM0 < CM1 no edge is generated for the first period, after CM0 is updated from SR0 with ’1’ and CM0 > 1 in the period before.

Workaround

In addition to configuring SR0=1 and letting the (A)TOM channel update CM0 with ‘1’ at the start of the next period, a hot reconfiguration of CM0=1 can be done. However, the hot reconfiguration needs to be done after the edge to SL was performed in the actual period. Otherwise the CM0 value would be overwritten by ‘1’ and the edge to SL would be generated immediately after hot reconfiguration and not at the intended old CM0 value.

The workaround is applicable where the system can update the CM0 value in time; otherwise the setting of CM0=1 should not be used.

2.155 [GTM_AI.398] DPLL: Incorrect DPLL_THVAL calculation leading to a false direction decision in case tbu_ts0 wraps around

Description

When

a) The inactive edge of TRIGGER input signal is used for detection of the direction (DPLL_CTRL_1.IDDS = 1)

and

b) The input delay information is used to correct time stamps (DPLL_CTRL_0.IDT = 1)

and

c) In between the active input signal edge and the inactive input signal edge on TRIGGER tbu_ts0 wraps around

then the calculation of DPLL_THVAL.THVAL is incorrect incurring a false direction decision.

Scope

DPLL

Effects

Wrong value of DPLL_THVAL and false direction decision.

Workaround

Do not use DPLL_CTRL_0.IDT = 1 when evaluating direction with DPLL_CTRL_1.IDDS = 1.

2.156 [GTM_AI.408] (A)TOM-RTL: Missing edge on output signal (A)TOM_OUT when CN0 is reset with force update event

Description

The channel is configured in continuous up-counter mode. Then a new period is started with a force update event and reset of CN0 is activated.

Configuration for TOM:

TOM[i]_CH[x]_CTRL.UDMODE = 0

TOM[i]_TGC[g]_FUPD_CTRL.FUPD_CTRL[k] = 10_B

TOM[i]_TGC[g]_FUPD_CTRL.RSTCN0_CH[k] = 10_B

Configuration for ATOM:

ATOM[i]_CH[x]_CTRL.MODE = 10_B (SOMP mode)

ATOM[i]_CH[x]_CTRL.UDMODE = 0

ATOM[i]_AGC_FUPD_CTRL.FUPD_CTRL[k] = 10_B

ATOM[i]_AGC_FUPD_CTRL.RSTCN0_CH[k]= 10_B

Expected behavior

After the counter (A)TOM[i]_CH[x]_CN0.CN0 has been reset and therefore a new period has to be started and the output signal (A)TOM_OUT has to be set immediately to the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL), and after the counter reaches (A)TOM[i]_CH[x]_CM1.CM1, an edge on (A)TOM_OUT to the inverted SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) is expected.

Observed behavior

An edge on the output signal (A)TOM_OUT to the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) at the beginning of the new period does not happen. Instead, the output signal (A)TOM_OUT holds its last value.

A second observation is in case the SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) changes synchronously together with the force update event, an edge on (A)TOM_OUT to the inverted SL value (ATOM[i]_CH[x]_CTRL_SOMP.SL, TOM[i]_CH[x]_CTRL.SL) when (A)TOM[i]_CH[x]_CN0.CN0 reaches (A)TOM[i]_CH[x]_CM1.CM1 does not happen.

Scope

TOM, ATOM

Effects

Missing edge and false output signal level on (A)TOM_OUT.

Workaround

None.

2.157 [GTM_AI.410] GTM_AEI: The AEI bridge might not execute an accepted write transaction

Description

If the AEI Bridge operates in pipeline mode while a soft-reset is issued (writing BRIDGE_MODE.BRG_RST = '1'), upcoming write transactions primed in the buffer although accepted may never be actually executed. The maximum number of non-executed transactions depends on the buffer depth (BRIDGE_BUFF_DPT).

Scope

GTM_AEI

Effects

Write transaction is signaled to be accepted but will never be executed.

Workaround

Issue a read access to any address after the soft reset.

2.158 [GTM_AI.419] TIM: Potentially wrong capture values

Description

Configuration: The TIM channel is configured in TIEM, TIPM, TGPS or TSSM mode by setting of TIM[i]_CH[x]_CTRL.TIM_MODE = {010_B, 011_B, 101_B, 110_B}. The TIM channel is disabled (TIM[i]_CH[x]_CTRL.TIM_EN=0) and later enabled again (TIM[i]_CH[x]_CTRL.TIM_EN = 1).

Expected behavior for TIEM/TIPM/TGPS mode

The registers TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_ECNT.ECNT[15:1], TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 are set to their reset values. In case of an input signal edge or an input capture event or an active selected CMU clock (TGPS mode) at the same time as the channel is enabled, this event has to be taken into account and the TIM[i]_CH[x]_CNT register must be updated/incremented based on its reset value. Due to this a capture event can happen depending on the configured TIM mode and the register values.

Expected behavior for TSSM mode

The registers TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_ECNT.ECNT[15:1], TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 are set to their initial values. The initial value for TIM[i]_CH[x]_CNT register depends on TIM[i]_CH[x]_CTRL.ISL and TIM[i]_CH[x]_CNTS.CNTS(22). If TIM[i]_CH[x]_CNTS.CNTS(22) is set to 0 and TIM[i]_CH[x]_CTRL.ISL is set to 0 the initial value of TIM[i]_CH[x]_CNT is 0x000000. An input signal event simultaneously to the channel enable is not taken into account.

Observed behavior for TIEM/TIPM/TGPS mode

If no input signal event or input capture event or active selected CMU clock (TGPS mode) occurs, the registers TIM[i]_CH[x]_CNT, TIM[i]_CH[x]_ECNT.ECNT[15:1], TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 are set to their reset values as expected.

If an input signal event or an input capture event or an active selected CMU clock (TGPS mode) occurs at same time as the channel gets enabled, the TIM[i]_CH[x]_CNT register continues to count (or update) based on the previous (old) value. As a result, a capture could be performed too early and/or with the wrong values. The TIM[i]_CH[x]_ECNT.ECNT[15:1] register is set to its reset value as expected.

Observed behavior for TSSM mode

The register TIM[i]_CH[x]_CNT is not set to its initial value of 0x000000 on channel enabling when TIM[i]_CH[x]_CNTS.CNTS(22) is set to 0 and TIM[i]_CH[x]_CTRL.ISL is set to 0.

***Note**: The TIM channel modes TPWM, TPIM and TBCM (TIM[i]_CH[x]_CTRL.TIM_MODE = {000_B, 001_B, 100_B}) are not affected.*

Scope

TIM

Effects

TIM[i]_CH[x]_CNT register is not reset and the wrong values could be captured into TIM[i]_CH[x]_GPR0 and TIM[i]_CH[x]_GPR1 registers.

Workaround 1

Reset the TIM channel by setting of TIM[i]_RST.RST_CH[x] = 1 before enabling the TIM channel.

Workaround 2

The following sequence has to be executed on the disabled channel, but before the actual enabling of the channel to ensure that the TIM[i]_CH[x]_CNT register is set to its reset value when the channel is enabled.

1. Configure TIM[i]_CH[x]_CNTS = 0
2. Enable the TIM channel with the following configuration inside the TIM[i]_CH[x]_CTRL register:
   - TIM_EN = 1
   - TIM_MODE = 101_B (TGPS)
   - ISL = 1
   - OSM = 1
   - ARU_EN = 0
   - select a fast CMU_CLK_RES, e.g. CLK_SEL = 000_B
3. Wait until an edge on the selected CMU_CLK_RES occurs. This can be observed on the NEWVAL IRQ notify register. This event sets the TIM[i]_CH[x]_CNT register to its reset value
4. Disable TIM channel (TIM[i]_CH[x]_CTRL.TIM_EN = 0)
5. Configure the former TIM channel configuration in TIM[i]_CH[x]_CTRL register and enable the TIM channel again

2.159 [GTM_AI.421] GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in pipeline mode can lead to violation of pipeline protocol

Description

In pipeline mode, a reconfiguration of the BRIDGE_MODE.MSK_WR_RSP directly after another write transaction can lead to a hang of following write transactions by not setting the AEI_READY.

***Note**: Please also check on errata GTM_AI.487 and GTM_AI.488.*

Scope

GTM_AEI

Effects

Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set.

Workaround

Make sure the transaction preceding the write of BRIDGE_MODE.MSK_WR_RSP is a read transaction.

2.160 [GTM_AI.422] DPLL: Wrong DPLL_RDT_S_ACT/DPLL_RDT_T_ACT value in case of overflow correction

Description

The wrong overflow correction occurs for DPLL_RDT_S_ACT when the DPLL is in normal mode (DPLL_CTRL_0.RMO=0, DPLL_CTRL_1.SMC=0), or for DPLL_RDT_T_ACT when the DPLL is in emergency mode (DPLL_CTRL_0.RMO=1, DPLL_CTRL_1.SMC=0).

Instead of 0xFFFFFF the value 0x000000 is written in both cases. A problem in the calculation of pulse frequency (settling behavior) or PMT values may occur when the mode in DPLL_CTRL_0.RMO is switched (normal mode <-> emergency mode). If the overflow value was not yet overwritten (due to engine revolution happening before mode's switch) the wrong value might come into use for the described calculations.

Scope

DPLL

Effects

Wrong value in either DPLL_RDT_T_ACT (emergency mode) or DPLL_RDT_S_ACT (normal mode) after detection of overflow condition. With the next active input signal slope a potentially wrong value of DPLL_RDT_T_ACT is stored to DPLL_RDT_T of RAM2 and DPLL_RDT_S_ACT is stored to DPLL_RDT_S of RAM1bc. This might lead to different settling behavior of the sub increments and wrong results for PMT calculations if these values are actually used.

Workaround

Modification of DPLL_RDT_T_ACT (emergency mode) or DPLL_RDT_S_ACT (normal mode) after detection of overflow condition is not possible but does not cause any negative effects on pulse generation or PMT calculation at all.

The values stored to DPLL_RDT_T of RAM2 or DPLL_RDT_S of RAM1bc need to be corrected by following workaround sequence:

1. Check if relevant overflow on either DPLL_RDT_T_ACT or DPLL_RDT_S_ACT occurred. This can be done by observation of DPLL_STATUS.CRO when interrupt DPLL_IRQ_NOTIFY.EI occurred.
2. Check which of the interrupts DPLL_IRQ_NOTIFY.TASI/SASI has occurred next and based on that DPLL_RDT_T or DPLL_RDT_S has to be corrected.
3. For DPLL_CTRL_0.RMO = 0 and DPLL_CTRL_1.SMC = 0, DPLL_RDT_S[DPLL_APS.APS -1] has to be written with 0xFFFFFF.

   For DPLL_CTRL_0.RMO = 1 and DPLL_CTRL_1.SMC = 0, DPLL_RDT_T[DPLL_APT.APT -1] has to be written with 0xFFFFFF.

2.161 [GTM_AI.429] TIM: Missing glitch detection interrupt event

Description

Configuration:

TIM filter is configured in immediate edge propagation mode by setting TIM[i]_CH[x]_CTRL.FLT_MODE_RE = 0 or TIM[i]_CH[x]_CTRL.FLT_MODE_FE = 0. The filter is enabled by setting TIM[i]_CH[x]_CTRL.FLT_EN = 1.

Expected behavior

As long as the filter threshold is not reached and the input signal level unexpectedly changes (it is an input glitch occurs), the internal glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) should have a HIGH pulse of one cluster clock cycle.

Observed behavior

When the input signal glitch occurs at the same time the filter counter reaches its threshold, the internal glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) does not occur.

Scope

TIM

Effects

The TIM[i]_CH[x]_IRQ_NOTIFY.GLITCHDET bit is not set. Thus, no interrupt is triggered. Furthermore, the external capture source EXT_CAPTURE(x) is not triggered if its source is set to TIM_GLITCHDET_IRQ.

Workaround

The filter counter threshold can be set to the next higher value. Thus, a former not detected glitch would be detected. In that case, the output signal would be changed (one clock cycle longer) when the input signal is a single cycle pulse.

2.162 [GTM_AI.430] TIM: Unexpected increment of filter counter

Description

Configuration: TIM filter is configured in immediate edge propagation mode by setting TIM[i]_CH[x]_CTRL.FLT_MODE_RE = 0 and/or TIM[i]_CH[x]_CTRL.FLT_MODE_FE = 0. The filter is enabled by setting TIM[i]_CH[x]_CTRL.FLT_EN = 1. The filter counter threshold is set to zero by setting TIM[i]_CH[x]_FLT_RE.FTL_RE = 0 and/or TIM[i]_CH[x]_FLT_FE.FTL_FE = 0.

Expected behavior

When the input signal level changes, the filter counter should not increment.

Observed behavior

When the input signal level changes, the filter counter increments by one and is not reset.

Scope

TIM

Effects

If an input edge occurs during the acceptance time, the following output signal change will happen one or more selected CMU clock cycles earlier than expected. This depends on the initial configuration and the reconfiguration of the filter mode and the filter counter threshold. If the filter mode for both edges is configured to immediate edge propagation and both filter counter thresholds are set to zero, the counter falsely can count up to a higher value than one without resetting. If one or both filter modes and/or thresholds are reconfigured during the application, the higher count of the filter counter can lead to a difference of more than one CMU clock cycle between the expected and actual output signal change at the next occurring input edge. If only one

filter counter threshold is set to zero, the difference of the expected and actual output signal change is one CMU clock cycle.

Workaround

If acceptable, use a threshold greater than zero. Otherwise there is no workaround available. However, there is a possibility of minimizing the absolute error, deriving from this bug. If possible, a faster CMU clock can be selected. This leads to a shorter absolute time difference between the expected and actual output signal change. Additionally when applying this, the filter counter thresholds need to be assimilated proportionally in order to make the filter work as before.

2.163 [GTM_AI.431] TIM: Glitch detection interrupt event of filter is not a single cycle pulse

Description

Configuration: The TIM filter must be enabled by setting TIM[i]_CH[x]_CTRL.FLT_EN = 1.

Expected behavior

As long as the filter threshold is not reached and the input signal level changes unexpectedly, the glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) should have a single cycle HIGH pulse.

Observed behavior

When the input signal level changes unexpectedly for longer than one clock cycle, the glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) is HIGH as long as the unexpected signal change is present.

Scope

TIM

Effects

- Effect 1: The longer lasting HIGH signal of the glitch detection interrupt event signal (TIM_GLITCHDET_IRQ) may lead to an unexpected behavior within the GTM only if TIM_GLITCHDET_IRQ is used for the external capture signal EXT_CAPTURE(x).
- Effect 2: If the related interrupt notify register (TIM[i]_CH[x]_IRQ_NOTIFY) is cleared by software while the TIM_GLITCHDET_IRQ signal is still HIGH, the interrupt will unexpectedly retrigger.

Workaround

No workaround in hardware.

For the unexpected retrigger of the interrupt directly after an interrupt clear step, the interrupt routine has to consider that the interrupt might be invalid.

2.164 [GTM_AI.450] DPLL: Stored time stamp values do not consider filter delays

Description

For the case where the filter delay values should be considered (DPLL_CTRL_0.IDT/IDS=1) the data values of the time stamp fields in RAM1c (DPLL_TSF_S) and RAM2 (DPLL_TSF_T) actually do not take them into account for the input signals TRIGGER/STATE.

Scope

DPLL

Effects

The missing correction of the stored time stamp values does lead to inaccuracies in DPLL PMT calculations.

Workaround

The entry of DPLL_TSF_T[p]/_S[p] can be read, corrected (by DPLL_FTV_T/_S), and written back.

The correction needs to be done after the DPLL has received new input data. For this reason it is necessary to read and store the filter value of the last but one DPLL input signal, which then will be used for the correction.

2.165 [GTM_AI.451] DPLL: Wrong measured position stamps in RAM

Description

For the synchronous motor control (DPLL_CTRL_1.SMC=1) in normal mode (DPLL_CTRL_0.RMO=0) wrong values are stored in RAM1b for DPLL_PSSM and DPLL_PSSM_OLD. The entries are not derived from CCM[0]_TBU_TS2 at the point of time when the active input signal arrives but they are derived erroneously from CCM[0]_TBU_TS1 instead.

Scope

DPLL

Effects

Wrong values for DPLL_PSSM and DPLL_PSSM_OLD stored in memory. Controlling of angle clock cannot rely on these values.

Workaround

Configure relevant TIM channels which are used to define the STATE input signal, such that CCM[0]_TBU_TS2 is captured in each one of the TIM[0]_CH[x]_GPR1.GPR1 registers.

After a STATE input signal has arrived, wait until the point in time when the DPLL should have calculated the DPLL_PSSM or DPLL_PSSM_OLD value. This is fulfilled when the content of the bit-field DPLL_STA.STA_S has passed the value 28_H.

Then write DPLL_PSSM or DPLL_PSSM_OLD with the value of the TIM[0]_CH[x]_GPR1.GPR1 register of the corresponding TIM channel causing the captured input signal edge of STATE input. Which of the DPLL_PSSM or DPLL_PSSM_OLD values has to be written might be figured out by using the content of the bit-field DPLL_OSW.SWON_S.

2.166 [GTM_AI.456] DPLL: No action calculation

Description

If DPLL_CTRL_1.SMC=1 and DPLL_CTRL_0.RMO=0 no action calculation is done in STATE processing unit for action channels NOAC/2 to NOAC-1 (NOAC: number of action channels).

***Note**: Starting with GTM V4.1.* NOAC=32, while in previous versions NOAC=32 for TC3xx and TC29x, and NOAC=24 for TC27x and TC26x.*

Scope

DPLL

Effects

No action calculation of channels NOAC/2 to NOAC-1.

Workaround

None

2.167 [GTM_AI.458] DPLL: Missing TOR interrupt and status flag

Description

***Note**: Register names in the text follow the TC3xx syntax conventions. Correlation of register names:*

- ***TC2xx:** DPLL_, DPLL_TS_T_0, DPLL_TS_T_1, DPLL_TS_T_OLD_0, DPLL_TS_T_OLD_1*
- ***TC3xx:** DPLL_, DPLL_TS_T, DPLL_TS_T_OLD*

If DPLL_CTRL_0.RMO=1 and DPLL_CTRL_1.SMC=0, the TOR interrupt (DPLL_IRQ_NOTIFY.TORI) is not triggered and the status flag (DPLL_STATUS.TOR) is not set on encountering an out of range TRIGGER.

Scope

DPLL

Effects

The TOR interrupt (DPLL_IRQ_NOTIFY.TORI) is not triggered and the status flag (DPLL_STATUS.TOR) is not set with the described configuration.

Workaround

No workaround available in hardware.

Nevertheless the application can detect the trigger out of range interrupt by observing TBU_TS0:

If the current TRIGGER time stamp (DPLL_TS_T.TRIGGER_TS/DPLL_TS_T_OLD.TRIGGER_TS_OLD) + DPLL_DT_T_ACT.DT_T_ACT* DPLL_TLR.TLR > TBU_TS0 and no active TRIGGER input was encountered, the CPU/MCS can force a TOR interrupt by writing a one to DPLL_IRQ_FORCINT.TRG_TORI.

2.168 [GTM_AI.462] (A)TOM: Missing CCU0TC_IRQ interrupt signal

Description

Configuration:

The channel is configured in SOMP (ATOM) up-counter mode with up/down counter mode disabled ((A)TOM[i]_CH[x]_CTRL.UDMODE=0) or not existing and triggering by a preceding channel with configuration of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1.

Expected behavior

When the counter (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0, the interrupt signal CCU0TC_IRQ must be triggered.

Observed behavior

In the first period after (A)TOM[i]_CH[x]_CM0.CM0 is changed to the value 0 or 1, no CCU0TC_IRQ interrupt signal is triggered.

***Note**: When the second period starts after (A)TOM[i]_CH[x]_CM0.CM0 is changed to the value 0 or 1 and stays at that value, then the CCU0TC_IRQ interrupt signal generation works correctly.*

Scope

TOM, ATOM

Effects

Interrupt signal CCU0TC_IRQ is not triggered.

Workaround

No workaround available.
It needs to be checked if the application can accept the interrupt occurring with the second period.

2.169 [GTM_AI.463] DPLL: DPLL_PVT not cleared after direction change

Description

For settings of DPLL_CTRL_1.SMC=1 or alternatively DPLL_CTRL_1.SMC=0 and DPLL_CTRL_1.IDDS=1 the direction change on TRIGGER channel is done via DPLL input port "TDIR" (generated via the control path SPE or TIM to MAP to DPLL).
If there is a direction change the RAM parameter DPLL_PVT is not cleared as specified.

Scope

DPLL

Effects

DPLL_PVT is not cleared and the PVT check is not suppressed under the described conditions. The PVT violation interrupt (DPLL_PWI_IRQ) could be unexpectedly triggered.

Workaround

Reset DPLL_PVT by CPU or MCS0 write operation, when direction change is detected via DPLL_IRQ_NOTIFY.DCGI interrupt.

2.170 [GTM_AI.474] DPLL: DPLL_PSTC, DPLL_PSSC erroneously modified

Description

If a direction change happens while the TRIGGER processing unit is not yet synchronized (DPLL_STATUS.SYT=0) then DPLL_PSTC is erroneously overwritten.
If a direction change happens while the STATE processing unit is not yet synchronized (DPLL_STATUS.SYS=0) then DPLL_PSSC is erroneously overwritten.

Scope

DPLL

Effects

Update of DPLL_PSTC and/or DPLL_PSSC after direction change. These values are unreliable then.

Workaround

Store the DPLL_PSTC, DPLL_PSSC values outside the DPLL, each time a TRIGGER/STATE input occurs.
If a direction change is detected, overwrite the newly calculated value by the value stored earlier. This is necessary as long as the DPLL is not yet synchronized (DPLL_STATUS.SYT=0 for DPLL_PSTC and/or DPLL_STATUS.SYS=0 for DPLL_PSSC).

2.171 [GTM_AI.475] DPLL: Incorrect values of DPLL_RCDT_TX, DPLL_RCDT_SX

Description

If during the reciprocal value calculation an overflow happens then the parameters DPLL_RCDT_TX.RCDT_TX and DPLL_RCDT_SX.RCDT_SX are set erroneously to 0x000000. The specified value is 0xFFFFFF.

Scope

DPLL

Effects

Wrong value is stored in either DPLL_RCDT_TX (normal mode) or DPLL_RCDT_SX (emergency mode) after a detection of a reciprocal overflow condition. The derived parameters DPLL_RCDT_TX_NOM.RCDT_TX_NOM and DPLL_RCDT_SX_NOM.RCDT_SX_NOM are diverging accordingly. This leads to a different calculation of the pulse generator frequencies (DPLL_ADD_IN_CAL1.ADD_IN_CAL1 or DPLL_ADD_IN_CAL2.ADD_IN_CAL2 in dependence of the configured DPLL mode), which might lead to a different settling behavior of the generated angle clocks in such cases.
The diverging settling behavior is not necessarily malicious.

Workaround

If a different settling behavior of the DPLL control loop is acceptable no specific countermeasure is necessary.

2.172 [GTM_AI.477] DPLL: DPLL_DCGI interrupt not triggered

Description

When synchronous motor control mode is active (DPLL_CTRL_1.SMC=1):
If a first direction change together with an input signal change (active edge) has happened, then for a consecutive direction change together with the next following input signal change the interrupt DPLL_DCGI does not occur.

Scope

DPLL

Effects

The interrupt DPLL_DCGI does not occur.

Workaround

When a direction change is detected by DPLL_IRQ_NOTIFY.DCGI the register DPLL_STATUS.BWD1 can be checked after the next relevant input signal edge on TRIGGER. If a second direction change is detected with the very next relevant input signal, the DPLL_DCGI can be set by writing DPLL_IRQ_FORCINT.TRG_DCGI =1. The next relevant input signal edge is the next input signal edge for DPLL_CTRL_1.SMC=1 (in contrast to the next inactive input signal edge when DPLL_CTRL_1.SMC=0).

2.173 [GTM_AI.478] DPLL: Incorrect calculation of DPLL_THVAL, DPLL_THVAL2

Description

***Note**: Register names in the text follow the TC3xx syntax conventions. Correlation of register names:*

- ***TC2xx**: DPLL_CTRL_, DPLL_THVAL*
- ***TC3xx**: DPLL_CTRL_, DPLL_THVAL, DPLL_THVAL2*

In case of LOW_RES=1, DPLL_CTRL_1.SMC=0, DPLL_CTRL_0.IDT=1, and DPLL_CTRL_1.TS0_HRT=0 the values of DPLL_THVAL, DPLL_THVAL2 are calculated incorrectly because the filter values are not divided by 8 as specified.

Scope

DPLL

Effects

Under the described conditions the values of DPLL_THVAL, DPLL_THVAL2 are incorrect. The divergence is small, but in theory this can still lead to a wrong direction decision as the THVAL is used for the evaluation of the direction change.

Example:

In case of a 45/90 µs sensor input signal for this failure to happen means to have a difference of the filter values between active and inactive input signal edge on TRIGGER larger than 450 clock cycles in case of a 20 MHz TBU_TS0 clock configuration.

Workaround

If a negative effect on the direction decision is not expected no workaround is necessary. If a negative effect cannot be excluded, the use of the filter values can be switched off by setting DPLL_CTRL_0.IDT=0.

2.174 [GTM_AI.487] GTM_AEI: Changing BRIDGE_MODE[2:0] in pipeline mode can lead to violation of pipeline protocol

Description

The issue from erratum GTM_AI.421 (“GTM_AEI: Changing BRIDGE_MODE.MSK_WR_RSP in pipeline mode can lead to violation of pipeline protocol”) not only appears when BRIDGE_MODE.MSK_WR_RSP changes, but also when it stays '1' while the other configuration bit-fields in BRIDGE_MODE.BYPASS_SYNC and/or BRIDGE_MODE.BRG_MODE change.

Please also check on erratum GTM_AI.488

Scope

GTM_AEI

Effects

Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set.

Workaround

Make sure the transaction preceding the write of the mentioned BRIDGE_MODE bit-fields is a read transaction.
This workaround matches the workaround from GTM_AI.421.

2.175 [GTM_AI.488] GTM_AEI: Turning off BRIDGE_MODE.MSK_WR_RSP in asynchronous mode might lead to following transactions being corrupted

Description

If the AEI bridge operates in asynchronous mode and in pipelined protocol, with Mask-Write-Response turned on (BRIDGE_MODE[2:0]==011_B) and the BRIDGE_MODE.MSK_WR_RSP is turned off (by writing BRIDGE_MODE[2:0]=001_B), the following transaction might be corrupted by the AEI_READY not being set.
This is an issue like in GTM_AI.421 and GTM_AI.487 but a different workaround is needed.

Scope

GTM_AEI

Effects

Transaction not terminated according to protocol, user might be stuck waiting for AEI_READY to be set.

Workaround

Change BRIDGE_MODE.MSK_WR_RSP together with setting the software reset (pipeline writing BRIDGE_MODE[16:0]=10001_H).

2.176 [GTM_AI.492] DPLL: Wrong value of DPLL_INC_CNT1.INC_CNT1 upon switching to normal mode

Description

***Note**: Register names in the text follow the TC3xx syntax conventions. Correlation of register and bit names:*

- ***TC2xx**: DPLL_, ICM_IRQG_1.DPLL_TAS_IRQ*
- ***TC3xx**: DPLL_, ICM_IRQG_1.DPLL_TASI_IRQ*

DPLL_CTRL_0.RMO: 1 -> 0:
Upon switching from emergency to normal mode (with DPLL_CTRL_1.SGE1 set to 1), DPLL_INC_CNT1.INC_CNT1 increments by DPLL_MLS1.MLS1 micro ticks every time an active STATE input is encountered till the first active TRIGGER input is encountered. The extra micro ticks accumulated in DPLL_INC_CNT1.INC_CNT1 will only be generated after encountering the first active TRIGGER.
The described behavior is not intended because the STATE input is not supposed to contribute to the pulse generation in normal mode.

Scope

DPLL

Effects

1. DPLL_CTRL_0.RMO: 1 -> 0

   The generation of the extra micro ticks accumulated in DPLL_INC_CNT1.INC_CNT1 after encountering the first active TRIGGER input ultimately leads to wrong angle clock (manifests in wrong CCM[0]_TBU_TS1) and wrong PMT calculations due to incorrect DPLL_PSTC.PSTC.

   Further effect, which is only applicable to GTM v4.1.0 devices:

   The value of DPLL_INC_CNT1.INC_CNT1 is not assigned to DPLL_MP_T.MP_T on the first active TRIGGER input in contrast to what is specified in MP_T description in "DPLL_MP_T" (GTM4.1 specs: DPLL_16159).

   Further observations without malicious effects:

   The value of the current position stamp is not assigned to DPLL_PSSM.PSSM at the active STATE input in contrast to what is specified in "State description of the State Machine Table" step 21 (GTM4.1 spec.: DPLL_6908). This is, however, insignificant because DPLL_PSSM.PSSM is deemed invalid in normal mode (see description of bit-field PSSM in the register DPLL_PSSM (GTM4.1 spec.: DPLL_6370)) and therefore should not be used and relied on.
2. DPLL_CTRL_0.RMO: 0 -> 1

   Upon switching from normal to emergency mode (with DPLL_CTRL_1.SGE1 set to 1), the value of the current position stamp is not assigned to DPLL_PSTM.PSTM at the active TRIGGER input "State description of the State Machine Table" step 1 (GTM4.1 spec.: DPLL_6908). This is, however, insignificant because DPLL_PSTM.PSTM is deemed invalid in emergency mode (see description of bit-field PSTM in the register DPLL_PSTM (GTM4.1 spec.: DPLL_6360)) and therefore should not be used and relied on.

   No effect is associated with not assigning the current position stamp to DPLL_PSSM.PSSM in normal mode and DPLL_PSTM.PSTM in emergency mode.

Workaround

Two possible workarounds for DPLL_CTRL_0.RMO: 1 -> 0

1. Defer setting DPLL_CTRL_1.SGE1 to 1 till the first DPLL_TASI interrupt is encountered (signaling the arrival of the first active TRIGGER)
2. Make sure that DPLL_MLS1.MLS1 is set to zero upon switching the mode. The user may then alter it on encountering the first DPLL_TASI interrupt

2.177 [GTM_AI.507] DPLL: Irregular pulse generation and wrong PMT results

Description

With the configuration of DPLL_CTRL_NUTC.NUTE = 2*(DPLL_CTRL_0.TNU +1) -1 for TRIGGER or DPLL_CTRL_NUSC.NUSE = 2* (DPLL_CTRL_0.SNU +1) -1 for STATE the prediction of the pulse generation frequency is incorrect.

This results in irregular pulse generation and wrong PMT results.

This problem occurs on either CCM[0]_TBU_TS1 or CCM[0]_TBU_TS2 or both depending on the DPLL operation mode (normal or emergency mode, or synchronous motor control).

Scope

DPLL

Effects

1. Wrong pulse generation frequency because of incorrect prediction. This leads to irregular pulse distributions
2. Wrong PMT results

Workaround

Avoid these configurations: DPLL_CTRL_NUTC.NUTE = 2*(DPLL_CTRL_0.TNU +1) -1 or DPLL_CTRL_NUSC.NUSE = 2* (DPLL_CTRL_0.SNU +1) -1.

Instead, use for example full scale configurations as described in the specification.

2.178 [GTM_AI.516] SPE-RTL: IRQ raised on disabled inputs

Description

The inputs for the interrupt generation of the SPE[i]_IRQ_NOTIFY.SPE_PERR are not fed by the masked input signals. Hence, an interrupt SPE[i]_IRQ_NOTIFY.SPE_PERR will occur when there is a pattern mismatch detected on the corresponding TIM channels beside active masking (SPE[i]_CTRL_STAT.SIE(k)=0).

Scope

SPE

Effects

An interrupt will be raised on masked input signals instead of ignoring these.

Workaround

Do not toggle (it is not used) the TIM channels that are disabled on the input side of the SPE.

2.179 [GTM_AI.517] (A)TOM: Missing edge on output signal (A)TOM_OUT

Description

If an (A)TOM channel is configured to be triggered by a previous channel by setting of (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1 (SOMP mode in ATOM) and there is a pipeline/synchronization register within the trigger chain between the triggering channel and the triggered channel, the edge to the inverse SL at the output signal (A)TOM_OUT is not generated for (A)TOM[i]_CH[x]_CM1.CM<2 and (A)TOM[i]_CH[x]_CM0.CM0>(A)TOM[i]_CH[x]_CM1.CM1. The problem only occurs if the selected clock resolution for the triggered channel has a divider factor of more than 1 related to the cluster clock CLS[i]_CLK.

Scope

ATOM, TOM

Effects

Missing edge on output signal (A)TOM_OUT.

Workaround 1

If available, use channels without a pipeline/synchronization register within the trigger chain between the triggering channel and the triggered channel.

Workaround 2a

Applicable for the error case with (A)TOM[i]_CH[x]_CM1.CM1=1:

- Switch the order of the edges, so that (A)TOM[i]_CH[x]_CM0.CM0 defines the first edge and (A)TOM[i]_CH[x]_CM1.CM1 the second edge. Additionally invert the SL value to get the same waveform on the output signal (A)TOM_OUT

***Note**: In this case, to generate 0% duty cycle, use (A)TOM[i]_CH[x]_CM1.CM1=0 and (A)TOM[i]_CH[x]_CM0.CM0>MAX.*

Workaround 2b

Applicable for the error case with (A)TOM[i]_CH[x]_CM1.CM1=0:

- Set (A)TOM[i]_CH[x]_CM0.CM0=MAX and (A)TOM[i]_CH[x]_SR0.SR0=MAX by writing them before the target period. Set (A)TOM[i]_CH[x]_CM1.CM1 to the original application value of (A)TOM[i]_CH[x]_CM0.CM0. Additionally, invert the SL value to get the same waveform on the output signal (A)TOM_OUT

Workaround 3

Use a clock resolution for the triggered channel with a divider value of 1 related to the cluster clock.

2.180 [GTM_AI.522] (A)TOM: Edge at output signal (A)TOM_OUT does not occur

Description

If the channel is configured to be triggered by a preceding channel with (A)TOM[i]_CH[x]_CTRL.RST_CCU0=1_B (SOMP mode for ATOM) and the duty cycle switches from 100% duty cycle with (A)TOM[i]_CH[x]_CM0.CM0=0_H and (A)TOM[i]_CH[x]_CM1.CM1>MAX to a left-aligned PWM or to 0% duty cycle with (A)TOM[i]_CH[x]_CM1.CM1=0_H and (A)TOM[i]_CH[x]_CM0.CM0>0 for left-aligned PWM or (A)TOM[i]_CH[x]_CM0.CM0>MAX for 0% duty cycle, the expected edge on the output signal (A)TOM_OUT to the inverted (A)TOM[i]_CH[x]_CTRL.SL value does not occur.

***Note**: If the setting after switching to a left-aligned PWM or to 0% duty cycle is not changed, the edge appears at the beginning of the next period.*

Scope

ATOM, TOM

Effects

Output signal (A)TOM_OUT remains at (A)TOM[i]_CH[x]_CTRL.SL value.

Workaround

In the period before the change to a left-aligned PWM or to 0% duty cycle, set the value of (A)TOM[i]_CH[x]_CM1.CM1 to MAX instead of greater than MAX. This can be done asynchronously by writing the bit-field (A)TOM[i]_CH[x]_CM1.CM1 within the period.

Alternatively, it can be done via the synchronous update mechanism by writing the bit-field (A)TOM[i]_CH[x]_SR1.SR1 two periods before switching to a left-aligned PWM or to 0% duty cycle.

2.181 [GTM_TC.010] Effects of GTM Resets

Description

The following recommendations to avoid side effects of GTM resets should be considered.

***Note**: These effects have not been seen yet in real applications, but have been reported by static timing analysis as potential failure.*

GTM Kernel Reset

The GTM module (including the implementation wrapper) can be reset via software by a kernel reset (bit RST in registers GTM_KRST0/1). Potential side effects are:

- The GTM SRAM contents may be unexpectedly modified
- False alarms might be generated after restarting the GTM sub-modules (FIFO, DPLL, MCS) as a result of it in case the SRAM contents was not re-initialized

Workaround

Initialize the GTM SRAMs after a GTM kernel reset is issued by the application. The SRAM contents must not be read by the GTM modules (FIFO, DPLL, MCS) before it is overwritten by initialization (i.e. none of the mentioned GTM modules must be switched on before).

GTM Global Reset

The GTM module (except the implementation wrapper) can be reset via software by a GTM global reset (bit RST in registers GTM_RST). Potential side effects include:

- The GTM SRAM contents may be unexpectedly modified
- PSI5 functionality might be unreliable while the GTM global reset is performed
- Starting/ongoing MSC transmissions might be unreliable while the GTM global reset is performed

Workaround

The GTM global reset must not be used. Use the GTM kernel reset instead.

2.182 [GTM_TC.012] Read Access Control by Register ODA

Description

Specific GTM registers have by default “destructive read” behavior as their normal read behavior (see section “GTM Software Debugger Support” in the GTM chapter of the User’s Manual for further details.)

Depending on the reading master and the configuration of bits DREN and DDREN in register GTM_ODA (OCDS Debug Access Register), the read can be performed “non-destructive” for debug related read operation.

According to the User’s Manual the read is performed “non-destructive” (i.e. debug related read operation)

- for all masters when ODA.DREN = 1_B
- for the Cerberus (OCDS) FPI master when ODA.DREN = 0_B and ODA.DDREN = 0_B

Problem Description

In the current implementation the read is performed “non-destructive” (i.e. debug related read operation)

- for all masters when ODA.DREN = 1_B
- for the DMA Partition 2 FPI master when ODA.DREN = 0_B and ODA.DDREN = 0_B

Workaround

The problem described above has 2 aspects:

1. For DMA Partition 2 Access to GTM

When the DMA Partition 2 FPI master is used to perform a normal (“destructive”) read of the GTM registers that by default have “destructive read” behavior as their normal read behavior, setting ODA.DREN = 0_B and ODA.DDREN = 1_B is required to avoid an unintended debug related (“non-destructive”) read access that would be caused by this issue.

2. For Cerberus (OCDS) Access to GTM

When ODA.DREN = 0_B and ODA.DDREN = 0_B, any read access of the Cerberus (OCDS) FPI master to the registers that by default have “destructive read” behavior as their normal read behavior will cause the normal (“destructive”) read behavior. To get the intended debug related (“non-destructive”) read behavior, ODA.DREN needs to be set to 1_B before each access of the Cerberus and set back to 0_B afterwards to not affect the access of other FPI masters on the registers described above.

2.183 [HSCT_TC.007] RX_FIFO overflow interrupt

Description

If a receive path FIFO overflow condition occurs, the corresponding event is not indicated via bit IRQ.SFO (Synchronization FIFO overflow in RX direction), and no interrupt (HSCT Service Request) is generated.

***Note**: This interrupt would be an indication about a too slow SRI clock in relation to the Physical layer clock, which results in an overflow situation. (Minimum SRI frequency 40 MHz @ a 320 Mbit baud rate.)*

2.184 [HSCT_TC.009] Sleep mode not to be used

Description

Due to problems with the wake-up functionality, sleep mode is not to be used.

2.185 [HSCT_TC.010] Master Mode Interface Test Mode not working

Description

The HSCT Master Mode Interface Test Mode to send out a 101010101..$_B$ test pattern continuously does not work correctly.

Workaround

Do not enable the HSCT Master Mode Interface Test Mode, i.e. leave bit IFCTRL.IFTESTMD = 0_B (default after reset). Instead, send out a test pattern under software control.

2.186 [HSCT_TC.014] HSCT PLL lock loss error during the start-up of PLL

Description

The High Speed Communication Tunnel (HSCT) implements a PLL used for high-speed mode operation.

The PLL is turned on:

1. In master mode operation by register CONFIGPHY.PLLON or
2. In slave mode operation by an interface control command "Slave interface clock multiplier start (in preparation for high speed mode)" sent from master device to slave device

After the PLL is turned on, it starts to lock to the PLL’s reference clock. The lock status of the PLL is indicated by the bit STATPHY.PLOCK.

Once the PLL has been locked and remains turned on, any transition of lock status to unlock status inside STATPHY.PLOCK triggers IRQ.PLER being set to"1". IRQ.PLER stays high, as long as is not cleared by software using IRQCLR.PLERCLR bit.

After STATPHY.PLOCK shows lock status, there is a possibility that the PLL is unlocked once for a short time (t_{glitch}) again at start-up phase, as shown in the figure below. This single unlock event as indicated by STATPHY.PLOCK recovers back to lock status without any software intervention.

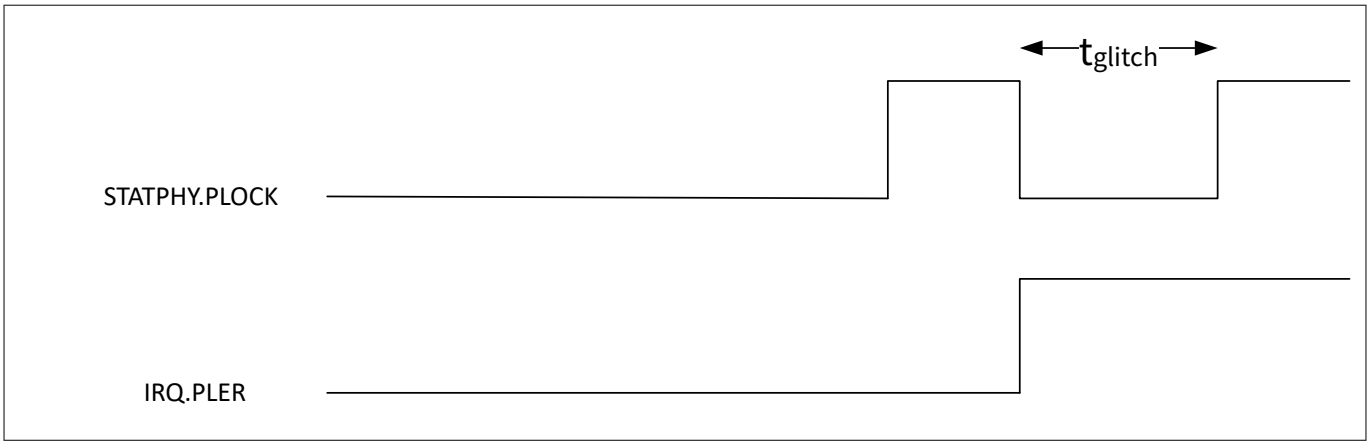

Figure 4 PLL Unlock Event Glitch

The minimum time duration of t_{glitch} is 224 cycles of the PLL reference clock (RefClk). An example of minimum t_{glitch} duration for RefClk with 20 MHz and 10 MHz is shown in the table below.

Table 8 Unlock Event Glitch Minimum Duration

	t_{glitch} in µs	t_{glitch} in number of RefClk cycles
RefClk = 20 MHz	11,2	224
RefClk = 10 MHz	22,4	224

Effects

At PLL start-up, the software is notified with the loss of lock error event through IRQ.PLER interrupt, even though the PLL recovers to lock state within t_{glitch}.

Workaround

To avoid any unnecessary treatment, it is recommended for each PLER interrupt event to wait a time of not less than t_{glitch} + 1 µs and check STATPHY.PLOCK. If STATPHY.PLOCK indicates that the PLL is locked again, then ignore the PLER interrupt event by clearing the interrupt using IRQCLR.PLERCLR.

2.187 [I2C_TC.001] I2C FIFO data buffer does not support double buffering

Description

Double buffering in the FIFO data buffer allows:

- The TPS value and characters of the next data packet to be written while data transmission on a previous data packet is still ongoing
- The MPRS value of the next data packet to be written and its characters received into the RXFIFO while the previous data packet is still not completely read out of the RXFIFO

However in the current implementation, this feature is not supported.

Workaround

For data transmission, the TPS value of the next data packet can be programmed only after the previous data packet has been successfully transmitted and the TXFIFO is empty again. After the new TPS value is programmed, the I2C module generates a data transfer request and the next data transmission will start when new data is available.

Similarly for data reception, the MPRS value of the next data packet can be programmed only after the full reception of the previous data packet. This means after all requests are handled and cleared, and data has been read out of the RXFIFO. The next data reception is then possible.

2.188 [I2C_TC.003] Limits on selectable INC and DEC values

Description

The two most significant bits of bit-field INC in registers FDIVCFG.[23:22] and FDIVHIGHCFG.[23:22], and the most significant bit of bit-field DEC in register FDIVHIGHCFG.10 cannot be used.

Workaround

When configuring the fractional divider for baud rate generation:

- Use only the least significant six bits of INC; i.e. values equal or less than 63_D
- Use only the least significant ten bits of DEC in register FDIVHIGHCFG; i.e. values equal or less than 1023_D

Example

The following Table 9 shows some examples for achieved baud rates and their deviation from the target baud rate depending on the settings of INC and DEC in registers FDIVCFG and FDIVHIGHCFG, respectively.

Table 9 Baud Rate Deviation depending on INC / DEC

Target Baud Rate [kbit/s]	Kernel_Clk [MHz]	Kernel Period [µs]	INC	DEC	Achieved Baud Rate [kbit/s]	Deviation
100	100	0.01	2_D	997_D	100	0.00%
400	100	0.01	2_D	247_D	400	0.00%
3400	100	0.01	31_D	170_D	3399.1	-0.03%

***Note**: As described in the User's Manual (section Baudrate Generation), the actual baud rate depends on further factors and differs from these theoretical calculations. The final settings of INC and DEC for a given system should be optimized by measurements.*

2.189 [I2C_TC.004] High speed mode: SCL clock ratio 1:2

Description

The standard for the clock ratio of the I2C high speed mode is 1:2. The ratio is programed in the DEC/INC bit-fields of the FDIVHIGHCFG register.

Recommendation

In order to achieve a 3.4 MHz frequency for high speed mode with the best deviation case for the 1:2 duty cycle ratio, DEC and INC have to be programmed with the following values. Note that not for every f_{baud1}/DEC/INC combination 0% deviation can be achieved.

Table 10 1:2 Duty Cycle Ratio

f_{baud1} (MHz)	INC	DEC	f_{SCL} (MHz)	Duty Cycle(%)
100	85	466	3.4	25.44
90	1	5	3.33	25.92
90	85	416	3.4	26.04
61	5	16	3.39	33.33

2.190 [I2C_TC.005] Hold Time Start violation in Multi-Master Mode

Description

The I2C Standard defines the parameter $t_{HD;STA}$ (Hold Time (repeated) START condition) as 4.0 µs for Standard mode and 0.6 µs for Fast mode. After this period, the first clock pulse is generated.

The parameter $t_{HD;STA}$ is represented in the Infineon TC2xx Data Sheets as t_7 (Hold Time for the (repeated) START condition).

In a special situation this design step of the I2C module violates this timing specification by ~30% for Standard mode and by ~18,6% for Fast mode (min . 2.8 µs instead 4.0 µs for Standard mode and min. 0,488 µs instead 0,6 µs for Fast mode).

This occurs when data is written into TX FIFO, the I2C module is ready to start transmission and another master starts driving its startbit shortly before the I2C module starts driving. In this case the I2C Finite State Machine tries to win arbitration by reloading approximately half period in baudrate generator, so next SCL clock edge of the I2C module comes earlier than defined by t_7.

2.191 [IOM_TC.002] Missed or spurious IOM events when pulse length exceeds Event Window counter range

Description

When using the Logic Analyzer Module (LAM) of the IOM, if the 24-bit counter for the Event Window exceeds its maximum value (0xFFFFFF) it wraps around and starts counting again from 0x0.

If the Event Window is not inverted (LAMCFG.IVW = 0_B), for example for measuring long pulses, and the edge that generates an event comes after the counter exceeded its maximum value, the event will not be generated if the counter, due to the rollover, is again below the threshold value (LAMEWS.THR), outside of the Event Window.

As an additional side effect of the wraparound, spurious events may be generated when expecting an alarm only in case of pulses that are too short, if a pulse is longer than the counter can handle.

Workaround

Avoid measuring pulses longer than the Event Window counter range.

2.192 [IOM_TC.003] Unexpected Event upon Kernel Reset

Description

If a kernel reset (via bits RST in registers KRST0/1) is performed on the IOM, an unexpected event may be signalled to the SMU.

Workaround

Before triggering a kernel reset via software, set the alarm reaction in SMU to “No Action” to avoid reaction on the unexpected event.

2.193 [IOM_TC.004] Write to IOM register space when IOM_CLC.RMC > 1

Description

If a clock divider value RMC > 1 is selected in register IOM_CLC, more than one write access may be performed to the IOM register address space within one IOM clock cycle.

This will cause unpredictable effects on the internal state for the following scenarios where two (or even multiples of 2) write accesses are performed within one IOM clock cycle to the following register groups:

- ECM registers ECMCCFG and/or ECMSELR, or

- ECM Event Trigger History registers ECMETH0 and/or ECMETH1, or
- FPC registers FPCESR, FPCCTRk and/or FPCTIMk, or
- LAM registers LAMCFGm and/or LAMEWSm

***Note**: No problem will occur for read accesses.*

Workaround

Set IOM_CLC.RMC = 1 when configuring (writing to the registers of) the IOM.
During runtime (not configuring IOM) IOM_CLC.RMC > 1 is not an issue.

2.194 [MSC_TC.012] Increased Jitter for Data Frame Transmission in Repetition Mode with ABRA

Description

When the MSC module is configured in repetition mode with ABRA active, command frames can be inserted at any time, starting at equidistant time reference points (TRPs).
The length of a command frame (including passive phase) is defined as follows:

- cmd_len = (1 + DSC.NBC + DSTE.PPCE + 2) x bit time[4)]

The time between two TRPs is defined in this context as

- tframe_len = number of bit times between 2 TRPs

Depending on the relation between cmd_len and tframe, two specific scenarios can occur that lead to an increased jitter for data frame transmission:

Scenario 1: cmd_len = tframe_len -1

If the length of the command frame (cmd_len) is equal to the number of bit times between two TRPs minus 1 (tframe_len - 1), then the data frame is not started at the next free TRP, but at the TRP when all passive time frames are finished (in equidistant raster).
This means there is an increased jitter for the equidistance of data frame starts, because there is a complete passive time frame sequence (NTPF) without any data frame transmission.

Scenario 2: cmd_len = tframe_len

If the length of the command frame (cmd_len) is equal to the number of bit times between two TRPs (tframe_len), then the next data frame is started correctly at the next TRP, but the passive phase of this data frame will erroneously be increased by one bit time, also increasing the jitter for TRPs in repetition mode.

Workaround

Avoid the two length configurations for the command frame including its passive phase that are equal to the two scenarios described above:

- cmd_len = tframe_len -1, or
- cmd_len = tframe_len

[4] where DSC.NBC and DSTE.PPCE is the (decimal) contents of the respective bit-fields in the corresponding registers

2.195 [MSC_TC.013] Missing Chip Select for Command Frame with Length zero

Description

When the MSC module is configured in repetition mode, and the asynchronous ABRA mode is enabled, and the serial clock output FCL is in permanent mode (OCR.CLKCTRL = 1_B), then the following problem may occur for command frames with length zero:

If a command frame is started with zero bit length (DSC.NBC = 000000_B), then the transmission of one bit (selection bit SEL) is started, and a command interrupt is generated correctly. In some cases, however, the chip select signal for the command frame may not be generated.

Workaround

Configure the MSC module such that not all of the following settings are active at the same time:

- DSC.TM = 1_B (data repetition mode enabled)
- OCR.CLKCTRL = 1_B (FCL always active)
- DSC.NBC = 000000_B (0 bits shifted during command frame transmission)
- ABC.ABB = 1_B (asynchronous block active, not bypassed)

If one of the conditions listed above is not valid, then the problem cannot occur.

2.196 [MSC_TC.014] Upstream Timeout Interrupt cannot be issued at Service Request Output SR4

Description

When the watchdog timer (defined by USTE.USTOPRE and USTE.USTOVAL) of the upstream channel is decremented to zero the timeout flag (USTE.USTF) will be set and an interrupt should be issued at one of the 5 service request outputs. The pointer USCE.USTOIP directs the interrupt correctly to the service request lines 0,1,2,3, but if the alternate service request output SR4 is configured (USCE.UTASR = 1_B), then erroneously no interrupt occurs if the ABRA overflow interrupt is also directed to SR4 (i.e. ABC.OASR = 1_B).

Workaround

Do not use the alternate service request output SR4 (USCE.UTASR = 1_B) for the upstream timeout interrupt if the ABRA overflow interrupt is also directed to SR4 (i.e. ABC.OASR = 1_B).

Instead, select one of the service request outputs SR0..SR3 via the SR multiplexer for the upstream timeout interrupt (USCE.UTASR = 0_B).

2.197 [MSC_TC.015] Emergency Stop not effective at Injected Bit Positions in Downstream Frame

Description

Before a data frame on the downstream channel is started, the configured data bits are loaded into the shift register (SRL, SRH).

If an emergency stop condition is active (signal EMGSTOPMSC = 1) during the load operation, all SRL[x] /SRH[y] bits that are enabled for the emergency stop feature in register ESR/ESRE are loaded directly with the corresponding bits of the downstream data registers DD/DDE.

However, the emergency stop feature is not effective for bits that are enabled in addition for an external injection (DSCE.INJENP0/1 =1, position defined by DSCE.INJPOS0/1). This means the injection feature will not be overruled by the emergency stop feature.

Workaround

Do not enable the same data bits with DSCE.INJPOS0/1 for injection and with ESR/ESRE for emergency stop.
Or disable injection via software when an emergency stop condition has occurred.

2.198 [MTU_TC.005] Access to MCx_ECCD and MCx_ETRRi while MBIST disabled

Description

It is possible to access the memory controller registers MCx_ECCD and MCx_ETRRi without the need of the MBIST mode being enabled (i.e. without MTU_MEMTEST.MEMxEN = 1_B). This may be used to avoid a complete SRAM initialization on certain security relevant SRAMs.

However, when a MBIST controller is disabled (MTU_MEMTEST.MEMxEN = 0_B), there is an inevitable corner case that causes the value read/written from/to registers MCx_ECCD and MCx_ETRRi of a disabled MBIST controller to be wrong. There is also a possibility that an SPB error is triggered when accessing the MCx_ECCD and MCx_ETRRi registers if other masters concurrently use the SPB bus in this situation.

***Note**: No workaround is required to access the registers of an enabled MBIST controller.*

Workaround

When MBIST mode is disabled (MTU_MEMTEST.MEMxEN = 0_B) for a MBIST controller,

- ensure that the module kernel clock is enabled for the access to MCx_ECCD and MCx_ETRRi
- and perform a dummy write to MCx_ECCD with value $780F_H$ before any read/write access to MCx_ECCD or MCx_ETRRi

***Note**: The module kernel clock (of the module in which the SRAM is present) does not need to be enabled if it can be ensured that no concurrent SPB bus accesses by other masters (CPU, DMA, HSM, debugger, ..) to other modules are performed during the MCx_ECCD/ETRRi access while the module kernel clock is disabled.*

The module kernel clock is enabled under the following conditions:

1. For CPU memories, the clock is enabled after reset (for CPUx with x>0 even when CPUx is still in BOOT-HALT mode), when the CPU is not explicitly put into IDLE mode by software
2. For SRAMs in peripherals, the module kernel clock is enabled when the module clock is enabled via the CLC register

The value $780F_H$ has been chosen as an example based on the following use cases and assumptions:

- If error reporting is turned on (i.e. notification enable bits *ENE are set), it does not disturb the system to write back $780F_H$ to register ECCD (write back of reset values, write to read-only bits and write of 1_B to error indication bits has no effect)
- If error reporting is turned off (i.e. notification enable bits *ENE are cleared), write back of $780F_H$ to register ECCD may trigger SMU alarms (if SMU is configured). It is assumed that the corresponding errors are already known by the system since error reporting had previously been deactivated

2.199 [MTU_TC.011] MBIST Bitmap not working for w0 - r1

Description

The simple test case of writing all 0 and checking for 1 should return a full bitmap.
However, in this device step, only one (the last) address of the SRAM is returned.

Workaround

Use the reverse test w1 - r0, which is working as expected and returns the full bitmap.

2.200 [MTU_TC.012] Security of CPU cache memories during runtime is limited

Description

MTU chapter “Security Applications” in the User’s Manual describes that selected memories with potentially security relevant content are initialized under certain conditions to prevent reading of their data or supplying manipulated data.

The description is correct, but the initialization of CPU cache and cache tag memories triggered by MBIST enable/disable and when mapping/un-mapping these memories to/from system address space using MEMMAP register is of limited value:

- These memories stay functional as cache in the address mapped state. Therefore software can enable address mapping and afterwards watch cache usage of the application (this is a debug feature). Even manipulation of the cache content is feasible
- It is possible to abort an ongoing memory initialization

The security of memory initialization during startup is not affected. Also protection of FSI0 and HSM memories is not limited.

Workaround

Handle security relevant data exclusively inside HSM. Protect the application code by locking external access (for example lock debug interface, prevent boot via serial interface). Consider validation of application code by HSM secure boot.

2.201 [MTU_TC.016] Wrong Address(es) Tracked in Registers ETRRx of TC1.6E CPU0 PSPR and DSPR

Description

***Note**: In **TC23x step AB**, this problem only affects variants TC23xLA, TC23xLX, and TC23xLF.*

Due to certain hardware limitations, the SRAM error address tracking functionality in the Memory Controller of the TC1.6E CPU0 PSPR and DSPR does not work correctly under the following sequence of conditions:

1. A read access occurs to an SRAM location ERR_ADDR with a (correctable or uncorrectable) ECC error, AND
2. Exactly in the next consecutive SRAM clock cycle another read or write occurs to a different location ADDR_A which does not have any error

Then, instead of ERR_ADDR, the address corresponding to this second location ADDR_A is stored in ETRRx.

For the problem to occur, it only matters that the accesses have to be in consecutive cycles, and both ERR_ADDR and ADDR_A are in the same SRAM (PSPR or DSPR). It does not matter whether the accesses are from the same or a different CPU or other bus master.

***Note**: The ECC error correction and detection still work as specified, and are not affected in any way by this problem. All the SMU alarms work as specified, i.e. there is no alarm lost due to this problem.*

Both the CPU0 PSPR and DSPR are protected by SECDED-ECC, which can correct a single-bit error notified by the Correctable Error Alarm ALM0[6], ALM0[10], and detect a double-bit error notified by the Uncorrectable Error Alarm ALM0[7], ALM0[11].

Only the above mentioned ECC errors are affected by this problem. Registers ETRRx additionally track Address Errors in the SRAMs notified by ALM0[8], ALM0[12]. These are not affected by this problem, and the SRAM Address Errors are still correctly tracked.

When registers ETRRx are filled, an additional error triggers an overflow error alarm notified by ALM0[9], ALM0[13].

Impact

When such a consecutive access sequence (read from ERR_ADDR followed by read/write of different address(es)) happens multiple times, registers ETRRx are filled with addresses that have actually no error – and the SRAM address which actually has an error is not stored indeed. Figure 5 shows such an example scenario.

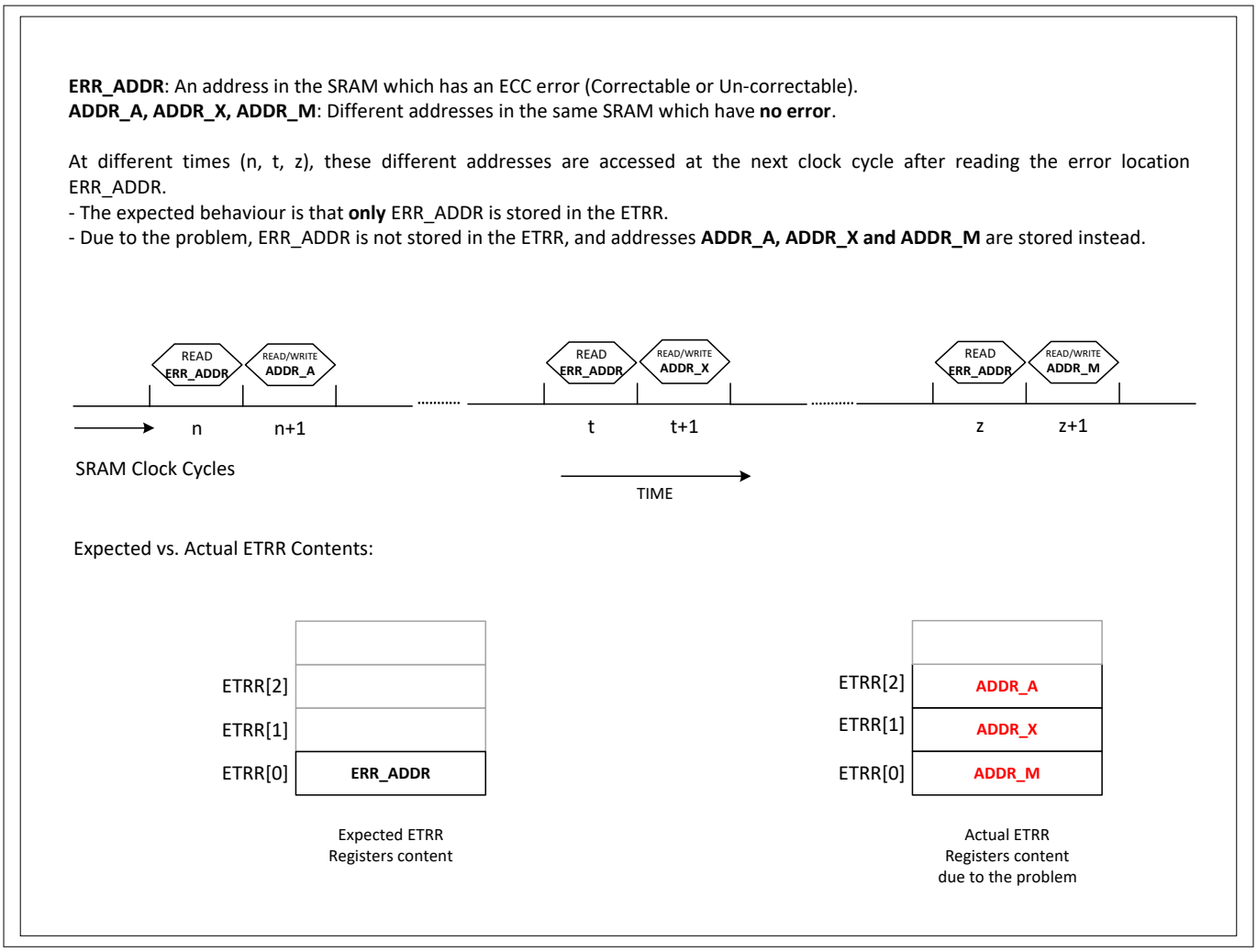

Figure 5 Example sequence showing how registers ETRRx may be filled with "Error Free" addresses

The consequence of the scenario explained in Figure 5 is that a single error in the SRAM – example just one correctable error at a location ERR_ADDR – can result in registers ETRRx getting filled with fault-free address, and thus potentially even triggering an ETRR overflow.

Conclusion

The problem explained here has two consequences:

1. For the affected SRAMs, the addresses stored in ETRRx may not be reliable. Depending on the access sequences, ETRRx may contain the correct error address, or in the worst case all ETRRx entries may contain fault-free addresses
2. Depending on the access sequences, an ETRR overflow might be triggered with one real error (for example correctable error) in the SRAM – consequence of the example shown in Figure 5

Workaround

A flowchart of the recommended software handling is shown in Figure 6.

For the affected SRAMs, disable the application reaction to the EOV (Error Overflow) alarm in the SMU. The ETRR error tracking in the memory controller shall remain enabled (MCx.ECCS.TRE = 1_B).

At the end of each multiple-point fault detection interval (MPFDI), check for at least one valid ETRR entry for the affected SRAMs (i.e. if MCx.ECCD.VAL > 0).

For each affected SRAM, if there are no valid ETRR entries (i.e MCx.ECCD.VAL = 0) this means that no error has occurred at all, hence the application can continue without any special measure.

If there is at least one valid ETRR entry (i.e. MCx.ECCD.VAL ≠ 0) then the software shall run a Non-Destructive-Inversion (NDI) Test on the affected SRAM. Please refer to application note AP32197 (AURIX™ Memory tests using the MTU) for an example regarding running this test.

At the end of this test, if an ETRR overflow is detected (MCx.ECCD.EOV = 1_B) then the MCU shall be considered non-operational. Refer to section on Correctable SRAM Error handling in the Safety Manual.

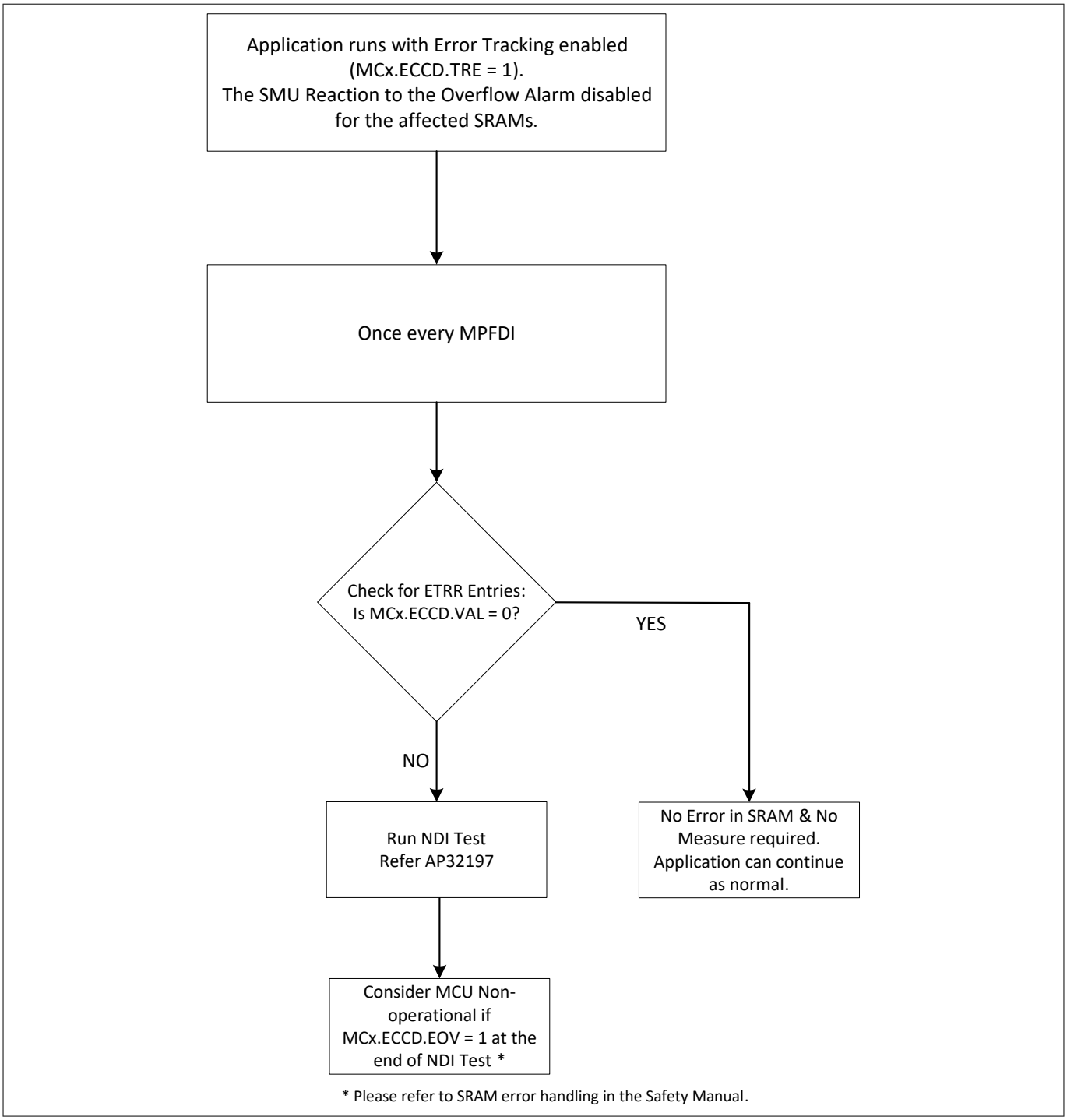

Figure 6 Recommended Software Handling - Flowchart

***Note**: There is no change in the concept of handling Uncorrectable error and Address error alarms in the affected SRAMs.*

Alternative Option

Run the Non-Destructive-Inversion Test at application start-up, and at the end of this test, if an ETRR overflow is detected (MCx.ECCD.EOV = 1_B) then the MCU shall be considered non-operational.

2.202 [MultiCAN_TC.041] Clock used in Bit Timing Mode

Description

Unlike described in some parts of the documentation, in Bit Timing Mode f_{CLC} is used instead of f_{CAN}. This means that the time information stored in bit-field NFCRx.CFC is measured in f_{CLC} clock cycles.

Workaround

No workaround is available.

2.203 [OCDS_TC.038] Disconnecting a debugger without device reset ("hot detach") may require reading of OCS registers

Description

If a debugger disconnects, it should activate at least the Debug Reset. This will reset all the main OCDS resources like CPUs, Cerberus, etc. However for peripherals having a BPI interface, there is the following issue: The Debug Reset is implemented as a synchronous clear on this level. If the OCDS registers are not clocked (for example for power saving reasons), the effect of this synchronous clear will be delayed to the next activation of the clock.

In general this will be more a theoretical problem. It's very unlikely that there is a use case, where a hot detach is required and critical OCDS resources of peripherals were used before. In nearly all cases this effect is invisible for a user, since any register access of the peripheral will generate the clock cycles which are required for the synchronous clear.

Workaround

In case of a hot detach, a tool should - after the Debug Reset activation - read the OCS registers of all peripherals where it used critical OCDS resources. These reads will initiate the required peripheral kernel clocks for the synchronous clear of the OCDS resources.

2.204 [OCDS_TC.040] DAP turn_off to JTAG telegram not working properly

Description

In case of an unsolicited PORST, a JTAG tool will usually not be able to activate the $\overline{\text{TRST}}$ pin as well and by this enable the JTAG interface again after this PORST is released. So the device interface is in DAP mode and not in JTAG mode afterwards.

For this situation the DAP telegram turn_off to JTAG exists, which is JTAG compliant in the sense, that it is a valid and uncritical JTAG TMS control pattern.

The erratum is that the telegram can't be used directly after a PORST, but requires a dapisc telegram before. This is no problem for DAP tools, but it requires a workaround for JTAG tools.

Please note that this behavior is still much more robust than regular JTAG behavior, where the JTAG operation of the device is completely uncontrolled (for example boundary scan enabled), when the tool continues to communicate without noticing that an unsolicited PORST occurred.

Workaround A

Use DAP instead of JTAG.

Workaround B

Recover with another PORST controlled by the JTAG tool.

Workaround C

A fast tool hardware can automatically activate $\overline{\text{TRST}}$ when a PORST is sensed. However this does not work for example for the TriBoard since there is a level shifter between OCDS L1 connector and device.

Workaround D

Apply an extended TMS pattern, which includes the dapisc telegram

1. Make sure that the JTAG interface is NOT enabled. Trying to read the JTAG ID with the robust sequence JTAG TAP reset followed by a DR scan. If the device is in DAP mode this request is ignored because it is an invalid telegram
2. Make sure that the device is in the DAP state `waiting for start bit`. Apply 64 clock cycles with TMS low to potentially drive the DAP module through a CRC error recovery
3. Apply dapisc telegram with a specific DAPISC.MODE value The DAPISC.MODE value is chosen that the reply telegram is output on TDO (DAP2). The complete dapisc TMS pattern are the 66 bits $2A4ABBAF530F20C23_H$, output with LSB first. This pattern has to be followed by 30 or more clocks with TMS low (device responds on TDO)
4. Apply turn_off to JTAG telegram The complete turn_off to JTAG TMS pattern are the 56 bits $FFFF0F8FCEF83F_H$, output with LSB first. After this the JTAG TAP controller is in reset state and JTAG communication can be started

2.205 [OCDS_TC.042] OTGS capture registers can miss single clock cycle triggers

Description

The Cerberus OTGS capture registers (TCTL, TCCB, TCCH, TCIP, TCTGB, TCM) can fail to capture a trigger if the trigger is of single clock cycle duration and arrives in the same cycle as the same trigger register is being read by the bus.

Workaround

Avoid polling of OTGS capture registers while the system is running.

If polling while running can’t be avoided use TLCCx counters for capturing critical Trigger Lines.

2.206 [OCDS_TC.043] Read-Modify-Write Bus Transactions to Cerberus Registers

Description

During read-modify-write (RMW) bus transactions to writable registers in the Cerberus (CBS), the target register is incorrectly updated with an undefined value during the Read-part. The correct value is always returned to the bus master for the Read-part, and the correct value is written to the register when the Write-part completes. But the register may contain an undefined value for a number of clock cycles between the Read-part and the Write-part.

The bus master (CPU) will see the RMW complete normally, but any logic driven by the hardware register's writable bits may be unexpectedly toggled.

This effects all registers that can be written by the SPB (using the FPI protocol) in the CBS block. It does not effect external access from the tool via JTAG/DAP.

Workaround

Do not use RMW bus operations targeting the CBS registers.

2.207 [PADS_TC.012] Pull-ups activate on specific analog inputs upon PORST

Description

If HWCFG[6] = 1 or PMSWCR0.TRISTREQ = 0, respectively, the following analog inputs in the V_{DDM} domain:

- analog inputs overlaid with general purpose inputs (class S pads) on all pins of P40
- analog inputs (class D pads) of channels with multiplexer diagnostics[5)]

will activate internal pull-ups during cold or warm PORST.

When PORST is deasserted and the internal circuitry is reset, the inputs mentioned above will be released to tri-state mode.

***Note**: This behavior differs from the description in the "Ports" chapter of the User's Manual (P40 always in tri-state mode during PORST) and the Data Sheet (corresponding pins marked with symbol "HighZ" in columns for buffer/pad type of the pin definition tables).*

2.208 [PLL_ERAY_TC.001] PLL_ERAY Initialization after Cold Power-up or Wake-up from Standby mode

Description

When the PLL_ERAY is configured by the application software after cold power-on reset or wake-up from Standby mode, it may not always reach the intended target frequency (either lock at a lower frequency, or go into unlock state), in particular at high temperature.

Workaround

The following code sequence, executed after power-on reset or wake-up from Standby mode and before initializing the PLL_ERAY, avoids the problem:

```
SCU_PLLERAYCON0.B.PLLPWD = 0;  // set PLL_ERAY to power saving mode
wait(10);                      // wait 10µs
SCU_PLLERAYCON0.B.PLLPWD = 1;  // set PLL_ERAY to normal behavior
...                            // initialize PLL_ERAY
```

2.209 [PLL_TC.005] PLL Initialization after Cold Power-up or Wake-up from Standby mode

Description

When the system PLL is configured by the application software after cold power-on reset or wake-up from Standby mode, it may not always reach the intended target frequency (either lock at a lower frequency, or go into unlock state), in particular at high temperature.

5 These channels are explicitly marked with (MD) in table "Analog Connections in the TC2yx" in the AURIX™ TC2yx User's Manual.

Workaround

The following code sequence, executed after power-on reset or wake-up from Standby mode and before initializing the system PLL, avoids the problem:

```
SCU_CCUCON0.B.CLKSEL = 0;       // switch system clock to another source different from PLL,
                                // e.g. back-up clock
SCU_CCUCON0.B.UP = 1;           // request update
while(SCU_CCUCON0.B.LCK == 1);  // wait for update handshake (see separate Note below)
SCU_PLLCON0.B.PLLPWD = 0;       // set PLL to power saving mode
wait(10);                       // wait 10µs
SCU_PLLCON0.B.PLLPWD = 1;       // set PLL to normal behavior
...                             // initialize PLL
```

***Note**: For devices with PLL_ERAY, see also problem PLL_ERAY_TC.001*

Note on update handshake

LCK = 0 indicates the end of the update handshake. Instead of polling LCK, other instructions may be executed that bridge this time.

The minimum number of instruction cycles n_{UH} (cycles of f_{SRI}) required to bridge the maximum time for the update handshake depends on the least common multiple of the active clock divider factors > 0 that are effective in CCUCON0/1/2/5 before the update by CCUCON0.B.UP = 1 in the sequence above is requested. For LPDIV = 0, this set includes FSIDIV, FSI2DIV, SPBDIV, SRIDIV, BAUD2DIV, BAUD1DIV, ASCLINSDIV, ASCLINFDIV, GTMDIV, STMDIV, CANDIV, MAXDIV, BBDIV.

This results in the following range when SRIDIV = 1 ($f_{SRI} = f_{SOURCE}$):

- n_{UH} ≥ 17 if the active clock divider factors are any of the elements of the set {1, 2, 3, 4, 6, 12}
- n_{UH} ≥ 29 if factor **8** is included in the set of {1, 2, 3, 4, 6, **8** , 12}
- n_{UH} ≥ 65 if factor **5** (or multiples of 5) are included in the set of {1, 2, 3, 4, **5** , 6, **10** , 12, **15**}
- n_{UH} ≥ 125 if factors **5** (or multiples of 5) and **8** are included in the set of {1, 2, 3, 4, **5** , 6, **8** , **10** , 12, **15**}

When SRIDIV = n > 1, only n_{UH} /n instruction cycles are required to bridge the maximum time for the update handshake, as the instructions take n times longer.

For LPDIV > 0, the divider factors for f_{SRI}, f_{SPB}, f_{BBB} and f_{MAX} are determined by LPDIV. As instruction execution is slowed down by the ratio defined by LPDIV, the number of instructions to bridge the time for the update handshake is scaled accordingly.

***Note**: For the allowed clock ratios see table “CCU allowed Clock Ratios” in the User’s Manual.*

2.210 [PLL_TC.007] PLL Loss of lock when oscillator shaper is used

Description

Under certain conditions the PLL loses lock when the oscillator shaper is used (OSCCON.SHBY = 0_B, recommended system configuration, default after reset).

The fail behavior is not observed for oscillator frequencies f_{OSC} ≤ 25 MHz when using an external crystal/ ceramic resonator or supplying the clock signal directly.

Workaround

It is recommended to use input clock frequencies f_{OSC} ≤ 25 MHz.

***Note**: For devices with PLL_ERAY, the problem also applies to PLL_ERAY.*

2.211 [PMC_TC.004] Field SDFREQSPRD in register EVRSDCTRL1 – Documentation update

Description

Due to the correction of problem PMC_TC.H003 (SMPS Regulator Static Voltage Output Accuracy) of earlier TC2xx design steps, the description of field SDFREQSPRD in register EVRSDCTRL1 needs to be modified.

Documentation update

In the PMC chapter of the User's Manual, the description of field SDFREQSPRD in register EVRSDCTRL1 shall be modified as follows:

Table 11 Field SDFREQSPRD in register EVRSDCTRL1 – Documentation update

Field	Bits	Type	Description
SDFREQSPRD	[15:0]	rw	**Frequency Spread Threshold** This bit-field defines the frequency spread of the nominal SMPS regulator switching frequency. 0x0 no random clock cycles added to the period 0x1 average 0.5 clock cycle of 10ns period randomly added to the period 0x2 average 1.5 clock cycles of 10ns period randomly added to the period 0x3 average 3.5 clock cycles of 10ns period randomly added to the period All other combinations are reserved

Examples

- SDFREQSPRD = 0x2: when the switching frequency is 1.8 MHz, the frequency spreading is: 1.5*10 ns*1.8 MHz = 2.7%
- SDFREQSPRD = 0x3: when the switching frequency is 1 MHz, the frequency spreading is: 3.5*10 ns*1 MHz = 3.5%

2.212 [PORTS_TC.002] Behavior of P21 Port Pins upon Power-on Reset

Description

The following problem affects port pins with LVDSH RX pads.

- For **TC29x**, these are P21.[3:0]
- For **TC27x** and **TC26x**, these are P21.[3:2]

As specified, these port pins are switched to non-LVDS input mode during cold and warm Power-on Reset.

However, in addition the 100 Ohm receiver internal termination between P21.0 and P21.1 (for TC29x) or P21.2 and P21.3 (for TC29x, TC27x, and TC26x) is switched on during Power-on Reset.

While no application impact is expected if these port pins will be used in LVDS mode, this behavior needs to be considered if one or more pins of these port pins will be used in non-LVDS mode.

If non-LVDS mode with 100 Ohm receiver internal termination is active during Power-on reset, a max. current of 5 mA is allowed without damaging the device (defining the stress for the 100 Ohm receiver internal termination).

***Note**: After power-on reset, the 100 Ohm receiver internal termination is only active if the corresponding bits RX_DIS = 0_B and TERM = 1_B in register P21_LPCR0 (for P21.0 and P21.1 in TC29x) or P21_LPCR1 (for P21.2 and P21.3 in TC29x, TC27x, TC26x), respectively.*

2.213 [PSI5_TC.005] Incorrect read pointer upon two consecutive RDFn read operations if two or more channels are configured

Description

Whenever two (or more) channels (CHm, CHn) are configured, the read pointer REP of CHn is not incremented correctly if the CHn FIFO read access (two consecutive accesses to RDFn) is performed one cycle before new data of CHm is written into its FIFO.

Scope

FIFO usage

Effects

Incorrect read pointer.

Workaround

1. Perform additional plausibility check every time there is an attempt to read the data from the receive data memory. Plausibility check verifies that the REP value is incremented after the two consecutive read operations by 2
2. If 1. is not the case, then read the stored sensor data through RDML/Hny registers, and once all the previously stored data is read, flush the FIFO buffer structure by setting bit RFCn.FLU (this will reset the WRP and REP values). From this point on, data could be read from the receive data memory through RDFn register

2.214 [QSPI_TC.006] Baud rate error detection in slave mode (error indication in current frame)

Description

According to the specification, a baud rate error is detected if the incoming shift clock supplied by the master has less than half or more than double the expected baud rate (determined by bit-field GLOBALCON.TQ).

However, in this design step, a baud rate error is detected not only if the incoming shift clock has less than half the expected baud rate (as specified), but also already when the incoming shift clock is somewhat (i.e. less than double) higher than the expected baud rate.

In this case, the baud rate error is indicated in the current frame.

Workaround

It is recommended not to rely on the baud rate error detection feature, and not to use the corresponding automatic reset enable feature (i.e. keep GLOBALCON.AREN = 0_B).

The baud rate error detection feature in slave mode is of conceptually limited use and is not related to data integrity. Data integrity can be ensured for example by parity, CRC, etc., while clocking problems of an AURIX™ master are detected by mechanisms implemented in the master.

Protection against the effects of high frequency glitches is provided by the spike detection feature in slave mode.

2.215 [QSPI_TC.017] Slave: Reset when receiving an unexpected number of bits

Description

A deactivation of the slave select input (SLSI) by a master is expected to automatically reset the bit counter of the QSPI module when configured as a slave.

This reset should help slaves to recover from messages where faults in the master or glitches on SCLK lead to an incorrect number of clocks on SCLK (= incorrect number of bits per SPI frame).

However, in this design step, the reset of the bit counter is unreliable.

Workaround

The slave should enable the Phase Transition interrupt (PT2EN = 1_B in register GLOBALCON1) to be triggered after the PT2 event “SLSI deselection” (PT2 = 101_B).

- **TC3xx**: In the interrupt service routine, after ensuring that the receive data has been copied, the software should issue a reset of the bit counter and the state machine via GLOBALCON.RESETS = 01_B
- **TC2xx**: In the interrupt service routine, after ensuring that the receive data has been copied, the software should issue a reset of the bit counter and the state machine via GLOBALCON.RESETS = 0111_B

2.216 [RESET_TC.005] Indication of Power Fail Events in SCU_RSTSTAT

Description

In case of consecutive cold resets triggered by EVR13, EVR33 or SWD power fail events, then only the last power fail event is registered in register SCU_RSTSTAT. It is not possible to distinguish individually between EVR13, EVR33 or SWD power fail events from RSTSTAT information.

Workaround

In case any power fail reset indication bit is set among EVR13, EVR33 or SWD power fail events in register SCU_RSTSTAT, it has to be assumed that all power fail events may have happened before.

2.217 [SCU_TC.034] $\overline{\text{TESTMODE}}$ pin shall be held at static high level during LBIST

Description

For a stable MISR signature, the level on pin $\overline{\text{TESTMODE}}$ (P20.2) must not change during LBIST execution.

Therefore, always keep pin $\overline{\text{TESTMODE}}$ (P20.2) at a static **high** level during LBIST execution.

2.218 [SMU_TC.006] OCDS Trigger Bus OTGB during Application Reset

Description

The SMU provides an alarm trigger and trace interface (Trigger Set TS16_SMU) using the OCDS Trigger Bus OTGB.

While the Application Reset is active, the SMU outputs the reset state of the OTGB interface instead of TS16_SMU.

This OTGB interface reset state is identical to TS16_SMU when no alarm is active.

After the Application Reset TS16_SMU is output again.

Workaround

Just ignore the phase in the OTGB trace where an alarm seems to become inactive while the Application Reset is active.

2.219 [SMU_TC.007] Size and Position of Field ACNT in Register SMU_AFCNT

Description

***Note**: This erratum might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.*

In the SMU chapter of the User's Manual, in the description of register SMU_AFCNT (Alarm and Fault Counter),

- Size and position of field ACNT (Alarm Counter) are incorrectly described as SMU_AFCNT.[15:8], and
- Bits SMU_AFCNT.[7:4] are incorrectly shown as "Reserved; read as 0"

The **correct** size and position of field ACNT (Alarm Counter) in register SMU_AFCNT is SMU_AFCNT.[**15:4**], as shown in the following Table 12. The position of the "Reserved" bits is aligned accordingly.

Table 12 Field ACNT in Register SMU_AFCNT - Correction

Field	Bits	Type	Description
ACNT	[15:4]	rh	**Alarm Counter** This field is incremented by hardware when the SMU processes an **internal** action related to an alarm event (see Figure **"Alarm operation"**). The counter value holds if the maximum value is reached.
0	[29:16]	r	**Reserved** Read as 0; should be written with 0.

***Note**: The other fields (ACO, FCO, FCNT) of register SMU_AFCNT are correctly described in the User's Manual.*

2.220 [SMU_TC.008] Behavior of Action Counter ACNT

Description

Register SMU_AFCNT (Alarm and Fault Counter) implements a Fault Counter (FCNT) that counts the number of transitions from the RUN state to the FAULT state. Register AFCNT is only reset by a power-on-reset.

Whenever a pending alarm event is processed, the corresponding status bit is set to 1_B by hardware in the Alarm Status register AG<x>.

If an internal SMU action is configured for this alarm, the Action Counter (ACNT) in register AFCNT is incremented anytime the SMU processes this internal action.

Corner Case

In this device step, some of the alarm signals may increment the Action Counter ACNT multiple times for a single alarm event.

Workaround

Do not rely on the value in the action counter ACNT.

2.221 [SMU_TC.010] Transfer to SMU_AD register not triggered correctly

Description

The SMU contains Alarm Debug registers which can be used for diagnostic purposes. If an alarm which is configured to generate a reset (application or system reset) is sent to the SMU, a copy of the Alarm Status registers – AGi – into the Alarm Debug registers – ADi – is automatically triggered.

The AGi are reset by Application reset while the ADi are reset only by power-on reset.

Corner Case

In the case that a first SMU alarm AGi[j] generates a reset request, and a second alarm AGx[y] (where x=i and y=j is possible) configured for a reset occurs a few cycles before the reset is actually executed, then the reset values of the AGi registers will be transferred to the ADi register.

In this case, the ADi registers will not reflect the root cause that lead to a SMU alarm/reset.

***Note**: This corner case will always be met for level alarms.*

2.222 [SMU_TC.012] Unexpected alarms when registers FSP or RTC are written

Description TC2xx

Due to a synchronization issue, ALM3[27] is sporadically triggered if the PRE2 field of register FSP is written while the SMU is configured in Time Switching protocol (FSP.MODE = 10_B) and FSP[0] is toggling with a defined T_{SMU_FFS} period.

Also, ALM3[27] is sporadically triggered if the PRE1 or TFSP_HIGH fields of register FSP are written while the SMU is in the Fault State and T_{FSP_FS} has not yet been reached (STS.FSTS=0_B) (regardless of the FSP.MODE configuration).

In addition, an unexpected ALM2[29] or ALM2[30] is sporadically triggered if field FSP.PRE1 or RTC.RTD is written, and at least one recovery timer is running based on a defined T_{SMU_FS} period (regardless of the FSP.MODE configuration).

The alarms can only be cleared with cold or warm Power-On reset.

Description TC3xx

Due to a synchronization issue, ALM6[7] and ALM10[21] are sporadically triggered if the PRE2 field of register FSP is written while the SMU is configured either

- in Time Switching protocol (FSP.MODE = 10_B) and FSP[0] is toggling with a defined T_{SMU_FFS} period
- or in Dual Rail protocol (FSP.MODE = 01_B) and FSP[1:0] are toggling with a defined T_{SMU_FFS} period

Also, ALM6[7] and ALM10[21] are sporadically triggered if the PRE1 or TFSP_HIGH fields of register FSP are written while the SMU is in the Fault State and T_{FSP_FS} has not yet been reached (STS.FSTS=0_B) (regardless of the FSP.MODE configuration).

In addition, an unexpected ALM10[16] or ALM10[17] is sporadically triggered if field FSP.PRE1 or RTC.RTD is written, and at least one recovery timer is running based on a defined T_{SMU_FS} period (regardless of the FSP.MODE configuration).

The alarms can only be cleared with cold or warm Power-On reset.

Workaround TC2xx

To avoid unexpected alarms, perform the configuration of the PRE1, PRE2 or TFSP_HIGH fields only when the SMU is not in the Fault State and FSP is in Bi-stable protocol mode (FSP.MODE = 00_B). Mode switching and configuration shall not be done with the same write access to register FSP.

This means that in the Fault Free State:

- before writing to PRE1, PRE2 or TFSP_HIGH while Time Switching protocol is enabled:
  - disable Time Switching protocol by setting FSP in Bi-stable protocol mode (FSP.MODE = 00_B);
  - wait until Bi-stable protocol mode is active (read back register FSP twice);
  - write desired value to PRE1, PRE2 or TFSP_HIGH;
  - then switch FSP.MODE to the desired protocol (optional step)
- If the mode shall be changed after writing to PRE1, PRE2 or TFSP_HIGH while in Bi-Stable protocol mode (FSP.MODE = 00_B):
  - write desired value to PRE1, PRE2 or TFSP_HIGH;
  - then switch FSP.MODE to Time Switching protocol

If field FSP.PRE1 or RTC.RTD shall be written, make sure no recovery timer is running. It is not allowed to write to the PRE1 or RTD field when at least one recovery timer is running (indicated by bits RTS0 and RTS1 in the STS register).

Workaround TC3xx

To avoid unexpected alarms, perform the configuration of the PRE1, PRE2 or TFSP_HIGH fields only when the SMU is not in the Fault State and FSP is in Bi-stable protocol mode (FSP.MODE = 00_B). Mode switching and configuration shall not be done with the same write access to register FSP.

This means that in the Fault Free State:

- before writing to PRE1, PRE2 or TFSP_HIGH while Time Switching or Dual Rail protocol is enabled:
  - disable Time Switching or Dual Rail protocol by setting FSP in Bi-stable protocol mode (FSP.MODE = 00_B);
  - wait until Bi-stable protocol mode is active (read back register FSP twice);
  - write desired value to PRE1, PRE2 or TFSP_HIGH;
  - then switch FSP.MODE to the desired protocol (optional step)
- If the mode shall be changed after writing to PRE1, PRE2 or TFSP_HIGH while in Bi-Stable protocol mode (FSP.MODE = 00_B):
  - write desired value to PRE1, PRE2 or TFSP_HIGH;
  - then switch FSP.MODE to Time Switching or Dual Rail protocol

If field FSP.PRE1 or RTC.RTD shall be written, make sure no recovery timer is running. It is not allowed to write to the PRE1 or RTD field when at least one recovery timer is running (indicated by bits RTS0 and RTS1 in the STS register).

3 Parametric deviations

3.1 [ADC_TC.P011] Leakage current for ADC reference pins VAREF, VAGND

Description

- **For TC29x and TC27x**: The values of the leakage current for the VADC reference pins (I_{OZ2} at VAREF and I_{OZ3} at VAGND) need to be slightly corrected as shown in the tables below (changes marked in **bold**).
- **For TC26x**: The values of the leakage current for the VADC and DSADC reference pins (I_{OZ2} and I_{OZ5} at VAREF, I_{OZ3} and I_{OZ6} at VAGND) need to be slightly corrected as shown in the tables below (changes marked in **bold**)

Documentation update

As a result, the adjusted numbers provide a coherent picture for the members of the AURIX™ family while ensuring a stable production.

Update for TC29x

Table 13 TC29x: Leakage Current for TC29x VADC Reference Pins - V_{DDM} = 4.5 V to 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive reference VAREF2 pin leakage[1]	I_{OZ2} CC	-7	-	7	µA	$V_{AREF} > V_{DDM}$; $T_J > 150°C$
		-4	-	4	µA	$V_{AREF} > V_{DDM}$; $T_J \leq 150°C$
		-1 instead of -2	-	**4** instead of 3	µA	$V_{AREF} \leq V_{DDM}$; $T_J > 150°C$
		-1	-	**2** instead of 1	µA	$V_{AREF} \leq V_{DDM}$; $T_J \leq 150°C$
Negative reference VAGND2 pin leakage[2]	I_{OZ3} CC	**-17** instead of -13	-	**7** instead of 13	µA	$V_{AGND} < V_{SSM}$; $T_J > 150°C$
		-8 instead of -7	-	7	µA	$V_{AGND} < V_{SSM}$; $T_J \leq 150°C$
		-5 instead of -4.5	-	**1** instead of 2.5	µA	$V_{AGND} \geq V_{SSM}$; $T_J > 150°C$
		-3 instead of -2.5	-	1	µA	$V_{AGND} \geq V_{SSM}$; $T_J \leq 150°C$

1) For TC290 (bare die version), the VADC positive reference VAREF leakage current is the sum of the leakage currents on pads VAREF2, VAREF3, VAREF4.
2) For TC290 (bare die version), the VADC negative reference VAGND leakage current is the sum of the leakage currents on pads VAGND2, VAGND3, VAGND4.

Table 14 TC29x: Leakage Current for TC29x VADC Reference Pins - V_{DDM} = 2.97 V to 4.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive reference	I_{OZ2} CC	**-2** instead of -6	-	6	µA	$V_{AREF} > V_{DDM}$; $T_J > 150°C$

(table continues...)

Table 14 (continued) TC29x: Leakage Current for TC29x VADC Reference Pins - V_{DDM} = 2.97 V to 4.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VAREF2 pin leakage[1]		-3.5	-	3.5	µA	$V_{AREF} > V_{DDM}$; $T_J \leq 150°C$
		-1 instead of -2	-	**3** instead of 2.5	µA	$V_{AREF} \leq V_{DDM}$; $T_J > 150°C$
		-1	-	**2** instead of 1	µA	$V_{AREF} \leq V_{DDM}$; $T_J \leq 150°C$
Negative reference VAGND2 pin leakage[2]	I_{OZ3} CC	-12	-	**6** instead of 12	µA	$V_{AGND} < V_{SSM}$; $T_J > 150°C$
		-6.5	-	6.5	µA	$V_{AGND} < V_{SSM}$; $T_J \leq 150°C$
		-3.5 instead of -2.2	-	**1** instead of 2	µA	$V_{AGND} \geq V_{SSM}$; $T_J > 150°C$
		-2 instead of -1	-	1	µA	$V_{AGND} \geq V_{SSM}$; $T_J \leq 150°C$

1) For TC290 (bare die version), the VADC positive reference VAREF leakage current is the sum of the leakage currents on pads VAREF2, VAREF3, VAREF4.
2) For TC290 (bare die version), the VADC negative reference VAGND leakage current is the sum of the leakage currents on pads VAGND2, VAGND3, VAGND4.

Update for TC27x

Table 15 TC27x: Leakage Current for TC27x (Steps DC/DB/CA) VADC Reference Pins - V_{DDM} = 4.5 V to 5.5 V

Parameter	Symbol	Values[1]			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive reference VAREF2 pin leakage[2]	I_{OZ2} CC	-7	-	7	µA	$V_{AREF} > V_{DDM}$; $T_J > 150°C$
		-4	-	4	µA	$V_{AREF} > V_{DDM}$; $T_J \leq 150°C$
		-1 instead of -2	-	3	µA	$V_{AREF} \leq V_{DDM}$; $T_J > 150°C$
		-1	-	**2** instead of 1	µA	$V_{AREF} \leq V_{DDM}$; $T_J \leq 150°C$
Negative reference VAGND2 pin leakage[3]	I_{OZ3} CC	**-15** instead of -13	-	**7** instead of 13	µA	$V_{AGND} < V_{SSM}$; $T_J > 150°C$
		-8 instead of -7	-	7	µA	$V_{AGND} < V_{SSM}$; $T_J \leq 150°C$
		-4 instead of -3.3	-	**1** instead of 2.5	µA	$V_{AGND} \geq V_{SSM}$; $T_J > 150°C$
		-3 instead of -2.85	-	1	µA	$V_{AGND} \geq V_{SSM}$; $T_J \leq 150°C$

1) Reference values (“instead of ..”) are taken from the TC27x Data Sheet for steps DB and DC; reference values in TC27x Data Sheet for step CA are slightly different. New limits documented in this table are identical for TC27x steps DC, DB and CA.
2) For TC270 (bare die version), the VADC positive reference VAREF leakage current is the sum of the leakage currents on pads VAREF2, VAREF3.

3) For TC270 (bare die version), the VADC negative reference VAGND leakage current is the sum of the leakage currents on pads VAGND2, VAGND3.

Table 16 TC27x: Leakage Current for TC27x (Steps DC/DB/CA) VADC Reference Pins - V_{DDM} = 2.97 V to 4.5 V

Parameter	Symbol	Values[1]			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive reference VAREF2 pin leakage[2]	I_{OZ2} CC	**-2** instead of -6	-	6	µA	$V_{AREF} > V_{DDM}$; $T_J > 150°C$
		-3.5	-	3.5	µA	$V_{AREF} > V_{DDM}$; $T_J \leq 150°C$
		-1 instead of -2	-	2.5	µA	$V_{AREF} \leq V_{DDM}$; $T_J > 150°C$
		-1	-	**2** instead of 1	µA	$V_{AREF} \leq V_{DDM}$; $T_J \leq 150°C$
Negative reference VAGND2 pin leakage[3]	I_{OZ3} CC	-12	-	**6** instead of 12	µA	$V_{AGND} < V_{SSM}$; $T_J > 150°C$
		-6.5	-	6.5	µA	$V_{AGND} < V_{SSM}$; $T_J \leq 150°C$
		-3 instead of -2.2	-	**1** instead of 2	µA	$V_{AGND} \geq V_{SSM}$; $T_J > 150°C$
		-2 instead of -1	-	1	µA	$V_{AGND} \geq V_{SSM}$; $T_J \leq 150°C$

1) Reference values (“instead of ..”) are taken from the TC27x Data Sheet for steps DB and DC; reference values in TC27x Data Sheet for step CA are slightly different. New limits documented in this table are identical for TC27x steps DC, DB and CA.
2) For TC270 (bare die version), the VADC positive reference VAREF leakage current is the sum of the leakage currents on pads VAREF2, VAREF3.
3) For TC270 (bare die version), the VADC negative reference VAGND leakage current is the sum of the leakage currents on pads VAGND2, VAGND3.

Update for TC26x

Table 17 TC26x: Leakage Current for TC26x VADC and DSADC Reference Pins - V_{DDM} = 4.5 V to 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive reference VAREF1 pin leakage[1]	I_{OZ2} CC I_{OZ5} CC	-7	-	7	µA	$V_{AREF} > V_{DDM}$; $T_J > 150°C$
		-4	-	4	µA	$V_{AREF} > V_{DDM}$; $T_J \leq 150°C$
		-1 instead of -3	-	3	µA	$V_{AREF} \leq V_{DDM}$; $T_J > 150°C$
		-1 instead of -2	-	2	µA	$V_{AREF} \leq V_{DDM}$; $T_J \leq 150°C$
Negative reference VAGND1 pin leakage[2]	I_{OZ3} CC I_{OZ6} CC	**-17** instead of -13	-	**7** instead of 13	µA	$V_{AGND} < V_{SSM}$; $T_J > 150°C$
		-8 instead of -7	-	7	µA	$V_{AGND} < V_{SSM}$; $T_J \leq 150°C$

(table continues...)

Table 17 (continued) TC26x: Leakage Current for TC26x VADC and DSADC Reference Pins - V_{DDM} = 4.5 V to 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	**Typ.**	**Max.**		
		-4.5 instead of -3	-	**1** instead of 3	µA	$V_{AGND} \geq V_{SSM}$; $T_J > 150°C$
		-3 instead of -2.5	-	**1** instead of 2.5	µA	$V_{AGND} \geq V_{SSM}$; $T_J \leq 150°C$

1) For TC260 (bare die version), the VADC/DSADC positive reference VAREF leakage current is the sum of the leakage currents on pads VAREF0, VAREF1.
2) For TC260 (bare die version), the VADC/DSADC negative reference VAGND leakage current is the sum of the leakage currents on pads VAGND0, VAGND1.

Table 18 TC26x: Leakage Current for TC26x VADC and DSADC Reference Pins - V_{DDM} = 2.97 V to 4.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	**Typ.**	**Max.**		
Positive reference VAREF1 pin leakage[1)]	I_{OZ2} CC I_{OZ5} CC	**-2** instead of -6	-	6	µA	$V_{AREF} > V_{DDM}$; $T_J > 150°C$
		-3.5	-	3.5	µA	$V_{AREF} > V_{DDM}$; $T_J \leq 150°C$
		-1 instead of -3	-	3	µA	$V_{AREF} \leq V_{DDM}$; $T_J > 150°C$
		-1 instead of -2	-	2	µA	$V_{AREF} \leq V_{DDM}$; $T_J \leq 150°C$
Negative reference VAGND1 pin leakage[2)]	I_{OZ3} CC I_{OZ6} CC	-12	-	**6** instead of 12	µA	$V_{AGND} < V_{SSM}$; $T_J > 150°C$
		-6.5	-	6.5	µA	$V_{AGND} < V_{SSM}$; $T_J \leq 150°C$
		-4 instead of -3	-	**1** instead of 3	µA	$V_{AGND} \geq V_{SSM}$; $T_J > 150°C$
		-2	-	**1** instead of 2	µA	$V_{AGND} \geq V_{SSM}$; $T_J \leq 150°C$

1) For TC260 (bare die version), the VADC/DSADC positive reference VAREF leakage current is the sum of the leakage currents on pads VAREF0, VAREF1.
2) For TC260 (bare die version), the VADC/DSADC negative reference VAGND leakage current is the sum of the leakage currents on pads VAGND0, VAGND1.

3.2 [FlexRay_TC.P002] Pad Configuration for E-Ray Parameters

Description

The sentence at the beginning of section “E-Ray Parameters” in the Data Sheet should read as follows regarding the output driver settings:

“The timings of this section are valid for the strong driver **sharp edge** settings (**speed grade 1**) of the output drivers with C_L = 25 pF. For the inputs the hysteresis has to be configured to inactive.”

3.3 [IDD_TC.H001] IPC Limits used in Production Test for IDD Max Power Pattern

Description

Instructions per cycle for a CPU is measured by dividing ICNT instruction counter value with the CCNT clock counter value.

***Note**: For a complete description of registers ICNT and CCNT refer to the TriCore™ Architecture Manual, chapter "Performance Counter Registers".*

Parameters using the max power pattern for device individual testing of power consumption limits (IDD) are tested for the following maximum IPC rates:

- **TC29x, TC27x**: for a maximum IPC rate of 1.2 for all CPUs available in the device
- **TC26x, TC23x, TC22x, TC21x**: for a maximum IPC rate of 1.3 for all CPUs available in the device

3.4 [IPA2_TC.P001] Pull-up/-down current for A2 pad - Documentation update

Description

In table "Class A2" in chapter "Electrical Specification" of the Data Sheet, the reference levels V_{IHmin} and V_{ILmax} in column "Note/Test Conditions" for parameters "Pull-up current for A2 pad" (symbol I_{PUHA2}) and "Pull-down current for A2 pad" (symbol I_{PDLA2}) have erroneously been swapped.

Correction

The correct assignment of the reference levels V_{IHmin} and V_{ILmax} to the pull-up/-down current parameters for A2 pads is shown in the following table:

Table 19 Corrections to column "Note/Test Conditions" for Pull-up/-down currents for A2 pads

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Pull-up current for A2 pad	I_{PUHA2} CC	-	-	|100|	µA	V_{ILmax}
		|25|	-	-	µA	V_{IHmin}
Pull-down current for A2 pad	I_{PDLA2} CC	|23|	-	-	µA	V_{ILmax}
		-	-	|100|	µA	V_{IHmin}

3.5 [KOVA_TC.P001] Increased overload coupling factor (KOVAP, KOVAN) for specific analog pins

Description

Due to an issue in the multiplexer structure, the overload coupling factor for analog inputs (KOVAP, KOVAN) may deviate by a factor > 1000 from the values specified in the Data Sheet for analog input pins which are connected to a DSADC instance with multiplexer:

- On TC29x, these are channels 2, 3, 6, 7, 8
- On TC27x, these are channels 2 and 3
- On TC26x, these are channels 0 and 3

The issue does not occur for analog input pins which are connected to a DSADC instance without multiplexer.

To trigger the issue, the overload current has to be injected on an analog pin where the DSADC common mode hold voltage is enabled.

Generally, the increased coupling factor occurs only within the DSADC specific multiplexer structure. There is no interference to other DSADC channels or VADC groups. Furthermore, the increased coupling factor is isolated either to the p-input of the related DSADC multiplexer or to the n-input of the related DSADC multiplexer. When the overload current is injected on any p-input of the multiplexer, only the remaining other p-inputs of this multiplexer are affected. When the overload current is injected on any n-input of the multiplexer, only the remaining other n-inputs of this multiplexer are affected.

3.6 [PADS_TC.P002] Restrictions for P00.1 .. P00.12 if V_{DDM} is lower than V_{EXT}

Description

Each input pin of the AURIX™ devices is equipped with ESD protection circuitry.

For the mixed analog/digital signal pins P00.1 .. P00.12, there is both ESD protection of the digital part to V_{EXT}, and ESD protection of the analog VADC inputs to V_{DDM}. P00.1, P00.2, P00.7 and P00.8 have additional ESD protection to V_{DDM} for the analog DSADC inputs.

In case V_{DDM} is lower than V_{EXT} (for example V_{DDM} = 3.3 V and V_{EXT} = 5.0 V), an increased cross current can be observed if the input or output voltage on these pins is above V_{DDM}, for example if:

- (one or more of) the internal pull-ups on P00.1 .. P00.12 are enabled, or
- (one or more of) the pins P00.1 .. P00.12 are driven high as output, or
- the input voltage on (one or more of) the pins P00.1 .. P00.12 is above V_{DDM}

The cross current observed on P00.1, P00.2, P00.7 and P00.8 is higher than on other P00 pins due to the dual ESD protection structure (VADC and DSADC inputs).

***Note**: This effect does not occur if V_{EXT} is lower than V_{DDM}.*

Workaround

Design the system such that $V_{DDM} \geq V_{EXT}$.

Otherwise, ensure that the (input or output) voltage on P00.1 .. P00.12 is lower or equal to V_{DDM}, and additionally disable pull-ups on P00.1 .. P00.12, and do not drive P00.1 .. P00.12 as (push/pull) outputs.

3.7 [PADS_TC.P003] Input Frequency f_{IN} for Class S Pads

Description

For the class S pads parameter “Input frequency” (symbol f_{IN}), only the “Hysteresis active” mode is available.

The “Hysteresis inactive” mode is not available for this pad type, therefore the corresponding row in the Data Sheet with “Hysteresis inactive” in column “Note/Test Condition” for f_{IN} does not apply for this pad type.

3.8 [PADS_TC.P006] P21.6/P21.7 Pull-up Reset Behavior

Description

In Table “Port 21 Functions” in the Data Sheet, the pull-up behavior of P21.6 and P21.7 is defined with symbol PU in column “Type”, and in Table “Pull-up/Pull-Down Reset Behavior of the Pins” in the Data Sheet, the behavior of TDI (P21.6) and TDO (P21.7) is described to be independent of the state of HWCFG[6].

However, the actual pull-up behavior for P21.6 and P21.7 is as defined for symbol PU1, i.e.

- P21.6 (TDI) and P21.7 (TDO) are pulled up during and after $\overline{\text{PORST}}$ if pin HWCFG[6] (P14.4) is pulled high or left unconnected
- P21.6 (TDI) and P21.7 (TDO) are High-Z during and after $\overline{\text{PORST}}$ if pin HWCFG[6] (P14.4) is pulled low

3.9 [PADS_TC.P009] Bonding of VGATE1P on Bare Die Variants

Description

***Note**: This information is only relevant for the TC290, TC270, and TC260 Bare Die variants.*

On packaged devices, pads VGATE1P (SMPS) and VGATE1P (LDO) are internally connected together, ensuring identical levels on both pads.

On the bare die variant, these pads should consequently be bonded to the same level, depending on the selected supply configuration.

The recommended connections of the supply pads for the individual supply options are summarized in table “Supply Mode and Topology selection” in the User’s Manual and described in detail therein.

TC290 documentation update

The documentation in table “TC29x Bare Die Pad List” of the Data Sheet has to be updated for pads VGATE1P (SMPS) and VGATE1P (LDO) as shown in the following table.

Table 20 TC290 VGATE1P Pads - Documentation Update

Number	Pad Name	Comment
310	VGATE1P (SMPS)	Connect to same level as VGATE1P (LDO).
311	VGATE1P (LDO)	Connect to same level as VGATE1P (SMPS).

TC270 documentation update

The documentation in table “List of the TC270x Bare Die Pads” of the Data Sheet has to be updated for pads VGATE1P (SMPS) and VGATE1P (LDO) as shown in the following table.

Table 21 TC270 VGATE1P Pads - Documentation Update

Number	Pad Name	Comment
161	VGATE1P (SMPS)	Connect to same level as VGATE1P (LDO).
163	VGATE1P (LDO)	Connect to same level as VGATE1P (SMPS).

TC260 documentation update

The documentation in table “List of the TC260x Bare Die Pads” of the Data Sheet has to be updated for pads VGATE1P (SMPS) and VGATE1P (LDO) as shown in the following table.

Table 22 TC260 VGATE1P Pads - Documentation Update

Number	Pad Name	Comment
126	VGATE1P (SMPS)	Connect to same level as VGATE1P (LDO).
128	VGATE1P (LDO)	Connect to same level as VGATE1P (SMPS).

3.10 [QSPI_TC.P001] Master Mode timing for MPss output pads (5 V) - Documentation update

Description

In the current version of the Data Sheet, table “Master Mode timing MPss output pads for data and clock, CL=50pF” is missing in section “QSPI Timings, Master and Slave Mode” for 5 V pad power supply.
A copy of this table is included in the figure below (source: TC29xB Data Sheet V1.2 2019-03).

Table 3-62 Master Mode timing MPss output pads for data and clock, CL=50pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	40	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-2	-	3.5+0.035 * C_L	ns	0 < C_L < 200pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-8	-	8	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-8	-	8	ns	MPss; C_L=50pF
		-1	-	15	ns	MP+sm; C_L=50pF
		0	-	50	ns	MP+m, MPm, LPm; C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	40 [4][5]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 [4][5]	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of $T_{MAX} = 1 / f_{MAX}$.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Figure 7 Master Mode timing MPss output pads for data and clock, CL=50pF

3.11 [RTH_TC.H001] Thermal characteristics of the package - Footnote update for LF-BGA-292-6 package

Description

- In the **TC27x** and **TC26x** Data Sheets, the JEDEC JESD51-1 standard for RQJA listed in the footnote for the LF-BGA-292-6 package in table “Thermal characteristics of the package” is not correct
- In the **TC23x** Data Sheet, the references to the JEDEC standards (JESD51-3/5/7) for RQJA in the footnote for the LF-BGA-292-6 package in table “Thermal characteristics of the package” are not correct. They only apply to the TQFP package

Correction

The correct footnote for the LF-BGA-292-6 package is: Value is defined in accordance with JESD51-**9**

3.12 [VDDPPA_TC.H001] Voltage to ensure defined pad states - Footnote update

Description

In the footnote for parameter “Voltage to ensure defined pad states” (symbol V_{DDPPA}) in table “Operating Conditions” of the Data Sheet, V_{DDP3} is mentioned as representative for “non-core supply voltages” in the text.

Update

The footnote for V_{DDPPA} should be extended to include all “non-core supply voltages” as follows:

*) This parameter is valid under the assumption the PORST signal is constantly at low level during the power-up/power-down of the “non-core supply voltages” (V_{DDP3}, V_{EXT}, V_{FLEX}, V_{DDFL3}, V_{DDM}, ..., depending on the respective TC2x device version).

4 Application hints

4.1 [ADC_AI.H003] Injected conversion may be performed with sample time of aborted conversion

Description

For specific timing conditions and configuration parameters, a higher prioritized conversion c_i (including a synchronized request from another ADC kernel) in cancel-inject-repeat mode may erroneously be performed with the sample time parameters of the lower prioritized cancelled conversion c_c. This can lead to wrong sample results (depending on the source impedance), and may also shift the starting point of following conversions.

The conditions for this behavior are as follows (all 3 conditions must be met):

1. **Sample Time setting**: injected conversion c_i and cancelled conversion c_c use different sample time settings, i.e. bit-fields STC* in the corresponding Input Class Registers for c_c and for c_i (GxICLASS0/1, GLOBICLASS0/1) are programmed to different values
2. **Timing condition**: conversion c_i starts during the first f_{ADCI} clock cycle of the sample phase of c_c
3. **Configuration parameters**: the ratio between the analog clock f_{ADCI} and the arbiter speed is as follows:

   $N_A > N_D * (N_{AR} + 3)$,

   with

   - N_A = ratio f_{ADC}/f_{ADCI} (N_A = 1 .. 32, as defined in bit-field DIVA)
   - N_D = ratio f_{ADC}/f_{ADCD} = number of f_{ADC} clock cycles per arbitration slot (N_D = 1 .. 4, as defined in bit-field DIVD)
   - N_{AR} = number of arbitration slots per arbitration round (N_{AR} = 4, 8, 16, or 20, as defined in bit-field GxARBCFG.ARBRND)

Bit fields DIVA and DIVD mentioned above are located in register GLOBCFG.

As can be seen from the formula above, a problem typically only occurs when the arbiter is running at maximum speed, and a divider $N_A > 7$ is selected to obtain f_{ADCI}.

Recommendation 1

Select the same sample time for injected conversions c_i and potentially cancelled conversions c_c , i.e. program all bit-fields STC* in the corresponding Input Class Registers for c_c and for c_i (GxICLASS0/1, GLOBICLASS0/1) to the same value.

Recommendation 2

Select the parameters in register GLOBCFG and GxARBCFG according to the following relation:

$N_A \leq N_D * (N_{AR} + 3)$.

4.2 [ADC_TC.H012] DSADC/VADC Connections to VAREF1/2, VAGND1/2

Description

In TC27x Bx-step devices, the VADC and DSADC modules are connected to the Analog Reference Voltage pins as shown in Table 23:

Table 23 Connections in TC27x Bx-step

Module	Analog Reference Voltage Pins
VADC	VAREF1, VAGND1
DSADC	VAREF2, VAGND2

To ensure module performance, the connection of the VADC and DSADC modules to the Analog Reference Voltage pins has been modified beginning with TC27x Cx-step devices as shown in Table 24 (same concept as in TC29x):

Table 24 Connections in TC27x Cx-step (and following)

Module	Analog Reference Voltage Pins
DSADC	VAREF1, VAGND1
VADC	VAREF2, VAGND2

The corresponding values for the reference load current I_{REF} (for the DSADC) and the charge consumption per conversion Q_{CONV} (for the VADC) can be found in the individual Data Sheets of the respective device steps.

4.3 [ADC_TC.H014] VADC Start-up Calibration

Description

The formula for the duration of the start-up calibration in some versions of the TC2x User's Manuals is incorrect with respect to the used frequency, or missing.

In the following, the contents of chapter "Calibration" is reprinted, including the correct Formula for Start-up Calibration below.

Calibration

Calibration automatically compensates deviations caused by process, temperature, and voltage variations. This ensures precise results throughout the operation time.

An initial start-up calibration is required once after a reset for all converters. All converters must be enabled (ANONS = 11_B). The start-up calibration is initiated globally by setting bit SUCAL in register GLOBCFG. Conversions may be started after the initial calibration sequence. This is indicated by bit CALS = 1_B AND bit CAL = 0_B.

Formula for Start-up Calibration

The start-up calibration phase takes 4352 f_{ADCI} cycles (4352 × **50 ns** = 217.6 µs for f_{ADCI} = 20 MHz).

After that, postcalibration cycles will compensate the effects of drifting parameters. The postcalibration cycles can be disabled.

***Note**: The ADC error depends on the temperature. Therefore, the calibration must be repeated periodically.*

4.4 [ADC_TC.H015] Conversion Time with Broken Wire Detection

Description

As described in a note in section "Broken Wire Detection" of the User's Manual, the duration of the complete conversion is increased by the preparation phase (same as the sample phase) if the broken wire detection is enabled, i.e. the sample time doubles for standard conversions when broken wire detection is enabled (GxCHCTRy.BWDEN = 1_B):

Formula for Standard Conversions without Broken Wire Detection

- $t_{CN} = t_s + (N + PC) \times t_{ADCI} + 2 \times t_{VADC}$ (see also User's Manual/Data Sheet)

Formula for Standard Conversions with Broken Wire Detection

- $t_{CN} = 2 \times t_s + (N + PC) \times t_{ADCI} + 2 \times t_{VADC}$

where:

t_s = (2 + STC) x t_{ADCI} for STC ≤ 15, and
t_s = (2 + (STC-15) x 16)) x t_{ADCI} for STC ≥ 16;
N = result width (8/10/12 bits);
PC = 2 if post-calibration selected, PC = 0 otherwise.

Examples

Conversion times for different configurations are shown in the following Table 25 (without broken wire detection) and Table 26 (with broken wire detection):

Table 25 Conversion Time for Standard Conversions - Without Broken Wire Detection - Examples

Result	Symbol	Time	Conditions
12-bit result	t_{C12}	(16 + STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration enabled, STC ≤ 15
10-bit result	t_{C10}	(12 + STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15
8-bit result	t_{C8}	(10 + STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15

Table 26 Conversion Time for Standard Conversions - With Broken Wire Detection - Examples

Result	Symbol	Time	Conditions
12-bit result	t_{C12B}	(18 + 2 x STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration enabled, STC ≤ 15
10-bit result	t_{C10B}	(14 + 2 x STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15
8-bit result	t_{C8B}	(12 + 2 x STC) x t_{ADCI} + 2 x t_{VADC}	Post-calibration disabled, STC ≤ 15

4.5 [ADC_TC.H016] P02 Output Driver Setting for External Multiplexer Control

Description

Short intermediate values can appear on outputs EMUX0y on P02 when the subchannel number changes, if the respective port drivers operate in strong driver / fast edge mode.
This may lead to unintended drawing of charge from a connected analog signal source.

***Note**: Strong driver / fast edge mode can only be selected for MP pads (speed grade 1), i.e. for EMUX0y outputs on port P02. EMUXxy outputs on ports P00 and P33 use LP pads that only feature medium driver mode, i.e. EMUXxy outputs on these ports are not affected.*

Recommendation

Avoid strong driver / fast edge mode, i.e. speed grade 1 on EMUX0y outputs on P02 pins. Select strong driver / medium edge mode (speed grade 2) instead to avoid the unwanted intermediate states.

4.6 [ADC_TC.H019] G6ARBCNT Connection to GTM

Description

The connection G6ARBCNT to GTM_TIM1_CH3 is erroneously listed in table “Digital Connections in the TC29x” and in table “Digital Connections in the TC27x” of the corresponding user manual. This connection does not exist on silicon.
G6ARBCNT is only connected to GTM_TIM1_CH6.

4.7 [ADC_TC.H020] Minimum/Maximum Detection Compares 12 Bits Only

Description

In minimum or maximum detection mode (FEN = 11_B or 10_B) new results are compared to the lower 12 bits of the respective result register bit-field RESULT.

Therefore, a value RESULT = $XFFF_H$ (X > 0_H) will not be updated for a new result value of $0FFF_H$ in minimum detection mode.

In a real application, this should be no problem, as the minimum detection usually sees values below $0FFF_H$.

Recommendation

For minimum detection, use the start value $0FFF_H$ (instead of $FFFF_H$ as mentioned in the User's Manual).

For maximum detection, use the start value 0000_H as mentioned in the User's Manual.

4.8 [ADC_TC.H022] Sample Time Control - Formula

Description

Table "Sample Time Coding" in section "Input Class Registers" of the VADC chapter in the User's Manual describes the additional clock cycles (selected in bit-fields STCS and STCE) to be added to the minimum sample time of two analog clock cycles.

As can be seen from the table in the User's Manual, the step width in the coding depends on the MSB of STCi (i = S or E). The following Table 27 has been copied from the User's Manual, with the corresponding formula added in the last column:

Table 27 Sample Time Coding

STCS / STCE	Additional Clock Cycles[1)]	Resulting Sample Time	Clock Cycle Formula
$0\ 0000_B$	0	2 / f_{ADCI}	2 + STCi
$0\ 0001_B$	1	3 / f_{ADCI}	
...	...	...	
$0\ 1111_B$	15	17 / f_{ADCI}	
$1\ 0000_B$	16	18 / f_{ADCI}	2 + (STCi - 15) x 16
$1\ 0001_B$	32	34 / f_{ADCI}	
...	...	...	
$1\ 1110_B$	240	242 / f_{ADCI}	
$1\ 1111_B$	256	258 / f_{ADCI}	

1) The number of resulting additional clock cycles listed in this column corresponds to the term "STC" used in the conversion timing formulas in the Data Sheet.

4.9 [ADC_TC.H024] Documentation: Filter control only in registers GxRCR7/GxRCR15

Description

In sections "Finite Impulse Response Filter Mode (FIR)" and "Infinite Impulse Response Filter Mode (IIR)" of the VADC chapter in the User's Manual,

- replace this sentence:

"Several predefined sets of coefficients can be selected via bit-field DRCTR (coding listed in Table xx-6) in registers G0RCRy (y = 0 - 15)ff and GLOBRCR."

- with this sentence:
  "Several predefined sets of coefficients can be selected via bit-field DRCTR (coding listed in Table xx-6) in registers **GxRCR7** and **GxRCR15**."

4.10 [ADC_TC.H038] Multiplexer Diagnostics Connection - Documentation update

Description

The multiplexer diagnostics feature can pull up the channel input line to V_{DDM} or pull it down to V_{SS}.
Figure "Signal Path Test" in the VADC chapter of the User's Manual erroneously shows a connection to V_{DDP} instead of V_{DDM}. Pull-up to V_{DDP} is not possible.

Correction

In figure "Signal Path Test" in the VADC chapter of the User's Manual, symbol "V_{DDP}" shall be replaced by "V_{DDM}".

4.11 [ASCLIN_TC.H001] Bit field FRAMECON.IDLE in LIN slave tasks

Description

For LIN performing slave tasks, bit-field FRAMECON.IDLE has to be set to 000_B (default after reset), i.e. no pause will be inserted between transmission of bytes.

If FRAMECON.IDLE > 000_B, the inter-byte spacing of the ASCLIN module is not working properly in all cases in LIN slave tasks (no bit errors are detected by the ASCLIN module within the inter-byte spacing).

4.12 [ASCLIN_TC.H003] Behavior of LIN Autobaud Detection Error Flag

Description

- Expected behavior:
  In ASCLIN, when auto baud detection (LINCON.ABD) is deactivated, the auto baud measurement should still be active and the Autobaud Detection Error Flag FLAGS.LA should be set when the value measured is outside the BRD.LOWERLIMIT and BRD.UPPERLIMIT range.
- Actual behavior:
  The Autobaud Detection Error Flag FLAGS.LA is not set, as the auto baud measurement is not active when auto baud detection is deactivated (LINCON.ABD = 0).

4.13 [ASCLIN_TC.H004] Changing the Transmit FIFO Inlet Width / Receive FIFO Outlet Width

Description

- **Expected behavior**:
  The Transmit FIFO should write the data to intended location of TxFIFO, even though the Transmit FIFO inlet width TXFIFOCON.INW is changed between the write operations.
  The Receive FIFO should read the data from intended location, even though the Receive FIFO outlet width RXFIFOCON.OUTW is changed between the read operations.
- **Actual behavior (Transmit FIFO)**:
  The Transmit FIFO does not write the data in the intended location when TXFIFOCON.INW is changed in an increasing order (from 1 to 2 to 4) between write operations.

The Transmit FIFO writes the data only to aligned write index based on the number of bytes to be written (TXFIFOCON.INW).

Example: Assuming that the write index of TxFIFO is from 0 to 15 (16 bytes), when TXFIFOCON.INW = 2, the TxFIFO writes two bytes of data starting only from half-word aligned write index (0, 2, 4, …, 14). Similarly when TxFIFO writes four bytes of data starting only from word aligned write index (0, 4, 8, 12).

***Note**: This misbehavior is seen only when TXFIFOCON.INW is changed in-between write operations.*

- **Actual behavior (Receive FIFO)**:

  The Receive FIFO does not read the data from intended location when RXFIFOCON.OUTW is changed in an increasing order (from 1 to 2 to 4) between read operations.

  The Receive FIFO reads the data only from aligned read index based on the number of bytes to be read (RXFIFOCON.OUTW).

  Example: Assuming that the read index of RxFIFO is from 0 to 15 (16 bytes), when RXFIFOCON.OUTW = 2, the RxFIFO reads two bytes of data starting only from half-word aligned write index (0, 2, 4, …, 14). Similarly when RxFIFO reads four bytes of data starting only from word aligned read index (0, 4, 8, 12).

  ***Note**: This misbehavior is seen only when RXFIFOCON.OUTW is changed in-between read operations.*

Effect

Previously written data in TxFIFO will be over-written by the new data, when the TxFIFO write index is not aligned with number of data bytes to be written.

Previously read data will be read again, when the RxFIFO read index is not aligned with number of data bytes to be read.

Recommendation

Flush the TxFIFO (TXFIFOCON.FLUSH) or RxFIFO (RXFIFOCON.FLUSH) before TXFIFOCON.INW or RXFIFOCON.OUTW is changed respectively.

4.14 [ASCLIN_TC.H005] Collision detection error reported twice in LIN slave mode

Description

An ASCLIN module configured as LIN slave node could report a wrong collision detection error during reception of LIN header after detecting a first correct collision detection error during the transmission of a response field of the previous LIN frame.

This misbehavior is observed under the following sequence:

- The LIN slave node detects a collision detection error when there is a bit error in its transmitted response frame, and then it goes to the idle state as expected
- The master transmits a header onto the LIN bus, and the LIN slave node receives header and tries to capture the identifier inside the header
- Then the LIN slave node reports another collision error which is wrongly detected during the reception of identifier although there is no corruption of LIN header on the bus

Recommendation

Ignore the collision detection error which happened during reception phase of a LIN slave node.

4.15 [ASCLIN_TC.H006] Sample point position when using three samples per bit

Description

As documented in the description of field BITCON.SAMPLEPOINT, "... if three sample points at position 7, 8, 9 are required, this bit-field would contain 9".

In general, if three samples per bit are selected (BITCON.SM = 1_B), field BITCON.SAMPLEPOINT defines the position of the last sample point.

Documentation update

The text related to three sample points in figure "ASCLIN Bit Structure" in the ASCLIN chapter of the user manual should be updated as follows:

- 16x Oversampling, 3 sample points, relevant sample position 7, 8, 9 (BITCON.OVERSAMPLING = 16, BITCON.SM = 1, BITCON.SAMPLEPOINT = 9)
  - instead of "16x Oversampling, 3 sample points, relevant sample position 8"
- 8x Oversampling, 3 sample points, relevant sample position 3, 4, 5 (BITCON.OVERSAMPLING = 8, BITCON.SM = 1, BITCON.SAMPLEPOINT = 5)
  - instead of "8x Oversampling, 3 sample points, relevant sample position 4"

4.16 [ASCLIN_TC.H008] SPI master timing – Additional information to Data Sheet characteristics

Description

The following note shall be added to chapter "ASCLIN SPI Master Timing" in the Data Sheet:

***Note**: The specified timings describe the pad capabilities for the respective driver strength configuration. For the maximum achievable baud rate in a given application, the MRST input timings need to be considered in particular.*

Background information

Chapter "ASCLIN SPI Master Timing" in the Data Sheet contains separate tables for different output driver configurations. As can be seen from these tables, the master output timings directly depend on the selected driver strength. The corresponding parameters are marked as controller characteristics with symbol "CC".

The setup and hold timings for input data received from the slave are marked as system requirements with symbol "SR". They must be provided by the system in which the device is designed in.

In a given application, the maximum rate at which data can be received from a slave on the master receive input MRST may be limited by the required setup time t_{52} (MRST setup to ASCLKO latching edge). As data is shifted by the slave on one edge of ASCLKO and latched by the master on the opposite edge, one phase of ASCLKO must always be greater than the minimum required MRST setup time (assuming the sampling point is in the middle). This means the ASCLKO period t_{50} must be > 2 x t_{52}.

4.17 [BCU_TC.H001] HSM Transaction Information not captured

Description

No HSM transaction information is captured by the System Bus Control Unit (SBCU). Therefore the following HSM related control/status register bits in the SBCU do not have any function:

- Register **SBCU_DBGRNT** (SBCU Debug Grant Mask Register):
  - **HSMCMI**: this control bit has no function. Behavior as described for SBCU_DBGRNT.ONE0
  - **HSMRMI**: this control bit has no function. Behavior as described for SBCU_DBGRNT.ONE0
- Register **SBCU_DGNTT** (SBCU Debug Trapped Master Register):
  - **HSMCMI**: this control bit has no function. Behavior as described for SBCU_DBGNTT.ONE0
  - **HSMRMI**: this control bit has no function. Behavior as described for SBCU_DBGNTT.ONE0

4.18 [BoardDesign_TC.H001] Common board design for PD and ED in QFP packages

Description

***Note**: This Application Hint only applies to TC265/TC275 devices in QFP-176 and TC264 devices in QFP-144 packages.*

The Emulation Devices (ED) in QFP-176 and QFP-144 packages use the “TDI” pin P21.6 as VDDPSB supply. This means that, unlike for the Production Device (PD), for the ED there is no JTAG interface (nor the other alternate functions of P21.6) available, and the VDDPSB pin needs to be supplied with 3.3V.

Recommendation

Use the DAP interface for PD and ED and connect TDI/VDDPSB as supply pin to VDDP3.

Please consult the AURIX ED documentation for further options if needed.

4.19 [BROM_TC.H003] Information related to Register FLASH0_PROCOND

Description

Chapters “TC2x BootROM Content” of the User’s Manuals contain a description of parts of the FLASH0_PROCOND register as used by the firmware. This description in subchapter “Configuration by Boot Mode Index (BMI)” shows an incorrect address F800 1030_H.

Correct is the description of this register in the PMU chapter with address F800 2030_H (FLASH0 base address F800 1000_H + offset 1030_H).

Additionally for TC26x

Furthermore, in the TC26x User’s Manual, the description for bit-field RAMIN = $0x_B$ is incorrect in chapter “TC26x Boot ROM Content”: RAMs are not initialized by system reset, RAMs are only initialized after power-on resets.

For a correct description, see the description of register FLASH0_PROCOND in the PMU chapter “Protection Configuration”.

4.20 [BROM_TC.H009] Re-enabling lockstep via BMHD

Description

For all CPUs with lockstep option, the lockstep functionality is controlled by Boot Mode Headers (BMHD) loaded during boot upon a reset trigger.

If lockstep is disabled for a CPUx with lockstep functionality, re-enabling (for example via a different BMHD) is not reliably possible if warm PORST, System or Application reset is executed.

Recommendation

Use cold PORST if lockstep is disabled and shall be re-enabled upon the reset trigger.

4.21 [BROM_TC.H010] Interpretation of value UNIQUE_CHIP_ID_32BIT

Description

As described in chapter “Debug System handling” in the AURIX™ TC2xx BootROM chapter, the value UNIQUE_CHIP_ID_32BIT is written to the COMDATA register by firmware.

***Note**: Unlike the name “UNIQUE_CHIP_ID_32BIT” may suggest, this value only identifies a particular product variant, but not an individual device.*

4.22 [BROM_TC.H019] CRC32 ethernet polynomial - Footnote correction

Description

As documented in the FCE chapter of the User’s Manual, CRC calculation is based on IEEE 802.3, the CRC32 ethernet polynomial used is 0x04C11DB7.

In footnote [2] below table “Boot Mode Header (BMHD) structure” in the BootROM chapter, the CRC32 ethernet polynomial is erroneously documented as $04C11DB71_H$.

Documentation correction

Footnote [2] below table “Boot Mode Header (BMHD) structure” in the BootROM chapter shall be corrected (trailing “1” deleted) as follows:

- [2] CRC calculation is based on IEEE 802.3, the CRC32 ethernet polynomial used is $04C11DB7_H$

4.23 [CCU6_AI.H001] Update of Register MCMOUT

Description

At every correct Hall event (CM_CHE), the next Hall patterns are transferred from the shadow register MCMOUTS into MCMOUT (Hall pattern shadow transfer HP_ST), and a new Hall pattern with its corresponding output pattern can be loaded (for example from a predefined table in memory) by software into MCMOUTS. For the Modulation patterns, signal MCM_ST is used to trigger the transfer.

Loading this register can also be done by writing MCMOUTS.STRHP = 1_B (for EXPH and CURH) or MCMOUTS.STRMCMP = 1_B (for MCMP).

***Note**: If in a corner case a hardware event occurs simultaneously with a software write where MCMOUTS.STRHP = 1_B or MCMOUTS.STRMCMP = 1_B, the current contents of MCMOUTS is copied to the corresponding bit-fields of MCMOUT. The new value written to MCMOUTS will be loaded upon the next event.*

4.24 [CCU6_AI.H002] Description of Bit RWHE in Register ISR

Description

Register ISR (Interrupt Status Reset Register) contains bits to individually clear the interrupt event flags by software. Writing a 1_B clears the bit(s) in register IS at the corresponding bit position(s), writing a 0_B has no effect.

In some versions of the User's Manual, the description of bit RWHE (Reset Wrong Hall Event Flag) in column "Description" of register ISR is wrong (description for status 0_B and 1_B inverted).

The correct description for bit RWHE is (like for all other implemented bits in register ISR) as shown in the following Table 28:

Table 28 Bit RWHE in register ISR

Field	Bits	Type	Description
RWHE	13	w	**Reset Wrong Hall Event Flag** 0_B No action 1_B Bit WHE will be cleared

4.25 [CCU6_AI.H003] Bit TRPCTR.TRPM2 in Manual Mode - Documentation Update

Description

In CCU6 chapter "Trap Control Register" of the User's Manual, the description for bit TRPCTR.TRPM2 = 1_B (Manual Mode) incorrectly states:

"Manual Mode:

Bit TRPF stays **0** after the trap input condition is no longer valid. It has to be cleared by SW by writing ISR.RTRPF = 1."

Correction

The correct description is as follows:

Manual Mode:

Bit TRPF stays **1** after the trap input condition is no longer valid. It has to be cleared by SW by writing ISR.RTRPF = 1.

4.26 [CCU_TC.H001] Clock Monitor Check Limit Values

Description

The values for the check limits of the clock monitor have been updated as shown in the tables below.

Documentation update for TC29x step BB, TC27x ≤ step DB, TC26x step BB, TC23x .. TC21x step AB

For TC29x step BB, TC27x ≤ step DB, TC26x step BB, TC23x .. TC21x step AB, Table 29 replaces the corresponding table in chapter "Clock Monitors" of the User's Manual.

Table 29 Target trimmed Check limits for TC29x step BB, TC27x ≤ step DB, TC26x step BB, TC23x .. TC21x step AB

Target Frequency	LOWER value	UPPER value	SELXXX[1)]	Error can be detected for min. deviation	Error is detected for min. deviation
7.5 MHz	0x24	0x27	11_B	-1.26% +1.54%	-6.45% +6.35%
6.$\overline{6}$ MHz	0x20	0x23	10_B	-0.91% +2.75%	-6.09% +7.50%
6 MHz	0x1C	0x1F	01_B	-3.35% +1.54%	-8.43% +6.35%
5 MHz	0x17	0x1A	00_B	-2.76% +4.07%	-9.41% +7.50%

1) refers to corresponding bit-field xxxSEL in respective CCUCON register

Documentation update for TC29x step BC, TC27x step DC, TC26x step BC, TC23x .. TC21x step AC

For TC29x step BC, TC27x step DC, TC26x step BC, TC23x .. TC21x step AC, Table 30 replaces the corresponding table in chapter “Clock Monitors” of the User’s Manual.

Table 30 Target trimmed Check limits for TC29x step BC, TC27x step DC, TC26x step BC, TC23x .. TC21x step AC

Target Frequency	LOWER value	UPPER value	SELXXX[1)]	Error can be detected for min. deviation	Error is detected for min. deviation
7.5 MHz	0x23	0x27	11_B	-4.07% +1.54%	-9.40% +6.35%
6.$\overline{6}$ MHz	0x1F	0x23	10_B	-4.07% +2.75%	-9.40% +7.50%
6 MHz	0x1C	0x1F	01_B	-3.35% +1.54%	-8.43% +6.35%
5 MHz	0x17	0x1A	00_B	-2.76% +4.07%	-9.41% +7.50%

1) refers to corresponding bit-field xxxSEL in respective CCUCON register

4.27 [CCU_TC.H002] Oscillator Gain Selection via OSCCON.GAINSEL

Description

The reset value of OSCCON.GAINSEL = 11_B provides the default and recommended setting for the oscillator gain. It is not required to modify this value, as the adaptation to a crystal frequency is done via the external circuitry.

Therefore, all other gain selections should be regarded as reserved for special application topics, as shown in the following Table 31.

Table 31 Oscillator Gain Selection via OSCCON.GAINSEL

Field	Bits	Type	Description
GAINSEL	[4:3]	rw	**Oscillator Gain Selection** This value should not be changed from the reset value 11_B. 00_B Low gain 1: reserved for adaptations 01_B Low gain 2: reserved for adaptations 10_B Low gain 3: reserved for adaptations 11_B **Maximum gain: default setting**

Recommendation

Always to keep the default configuration of OSCCON.GAINSEL = 11_B.

4.28 [CCU_TC.H005] References to f_{PLL2}, f_{PLL2_ERAY} and K3 Divider in User's Manual

Description

The VADC incorporated in this device uses clocks derived from f_{SPB}.

Previous design steps (for example TC27x Bx, TC26x Ax, TC29x Ax) incorporated a different VADC module also clocked by f_{ADC}, which could be derived via the K3 divider from f_{PLL2}, f_{PLL2_ERAY}. These clocks were selected in CCUCON0.[27:26], which is described as "Reserved/Should be written with 0" in the present version of the User's Manual.

Clocks f_{PLL2}, f_{PLL2_ERAY} and the K3 divider are still described in the present version of the User's Manual.

Recommendation

- New software implementations should not consider f_{PLL2}, f_{PLL2_ERAY} and the K3 divider
- Software ported from previous design steps with a VADC module clocked by f_{ADC} may be reused on this device step (for TC29x, TC27x, and TC26x see also SMU_TC.H004)

4.29 [CCU_TC.H006] Clock Monitor Support - Documentation Update

Description

The note at the end of section "Operating the Clock Monitors" in chapter "Clock Monitors":

***Note**: This feature is supported by the Infineon safety driver [safTlib] and there is no additional customer software required.*

should state more precisely:

***Note**: The Infineon SafeTlib provides a test for the clock monitor. The clock monitor shall be configured by the application software.*

4.30 [CCU_TC.H007] Oscillator Watchdog Trigger Conditions for ALM3[0]

Description

As described in the User's Manual in section "Oscillator Watchdog", the divider value OSCCON.OSCVAL has to be selected in a way that f_{OSCREF} is within the range of 2 MHz to 3 MHz, and should be as close as possible to 2.5 MHz.

The Oscillator Watchdog (OSC_WDT) will trigger the "input clock out of range" alarm ALM3[0] under the following conditions:

- Boundary for **too high** frequencies:
  - for (OSCVAL+1) x 6.25 ≤ f_{OSC} [MHz] ≤ (OSCVAL+1) x 7.5, an alarm can be generated, but there is no guarantee that it is generated
  - for f_{OSC} [MHz] > (OSCVAL+1) x 7.5, an alarm is always generated
- Boundary for **too low** frequencies:
  - for (OSCVAL+1) x 1.25 ≤ f_{OSC} [MHz] ≤ (OSCVAL+1) x 1.67, an alarm can be generated, but there is no guarantee that it is generated
  - for f_{OSC} [MHz] < (OSCVAL+1) x 1.25, an alarm is always generated

The accuracy of these limits [in %] depends on the variation [in %] of the back up clock (see specification of f_{BACKUT} and f_{BACKT} in the Data Sheet).

Example

- For f_{OSC} = 20 MHz, selecting OSCVAL = 7 results in f_{OSC} = 2.5 MHz.
  - An alarm for too high frequencies can be generated for f_{OSC} ≥ 50 MHz
  - An alarm for too high frequencies is always generated for f_{OSC} > 60 MHz
  - An alarm for too low frequencies can be generated for f_{OSC} ≤ 13.36 MHz
  - An alarm for too low frequencies is always generated for f_{OSC} < 10 MHz

4.31 [CCU_TC.H010] Oscillator Mode control in register OSCCON - Documentation Update

Description

The description for setting OSCCON.MODE = 00_B in register OSCCON must be changed from

- "External Crystal / Ceramic Resonator Mode and External Input Clock Mode. The oscillator Power-Saving Mode is not entered."

to:

- "External Crystal / Ceramic Resonator Mode. The oscillator Power-Saving Mode is not entered."

Recommendation

When using an external input clock signal connected to XTAL1 (XTAL2 open), do not use setting OSCCON.MODE = 00_B. Instead, use setting OSCCON.MODE = 10_B.

4.32 [CPU_TC.H006] Store Buffering in TC1.6/P/E Processors

Description

Store buffering is a method of increasing processor performance by decoupling memory write operations from the instruction execution flow within the CPU. All write data is placed in a FIFO buffer (known as the store buffer) by the CPU prior to being read by the memory/bus interfaces and written to memory. This allows the processor to continue execution without waiting for the write data to be written to the target memory location. Data is written to the store buffer at processor speed and read from the store buffer at memory/bus speed.

Typically the read bandwidth from the store buffer will exceed the write bandwidth from the processor, only if the store buffer fills will the processor stall.

To further increase performance memory read operations are prioritized ahead of memory write operations from the store buffer. This ensures that the processor does not stall on data loads while data writes are pending in the store buffer. A side effect of this prioritizing is that memory may not be accessed in program order.

Operational Details

The function of the store buffer is designed to be invisible to the end user under normal operation:

- All CPU load operations are checked against the store buffer contents. Data for matching load addresses is either immediately forwarded to the CPU from the store buffer (TC1.6, TC1.6P) or written to memory prior to the load operation proceeding (TC1.6E)
- All loads and store operations to peripheral regions (typically segments E_H and F_H) are performed in strict program order (no load prioritization)

The operation of the store buffer can become visible when in-order memory access is required to non-peripheral segments.

This can occur under the following circumstances:

- When programming flash memory
- When performing memory testing with the processor
- When data is required to be in memory for inter-core/inter-module communication

In such cases the following solutions may be employed:

- The store buffer may be explicitly flushed by use of a DSYNC instruction
- In-order data transactions may be enabled by setting SMACON.IODT = 1_B. This should not be done during normal operation, but should only be performed by test routines at start-up or shut-down, as it significantly impacts performance

***Note**:* *In this context, the following statements included in chapter "Store buffers" and in the description of register SMACON for IODT =1_B in the user manual may be misleading:*

- *"Store buffer operation may be disabled by setting the SMACON.IODT bit"*
- *SMACON.IODT = 1_B: "... processor store buffer disabled"*

Effectively, setting SMACON.IODT = 1_B results in memory operations to be performed in program order, where loads always flush preceding stores.

Examples

The following examples refer to memory accesses to non-peripheral regions (i.e. segments 0_H .. D_H):

Example-1a Out of order memory access due to load prioritization

```
Program Flow    -    Memory Access
 st-1                 ld-4
 st-2                 ld-5
 st-3                 ld-6
 ld-4                 st-1
 ld-5                 st-2
 ld-6                 st-3
```

Example-1b In order memory access enforced by DSYNC

```
Program Flow    -    Memory Access
 st-1                 st-1
 st-2                 st-2
 st-3                 st-3
 dsync
 ld-4                 ld-4
 ld-5                 ld-5
 ld-6                 ld-6
```

Example-2a Load forwarding from store buffer - no memory read (TC1.6/1.6P)

```
Program Flow    -    Memory Access
 st.w [a0], d0
 ld.w d1,  [a0]       st.w [a0], d0
```

Example-2b In order memory access enforced by DSYNC (TC1.6/1.6P)

```
Program Flow    -    Memory Access
 st.w [a0], d0        st.w [a0], d0
 dsync
 ld.w d1,  [a0]       ld.w d1,  [a0]
```

4.33 [CPU_TC.H008] Instruction Memory Range Limitations

Description

To ensure the processor cores are provided with a constant stream of instructions the Instruction Fetch Units will speculatively fetch instructions from up to 64 bytes ahead of the current Program Counter (PC).

If the current PC is within 64 bytes of the top of an instruction memory the Instruction Fetch Unit may attempt to speculatively fetch instructions from beyond the physical range. This may then lead to error conditions and alarms being triggered by the bus and memory systems.

Recommendation

It is therefore recommended that either the MPU is used to define the allowable executable range or that the upper 64 bytes of any memory be initialized but unused for instruction storage for the TC1.6.* class processors. For TC1.3.* class processors this may be reduced to 32 bytes.

4.34 [CPU_TC.H009] Details on CPU Clock Control

Description

As described in chapter “Clock Control Unit” of the User’s Manual, the effective CPU execution frequency may be reduced by programming the associated bit-field CPUxDIV in register CCUCONn (where x is the core number, and n = x+6).

The effective execution frequency f_{CPUx} seen by CPUx is given by the following equation (where f_{SRI} is the base SRI frequency):

- $f_{CPUx} = f_{SRI} * (64 - CPUxDIV) / 64$

A CPUxDIV value of 0 results in the core CPUx being clocked at the SRI frequency (no frequency reduction).

To avoid synchronisation issues typically associated with clock division the clock control mechanism stalls the issue of instructions into the processor pipeline rather than by modifying the actual applied clock. An incoming instruction fetch packet is stalled for the number of cycles required to approximate the required execution frequency. The stall is seen by the processor as a stall in the instruction stream in the same way a stalling instruction memory would be seen.

In most scenarios this mechanism provides a good approximation to clock division based control. The actual reduction in effective frequency will be dependent on the code executed.

When determining IPC rates as described in AP32168 (Application Performance Optimization for TriCore V1.6 Architecture), note that for CPUxDIV > 0, field Count Value in register CCNT still represents SRI clock cycles.

4.35 [CPU_TC.H010] External Accesses to CPU Local Memory may delay CPU Execution Progress

Description

A sequence of contiguous external accesses to the CPUx local memory (DSPR/DCache, PSPR/PCache) may delay the CPUx execution progress for a potentially long time.

External accesses to the CPUx local memory may arrive from several agents (CPUy, DMA, etc.), therefore, the resulting sequence of external accesses to the CPUx local memory may be contiguous, even if each of the agents is leaving some gaps between its requests.

***Note**: The CPUx execution continues when the external access sequence is finished. There is no impact on the correctness of code execution.*

Known Cases

- An external access to DSPR memory may delay CPUx execution progress, if CPUx is accessing its local DSPR memory or using Data Cache. Local accesses to DSPR memory include: data load and store, context save and restore operations
- An external access to PSPR memory may delay CPUx execution progress, if CPUx is executing code from a memory other than its own local PSPR and Program Cache is enabled

Recommendations

- Reduce the frequency of external accesses to DSPR and PSPR memory
- Introduce gaps in long access sequences to DSPR and PSPR memory

4.36 [CPU_TC.H012] Behavior of bit-wise operations on certain peripheral register bits which need to be written back with the same value

Description

The LDMST, ST.T, CMPSWAP.W, SWAPMSK.W and SWAP.W instructions in the AURIX™ microcontrollers are instructions intended to provide atomicity as well as bit-wise operations to a targeted memory location or peripheral register. They are also referred to as Read-Modify-Write (RMW) instructions.

In some registers in certain modules, a bit has to be written with the same value (for example a bit set to 1_B has to be written with a 1_B to perform an operation).

When using a RMW instruction to write to such a bit, the write is masked away and will not happen at all.

***Note**: Writing a different value (for example writing a 1_B to a bit currently at 0_B) is not affected, and works as expected to modify only the selected bit.*

Example

Consider the GxVFR register in the VADC module:

GxVFR (x = 0 - 10)
Valid Flag Register, Group x ($x * 0400_H + 05F8_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VF15	VF14	VF13	VF12	VF11	VF10	VF9	VF8	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VFy (y = 0 - 15)	y	rwh	**Valid Flag of Result Register x** Indicates a new result in bitfield RESULT or in bit FCR. 0_B Read access: No new valid data available Write access: No effect 1_B Read access: Result register x contains valid data and has not yet been read, or bit FCR has been updated Write access: Clear this valid flag and bitfield DRC in register GxRESy (overrides a hardware set action)

Figure 8 Register GxVFR in the VADC Module of TC2xx Devices

The bits in the GxVFR register have to be written with 1_B to clear a valid flag VFy indicating a valid result. Assuming VFy = 1_B, if one of the RMW instructions listed above is used, the write to VFy would never happen since VFy is already set to 1_B. This means that the next read of VFy may lead to incorrect conclusions by software.

Affected Modules and Registers in the AURIX™ Platform

- CCU6: IMON
- VADC: GxVFR, GxSEFLAG, GxCEFLAG, GxREFLAG, GLOBEFLAG

***Note**: VADC is located outside the addressable range of ST.T, so ST.T need not be considered in the context of VADC.*

Recommendation

In the affected modules, use only direct writes (i.e, write the whole register as a 32-bit word), and do not use RMW operations to write to such bits.

For example, to clear bit VF0 in the GxVFR register, the software should write:

```
VADC_GxVFR.U = 0x00000001;
```

Here .U implies writing the whole 32-bit register as an unsigned integer.

4.37 [CPU_TC.H014] ACCEN* Protection for Write Access to Safety Protection Registers - Documentation Update

Description

The access protection symbol ‘P’ to indicate protection by the ACCEN* register mechanism is missing in column “Access Mode - Write” in table “Safety Protection Registers” in the CPU chapter of the User’s Manual for RGN*x registers with an index x ≥4, and for register ACCENA.

Actually, these registers also have write access attribute ‘P’.

4.38 [CPU_TC.H015] Register Access Modes for Safety Protection Registers - Documentation Update

Description

The access protection symbol ‘U’ is erroneously included and should be removed in column “Access Mode - Write” for all registers in table “Safety Protection Registers” in the CPU chapter of the User’s Manual.

The note below this table is rephrased as follows:

***Note**: A disallowed access to any CPU register (for example attempted write to non-existent register, attempted write to read only register, attempted access to E without Endinit, etc.) will NOT result in a Bus Error*

4.39 [CPU_TC.H017] MSUB.Q does not match MUL.Q+SUB - Documentation Update

Description

The AURIX™ implementation of MSUB.Q uses infinitely precise intermediate results. In contrast with AUDO™ devices this can lead to different observable results for MSUB.Q when compared with a MUL.Q+SUB sequence.

The following table describes these differences in the MSUB.Q behaviour in AURIX™ 1st and 2nd generation products.

***Note**:*
- *For 1st generation AURIX™ devices (TC2xx), this is a documentation update to the TriCore™ TC1.6P & TC1.6E Core Architecture Manual V1.0D15 (Vol.2 Instruction Set)*
- *The TriCore™ TC1.6.2 Core Architecture Manual (Vol.2 Instruction Set) V1.1 and following for 2nd Generation AURIX™ (TC3xx) contains these new definitions*

Table 32 MSUB.Q Definitions in AURIX™ different from AUDO™

Secondary Opcode [23:18]	Instruction Mnemonic	Updated Description
0x00	**MSUB.Q D[c], D[d], D[a], D[b] U, n** 32 - (32 * 16U)Up --> 32	result = ({D[d], 16’h0000} - ((D[a] * D[b][31:16]) << n)) >> 16;D[c] = result[31:0]; // Fraction
0x01	**MSUB.Q D[c], D[d], D[a], D[b] L, n** 32 - (32 * 16L)Up --> 32	result = ({D[d], 16’h0000} - ((D[a] * D[b][15:0]) << n)) >> 16;D[c] = result[31:0]; // Fraction
0x02	**MSUB.Q D[c], D[d], D[a], D[b], n** 32 - (32 * 32)Up --> 32	result = ({D[d], 32’h0000_0000} - ((D[a] * D[b]) << n)) >> 32;D[c] = result[31:0]; // Fraction
0x20	**MSUBS.Q D[c], D[d], D[a], D[b] U, n** 32 - (32 * 16U)Up --> 32	result = ({D[d], 16’h0000} - ((D[a] * D[b][31:16]) << n)) >> 16;D[c] = ssov(result, 32); // Fraction

(table continues...)

Table 32 (continued) MSUB.Q Definitions in AURIX™ different from AUDO™

Secondary Opcode [23:18]	Instruction Mnemonic	Updated Description
0x21	**MSUBS.Q D[c], D[d], D[a], D[b] L, n** 32 - (32 * 16L)Up --> 32	result = ({D[d], 16'h0000} - ((D[a] * D[b][15:0]) << n)) >> 16;D[c] = ssov(result, 32); // Fraction
0x22	**MSUBS.Q D[c], D[d], D[a], D[b], n** 32 - (32 * 32)Up --> 32	result = ({D[d], 32'h0000_0000} - ((D[a] * D[b]) << n)) >> 32;D[c] = ssov(result, 32); // Fraction

4.40 [CPU_TC.H019] Semaphore handling for shared memory resources

Description

In a multiprocessor system, sharing state between different cores is generally guarded by semaphores or mutexes.

In AURIX™ TC3xx and TC2xx devices specific synchronization steps are needed to achieve specific results for programs running concurrently on multiple processors.

Special care needs to be taken in software when guarded state and semaphores are located in different memory modules.

When the paths from two CPUs to common memory resources are not the same for both CPUs, the effect of two generic stores from one CPU can appear in the opposite order to two generic loads from the other CPU if correct synchronization steps are not taken. This can happen when the master releasing the semaphore has a different access path to a shared resource than to its associated semaphore. In this case, it is possible for another master to observe the semaphore update prior to the final update of the guarded state.

In order to guarantee that the guarded state update is globally visible, both correct sequence and correct synchronization are required. A master must first acquire the semaphore to ensure correct synchronization. It is also required to include a DSYNC in the semaphore acquire and release methods. DSYNC waits until the store buffer is empty and then DSYNC completes ensuring correct sequence. In a multi-domain crossbar where one of the paths from the master to the shared resource involves an SRI extender, additional steps are required to ensure correct sequence. In such a case it is highly recommended to locate the semaphore and shared buffer in the same memory module.

Operational Details

From a CPU's point of view, resources can be accessed in different ways:

- Local resource to the CPU
  - Local DSPR
  - Local DLMU (AURIX™ TC3xx)
- SRI accessed resource
  - Any resource accessed via the SRI on the local crossbar
- SRI accessed resource via SRI bridge (AURIX™ TC3xx)
  - Any resource located behind an SRI to SRI bridge in a multi-domain crossbar (relative to the accessing master)

In the case of multi-domain crossbars connected by SRI to SRI bridges there may be multiple paths of different latency from masters to shared resources potentially involving different bridges. When the guarded state is a shared memory location, the sequence observed by each master is guaranteed to be the same as long as the semaphore and guarded state are located in the same memory module. If semaphore and guarded state are not located in the same memory module then a load from the module is required prior to releasing the semaphore.

In order to achieve correct synchronization between the different masters, correct semaphore handling is required.

Acquiring and Releasing semaphores - Recommendations

In order to ensure correct sequence and synchronization a DSYNC instruction should be used as part of the semaphore acquire and release sequences. Additionally, a typical use case always requires the acquisition of the semaphore prior to accessing the guarded resource. The DSYNC waits until the store buffer is empty and then completes.

- Acquiring semaphores: A sequence of atomic compare and swap followed by a DSYNC
- Releasing semaphores: A sequence of DSYNC followed by the clearing of the semaphore

Examples

The following examples refer to memory accesses to non-peripheral regions (i.e. segments 0_H ..D_H). These examples are just describing the memory operations and not the complete sequence of operations

Example 1a: Out of order memory access due to different access paths to semaphore and shared resource

In this example, the semaphore is local to CPUx and the resource is local to CPUy. CPUx already owns the semaphore at the start of the described sequence. CPUy has not acquired the semaphore prior to accessing the resource.

Table 33 Example 1a: Out of order memory access due to different access paths to semaphore and shared resource

CPUx	CPUy	Memory Access Sequence
st-1 (resource-update)	ld-1 (semaphore-check)	
st-2 (semaphore-release)	ld-2 (resource-read)	
		st-2 (semaphore-release)
		ld-1 (semaphore-check)
		ld-2 (resource-read) “stale data”
		st-1 (resource-update)

Example 1b: Access order is enforced by correct semaphore handling

Table 34 Example 1b: Access order is enforced by correct semaphore handling

CPUx	CPUy	Memory Access Sequence
st-1 (resource-update)	CMPSWAP.W (semaphore-acquire)	
DSYNC	DSYNC	
st-2 (semaphore-release)	ld-1(resource-read)	
		st-1 (resource-update)
		st-2 (semaphore-release)
		CMPSWAP.W (semaphore-acquire)
		ld-1(resource-read)

A master may only access a resource if the associated semaphore is acquired successfully.

***Note**: CMPSWAP.W is only used here as an example. TriCore™ provides several other instructions supporting the implementation of semaphore operations*

4.41 [CPU_TC.H021] Resource update failure despite correct SW synchronization upon retried FPI write transactions by CAN and E-Ray modules

Description

***Note**: Module names in the text follow the TC3xx syntax conventions. Correlation of module names:*

- ***TC3xx**: MCMCAN*
- ***TC2xx**: MultiCAN+*

In a multiprocessor system, sharing the same resource between different CPUs is generally guarded by semaphores or mutexes. A DSYNC instruction is used in the semaphore's acquire and release methods in order to guarantee correct synchronization between the CPUs.

In certain situations, peripherals including MCMCAN and E-Ray may not immediately accept some write operations and they remain pending and will be retried. Ordinarily this behavior is invisible to the system as the CPU's subsequent FPI transactions will be delayed till the operation is complete.

In this scenario, CPUx's (which has the semaphore) execution of DSYNC incorrectly views the pending store operation as complete and itself completes too early. CPUx then releases the semaphore, allowing the other CPU (CPUy) to acquire the semaphore and commence accessing the shared resource.

Under certain circumstances, the pending write operation by CPUx may be retried multiple times by the module and may still not have completed. This can lead to CPUy accessing the MCMCAN or E-Ray module before the state intended by CPUx has been established. An example sequence in the table below shows the incorrect behavior.

Table 35 Possible SW/HW interaction producing incorrect state

CPUx	CPUy	Incorrect resource access sequence
Resource update (store instruction)	Semaphore check	CPUx – Resource update first attempt (becomes pending FPI write)
DSYNC	...	CPUx - DSYNC incorrectly completes
Semaphore release	...	CPUx – Semaphore release
...	Semaphore acquire	CPUy – Semaphore acquire
...	Resource read (load instruction)	CPUy – Resource read (incorrect state)
...	...	CPUx - Pending FPI write succeeds (Resource update completed)

Scope

This problem is limited to software running in different CPUs using the same shared resource of the peripherals MCMCAN or E-Ray.

Recommended sequence (workaround)

A read operation to the shared resource must be performed by the first CPU (CPUx) before execution of the DSYNC instruction.

Hence, the modified sequence of CPUx for the example given above must be:

- Resource update (store instruction)
- Resource read (load instruction)
- DSYNC
- Semaphore release

4.42 [DAP_TC.H002] DAP client_blockread in Combination with TGIP and all Parcels with CRC6

Description

***Note**: This problem is only relevant for tool development, not for application development.*

When issuing a DAP client_blockread telegram together with the TGIP (Trigger in Protocol) option (DAPISC.TGIP = 1) the TGIP extra bit is appended for each parcel in case “all parcels with CRC6” is enabled. This causes a slight increase in the communication length compared to the correct behavior of having a TGIP bit only for the last parcel.

Recommendation

Do not use the TGIP and “CRC6 for all parcels” features together in case this extra bit can not be tolerated. If the Trigger in Protocol and increased communication safety is required TGIP can be used together with the CRC32 option (see also DAP_TC.002 DAP client_blockread has Performance issue in Specific Operation Modes).

4.43 [DAP_TC.H003] Not acknowledged DAP telegrams in noisy environments

Description

***Note**: This problem is only relevant for tool development, not for application development.*

DAP telegrams always follow a request-reply scheme. The request is driven by the tool, the reply by the AURIX™. The AURIX™ acknowledges a correctly received telegram always by a reply, which consists at least of a start-bit. DAP communication in noisy environments might result in invalid telegrams. This can leave the IOClient in an intermediate state which requires an IOClient reset.

If AURIX™ receives an invalid telegram with a wrong CRC6 or length field, it does not reply at all and in some cases the selected IOClient might be left in an intermediate state in case of a detected client_write/blockwrite/readwrite tool request.

Recommendation

If a tool does not receive a start bit as an acknowledge for an IOClient request, a client_reset must be sent as the next telegram for the selected IOClient. Tool interaction with the DAP module itself is not affected and can be done in between.

4.44 [DMA_TC.H002] Bit CHCSRz.BUFFER can be toggled when not in Double Buffer Mode

Description

The purpose of bit CHCSRz.BUFFER is to indicate which buffer is read or filled during DMA double buffering (selected in bit-field ADICRz.SHCT).

However, bit CHCSRz.BUFFER can also be toggled by writing bit CHCSRz.SWB = 1_B when not in Double Buffer Mode.

Recommendation

Do not write bit CHCSRz.SWB = 1_B when not in Double Buffer Mode.

4.45 [DMA_TC.H003] Spurious Error Interrupt Service Requests after Transaction Lost Event in Double Buffer Mode

Description

When a DMA channel is configured for any double buffering operation (ADICRz.SHCT[3:2] = 10_B) then there is a possibility of spurious error interrupt service requests.

If a Transaction Request Lost event occurs (TSRz.TRL = 1_B) AND if the transaction request lost interrupt is enabled (ADICRz.ETRL = 1_B) then there is a possibility that spurious error interrupt service requests will be generated.

No Transaction Request Lost (TRL) events will be missed, but one TRL event may result in multiple error interrupt service requests.

Recommendation

It is recommended that if an error interrupt service request is triggered then bit TRL should be cleared immediately by writing TSRz.CTL = 1_B to prevent further spurious error interrupt service requests.

4.46 [DMA_TC.H004] Transaction Request Lost upon software trigger with pattern match

Description

If a DMA channel is configured for pattern detection and software triggering of each DMA transfer (CHCSRz.RROAT = 0_B), then if there is a new DMA software request received while a DMA transfer is executing then a Transaction Request Lost event may be lost.

Recommendation

The loss of TRL status is a debug feature. A DMA channel should be used such that TRL is not set.

The user must ensure that the CPU triggers a new DMA software request when no DMA access is pending.The software could poll the TSRz.CH bit to confirm it is 0_B before issuing a DMA software trigger.

4.47 [DMA_TC.H005] Linked List Transfer leading to loading of non-Linked List TCS causes corruption

Description

If on completion of a Linked List (LL) a non-LL Transaction Control Set (TCS) is loaded with shadow address buffering enabled (read only and direct write) then the new non-LL TCS can be corrupted.

Recommendation

Shadow address buffering must be disabled in the non-LL TCS (SHCT[3:0] = 0000_B)

4.48 [DMA_TC.H006] Clearing of HTRE when DMA channel is configured for Single Mode

Description

The DMA may be used to support a peripheral with a high interrupt rate where the interrupts are generated in quick succession (for example a QSPI filling a TXFIFO).

The DMA channel z is configured with the following settings:

- Single Mode (HTRE is reset by hardware on completion of a DMA transaction)
  - TSRz.CHMODE = 0_B
- Request required for each DMA Transfer
  - TSRz.RROAT = 0_B

If the DMA channel is configured to execute a DMA transaction of 1 x DMA transfer of 2 x DMA moves:

- Block Mode: 2 x DMA Move per DMA transfer
  - DMA_CHCFGRz.BLKM = 001_B
- Transfer Reload Value: 1 x DMA transfer
  - DMA_CHCFGRz.TREL = 1_B

then additional DMA moves are executed unexpectedly.

Explanation of Effect

If the peripheral generates two interrupt service requests in relatively quick succession then the first DMA hardware request is serviced by the DMA and performs one DMA transfer comprising two DMA moves. The second DMA hardware request arrives before the completion of the first DMA transfer (i.e. before the clearing of HTRE at the end of the DMA transaction). The second hardware request is serviced by the DMA and performs a second DMA transfer comprising two DMA moves.

Recommendation

If the second DMA hardware request arrives before completion of the first DMA transfer then the DMA channel Block Mode must limit a DMA transfer to one DMA move:

- DMA_CHCFGRz.BLKM = 000_B; //1 x DMA move/DMA transfer

The total number of DMA moves must be defined by the Transfer Reload Value DMA_CHCFGRz.TREL.

4.49 [DMA_TC.H007] Selecting the Priority for DMA Channels

Description

All used DMA channels should be configured with the **highest** priority on SPB in respect to other used SPB master agents (CPUs, HSSL, ETH) to enable a robust execution of the configured DMA transactions.

The DMA channels are configured per default with the **lowest** priority on SPB:

- DMA_CHCFGRz.DMAPRIO = 00_B --> maps DMA channel z SPB requests to SPB priority DMAL
- SBCU_PRIOH.DMAL = 1111_B --> configures DMAL with the lowest priority on SPB

Recommendation

There are several ways to configure used DMA channels with the highest priority on SPB with respect to other SPB master agents. Two examples follow:

Example1

Map the used DMA channels to SPB priority DMAH by setting DMA_CHCFGRz.DMAPRIO = 11_B and keep the configuration of the DMAH priority (SBCU_PRIOL.DMAH = 0000_B).

Example2

Keep the mapping of the used DMA channels to DMAL (DMA_CHCFGRz.DMAPRIO = 00_B) and change the priority configuration of DMAL (for example set SBCU_PRIOH.DMAL = 0001_B).

Background

The DMA can request for SPB access with three different requests (DMAH, DMAM, DMAL) that are configured with different SPB priorities with respect to the other SPB master agents (CPUx, HSCT, ETH). The priority of the DMA requests DMAH, DMAM and DMAL on the SPB in respect to the priority of other SPB master agents can be configured via the SBCU registers SBCU_PRIOL / SBCU_PRIOH.

Each DMA channel z can be configured via DMA_CHCFGRz.DMAPRIO regarding which of three priorities (DMAH, DMAM or DMAL) it uses for SPB access.

The default configuration of DMA_CHCFGRz.DMAPRIO = 00_B. This means that the channels will request for SPB access with the DMAL priority.

The priority of a DMAL request on SPB is configured per default with the lowest priority (SBCU_PRIOH.DMAL = 1111_B).

4.50 [DMA_TC.H008] Transaction Request State

Description

The DMA Transaction Request State bit DMA_TSRz.CH is cleared when the DMA transfer starts (RROAT = 0_B) or at the end of a DMA transaction (RROAT = 1_B).

Figure “Channel Request Control” and RROAT bit-field description of register DMA_MExCHCR in chapter “Register Description” of the User’s Manual are wrong.

4.51 [DMA_TC.H009] Resetting Bits ICH and IPM in register CHCSRz

Description

The Clear Interrupt from Channel bit (CICH) is accessible via the DMA channel CHCSR register.

The AURIX™ TC2xx User Manuals are incorrect with respect to the following statement:

- The DMA channel DMA_CHCSRz ICH and IPM bit-field description states: “is reset by software when writing a 1 to ADICRz.CICH”

Correction

- The text should read: “is reset by software when writing a 1 to **CHCSRz**.CICH”

4.52 [DMA_TC.H010] Calculation of DMA Address Checksum for DMA read moves to Cacheable Addresses

Description

The DMA Move Engine (ME) stores the DMA read move data in eight 32-bit read registers. If a DMA read move is to a cached address (Segment 8 or 9), the ME shall translate the DMA read move access to the on chip bus into an SRI BTR4 access to a 32-byte aligned address. The DMA shall calculate the DMA address checksum from the on chip bus address i.e. the 32-byte aligned address. The DMA shall store the DMA address checksum in the SDCRCR.

Recommendation

If an expected DMA address checksum is pre-calculated to test the DMA address generation, the user shall take note of the address translation to 32-byte aligned addresses when calculating the expected DMA address checksum from a cacheable DMA source address.

Alternatively, DMA read moves should be performed to non-cacheable source addresses (segments A and B).

4.53 [DMA_TC.H011] DMA_ADICRz.SHCT - Reserved Values

Description

The DMA channel shadow control bit-field DMA_ADICRz.SHCT controls the function of the shadow address register. If software programs a reserved value in DMA_ADICRz.SHCT, the DMA may deadlock the operation of the DMA.

Therefore, software shall not program DMA_ADICRz.SHCT with the following reserved values:

- 0011_B Reserved
- 0100_B Reserved
- 0111_B Reserved

4.54 [DMA_TC.H012] TCS Update in Halt State

Description

If a DMA channel is in halt state,

- The DMA shall stop performing DMA moves to the destination location
- Software may perform a background test on the destination location
- Software may modify the DMA channel Transaction Control Set (TCS)

Recommendation

If software modifies the DMA channel TCS, software shall only modify the DMA channel source address (DMA_SADRz.SDAR) and the DMA channel destination address (DMA_DADRz.DADR).

4.55 [DMA_TC.H013] MExSR.WS and MExSR.RS Status Bits

Description

As documented in the User's Manual, the Move Engine (ME) status bits RS/WS in register MExSR are set when the ME is performing a read move or DMA write move. This means:

- MExSR.RS = 1_B when the ME is performing a DMA read move for the active DMA channel
- MExSR.WS = 1_B when the ME is performing a DMA write move for the active DMA channel

It should be noted that the setting of these bits is not restricted to DMA read move and DMA write move. Additionally the status bits may be set when the ME is performing other operations:

- MExSR.RS = 1_B when the ME is loading a new Transaction Control Set in a linked list
- MExSR.WS = 1_B when the ME is writing a DMA timestamp

***Note**: The additional setting of the ME status bits may be observed when debugging the operation of the DMA. There is no effect on the operation of the DMA.*

4.56 [DMA_TC.H014] DMARAM Error Interrupt Service Request

Description

If the DMA is enabled to trigger a RAM error interrupt service request (DMA_EERx.ERER = 1_B) and the DMA detects a fault during a DMARAM read access, it will correctly store the error status (DMA_ERRSRx.RAMER = 1_B) and trigger an error interrupt service request.

However, if the MTU is not clocked, the DMA will trigger an error interrupt service request for all subsequent accesses to DMARAM.

Recommendation

The MTU must be clocked to prevent the erroneous triggering of RAM error interrupt service requests.

4.57 [DMA_TC.H015] DMARAM Address Integrity Errors

Description

DMARAM address integrity errors are routed to the Safety Management Unit (SMU) via the Memory Test Unit (MTU).

Recommendation

The MTU must be clocked in order for the system to capture DMARAM address integrity errors.

If the application software receives notification of an alarm, the application software shall first check which alarm is set inside the SMU by reading the SMU alarm status registers. If the alarm is ALM4[18] (MISC alarm, SRAM address alarm), the software should check which MBIST controller is the source of the alarm. The application software must resolve the alarm in accordance with the AURIX Safety Manual (AP32224).

4.58 [DMA_TC.H016] DMARAM ECC Error Disable

Description

If software disables SPB bus errors caused by DMARAM ECC errors (DMA_MEMCON.ERRDIS = 1_B), the DMA will not correctly acknowledge a Read Modify Write (RMW) access on the SPB bus.

Recommendation

The application software must always enable the reporting of SPB errors (DMA_MEMCON.ERRDIS = 0_B; default after reset).

4.59 [DMA_TC.H017] DMA Channel Request Control - Documentation Update

Description

The following text (located below figure “Channel Request Control” in section “DMA Channel Request Control” of the DMA chapter in the User’s Manual):

“If CHCFGRz.PRSEL = 1 in the current DMA channel z can bypass the ICU and trigger a DMA hardware request in the next lower DMA channel z-1. The latency to service a DMA channel z-1 request is reduced. DMA channel z interrupt service requests are disabled.”

should read as :

“If DMA_CHCFGRz.PRSEL = 1 **is selected** in the current DMA channel z, **a DMA channel trigger** can bypass the ICU and trigger a DMA hardware request in the next lower DMA channel z-1. The latency to service a DMA channel z-1 request is reduced. DMA channel z interrupt service requests are disabled.”

4.60 [DSADC_TC.H002] Influence of Temperature on DC Offset Error EDOFF (calibrated)

Description

The performance of the DSADC can be improved by applying some calibration techniques to compensate temperature effects.

For example, parameter “DC Offset Error” (symbol *EDOFF*) may exceed the specified Data Sheet value of ±5 mV (test condition = calibrated) when temperature has changed by more than approximately 20°C after calibration.

Recommendation

To compensate temperature effects it is recommended to repeat the calibration sequence when the device temperature has changed by approximately 20°C. (see section “Calibration Support” in DSADC chapter of the User’s Manual).

4.61 [DSADC_TC.H003] FIR Filters not reset when Integration starts

Description

When the integration window is started, the CIC filter and the integrator are reset. However, the FIR filters are not reset in this case.

If the FIR filters are active, the time delay to the first result value is not constant, but is shortened by 1/4, 2/4, or 3/4 of a result data period, depending on the current state of the FIR filters.

For repeated measurements, this may cause a timing jitter from the start of the integration window until the first result is available.

Recommendation

To compensate the effect on the discard phase, the number of values discarded may be increased by 1 (bit-field NVALDIS in register IWCTRx).

In case the jitter in the result timing is not tolerable,

- either do not use the FIR filters and perform integration by software
- or force a reset of the entire chain including the FIR filters by switching off/on the corresponding CHxRUN bit in register GLOBRC for example via DMA

4.62 [DSADC_TC.H004] Full-scale Values produced by On-chip Modulator

Description

Due to SNR improvements, the full-scale values produced by the on-chip modulator in this device step differ by a factor of about 2 from previous device steps, as shown in the following table. See also chapter “Filter Configuration and Control”, subchapter “Recommended Settings” in the User’s Manual.

Table 36 Full-scale Values produced by On-chip Modulator

Full-Scale Values	TC27x Step ≥ DA, TC29x and TC26x Step ≥ BA	TC27x Step ≤ CA, TC29x and TC26x Step = Ax
Uncalibrated average value	$\pm 3600_D$ ($0E10_H$ / $F1F0_H$)	
Value used in example calculation to avoid filter overflows	$\pm 3800_D$ ($0ED8_H$ / $F129_H$)	$\pm 1900_D$ ($076C_H$ / $F894_H$)

Recommendation

For this device step (TC27x step ≥ DA, TC29x and TC26x step ≥ BA), use the value of 3800_D to calculate the setup of the filter chain. To avoid overflow and clipping of values within the filter chain, the magnitude of the result values must not exceed $\pm 2^{15}$ at any stage.

When migrating from previous design steps, the increased output amplitude of this design step may be compensated by the data shifter setting (FCFGMx.FSH = 0_B instead of 1_B in the example given in the User’s Manual).

4.63 [DSADC_TC.H005] Data Strobe Setting for On-chip Modulator

Description

In this device step, the improved on-chip modulator uses the rising edge of the modulator clock to transfer the data values to the digital filter chain. To ensure proper reception of this data, the filter chain must evaluate the data values with the **falling** edge of the modulator clock.

Recommendation

Bitfield STROBE in register DICFGx must be set to 0010_B.

The description of bit-field DICFGx.STROBE will be adjusted accordingly in the next revision of the User's Manual as shown in Table 37.

Table 37 DICFGx (Demodulator Input Configuration Register x), Bitfield STROBE

Field	Bits	Type	Description
STROBE	[23:20]	rw	**Data Strobe Generation Mode** 0000_B No data strobe **0010_B** Direct clock, a sample trigger is generated at each **falling** clock edge Other combinations are reserved

4.64 [DSADC_TC.H006] Avoiding Intermediate States

Description

The DSADC may experience unintended intermediate states in the two scenarios identified below. To avoid these states, consider the following recommendations:

Intermediate States due to External Signals

External control signals are not specially filtered. Therefore, glitches on those external signals may also affect the internal functions controlled by them.

To ensure proper operation of the externally controlled functions, it is recommended to provide glitch-free control signals.

The following input signals should be considered:

- Trigger inputs (ITRxy)
- External carrier sign (SGNA, SGNB)

Alternatively, internal signal sources can be selected for the respective functions.

Intermediate States during Configuration

Similarly, it is recommended to change configurations only while modulator and channel are stopped.

This avoids unintended intermediate states.

Recommended sequence:

1. Write the static configuration while modulator and demodulator are disabled (GLOBRC.MxRUN = 0_B, GLOBRC.CHxRUN = 0_B)
2. Enable the modulator (GLOBRC.MxRUN = 1_B) and wait for the modulator to settle (see Data Sheet, parameter "Modulator settling time" t_{MSET})
3. Enable the demodulator (GLOBRC.CHxRUN = 1_B)

4.65 [DSADC_TC.H007] Dithering Control

Description

The dithering feature reduces the idle tones caused by low-frequency input signals and minimizes the dead-zone.

After reset, dithering is enabled, but the dithering trim value is 000_B (minimum intensity).

Recommendation

To optimize the effect, it is recommended to select a higher dithering intensity:

- DITRIM = 001_B (low intensity) ensures the conversion performance (SNR) in all cases, but leaves a residual dead-zone of approximately 2 mV
- DITRIM = 011_B (medium intensity) reduces the residual dead-zone below -80 dB. In this case, the voltage of the input signal must not exceed 90% of the reference voltage and an oversampling rate of OSR ≥ 200 is required to achieve an SNR of 80 dB

4.66 [DSADC_TC.H008] DSADC Gain Calibration Procedure

Description

In order to improve the overall accuracy of the DSADC, an algorithm for the gain calibration using the High-Precision Square wave Generator (HPSG) is proposed in section “Gain Calibration Support” of the User’s Manual.

The calibration is done by following the sequence for measuring the output signal of the HPSG as described in the User’s Manual. After enabling the calibration mode, the HPSG needs up to half a period for settling. In order to achieve a reproducible result it is highly recommended to read a sequence of values for at least two full periods. Then evaluate a complete period for example between two rising edges of the square wave for calculating the amplitude of the waveform and go on with the calculation as proposed in the User’s Manual.

For your reference, the corresponding bullet points are copied from the description in the Users Manual and extended accordingly:

- Enable gain calibration mode (MODCFGx.GCEN = 1)
- Determine the actual amplitude by converting the high level and the low level of the square wave signal. Result = AM.
  - Read a sequence of result values for at least two full periods
  - Then evaluate a complete period for example between two rising edges of the square wave for calculating the amplitude of the waveform
  - Ignore the values close to the signal transitions to exclude the overshoots/undershoots caused by the Gibbs phenomenon (see Figure in User’s Manual)
  - ..

4.67 [DSADC_TC.H009] DSADC digital connections

Description

The port function tables in the current version of the Data Sheet and in the Ports chapter of the User’s Manual may show the following connections in relation to the DSADC

- DSDIN[0:9].[A:B], DSCIN[0:9].[A:C], DSCOUT[0:9]

These signals result from an earlier DSADC design step. They are not supported in the present DASDC implementation and should be disregarded.

Recommendation

For the actually implemented digital connections, see table “Digital Connections in the TC2xx” in the DSADC chapter of the corresponding TC2xx User’s Manual.

4.68 [DSADC_TC.H010] Support for synchronous use of two or more DSADC channels

Description

The Global Run Control register GLOBRC controls the general operation of the available channels of the DSADC module. For every DSADC channel, register GLOBRC supports an individual bit for the related modulator (GLOBRC.MxRUN) and the related digital filter chain (GLOBRC.CHxRUN), where x depends on the number of implemented channels in the respective AURIX™ microcontroller device.

For applications where two or more DSADC channels have to provide synchronous results, all related channels shall be enabled synchronously using a single write access to register GLOBRC. This approach guarantees synchronization between DSADC channels under all loading conditions of the system peripheral bus (SPB).

Recommendation

To handle the DSADC channel specific modulator settling time, the following sequence is proposed:

- Enable all modulators of the application specific synchronization group by a single write access to the corresponding MxRUN bits in the upper half-word of the Global Run Control Register:
  - GLOBRC = 0XXX 0000_H , where XXX_H depends on the number of implemented modulators
- Wait for modulator settling time t_{MSET} (see Data Sheet)
- Enable all modulators and corresponding digital filter chains of the application specific synchronization group by a single write access to the corresponding MxRUN and CHxRUN bits in the Global Run Control Register:
  - GLOBRC = 0XXX $0XXX_H$, where XXX_H depends on the number of implemented modulators/demodulator channels

4.69 [DTS_TC.H001] Update of Bit DTSSTAT.BUSY

Description

The following statement in the description of bit BUSY in register DTSSTAT in the SCU chapter “Die Temperature Measurement” is incorrect:

***Note**: This bit is updated 2 cycles after bit DTSCON.START is set.*

Correction

The correct description is as follows:

***Note**: This bit is updated **7** cycles after bit DTSCON.START is set.*

4.70 [ENDINIT_TC.H001] Endinit Protection for Registers KRST0, KRST1, KRSTCLR

Description

The access protection symbol ‘E’ to indicate Endinit-protection is missing in column “Access Mode - Write” in table “Register Overview” in the User’s Manual for the following registers:

- KRST0, KRST1, KRSTCLR

of the following modules (if implemented):

- E-Ray, ETH, PSI5

4.71 [ETH_AI.H001] Sequence for Switching between MII and RMII Mode

Description

When switching between MII and RMII mode is required, the ETH module must be clocked (MII: RXCLK and TXCLK; RMII: REFCLK) and be in a defined state to avoid unpredictable behavior.

Therefore, it is recommended to use the defined sequence listed below:

1. Finish running transfers and make sure that transmitters and receivers are set to stopped state:
   a. Check the RS and TS status bit-fields in register ETH_STATUS
   b. Check that ETH_DEBUG register content is equal to zero. Note: it may be required to wait 70 f_{SPB} cycles after the last reset before checking if ETH_DEBUG.RXFSTS is zero
2. Wait until a currently running interrupt is finished and globally disable interrupts
3. Apply kernel reset to ETH module:
   a. Deactivate Endinit protection, as registers KRST0/1 and KRSTCLR can only be written in Supervisor Mode and when Endinit protection is not active.

      Write to corresponding RST bits of KRST0/1 registers to request a kernel reset. The reset status flag KRST0.RSTSTAT may be cleared afterwards by writing to bit CLR in the KRSTCLR register.

      Re-activate Endinit protection
   b. Wait 70 f_{SPB} cycles, then check if ETH_DEBUG.RXFSTS is zero
4. Initialize the new mode (MII or RMII) in bit-field GPCTL.EPR
5. Apply software reset by writing to the ETH_BUS_MODE.SWR bit.
   Wait 4 f_{SPB} cycles, then check if ETH_BUS_MODE.SWR = 0_B

4.72 [ETH_TC.H001] ETHMDIO on P21.1 not to be used for productive systems

Description

Unlike the other mapping options for signal ETHMDIO, P21.1 does not have the hardware direction control functionality to automatically switch the direction of ETHMDIO.

Therefore, do not use ETHMDIO on P21.1 in productive systems.

Instead, use the ETHMDIO mappings on P00.0, P12.1, or P21.3 (availability depends on device version and package pin count, see product documentation).

Changing the driver setting of pin P21.1 to speed grade 4 (in P21 Pad Driver Mode register) may allow the external PHY to overdrive the MDIO line. However, this configuration must not be used for productive systems.

4.73 [ETH_TC.H002] Minimum operation frequency for Ethernet MAC

Description

When using the Ethernet MAC module, f_{RAM} must not be lower than 120 MHz.

Recommendation

Use $f_{SPB} \geq 60$ MHz and do not enable the Module Clock Divider, i.e. leave bit ETH_GPCTL.DIV = 0_B (default after reset).

4.74 [ETH_TC.H003] Interrupt Generation by Wake-up or Magic Packet Frames

Description

In order to properly wake up by network (remote) wake-up frames or AMD Magic Packet, the SPB clock must not be switched off.

Recommendation

Therefore, keep the Module Disable Request Bit CLC.DISR = 0_B.

4.75 [ETH_TC.H004] Ethernet MAC Clock Control – Documentation update

Description

The ETH module has multiple clock inputs connecting it to the TC2xx infrastructure, as shown in table “Clock Lines of Ethernet MAC” in the ETH chapter of the TC2x User’s Manual.

Clocks of the ETH module can be disabled/enabled via bit DISS in register ETH_CLC.

***Note**: Field CCUCON1.ETHDIV, described in the SCU chapter, has no effect on the clocks in the ETH module.*

4.76 [FLASH_TC.H007] Advice for using Suspend and Resume

Description

As documented in the User’s Manual section “Operation Suspend and Resume”, an operation is suspended by writing ‘1’ to MARD.SPND. The Flash operation stops when it reaches an interruptible state. After that the flag FSR.SPND is set and BUSY is cleared.

The 1-to-0 transition of MARD.SPND alone is not indicating if the suspend request has been executed and the Flash can accept a new command. The BUSY flags have to be checked to determine if the Flash is still busy with the current operation. Only after the 1-to-0 transition of the BUSY flags the flag FSR.SPND indicates if the operation has finished or if it is in suspended state.

The following recipe describes the best practice for using suspend and resume.

Suspending an Erase Operation

In case of a request for suspending an ongoing erase operation:

As documented in the User's Manual: Please ensure that between start or resume of an erase process and the suspend request normally at least ~1 ms erase time can pass.

- Check if the corresponding BUSY flag has already cleared. If yes, no suspend is necessary
- Request the suspend with control flag MARD.SPND = 1_B

- Wait until the BUSY flag clears
- After that check FSR.SPND. If this is 1_B then the operation was suspended and needs to be resumed later. If this is 0_B the operation has already finished, therefore no resume is necessary
- Now new Flash operations are allowed with the restrictions documented in User's Manual section “Operation Suspend and Resume”

Note for PFlash erase operations in bank x that PxBUSY and D0BUSY are set at the beginning. The D0BUSY is cleared early after updating the Erase Counters, and PxBUSY is cleared when the erase operation has finished. Therefore, for PFlash the PxBUSY flag has to be used. (Polling for PxBUSY and DxBUSY can be a generic solution for suspend sequences before checking the SPND state.) Interrupt driven software receives two interrupts!

Resuming a Suspended Erase Operation

The resume of the suspended erase operation is done in these steps:

- Resume the operation with the command sequence “Resume Prog/Erase”
- Wait until FSR.SPND is 0_B
- After that wait for the end of the operation signalled by BUSY going to 0_B

Suspending a Program Operation

In case of a request for suspending an ongoing programming operation:

- Request the suspend with control flag MARD.SPND = 1_B
- Wait until the BUSY flag clears
- After that check FSR.SPND. If this is 1_B then the operation was suspended and needs to be resumed later. If this is 0_B the operation has already finished, therefore no resume is necessary
- Now new Flash operations are allowed with the restrictions documented in User's Manual section “Operation Suspend and Resume”

Resuming a Suspended Program Operation

The resume of the suspended programming operation is done in these steps:

- Resume the operation with the command sequence “Resume Prog/Erase”
- Wait until FSR.SPND is 0_B
- After that wait for the end of the operation signalled by BUSY going to 0_B

4.77 [FLASH_TC.H008] Understanding Flash Retention/Endurance Figures in the Data Sheet

Description

Flash retention/endurance is documented in the Data Sheet by the following parameters

- Program Flash Retention Time t_{RET} for PFlash
- UCB Retention Time t_{RTU} for the UCBs
- Data Flash Endurance per EEPROMx sector N_{E_EEP10} for DFlash0
- Data Flash Endurance per HSMx sector N_{E_HSM} for DFlash1 (if available)

Retention

To emphasize the importance of retention, the PFlash and UCB parameters are described as retention time under the condition of a maximum number of cycles.

The value “Min. x years” has to be interpreted as: the data retention is at least x years, i.e. x years or longer after the last programming data stays readable.

The condition “Max. y erase/program cycles” means: this data retention figure is valid if there were not more than y erase/program cycles.

Endurance

For the DFlash the endurance is most important, therefore as parameter the number of cycles under the condition of the retention is given.

The value “Min. x cycles” has to be interpreted as: at least x cycles can be applied.

The condition “Max. data retention time y years” means: this endurance figure is valid if the expected data retention after the last programming is maximum y years.

***Note**: As general remark, these figures are only valid if the parameters given in the Data Sheet are adhered to in their entirety.*

4.78 [FLASH_TC.H009] PFlash Operations Concurrent to DF1 Operations

Description

***Note**: The effect described in the following affects only devices with activated HSM.*

In the PMU chapter, the User’s Manual describes under the headline “Time Slice Control” in chapter “HSM Command Interface” how time slicing is used to share common Flash resources between operations by the host in DF0 and by the HSM in DF1.

In order to ensure isolation of HSM DF1 operations from the host side, the PMU doesn't prevent concurrent operations of PFlash and DF1. This mode is however considered as operation “out of specification”. The correct functionality of the operations is ensured but their timing can deviate from Data Sheet values.

Notably parameter “PFlash suspend to read latency” t_{SPNDP} may increase to ~ 5 ms. Due to time slicing the duration of PFlash operations is increased as described in the User's Manual for the DF0/DF1 concurrency.

Recommendation

Don't let HSM perform DF1 operations while the host performs Flash operations in the PFlash. In typical applications this is anyhow ensured because HSM needs to execute from its RAM during ongoing PFlash operations as these prevent read access to its code sectors.

4.79 [FLASH_TC.H022] Flash Wait State configuration

Description

Configuring flash wait states in your application is critical for correct operation.

Refer to these parts of the documentation of the respective TC2*x design step for guidance on avoiding data read errors over the lifetime of the device:

- Data Sheet, chapter “Flash Parameters”:
  - minimum access times t_{PF} / t_{PFECC} for PFLASH
  - and t_{DF} / t_{DFECC} for DFLASH
- AURIX™ TC2*x User’s Manual, PMU chapter “Configuring Flash Wait Cycles”

When **increasing** the SRI and FSI clock frequencies: first set the wait state bit-fields (WSECPF, WSPFLASH, WSECDF, and WSDFLASH) in register FCON to the correct values, and then change the clock configuration.

When **decreasing** the SRI and FSI clock frequencies: first change the clock configuration, and then set the wait state bit-fields (WSECPF, WSPFLASH, WSECDF, and WSDFLASH) in register FCON to the correct values.

***Note**: Applications that omit configuration of FCON may work in the development phase, but encounter data read errors in the field.*

4.80 [FlexRay_AI.H004] Only the first message can be received in External Loop Back mode

Description

If the loop back (TXD to RXD) will be performed via external physical transceiver, there will be a large delay between TXD and RXD.

A delay of two sample clock periods can be tolerated from TXD to RXD due to a majority voting filter operation on the sampled RXD.

Only the first message can be received, due to this delay.

To avoid that only the first message can be received, a start condition of another message (idle and sampling '0' -> low pulse) must be performed.

The following procedure can be applied at one or both channels:

- wait for no activity (TEST1.AOx = 0 -> bus idle)
- set Test Multiplexer Control to I/O Test Mode (TEST1.TMC = 2), simultaneously TXDx = TXENx = 0
- wait for activity (TEST1.AOx = 1 -> bus not idle)
- set Test Multiplexer Control back to Normal signal path (TEST1.TMC = 0)
- wait for no activity (TEST1.AOx = 0 -> bus idle)

Now the next transmission can be requested.

4.81 [FlexRay_AI.H005] Initialization of internal RAMs requires one eray_bclk cycle more

Description

The initialization of the E-Ray internal RAMs as started after hardware reset or by CHI command CLEAR_RAMS (SUCC1.CMD[3:0] = 1100_B) takes 2049 eray_bclk cycles instead of 2048 eray_bclk cycles as described in the E-Ray Specification.

Signalling of the end of the RAM initialization sequence by transition of MHDS.CRAM from 1_B to 0_B is correct.

4.82 [FlexRay_AI.H006] Transmission in ATM/Loopback mode

Description

When operating the E-Ray in ATM/Loopback mode there should be only one transmission active at the same time. Requesting two or more transmissions in parallel is not allowed.

To avoid problems, a new transmission request should only be issued when the previously requested transmission has finished. This can be done by checking registers TXRQ1/2/3/4 for pending transmission requests.

4.83 [FlexRay_AI.H007] Reporting of coding errors via TEST1.CERA/B

Description

When the protocol engine receives a frame that contains a frame CRC error as well as an FES decoding error, it will report the FES decoding error instead of the CRC error, which should have precedence according to the non-clocked SDL description.

This behavior does not violate the FlexRay protocol conformance. It has to be considered only when TEST1.CERA/B is evaluated by a bus analysis tool.

4.84 [FlexRay_AI.H009] Return from test mode operation

Description

The E-Ray FlexRay IP-module offers several test mode options

- Asynchronous Transmit Mode
- Loop Back Mode
- RAM Test Mode
- I/O Test Mode

To return from test mode operation to regular FlexRay operation we strongly recommend to apply a hardware reset via input eray_reset to reset all E-Ray internal state machines to their initial state.

***Note**: The E-Ray test modes are mainly intended to support device testing or FlexRay bus analyzing. Switching between test modes and regular operation is not recommended.*

4.85 [FlexRay_AI.H011] Behavior of interrupt flags in FlexRay™ Protocol Controller (E-Ray)

Description

In the corner case described below, the actual behavior of the interrupt flags of the FlexRay™ Protocol Controller (E-Ray) differs from the expected behavior.

***Note**: This behaviour only applies to E-Ray interrupts INT0 and INT1. All other E-Ray interrupts are not affected.*

Expected behavior

When clearing an interrupt flag by software, the resulting value of the flag is expected to be zero.

A hardware event that occurs afterwards then leads to a zero to one transition of the flag, which in turn leads to an interrupt service request.

Actual behavior in corner case

When the interrupt flag is being cleared by software in the same clock cycle as a new hardware event sets the flag again, then the hardware event wins and the flag remains set without being cleared.

As interrupt requests are generated only upon zero to one transitions of the flag, no interrupt request will be generated for this flag until the flag is successfully cleared by software later on.

Workaround

After clearing the flag, the software shall read the flag and repeat clearing until the flag reads zero.

4.86 [FlexRay_TC.H002] Initialization of E-Ray RAMs

Description

After Power-on reset the ECC codes in the E-Ray RAMs may be set to an arbitrary state. Therefore the E-Ray RAM must be cleared and the ECC codes set to a defined state to avoid unintended traps.

To achieve this the following alternative methods are proposed:

Method 1 using the MTU/MBIST

- Clear all E-Ray RAMs and the related ECC code storage by executing writes to all RAM locations using the AURIX™ MBIST engine. The MBIST engine supports filling the E-Ray RAM with ECC-correct patterns. For this purpose the AURIX™ MBIST auto-initialization algorithm can be used. See section “Filling a Memory with Defined Contents” in the corresponding User’s Manual/Target Specification. The following E-Ray RAM blocks have to be initialized with correct data:
  - Output Buffer
  - Input Buffer
  - Message Buffers The MBIST function to be executed for each buffer is the same, only the function parameters have to be adapted
- Execute one read from each E-Ray RAM block using the AURIX™ MBIST engine (reading from all E-Ray RAM locations is an alternative but not necessary solution). For this purpose the AURIX™ MBIST engine can also be used
- Insert at the end of all MBIST function calls a status check, which makes sure that the launched MBIST tests are finished (check MSTATUS.DONE status flag)
- Clear all ECC error flags in the E-Ray module: these are flag EERR in register EIR, flags EIBF, EOBF, EMR, ETBF1, ETBF2 in register MHDS. The flags are cleared by writing a ‘1’ to the according bit position in the flag register

After these steps the E-Ray RAM can be used for further operation, for example for initialization of the E-Ray buffer.

***Note**:* *For **TC27x step BC**, due to issue MTU_TC.008 (Reading register MSTATUS while a test is running), the following delay times (including a 100 clock cycle “safety margin” for communication overhead between CPU and MBIST) must be respected before checking bit MSTATUS.DONE:*

- *Output Buffer fill operation: 164 clocks*
- *Input Buffer fill operation: 228 clocks*
- *Message Buffer fill operation: 2148 clocks*

Method 2 using “CLEAR RAMS” Command

Step 1 to 4: Enable the clock of the module:

1. Remove EINIT protection for the writing of the CLC register
2. Enable the clock in the CLC register
3. Read the CLC register
4. Enable the EINIT protection

Enable the test mode, check if the state of the module is according to the expected settings and start clearing the RAMs.

5. Take care of the unlock sequence. See description of LCK.TMK and TEST1.WRTEN in User’s Manual:
   - Test Mode Key: To set bit TEST1.WRTEN the write operation has to be directly preceded by two consecutive write accesses to the Test Mode Key
   - If the write sequence is interrupted by other write accesses between the second write to the Test Mode Key and the write access to the TEST1 register, bit TEST1.WRTEN is not set to 1 and the sequence has to be repeated.

     First write: LCK.TMK = 75_H = $0111\ 0101_B$

     Second write: LCK.TMK = $8A_H$ = $1000\ 1010_B$

     Second write: TEST1.WRTEN = 1_B
6. Check if CCSV.POCS is either 0x0 (DEFAULT_CONFIG) or 0xF (CONFIG). If not in any of these states, perform the according command to get to CONFIG state
7. Check if SUCC1.PBSY is equal 0x0. If 0x1 wait until 0x0
8. Set SUCC1.CMD to 0xC meaning that the CLEAR_RAMS command is entered

9. Read SUCC1.CMD. If 0x0 the command has not been accepted. Repeat up from step 7. Otherwise continue
10. Wait 1024 module cycles
11. Enable RAM Test mode: TEST1.TMC = 01_B. This mode enables access of all RAM blocks in E-Ray modules to the host
12. CUST1.IBF1PAG := 1_B
13. CUST1.IBF2PAG := 1_B
14. Repeat steps 7 to 10
15. Read at least one address in all the RAM blocks within E-Ray module
16. Switch off Test mode: TEST1.TMC = 00_B and TEST1.WRTEN = 0_B
17. Clear ECC error flags in MHDS and EIR registers
18. From here you can start the normal initialization process of the module

***Note**: In order to ensure proper FlexRay communication, RAM test mode must be explicitly disabled via TEST1.TMC = 00_B in step 16 at the end of the initialization sequence.*

4.87 [FlexRay_TC.H004] Bit WRECC in register TEST2 has no function

Description

In the AURIX™ implementation of the E-Ray module, bit WRECC in register TEST2 has no function.

Recommendation

The value read from WRECC should not be evaluated by software, the value written (0_B or 1_B) to it is irrelevant.
For new software projects, keep bit WRECC at its reset value (0_B) for easier migration to future AURIX™ generations.

4.88 [FlexRay_TC.H005] E-Ray OTGB2 trigger set active even if disabled

Description

The trigger set TS32_SCSC of the E-Ray IP-module is associated with OTGB2. An internal “valid” signal should be asserted only in case the trigger set is selected via OTSS.OTGB2.

Expected behavior

The OTGB2 trigger set valid signal should be gated by the bit-field OTSS.OTGB2.

Actual behavior

The E-Ray IP does not gate the valid signal with the OTSS.OTGB2 state, but only the data are gated. Meaning the OTGB2 trigger valid signal is only dependent on the slot counter and transfer buffer state changes, irrespective of the OTSS.OTGB2 value.

Recommendation

Ignore all OTGB2 E-Ray triggers when data reported is only 0s.

4.89 [FPI_TC.H002] Write access to register ACCEN1

Description

The ACCEN1 (Access Enable Register 1) registers in the AURIX™ devices are reserved for future expansion. The bits in the ACCEN1 registers are described as "Reserved", read-only. There is no need for software to configure (write to) the ACCEN1 registers.

***Note**: For a write access to the ACCEN1 registers in the following modules, a bus error will be generated:*

- ***TC2xx**: MTU, SMU, ETH, I2C, FFT, CIF*
- ***TC3xx**: MTU, SMU (documented in TC3xx user manual), CIF*

4.90 [GPT12_TC.H001] Timer T5 Run Bit T5R - Documentation Correction

Description

In the current version of the User's Manual, the lines for T5R=0_B and T5R=1_B in the register description of the Timer T5 Run Bit (T5R) erroneously have been swapped.

Correction

The correct behavior of bit T5R is as shown in Table 38: T5R=0_B (Timer T5 stops; default after reset), T5R=1_B (Timer T5 runs).

Table 38 Timer T5 Control Register T5CON, Bit T5R - Correction

Field	Bits	Type	Description
T5R	6	rw	**Timer T5 Run Bit** 0_B Timer T5 **stops** 1_B Timer T5 **runs** ***Note**: This bit only controls timer T5 if bit T5RC = 0.*

4.91 [GPT12_TC.H002] Bits TxUD and TxUDE in incremental interface mode - Additional information

Description

The present description of the incremental interface mode for timers T2, T3, T4 in the User's Manual, including figures and tables, implicitly refers to the following configuration of bits TxUD and TxUDE (x = 2, 3, 4):

- TxUD = 0_B
- TxUDE = 1_B

This is the recommended and validated setting for these bits in incremental interface mode.

Additional information

When bit TxUD = 1_B, the count direction of timer Tx is inverted compared to the setting with TxUD = 0_B in incremental interface mode.

The setting of bit TxUDE is irrelevant in incremental interface mode, the behavior of Tx for TxUDE = 0_B and TxUDE = 1_B is identical. The figures related to incremental interface mode shall be interpreted as if TxUDE is permanently tied to 1_B.

4.92 [GTM_AI.H473] SPEC-FIFO: Wrong description of FIFO flush operation

Description

***Note**: Register names in the text follow the TC3xx syntax conventions. Correlation of register names:*

- ***TC2xx:** FIFOi_CHx_*
- ***TC3xx:** FIFO[i]_CH[x]_*

FLUSH bit-field description of register FIFO[i]_CH[x]_CTRL (GTM4.1 spec.: FIFO_585):

The specification describes that the FIFO[i]_CH[x]_FILL_LEVEL.LEVEL, the FIFO[i]_CH[x]_RD_PTR.ADDR, and FIFO[i]_CH[x]_WR_PTR.ADDR will be reset to their initial values.

This is valid for FIFO[i]_CH[x]_FILL_LEVEL.LEVEL but not for FIFO[i]_CH[x]_RD_PTR.ADDR and FIFO[i]_CH[x]_WR_PTR.ADDR, which are set to the value of FIFO[i]_CH[x]_START_ADDR.ADDR on a FIFO flush operation.

Also it should be mentioned in the specification that the status bits EMPTY, FULL, LOW_WM and UP_WM of register FIFO[i]_CH[x]_STATUS are set to EMPTY=1, FULL=0, LOW_WM and UP_WM depending on the values programmed into FIFO[i]_CH[x]_LOWER_WM.ADDR and FIFO[i]_CH[x]_UPPER_WM.ADDR.

UP_WM bit-field description of register FIFO[i]_CH[x]_STATUS (GTM4.1 spec.: FIFO_628):

The condition for the UP_WM bit-field of the register FIFO[i]_CH[x]_STATUS is not correct in case the register for FIFO[i]_CH[x]_UPPER_WM.ADDR is programmed to 0 and afterward a FIFO flush is requested. In this case the bit UP_WM will signal 0 in RTL, but the evaluation due to the specification expects a 1.

To overcome this inconsistency between RTL and the specification, the value 0 for FIFO[i]_CH[x]_UPPER_WM.ADDR has to be excluded in the specification (see Note in the ADDR bit-field description of register FIFO[i]_CH[x]_UPPER_WM, GTM4.1 spec.: FIFO_609), as this value does not make sense from an application point of view.

Prose text in the Overview chapter of FIFO (GTM4.1 spec.: FIFO_836):

It is mentioned that the read and write pointer and also the fill level of the corresponding FIFO channel will be reset.

Here the word reset is used in context with the flush. Typically reset is combined with setting the initial values, but this is not true here. Instead of "reset" another term should be used, for example: "set to previously configured values".

Following note is missing in the specification:

A FIFO flush operation does not influence the state of the FIFO[i]_CH[x]_IRQ_NOTIFY register.

Scope

FIFO

Effects

1. The values of FIFO[i]_CH[x]_RD_PTR.ADDR and FIFO[i]_CH[x]_WR_PTR.ADDR are not set to the initial value as described in the specification
2. False value of FIFO[i]_CH[x]_STATUS.UP_WM after a flush request in case FIFO[i]_CH[x]_UPPER_WM.ADDR is programmed to 0

Recommendation

Please apply either 1 or 2:

1. Configure FIFO[i]_CH[x]_START_ADDR.ADDR to its initial value before executing the flush operation
2. Do not configure value 0 for FIFO[i]_CH[x]_UPPER_WM.ADDR

4.93 [GTM_AI.H481] SPEC-TIM: Wrong description for TBCM mode

Description

***Note**: Register names in the text follow the TC3xx syntax conventions. Correlation of register names:*

- ***TC3xx**: TIM[i]_CH[x]_CTRL*
- ***TC2xx**: TIMi_CHx_CTRL*

In TIM Bit Compression Mode with External Capture (TIM[i]_CH[x]_CTRL.EXT_CAP_EN=1), the capture is done only with the external capture signal without dependency to the input signal level. Therefore the bit-field TIM[i]_CH[x]_CTRL.ISL must be set to 1. The value 0 for TIM[i]_CH[x]_CTRL.ISL is prohibited. The bit-field TIM[i]_CH[x]_CTRL.DSL is not relevant.

The following parts in section "External capture Bit Compression Mode (TBCM)" in the TBCM chapter have to be adapted as follows:

- In the prose text

  "If external capture is enabled, capturing is done for TIM[i]_CH[x]_CTRL.ISL=1 as defined in the next table. The value 0 for TIM[i]_CH[x]_CTRL.ISL is prohibited."
- In the table
  - In the action description of row 1 the part "TIM[i]_CH[x]_CNT++" has to be removed
  - All rows starting with row 3 have to be replaced with only one row where the content for the column of TIM[i]_CH[x]_CTRL.ISL has to be filled with "0 - prohibited". All other columns in row 3 have to be marked with "-" (don't care)

Table 39 Resulting table for TC3xx and TC2xx

- TC3xx - Capturing depended on the DSL, ISL and the input signal value, if external capture is enabled
- TC2xx - TIM Input Event Mode

Input signal F_OUTx	External capture	ISL	DSL	Action description
-	Rising edge	1	-	do capture; issue NEWVAL_IRQ
-	0	1	-	No
-	-	0 - prohibited	-	-

Scope

TIM

Effects

The input signal level defined by TIM[i]_CH[x]_CTRL.DSL with TIM[i]_CH[x]_CTRL.ISL = 0 is not taken into account.

Recommendation

Consider the information given above. Do not configure TIM[i]_CH[x]_CTRL.ISL to 0.

4.94 [GTM_AI.H497] SPEC-SPE wiring in figure is wrong

Description

In the GTM chapter of the corresponding user manual, the usage of the SIE inputs SIE0 and SIE2 must be swapped in the following figure:

- TC3xx: figure "SPE[i]_IN_PAT register representation"

In the GTM chapter of the corresponding user manual, the usage of the SIE inputs is missing in the following figure:

- TC2xx: figure "SPE[i]_IN_PAT register representation"

Scope

SPE

Effects

The enabling of the affected TIM input signals of the SPE is not working as expected when considering the figure as basis.

Recommendation

For the correct functionality, see the description of bits SIE0..2 in the following register:

- TC3xx, TC2xx: SPEi_CTRL_STAT

4.95 [GTM_AI.H502] SPEC-DPLL input selection for SUB_INC1 is incomplete

Description

The bit field DPLL_CTRL_0_SHADOW_TRIGGER.RMO is updated on active TRIGGER input, whereas DPLL_CTRL_0_SHADOW_STATE.RMO is updated on active STATE input. The active TRIGGER input and active STATE input might arrive at different times. Therefore, on a switch from normal mode to emergency mode (or the other way around), the two bit fields might be updated at different points in time leading to them having different values.

The SPEC deficiency:

The coding for DPLL_CTRL_0_SHADOW_TRIGGER.RMO (GTM4.1 spec.: DPLL_16133) and for bit field DPLL_CTRL_0_SHADOW_STATE.RMO (GTM4.1 spec.: DPLL_16132) does not take into account that the two bit fields may have different values. As a consequence it is ambiguous which input contributes to the calculation of INC_CNT1.

In order to fix the specification:

Add a note to bit field DPLL_CTRL_0_SHADOW_TRIGGER.RMO and also to bit field DPLL_CTRL_0_SHADOW_STATE.RMO:

"The coding is applicable if DPLL_CTRL_0_SHADOW_TRIGGER.RMO = DPLL_CTRL_0_SHADOW_STATE.RMO.

If not (they are unequal) the DPLL_CTRL_0.RMO defines which input is evaluated: STATE is selected if DPLL_CTRL_0.RMO=1 else TRIGGER is selected".

Scope

DPLL

Effects

DPLL behaves in an unspecified manner if DPLL_CTRL_0_SHADOW_TRIGGER.RMO ≠ DPLL_CTRL_0_SHADOW_STATE.RMO.

Recommendation

None.

4.96 [GTM_AI.H519] SPEC-(A)TOM: Misleading description of Continuous Counting Up Mode

Description

In the third list item of the paragraph, where some statements are given for Continuous Counting Up Mode with RST_CCU0=1, the following statement for the case (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1 is given:

"If (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1, the output switches to (A)TOM[i]_CH[x]_CTRL_SOMP.SL if (A)TOM[i]_CH[x]_CN0.CN0=(A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1 ((A)TOM[i]_CH[x]_CM0.CM0 has higher priority."

or in the older specification versions (before GTM3 generations):

"If (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1, the output is 100% (A)TOM[i]_CH[x]_CTRL.SL ((A)TOM[i]_CH[x]_CM0.CM0 has higher priority."

Both statements are misleading and have to be replaced by the following statement:

"As soon as (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0 while (A)TOM[i]_CH[x]_CM1.CM1 is equal to (A)TOM[i]_CH[x]_CM0.CM0, an edge to (A)TOM[i]_CH[x]_CTRL.SL is generated at the output or the output remains at (A)TOM[i]_CH[x]_CTRL.SL level, depending on the former level of the output ((A)TOM[i]_CH[x]_CM0.CM0 has higher priority)."

***Note**: The above configuration is not suitable for generating 100% duty cycle.*

Scope

ATOM, TOM

Effects

Textual description can be erroneously interpreted as the configuration of (A)TOM[i]_CH[x]_CM0.CM0=(A)TOM[i]_CH[x]_CM1.CM1 is suitable to generate 100% duty cycle for the current PWM period.

This is because the potential value change to SL will happen as soon as (A)TOM[i]_CH[x]_CN0.CN0 reaches the value of (A)TOM[i]_CH[x]_CM0.CM0 while (A)TOM[i]_CH[x]_CM1.CM1 is equal to (A)TOM[i]_CH[x]_CM0.CM0.

Recommendation

For a setup of 100% duty cycle for Continuous Counting Up Mode with RST_CCU0=1, the following setting must be used:

- ATOM[i]_CH[x]_CM0.CM0 = 0 and ATOM[i]_CH[x]_CM1.CM1 > MAX

4.97 [GTM_AI.H803] SPEC-(A)TOM: Missing priority information for register update

Description

The following information is missing in the specification and has to be placed inside the TGC Sub-unit/AGC Sub-unit chapter:

- Inside ATOM chapter: The trigger condition has always priority over the bus write access to the ATOM[i]_AGC_OUTEN_STAT and ATOM[i]_AGC_ENDIS_STAT registers, even if ATOM[i]_AGC_OUTEN_CTRL.OUTEN_CTRL[k] / ATOM[i]_AGC_ENDIS_CTRL.ENDIS_CTRL[k] is set to 00_B. This means that the bus write access to ATOM[i]_AGC_OUTEN_STAT and ATOM[i]_AGC_ENDIS_STAT register is ignored in the clock cycle when the trigger condition is active
- Inside TOM chapter: The trigger condition has always priority over the bus write access to the TOM[i]_TGC[g]_OUTEN_STAT and TOM[i]_TGC[g]_ENDIS_STAT registers, even if TOM[i]_TGC[g]_OUTEN_CTRL.OUTEN_CTRL[k] / TOM[i]_TGC[g]_ENDIS_CTRL.ENDIS_CTRL[k] is set to 00_B. This means that the bus write access to TOM[i]_TGC[g]_OUTEN_STAT and TOM[i]_TGC[g]_ENDIS_STAT register is ignored in the clock cycle when the trigger condition is active

***Note**: The trigger override does not happen if the trigger is a HOST_TRIG, as this is initiated by a bus write itself and cannot happen at the same time as another bus write to the register.*

***Note**: This AppHint is published as GTM-IP-523 by Bosch.*

Scope

ATOM, TOM

Effects

In (A)TOM the bus write access to the "OUTEN_STAT" and "ENDIS_STAT" registers is overridden by a trigger update and the desired values are not written into the register.

Recommendation

To nevertheless ensure that the desired value is actually stored in the target register, consider one of the following hints:

1. Write first the channel k within "ENDIS_CTRL" ("OUTEN_CTRL") and write the desired channel k in "ENDIS_STAT" ("OUTEN_STAT") afterward. This way, either the asynchronous write or the synchronous write becomes effective
2. If recommendation 1 is not the case, then read back the value of the "OUTEN_STAT" and "ENDIS_STAT" register to ensure the written value is actually present in the register

4.98 [GTM_TC.H003] Typo: GTM Chapters “Multi Channel Sequencer (MCS)” and “Memory Configuration (MCFG)” sometimes use “MSC” instead of “MCS”

Description

Due to an editorial issue, in chapters “Multi Channel Sequencer (MCS)” and “Memory Configuration (MCFG)” sometimes the term “MSC” is erroneously used instead of “MCS” within the text and in figure/section titles.

***Note**: The register names defined in these chapters are correct, such that register definition files extracted from these chapters will include the correct register names.*

4.99 [GTM_TC.H004] Correction to Bit Fields GTM_TIMi_IN_SRC.VAL_x

Description

In the description of bit-field VAL_0, the encoding 01_B was erroneously repeated while 10_B and 11_B were missing.

The affected registers are

- GTM_TIMi_IN_SRC in the TC29x, TC27x, and TC26x User's Manual
- GTM_TIM0_IN_SRC in the TC21x/TC22x/TC23x Family User's Manual

The correct description is included in the following tables. As the description of bit fields VAL_x, x>0 refers to VAL_0, this description is valid for all VAL_x bit fields in registers GTM_TIMi_IN_SRC and GTM_TIM0_IN_SRC, respectively.

Correction for TC29x, TC27x, and TC26x

Table 40 TC29x .. TC26x: Corrected Description of Bit Field VAL_0 in Registers GTM_TIMi_IN_SRC

Field	Bits	Type	Description
VAL_0	[1:0]	rw	**Value to be fed to Channel 0** multicore encoding in use (VAL_x(1) defines the state of the signal) 00_B State is 0 (ignore write access) 01_B Change state to 0 10_B Change state to 1 11_B State is1 (ignore write access) ...

Correction for TC21x/TC22x/TC23x

Table 41 TC23x .. TC21x: Corrected Description of Bit Field VAL_0 in Register GTM_TIM0_IN_SRC

Field	Bits	Type	Description
VAL_0	[1:0]	rw	**Value to be fed to Channel 0** 00_B Input signal 0 (ignore write access) 01_B Input signal is set to 0 10_B Input signal is set to 1 11_B Input signal 1 (ignore write access) ...

4.100 [GTM_TC.H005] External Capture in TIM Pulse Integration Mode (TPIM)

Description

In table "TIM integration Mode" in section "External Capture in TIM Pulse Integration Mode (TPIM)" of the GTM chapter in the User's Manual, the information that CNT is cleared upon external capture is missing in column "Action description".

The corrected Table 42 is shown below:

Table 42 TIM integration Mode

Input signal F_OUTx	selected CMU clock	External capture	ISL	DSL	Action description
0	1	0	-	0	CNT++

(table continues...)

Table 42 (continued) TIM integration Mode

Input signal F_OUTx	selected CMU clock	External capture	ISL	DSL	Action description
1	1	0	-	0	no
1	1	0	-	1	CNT++
0	1	0	-	1	no
-	-	rising edge	-	-	do GPRx capture; issue NEWVAL_IRQ; **CNT = 0**
-	0	0	-	-	no

4.101 [GTM_TC.H007] GTM to CAN Timer Triggers

Description

The CAN transmit trigger inputs of the individual CAN nodes are connected to GTM trigger outputs as specified in table “CAN Transmit Trigger Inputs” in the MultiCAN+ chapter of the User’s Manual.

The corresponding GTM TOM/ATOM channel is selected in register GTM_CANOUTSEL as specified in tables “CAN Timer Triggers” in the GTM chapter. Note that not all specified SELx bit-fields in register CANOUTSEL are used for trigger selection.

The following GTM to CAN connections are implemented:

Table 43 GTM to CAN Connections in TC29x

CAN Node	GTM Trigger Selection via Bit Field
CAN Node 0	CANOUTSEL.SEL0
CAN Node 1	CANOUTSEL.SEL1
CAN Node 2	CANOUTSEL.SEL2
CAN Node 3	CANOUTSEL.SEL3
CANR Node 0	No GTM trigger
CANR Node 1	No GTM trigger

Table 44 GTM to CAN Connections in TC27x

CAN Node	GTM Trigger Selection via Bit Field
CAN Node 0	CANOUTSEL.SEL0
CAN Node 1	CANOUTSEL.SEL1
CAN Node 2	CANOUTSEL.SEL2
CAN Node 3	CANOUTSEL.SEL3

Table 45 GTM to CAN Connections in TC26x

CAN Node	GTM Trigger Selection via Bit Field
CAN Node 0	CANOUTSEL.SEL0
CAN Node 1	CANOUTSEL.SEL1
CAN Node 2	CANOUTSEL.SEL2
CAN Node 3	CANOUTSEL.SEL3
CAN Node 4	CANOUTSEL.SEL4

Table 46 GTM to CAN Connections in TC23x

CAN Node	GTM Trigger Selection via Bit Field
CAN Node 0	CANOUTSEL.SEL0
CAN Node 1	CANOUTSEL.SEL1
CAN Node 2	CANOUTSEL.SEL2
CAN1 Node 0	CANOUTSEL.SEL0
CAN1 Node 1	CANOUTSEL.SEL1
CAN1 Node 2	CANOUTSEL.SEL2

Table 47 GTM to CAN Connections in TC22x/TC21x

CAN Node	GTM Trigger Selection via Bit Field
CAN Node 0	CANOUTSEL.SEL0
CAN Node 1	CANOUTSEL.SEL1
CAN Node 2	CANOUTSEL.SEL2

4.102 [GTM_TC.H008] Correction to Figure “SPE to TOM Connections”

Description

In figure “SPE to TOM Connections” in the GTM chapter of the User’s Manual, the signal originating from block TOM_CH2 is incorrectly shown as TOM[i]_CH2_TRIG_CCU0.

The correct signal originating from block TOM_CH2, as shown in figure “SPE Submodule architecture” and documented in the description of register GTM_SPEi_CTRL_STAT for TRIG_SEL = 11_B, is TOM[i]_CH2_TRIG_**CCU1**.

4.103 [GTM_TC.H011] First CM0 updates in case of SR0=1 and (A)TOM used as Triggered Channel

Description

In case the CM0 register should be updated from the shadow register with 1, the Force Update mechanism (FUPD(x) signal) has to be enabled on the (A)TOM channel. Otherwise the first edge triggered from CM0 will not be generated after 1 appears in CM0.

4.104 [GTM_TC.H014] Synchronous Bridge Mode Restrictions

Description

The reset value for register GTM_BRIDGE_MODE is specified as 0400 1001_H, and should never be changed according to the User’s Manual, i.e. the AEI bridge should always operate in async_bridge mode.

Exception

In order to improve access latency, operation in synchronous bridge mode is possible if it is ensured that the SPB frequency is identical to the GTM frequency:

- $f_{SPB} == f_{GTM}$

Sequence to configure the bridge in synchronous mode (pseudocode):

```
/* ensure that no data are read or written in the GTM */
if(fSPB == fGTM)
{
GTM_BRIDGE_MODE = 0x04011000; /* switch to sync mode, reset bridge*/
while(GTM_BRIDGE_MODE & 0x100) /* wait till mode change completed */
;
}
else
;
```

4.105 [GTM_TC.H015] Register TIMi_CHx_CTRL - Correction to Register Image

Description

The register image of the following registers erroneously shows bit 19 as “Reserved” with type “r” (read only):

- TIMi_ CHx_CTRL in the TC29x, TC27x and TC26x User’s Manual
- TIM0_ CHx_CTRL in the TC21x/TC22x/TC23x Family User’s Manual

Correction

Actually, bit 19 has type “rw” and is correctly described in the register table as copied from the User’s Manual in the table below:

Table 48 Bit EXT_CAP_EN in Register TIMi_CHx_CTRL and TIM0_CHx_CTRL, respectively

Field	Bits	Type	Description
EXT_CAP_EN	19	**rw**	**Enables external capture mode** The selected TIM mode is only sensitive to external capture pulses, the input event changes are ignored 0_B External capture disabled 1_B External capture enabled

4.106 [GTM_TC.H016] Evaluating DSADC Signals SAULx/SBLLx

Description

The DSADC provides the following signals to indicate whether the results of the parallel filter are outside the limits defined in the BOUNDSELx registers:

- Signal SAULx is active while the results are above the upper limit
- Signal SBLLx is active while the results are below the lower limit

In the GTM, these signals can be selected as TIM inputs in the DSADCINSEL register(s).

The rising edge of these signals is transformed to a pulse inside the GTM, so that it is not possible to directly measure the high/low phase of SAULx/SBLLx via TIM, but the duration between two rising edges.

4.107 [GTM_TC.H017] Bit DXINCON.24 (DSS10) - Documentation Correction

Description

In the register image of register DXINCON in the User's Manual, bit 24 is erroneously named DSS00 instead of DSS10.

Correction

The correct symbolic name for bit DXINCON.24 is DSS10, as listed in the table below the register image in the User's Manual:

Table 49 Register DXINCON - Data Source Select 1x Control

Field	Bits	Type	Description
DSS1x (x = 0..n[1)])	x+24	rw	Data Source Select 1x Control

1) n=5 for TC29x, n=3 for TC27x, n=2 for TC26x

***Note**: The SFR C Header Definitions are not affected, as they are generated from the table (not from the register image).*

4.108 [GTM_TC.H020] GTM can cause unintended bus errors after enabling when SPB or GTM frequency is very low

Description

When the SPB frequency is low compared to the CPU frequency, or the GTM frequency is low compared to the SPB frequency, the GTM can cause an FPI bus error when it is accessed too early after being enabled.

Recommendation

To avoid an FPI bus error, after enabling the GTM via the DISR bit in register CLC, a time delay of 10 SPB clock cycles and 10 GTM clock cycles must be inserted before accessing any GTM kernel register.

4.109 [HSCT_TC.H003] Functionality of bit TX_PWDPD

Description

Bit TX_PWDPD in register P21_LPCR2 directly disables or enables the LVDS pull down.

The application software must disable the TX power down pull down after power-up. With a LVDS power down configuration, the pull down function must be enabled, if required.

4.110 [HSCT_TC.H005] Access to reserved address 0xF009 0060 when $f_{SPB} = f_{SRI}$

Description

Unlike an access to other reserved addresses within the HSCT, an access a_x to address 0xF009 0060 will not result in a bus error when $f_{SPB} = f_{SRI}$.

If another HSCT access a_y follows back-to-back to a_x, a bus error will be generated for a_y, even if the access is to a valid address.

***Note**: With the default reset value of register CCUCON0 = 0202 0112$_H$, i.e. f_{SRI} = 2 * f_{SPB}, these effects will not occur.*

4.111 [HSCT_TC.H007] HSSL Integrated Phase Noise

Description

The diagram below shows the phase noise characteristics at the SysClk output of the HSCT PHY in the master device.

- The Integrated Phase Noise I_{PN} limit is violated. Target value is:
  - I_{PN} = -58 dBc, corresponding to J_{ABS20} = 14 ps[6)]
- The achieved value with max power pattern running on the master microcontroller is:
  - I_{PN} = -43 dBc, corresponding to J_{ABS20} = 80 ps[6)]
- The achieved value with no application running on the master microcontroller is:
  - I_{PN} = -49 dBc, corresponding to J_{ABS20} = 40 ps[6)]

Nevertheless, such a target value on the random jitter of the SysClk signal is only an intermediate specification. The real target to be respected in order to assure BER_{20} of 10^{-12} is the total jitter of the link. The total jitter target is met. Consistently, measurements on the HSSL/HSCT communication channel using the SysClk signal with I_{PN} from above show that the ultimate target of BER_{20} = 10^{-12} is met. In such a measurement setup, both the master and the slave are microcontrollers of the AURIX™ family.

The diagram below shows the phase noise density on the SysClk pin when no application pattern but only the HSSL/HSCT subsystem is running:

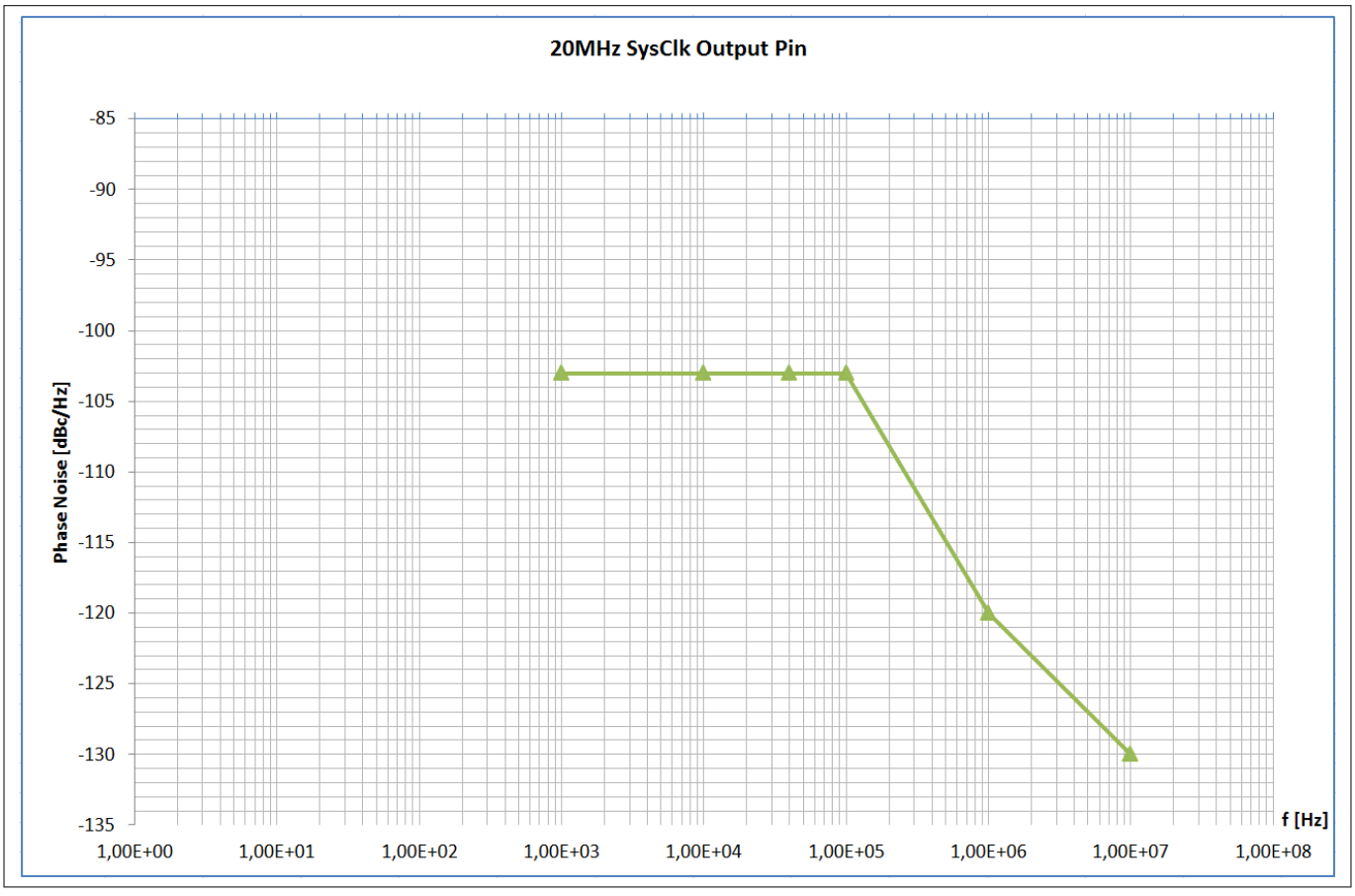

Figure 9 Phase Noise Density on SysClk Output Pin

6 integration range from 10 kHz to 10 MHz

Recommendation

When designing the PLL for an HSSL/HSCT ASIC, the values for I_{PN} and J_{ABS20} above and ultimately BER_{20} = 10^{-12} can be achieved with the following recommendations:

- DCO frequency = 640 MHz
- DCO free running phase noise @1 MHz ≤ -98 dBc
- PLL bandwidth = 1 MHz[7)]

Comprehensive information on this topic is provided in Application Note AP32292 “HSCT Jitter Considerations”.

4.112 [HSCT_TC.H008] Details on PLL Lock-in Time

Description

The HSCT parameter “PLL lock-in time” t_{LOCK} ≤ 50 µs defined in the Data Sheet refers to the pure HSCT PLL lock time not including the internal voltage regulator (IVR) start-up time t_{IVR}.

In case of Master Mode the PLL reference clock is SysClk = 20 MHz. The total PLL lock time including the IVR start-up time is ≤ 70 µs.

In case of a HSCT slave receiving SysClk = 20 MHz, the total PLL lock time including the IVR start-up time is ≤ 70 µs.

In case of a HSCT slave receiving SysClk = 10 MHz, the PLL lock time is longer and the total time including the IVR start-up time is ≤ 100 µs (see Table 50).

Table 50 Total PLL Lock-in Time for SysClk = 20 MHz and SysClk = 10 MHz

	Total PLL Lock-in Time (max.)	
SysClk	**Master**	**Slave**
20 MHz	70 µs	70 µs
10 MHz	not applicable	100 µs

4.113 [HSCT_TC.H010] Interface control command timing on the LVDS ports

Description

As described in section “Interface Control” of the HSCT chapter in the user manual, a HSCT master device is sending interface control commands to a slave device by setting the command in register IFCTRL.IFCVS and triggering IFCTRL.SIFCV.

Once triggered, the interface command is scheduled for take over into the transmission FIFO for sending. Only when the interface command has been taken over into the FIFO, sending of the next interface command must be triggered by software. Therefore, software must monitor the takeover by a transition of IRQ.IFCFS from 0 to 1.

As flag IRQ.IFCFS only indicates

- takeover of the interface command into the FIFO
- readiness for the next interface command to be triggered

the user might falsely assume that also the actual sending on the LVDS TX port has already occurred once the IRQ.IFCFS flag is set, which is not true.

Instead the timing shown in the following figure applies.

7 the bandwidth can go as low as 200 kHz, at which point the DCO noise exceeds the reference noise

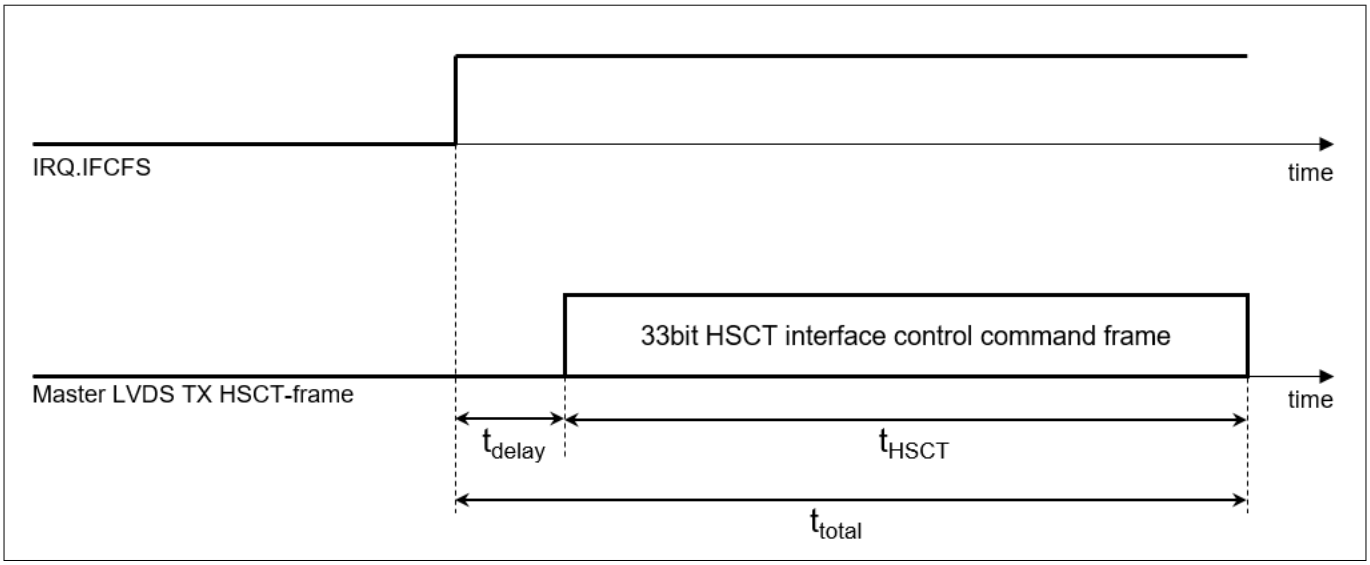

Figure 10 Timing of LVDS TX interface command sending in relation to IRQ.IFCFS

Recommendation

Before changing interface configurations, software must guarantee not having transfers active on the interface. Therefore the time of t_{total} has to be taken into account:

- $t_{total} = t_{delay} + t_{HSCT}$

While t_{HSCT} of the HSCT control command frame is determined and can be calculated from the actual baud rate, the additional time t_{delay} has to be taken into account with:

- $t_{delay} \geq 10\ \mu s$

This value is valid for $f_{SRI} \geq 100$ MHz, $f_{SPB} \geq 100$ MHz and baud rate ≥ 5 MBaud.

4.114 [I2C_TC.H001] I2C Module Behavior in OCDS Suspend Mode

Description

The register bit CLC1.FSOE selects between Secure Clock Shut Off (FSOE=0_B) and Fast Clock Shut Off (FSOE=1_B) when entering the OCDS Suspend Mode.

In the current implementation, the behavior of the module upon an OCDS suspend request is as follows:

- In **master** mode, where the master generates the clock, the I2C module always stops immediately, independent of the setting of bit FSOE. The bus lines (SDA and SCL) are stalled, and it is likely that I2C protocol (for example SCL_LOW / SCL_HIGH) is not fulfilled in this case
- In **slave** mode with **FSOE=0_B**, the I2C module stops after an acknowledge has been sent on the bus, and then drives SCL low to delay operation
- In **slave** mode with **FSOE=1_B**, the I2C module immediately stops in any state, without generating/waiting for an acknowledge

Recommendation

It is recommended to reset the system after the clock shut off and restart the I2C sequence again for further debugging and analysis.

4.115 [I2C_TC.H002] Initialization of INC/DEC values in Slave mode

Description

Baudrate generation is mainly used for master mode, but there is one corner case where a support of the baudrate generation is required in slave mode: when I2C is in slave mode with a pending transmit data request and FIFO is currently empty, then SCL is kept low until FIFO is filled after some time. Then transmit data is sent out immediately. SCL is kept low for a min. time of $t_{SU;DAT}$.

Recommendation

It is recommended to program INC/DEC in slave mode also with values to ensure a suitable setup time for transmit data according $t_{SU;DAT}$ of I2C standard.

The parameter $t_{SU;DAT}$ is represented in the Infineon TC2xx Data Sheets as t_4.

In order to keep the set-up time, t_4, according to I2C standard, the baudrate generation is used to guarantee the delay on SCL. The formulas in the 3rd and the 4th column of Figure 11 show how to configure DEC and INC for a given f_{I2C} and the intended set-up time. The formulas in column Resulting t_4 [µs] define the real value of t_4 with the selected DEC and INC values.

The same value for DEC and INC as in master mode is not recommended and would lead to additional delay, as requested by the standard, in most cases.

MODE	min t_4[µs]	DEC / INC	Resulting t_4 [µs] 1)2)
Standard	0.25	(28.12) $DEC = \frac{8}{9}((fI2C) \times (t_4) \times INC + INC)$	(28.13) $C = INT\left(\frac{DEC + DEC(div)8}{INC} - 1\right)$ (28.14) $\frac{C}{fI2C} = t_4$
Fast	0.1	(28.15) $DEC = \frac{4}{5}((fI2C) \times (t_4) \times INC + INC)$	3) (28.16) $C = INT\left(\frac{DEC + DEC(div)4}{INC} - 1\right)$ (28.17) $\frac{C}{fI2C} = t_4$
High speed	0.01	(28.18) $DEC = INC + 1$	(28.19) $C = INT\left(\frac{DEC}{INC} + 1\right)$ (28.20) $\frac{C}{fI2C} = t_4$

1) *The used abbreviation INT is the integer function.*
2) *The operator div denotes the integer division: a div b = greatest integer not greater than a/b.*
3) *SCL_LOW_LEN can not be greater than DEC.*

Figure 11 I2C Baudrate Generation Configuration for Slave Mode

In the following table some example settings are given to program INC / DEC. The used abbreviation INT is the integer function.

Table 51 INC/DEC Settings for Slave Mode

kernel_clk	Standard Mode			Fast Mode			High-Speed Mode		
[MHz]	INC	DEC	t_4	INC	DEC	t_4	INC	DEC	t_4
10	75	250	275 ns	100	240	200 ns	250	251	200 ns
50	20	249	260 ns	44	247	120 ns	250	251	40 ns
100	10	240	260 ns	55	528	110 ns	250	251	20 ns

4.116 [I2C_TC.H003] DMA Channel Configuration

Description

The I2C module expects an acknowledge from the DMA after a data transfer to FIFO/from FIFO. But the DMA implemented in AURIX™ does not provide the acknowledge. If the CPU would have to provide it, this would make the use of a DMA pointless.

Recommendation

A linked list should be used to avoid that the CPU has to get active to provide the acknowledge. The DMA channel that serves I2C has to be configured with a linked list that first clears the interrupt by writing 0x0 to register ICR (Interrupt Clear Register) and second makes the FIFO-TX/RX transfer.

4.117 [I2C_TC.H004] Transfers of more than 32 Bytes

Description

When the I2C module FIFO isn't serviced in time (send: filled with transmit data, receive: read the received data), an underflow/overflow event will lead to (TX_END) abortion of the transmission, like specified in the User's Manual.

Recommendation

To avoid this behaviour the software shall be configured to transfer a maximum of 32 bytes per transfer.

If more than 32 bytes should be transmitted, the transmissions should be divided in maximum 32 data bytes per transfer.

4.118 [I2C_TC.H005] FIFO Data is lost during Transaction RX->TX

Description

When the I2C module is changing the state from receive to transmit mode, the FIFO is "flushed". This is needed in many cases due to the half duplex nature of the FIFO.

If the software does not proceed in the right sequence, this "flush" can lead to data loss.

Recommendation

To avoid loosing data when the FIFO is "flushed" the software should proceed as follows:

In a scenario where the device is addressed as slave and is asked to return data, this new data must be entered in the FIFO only after detection of the address and "end" indication, so the software shall wait for AM (Address Match) and TX_END (Transmission End) interrupt requests and then can transfer the data to the FIFO or can trigger the DMA that fills the FIFO for the TX transfer.

4.119 [I2C_TC.H008] Handling of RX FIFO Overflow in Slave Mode

Description

If the I2C kernel has detected a RX FIFO overflow in slave mode, a RX_OFL_srq request in generated, the incoming character is discarded, and the kernel puts a not-acknowledge on the bus and changes to listening state.

However, it does not generate an EORXP_ind signal, so that the remaining characters in the FIFO can not be moved out by means of data transfer requests.

Recommendation

Upon an RX FIFO overflow in slave mode, received data may be invalid. However, they may be read from the FIFO for example for analysis if required.

In order to flush the FIFO and correctly resume communication

- set bit RUNCTRL.RUN = 0_B (switch to configuration mode)
- set bit RUNCTRL.RUN = 1_B (participate in I2C communication)

4.120 [IOM_TC.H001] How to clear the IOM_LAMEWCm register

Description

The Logic Analyzer Module Event Window Count Status register IOM_LAMEWCm stores the window count value reached prior to being cleared in the LAM block once an event has been generated.

Writing to IOM_LAMEWCm by software will result in a bus error.

The IOM_LAMEWCm register can be reset (cleared) by software with a write to the IOM_LAMCFGm or IOM_LAMEWSm registers, for example by writing the same configuration data that have been read to either of these registers.

***Note**: The clock divider should be set to IOM_CLC.RMC = 1 when configuring the IOM (see issue IOM_TC.004 "Write to IOM register space when IOM_CLC.RMC > 1").*

4.121 [IOM_TC.H002] IOM Clock Control

Description

Contrary to the named clocks given within the subsections of the IOM chapter, the entire IOM operates at the higher of the SPB or GTM clock frequencies. This may be further divided via the RMC bit-field of the IOM_CLC register, where the physical RMC value represents the divisor. For example, RMC = 00000001_B divides clock by 1, RMC = 00000010_B divides clock by 2, and so on. Note that RMC = 00000000_B disables the clock.

See also the following revised description of the IOM_CLC register.

IOM Clock Control Register (IOM_CLC)

The Clock Control Register CLC allows the programmer to adapt the functionality and power consumption of the module to the requirements of the application. The description below shows the clock control register functionality which is implemented in the BPI_FPI for the module. Where a module kernel is connected to the CLC clock control interface, CLC controls the f_{IOM} module clock signal, sleep mode and disable mode for the module.

Table 52 Description of Fields in IOM Clock Control Register (IOM_CLC)

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module. 0_B Module disable is not requested 1_B Module disable is requested
DISS	1	rh	**Module Disable Status Bit** Bit indicates the current status of the module. 0_B Module is enabled 1_B Module is disabled
0	2	rw	**Reserved** Read as 0; should be written with 0.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode. 0_B Sleep mode request is regarded. Module is enabled to go into Sleep Mode. 1_B Sleep mode request is disregarded. Sleep Mode cannot be entered upon a request.
RMC	[15:8]	rw	**Clock Divider Value in Run Mode** 00000000_B No clock signal f_{IOM} generated (default after reset) 00000001_B Clock f_{IOM} = max (f_{SPB}, f_{GTM}) selected 00000010_B Clock f_{IOM} = max (f_{SPB}, f_{GTM})/2 selected 00000011_B Clock f_{IOM} = max (f_{SPB}, f_{GTM})/3 selected ... 11111111_B Clock f_{IOM} = max (f_{SPB}, f_{GTM})/255 selected
0	[31:16], [7:4]	r	**Reserved** Read as 0; should be written with 0.

4.122 [IOM_TC.H003] Configuration of LAMCFG.IVW and LAMEWS.THR

Description

As shown in figure "Logic Analyzer Module (LAM) block diagram" in the IOM chapter of the User's Manual, an EVENT will be generated if the required edge is detected and the XOR between the Event Window value and the invert bit (LAMCFG.IVW) is 1.

When the edge to be detected arrives at LAMEWSn.THR value of the counter, the EVENT will be generated depending on LAMCFG.IVW value:

- If LAMCFG.IVW==0 event will be generated
- if LAMCFG.IVW==1 event will not be generated

Taking this behavior into account, the description of the LAMCFG.IVW and/or LAMEWS.THR configuration in examples 2, 4, 5 and 6 of section "Example Monitor/Safety Measures" is misleading.

Correction

The corrected description, including the case "equal to", is as follows (only modified lines are printed):

Example 2 - Pulse or duty cycle too long

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

LAMEWS.THR: select appropriate threshold (maximum duty cycle length required. If duty cycle is longer than this value then an event will be triggered).

Example 4 - Period too long

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

LAMEWS.THR: select appropriate threshold (maximum period length required. If period is longer than this value then an event will be triggered).

Example 5 - Diagnosis of Command and Feedback - acceptable propagation window and/or signal consistency check

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

LAMCFG.THR: set to max delay allowed (if the delay between corresponding edges of reference and monitor signals is longer than this value, the event will be triggered).

Example 6 - Diagnosis of Set-up and Hold times

- Example settings for LAM block registers for Set-up

LAMCFG.IVW: 0x0 ; don't invert window, capture events when the counter is **equal or** above the threshold.

- Example settings for LAM block registers for Hold

LAMCFG.IVR: **0x1** ; invert reference signal (use for gating).

LAMCFG.THR: Acceptable Hold (ref Threshold 2 on waveforms shown, changes in monitor signal will generate an alarm if they occur inside the "THR" cycles after a falling edge in the reference signal).

4.123 [IOM_TC.H004] Behavior of LAMEWCn.CNT when LAMEWSn.THR is 0

Description

When LAMEWSn.THR is set to 0, no event will be sent from the Logic Analyzer Module (LAM) to the Event Combiner Module (ECM) and no ALARM towards the SMU will be generated.

The rest of the effects derived from the cause generating the event inside the LAM will be maintained, for instance copying the counter to LAMEWCn.CNT (this means LAMEWCn.CNT also may change when LAMEWSn.THR is 0).

4.124 [IOM_TC.H006] ACCEN* Protection for Write Access to IOM Registers

Description

The access protection symbol 'P' to indicate protection by the ACCEN* register mechanism is missing in column "Access Mode - Write" in table "Register Overview" in the User's Manual for IOM registers with an offset address $\geq 30_H$. Actually, these registers have write access attributes 'U,SV,P'.

Exception

In this design step, a write access to register LAMEWCm will result in a bus error, as correctly reflected by symbol 'BE' in column "Access Mode - Write" in table "Register Overview" in the User's Manual.

4.125 [IOM_TC.H007] Write Access to FPCESR

Description

The Filter and Prescaler Edge Status Register FPCESR stores the state of detected rising and falling edges from each of the Filter and Prescaler Channels k (k = 0..15).

The flags in this register can be selectively cleared by writing a 0 in the respective bit-field.

However, writing to register FPCESR with a sub-word granularity (for example byte or half-word) leads to undefined behavior.

Recommendation

Individual bits for channel k in FPCESR are cleared with a write to the control register (FPCCTRk) or timer register (FPCTIMk).

Writing to FPCESR directly shall be done always to the whole register (32-bit writes), with bits that should not be modified set to 1_B. In particular, LDMST or SWAPMSK.W should be used only with bit mask enabled for all ´rwh´ bits in register FPCESR.

4.126 [LBIST_TC.H004] Update reset behavior of LBISTCTRL2 register - Additional information

Description

Even though the LBISTCTRL2.[31:0] register bits are cleared by a power-on reset they will automatically recover their values from stored contents of the central LBIST controller in the TCU (Test Control Unit) afterwards.

So on first software access the user will never see the initial reset values, but the updated LBIST done status and MISR result from the TCU LBIST controller.

The stored LBIST done status and MISR result in the central TCU LBIST controller will be cleared only through an externally applied warm power-on reset or during any cold power-on reset (triggered from EVR voltage monitors).

4.127 [LMU_TC.H002] On-the-fly BBB:SRI clock ratio switching

Description

***Note**: This problem only occurs in an ADAS or Emulation Device (ED), but may already need to be considered during software development for the target device.*

When switching the clock ratio for f_{BBB} relative to f_{SRI}, make sure that no MMES (Memory Mapped Emulation System) access to EMEM is performed by an SRI master via the LMU. Otherwise, data read/written may be incorrect.

Recommendation

After a MMES read is complete, allow at least 12 SRI clock cycles before initiating a clock ratio change.

After a MMES write is complete, allow at least 20 SRI clock cycles before initiating a clock ratio change.

After a clock ratio change, allow the clock ratio change to become effective before performing any MMES transfer (for example read back control register that was written for the clock ratio change).

4.128 [LMU_TC.H003] Function of Bit MEMCON.PMIC (Protection Bit for Memory Integrity Control Bit)

Description

In the LMU chapter of the User's Manual, the following text (last paragraph in section "Local Memory (LMU SRAM)") is incorrect: Some bit-fields of the LMU_MEMCON register are protected by LMU_MEMCON.PMIC bit. If the data written to the register has the bit-field set to 0_B, no change will be made to bits 15_D to 9_D of the register regardless of the data written to these fields.

Correct Description

For the correct description (only bit 9 (ERRDIS) is protected) see the description of bit PMIC in the LMU Memory Control Register in section "LMU Registers", copied in Table 53 below:

Table 53 Bit PMIC in Register LMU_MEMCON

Field	Bit	Type	Description
PMIC	8	w	**Protection Bit for Memory Integrity Control Bit** Will always return 0_B when read 0_B Bit Protection: Bit 9 remains unchanged after LMU_MEMCON write. 1_B Bit 9 will be updated by the current write to LMU_MEMCON
ERRDIS	9	rw	**ECC Error Disable** When set SRI bus errors caused by ECC errors in data read from the SRAM will be disabled. ...

4.129 [MSC_TC.H010] Configuration of SCU.EMSR for the EMGSTOPMSC Signal

Description

The emergency stop input signal EMGSTOPMSC of the MSC module is connected to the output signal of the emergency stop control logic located in the SCU. Its functionality is controlled by the SCU emergency stop register SCU.EMSR.

The emergency stop input line EMGSTOPMSC is used to indicate an emergency stop condition of a power device. In emergency case, shift register bits can be loaded bit-wise from the downstream data register instead from the ALTINL and ALTINH buses.

The emergency stop frame is sent out at each trigger event as long as the emergency stop signal is active. This means that in data repetition mode the emergency stop frame is repeatedly sent as long as the emergency stop signal is active.

***Note**: If the emergency stop signal is used by the MSC module with setting SCU.EMSR.MODE = 1_B (Asynchronous Mode), there is some low probability that the first emergency stop frame could be corrupted, but the following emergency stop frames will be correct.*

Recommendation

- If the emergency stop signal is used by the MSC module, setting SCU.EMSR.MODE = 0_B (Synchronous Mode) is mandatory
- Setting SCU.EMSR.MODE = 1_B (Asynchronous Mode) is not allowed to be used with the MSC module

4.130 [MSC_TC.H011] Effect of kernel reset on MSC0_FCLP when selected in Event Trigger Logic

Description

If a kernel reset of the MSC0 module is performed, and signal MSC0_FCLP is selected to trigger an event via the Event Trigger Logic (ETL), an unintended trigger may be generated.

Recommendation

Disable edge detection for both the rising and the falling edge of MSC0_FCLP in the SCU, i.e. set bits EICR0.REN0 = 0_B and EICR0.FEN0 = 0_B, before performing the kernel reset on MSC0.

After the MSC0 kernel reset, restore the intended settings in register EICR0 as part of the MSC re-initialization.

4.131 [MSC_TC.H012] Handling the overflow interrupt of the ABRA block

Description

The configuration of the ABRA block and the MSC kernel is static and the timing behavior is deterministic. Therefore, an overflow/underflow event primarily signals some configuration error resulting in an unadjusted input/output baud rate ratio of MSC and ABRA. In normal operation with correctly configured baud rates this error mechanism does not occur.

However, due to an internal synchronization problem, in very rare cases an overflow interrupt might occur with the overflow flag ABC.OVF set to 1_B despite correct configuration (baud rate ratio, length of passive phase, ...).

Recommendation

The probability of the synchronization problem is low enough to allow evaluation of the overflow interrupt and the overflow flag ABC.OVF during the software development and debugging phase to identify incorrect MSC/ABRA configurations.

In the final software implementation, disable the overflow interrupt via bit ABC.OIE = 0_B, and do not evaluate the overflow flag ABC.OVF.

4.132 [MSC_TC.H013] Empty Data Frames not supported with ABRA

Description

When using the Asynchronous Baud Rate Adjustment block (ABRA), transmission of empty data frames (consisting only of a selection bit and no data bits) is not supported.

In this corner case, enable signals (ENL, ENH) may not be correctly activated, and a SYNC FIFO underflow may erroneously be signalled.

Recommendation

Do not use configurations where empty data frames (DSC.NDBL/NDBH = 00000_B) are sent in combination with ABRA.

4.133 [MTU_TC.H003] AURIX™ Memory Tests using the MTU

Description

The use of destructive tests such as March-U and Checkerboard etc. in conjunction with FAILDMP mode to get detailed failure information (errors, fail addresses) will cause the SRAM redundancy information to be overwritten.

Therefore, the MTU/MBIST module effectively only supports the Non-Destructive Inversion Test (NDIT).

Recommendation

To avoid overwriting the SRAM redundancy information, only use Non-Destructive Inversion Test. In this case, failure is detected by ECC and the detailed information can be obtained from ETRR and ECCD registers.

Refer to the latest version of Application Note AP32197 “AURIX™ Memory Tests using the MTU” for more details on MTU/MBIST usage and fault coverage.

4.134 [MTU_TC.H004] Handling the Error Tracking Registers ETRR

Description

CPU and on-chip peripheral SRAMs are capable of detecting errors and generating SMU alarms for correctable, uncorrectable, and address errors. The failing addresses are stored in Error Tracking Registers (ETRR), and the corresponding indicator (CERR/UERR/AERR and SERR) and valid bits (VAL) are set in the Memory ECC Detection Register (ECCD). Only new errors will be considered; i.e. errors at already stored addresses will be ignored. In case the maximum number of ETRR for a memory is used up and a new error occurs, the error overflow bit ECCD.EOV is set, and the corresponding “address buffer overflow” SMU alarm is generated. For peripheral SRAMs, the second error will cause a buffer overflow, and for CPU SRAMs, up to five errors can be registered before the buffer overflow alarm is triggered.

Bit ECCD.TRC (Tracking Clear) allows to clear the EOV and VAL bits in register ECCD and the associated ETRR registers, for example in response to a tolerated corrected single bit error.

Corner Case

If in an exceptional corner case software would set TRC at the same time an error overflow occurs, then the EOV bit is not set, and the SMU alarm is not generated.

Recommendation

- It is not necessary to clear the Error Tracking Registers ETRR by software as part of an SRAM error handling concept. For correctable errors, the application software should only react on the address buffer overflow alarm (for example with a reset). Single correctable error events may be ignored (within limits) to increase the fault tolerance of the system without impacting the safety
- If a different concept is used requiring clearing of the ETRR registers by software via ECCD.TRC, make sure that the corresponding SRAM instance is not functionally accessed while the application software writes ECCD.TRC, so that an overflow error cannot be generated during the clear operation

Information on using the MTU for memory diagnosis is given in Application Note AP32197 “AURIX™ Memory Tests using the MTU”.

4.135 [MTU_TC.H005] Handling SRAM Alarms

Description

Alarms are generated for CPU and on-chip peripheral SRAMs when correctable, uncorrectable, and address errors are detected.

The failing addresses are stored in Error Tracking Registers (ETRR), and information on the error type is stored in the Memory ECC Detection Register (ECCD). Only new errors will be considered, i.e. errors at already stored addresses will be ignored. In case the maximum number of ETRR for a memory is used up and a new error occurs, the error overflow bit ECCD.EOV is set, and the corresponding “address buffer overflow” SMU alarm is generated.

For peripheral SRAMs, the second error will cause a buffer overflow, and for CPU SRAMs, up to five errors can be registered before the buffer overflow alarm is triggered.

In addition, traps and bus errors are generated for uncorrectable errors, depending on the bus master and type of access.

Corner Case

If in an exceptional corner case

- two errors at different locations are present in the same SRAM
- and accesses are made to both locations within a time window of ~ 10 CPU clock cycles

then the first access to the location with an error will correctly trigger an SMU alarm, while the second access to the other location with an error will not trigger an SMU alarm. In the worst case, a correctable error may thus mask an uncorrectable or address error.

***Note**: In case the second error would result in an address buffer overflow, the corresponding bit ECCD.EOV is set and the "address buffer overflow" SMU alarm is correctly generated. Therefore, this problem is **not** relevant for peripheral SRAMs that only have one ETRR, as the second error will always cause an SMU alarm.*

Recommendations

- As recommended in Application Hint MTU_TC.H004 (Handling the Error Tracking Registers ETRR), for correctable errors, the application software should only react on the address buffer overflow alarm (for example with a reset). Single correctable error events may be ignored (within limits) to increase the fault tolerance of the system without impacting the safety
- In case an uncorrectable error for a CPU SRAM would neither generate an "address buffer overflow" nor an "uncorrectable" or "address error" SMU alarm, the error handling (typically resulting in a reset) should be performed in the corresponding trap routine
- In particular for EMEM or FFT SRAMs used in Emulation, ADAS or Extended SRAM devices of the AURIX™ family, a workaround is possible by triggering a correctable error before application startup. This would result in the ECCD.CERR bit of the corresponding MBIST to be set. Any future correctable alarms will not be forwarded[8] and this issue can be avoided completely

4.136 [MTU_TC.H006] Alarm Propagation to SMU via Error Flags in MCx_ECCD

Description

Upon any correctable, un-correctable or address error alarm in an SRAM, the corresponding error flags (CERR, UERR or AERR bits) in the MCx_ECCD register are set, and the corresponding alarm is forwarded to the SMU.

However, in case these bits are set to 1_B, and a further error of the same type occurs, then the corresponding alarm is no longer forwarded to the SMU.

If in a corner case software writes to Mx_ECCD in the same cycle where an error event would set one of the CERR, UERR or AERR bits from 0_B to 1_B, the software write has priority and the status flags remain at 0_B. In this case, however, the alarm is correctly propagated to the SMU.

***Note**: This behavior does not endanger the concept recommended in Application Hints MTU_TC.H004 and MTU_TC.H005 (ignore correctable errors, react on first uncorrectable/address error/buffer overflow alarm).*

Recommendation

Upon any alarm from an SRAM/MBIST, if a further alarm of the same type is required to be sent to the SMU and processed, then the software shall clear the error flag (CERR, UERR, AERR) in the ECCD register.

The flags can be cleared by writing MCx_ECCD.CERR (or UERR or AERR, respectively) with 0_B.

8 see MTU_TC.H006 (Alarm Propagation to SMU via Error Flags in MCx_ECCD)

4.137 [MTU_TC.H007] Reset Values of Bit ECCS.TRE

Description

The default reset value of bit MTU_ECCS.TRE (Tracking Enable) is 0_B.

A special reset value of 1_B is implemented for the MTU_ECC.TRE bit of MCs of all TriCore™ Memories. In this context, 'TriCore™ Memories' means all available DTAG, PTAG, PSPR, DSPR and DSPR2 Memory Controllers of all CPUs implemented in the product.

4.138 [MTU_TC.H009] Reset Value for Register ECCD

Description

The reset value of the ECC Detection Register ECCD is documented as 7800_H in the User's Manual. This is always the case for the SRAMs listed in the tables below (if available in the corresponding product).

For other SRAMs the ECCD reset value may either be $7C00_H$ or 7800_H.

Bit ECCD.10 is marked as 'Reserved' in the User's Manual:

- When writing to ECCD, bit ECCD.10 should be written as 0_B
- When reading register ECCD, bit ECCD.10 should not be evaluated. Memory errors will be reported by the notification bits CERR, UERR, AERR and EOV in register ECCD

TC29x SRAMs with ECCD Reset Value = 7800_H

Table 54 TC29x SRAMs with ECCD Reset Value = 7800_H

Memory Controller No.	Associated SRAM	Comments / Memory available in
2	CPU2 TC16P_DTAG	
5	CPU2 TC16P_PTAG	
8	CPU1 TC16P_DTAG	
11	CPU1 TC16P_PTAG	
17	CPU0 PTAG	
19	CPU0 TC16P_DTAG	
30	GTM MCS1	
31	GTM DPLL RAM1A	
32	GTM DPLL RAM1B	
34	PSI5	
38	ERAY0 OBF	
39	ERAY0 IBF_TBF	
80	CIF1	ADAS products only
81	CIF2	ADAS products only
83	DMA	

TC27x SRAMs with ECCD Reset Value = 7800_H

Table 55 TC27x SRAMs with ECCD Reset Value = 7800_H

Memory Controller No.	Associated SRAM	Comments / Memory available in
2	CPU2 TC16P_DTAG	
5	CPU2 TC16P_PTAG	
8	CPU1 TC16P_DTAG	
11	CPU1 TC16P_PTAG	
17	CPU0 PTAG	
30	GTM MCS1	
31	GTM DPLL RAM1A	
32	GTM DPLL RAM1B	
34	PSI5	
38	ERAY0 OBF	
39	ERAY0 IBF_TBF	
80	CIF1	ADAS products only
81	CIF2	ADAS products only
83	DMA	

TC26x SRAMs with ECCD Reset Value = 7800_H

Table 56 TC26x SRAMs with ECCD Reset Value = 7800_H

Memory Controller No.	Associated SRAM	Comments / Memory available in
8	CPU1 TC16P_DTAG	
11	CPU1 TC16P_PTAG	
17	CPU0 PTAG	
30	GTM MCS1	
31	GTM DPLL RAM1A	
32	GTM DPLL RAM1B	
34	PSI5	
38	ERAY0 OBF	
39	ERAY0 IBF_TBF	
80	CIF1	ADAS products only
81	CIF2	ADAS products only
83	DMA	

TC23x SRAMs with ECCD Reset Value = 7800_H

Table 57 TC23x SRAMs with ECCD Reset Value = 7800_H

Memory Controller No.	Associated SRAM
17	CPU0 PTAG
38	ERAY0 OBF
39	ERAY0 IBF_TBF

TC22x/TC21x SRAMs with ECCD Reset Value = 7800_H

Table 58 TC22x/TC21x SRAMs with ECCD Reset Value = 7800_H

Memory Controller No.	Associated SRAM
17	CPU0 PTAG

4.139 [MTU_TC.H010] Register MCONTROL - Bit Field Res4

Description

The position of the 3-bit-field Res4 within register MCONTROL is incorrectly described as [14:10] in the register description of the User's Manual.

Documentation correction

The correct position of the 3-bit-field Res4 is MCONTROL.[14:12], as shown in the register image in the User's Manual, and in the following Table 59:

Table 59 Register MCONTROL - Position of Bit Field Res4

Field	Bits	Type	Description
Res	15	r	**Reserved** Read returns 0_B, should be written with 0_B
Res4	14:12	**rw**	**Reserved** Read returns 0x4 Must always be written with 0x4
Res	11:10	r	**Reserved** Read returns 00_B, should be written with 00_B

4.140 [MTU_TC.H011] Access Protection for Memory Control Registers

Description

The access protection symbol 'P' to indicate Access Enable Register protection is missing in column "Access Mode - Write" in table "Register Overview of each MTU Memory Control register block" of the MTU chapter in the User's Manual.

The MTU Memory Control register block actually has protection via the Access Enable registers (ACCEN0/1).

4.141 [MTU_TC.H012] Kernel Reset triggers Reset of MBIST Registers

Description

When a kernel reset is executed (via bit RST in registers KRST0/1) for a module equipped with Memory Controllers (MC) for its internal RAMs, also the corresponding MTU Memory Control (MBIST) registers are reset.

Recommendation

If required, analyze/save the contents of the MBIST registers before executing a kernel reset.

After a kernel reset, reconfigure the MBIST registers.

4.142 [MTU_TC.H014] Access to SRAM while MTU operations are underway

Description

When MTU operations on the SRAM are underway, the memories cannot be accessed. MTU operations in this context include:

1. Running an MBIST test (for example Non-destructive test)
2. Performing an SRAM initialization using the MTU
3. When an Auto-data-initialization is underway

During these operations, the SRAM shall not be accessed. If the SRAM is accessed during this time, unexpected behavior may occur (for example access timeout).

Cases 1. and 2. are easily identified, i.e. whenever the application has triggered an MBIST test or SRAM initialization.

Case 3. occurs whenever bit-field PROCOND.RAMIN is not equal to 0x3. Whenever this is the case in specific MBIST controllers, the SRAM is fully or partially cleared under certain conditions:

- When MTU_MEMTEST.*EN bit is enabled or disabled
- When MTU_MEMMAP.*MAP bit is set or cleared (applicable only to cache memories)

This means, when the above mentioned bits are set or cleared, it takes some time (~hundreds of clock cycles) for the associated SRAMs to be (fully or partially) initialized. During this time the SRAM is not accessible.

Affected SRAMs are:

- CPUx DMEM (DSPR+DCACHE)
- CPUx PMEM (PSPR + PCACHE)

Recommendation

- For all memories, ensure that the SRAM is not accessed when any MTU operation is underway
- For the specific memories listed above, ensure that the SRAM is not accessed:
  - When setting MTU_MEMTEST.*EN bit: as long as MEMSTAT.*AIU bit is set or as long as the MEMTEST.*EN bit is not yet set
  - When clearing MTU_MEMTEST.*EN bit: as long as MEMSTAT.*AIU bit is set or as long as the MEMTEST.*EN bit is not yet cleared
  - When setting or clearing MTU_MEMMAP.*MAP bit for DMEM/PMEM: as long as MEMSTAT.*AIU bit is set

4.143 [MultiCAN_AI.H005] TxD Pulse upon short disable request

Description

If a CAN disable request is set and then canceled in a very short time (one bit time or less) then a dominant transmit pulse may be generated by MultiCAN module, even if the CAN bus is in the idle state.

Example for setup of the CAN disable request:

CAN_CLC.DISR = 1 and then CAN_CLC.DISR = 0

Workaround

Set all INIT bits to 1 before requesting module disable.

4.144 [MultiCAN_AI.H006] Time stamp influenced by resynchronization

Description

The time stamp measurement feature is not based on an absolute time measurement, but on actual CAN bit times which are subject to the CAN resynchronization during CAN bus operation.The time stamp value merely indicates the number of elapsed actual bit times. Those actual bit times can be shorter or longer than nominal bit time length due to the CAN resynchronization events.

Workaround

None.

4.145 [MultiCAN_AI.H007] Alert Interrupt Behavior in case of Bus-Off

Description

The MultiCAN module shows the following behavior in case of a bus-off status:

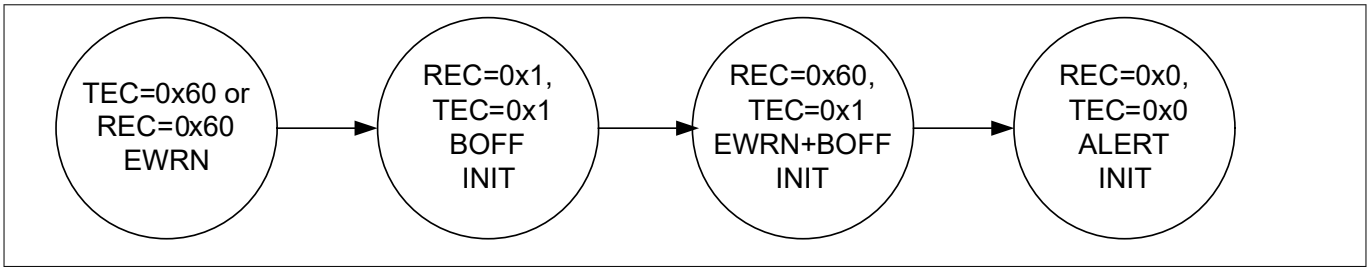

Figure 12 Alert Interrupt Behavior in case of Bus-Off

When the threshold for error warning (EWRN) is reached (default value of Error Warning Level EWRN = 0x60), then the EWRN interrupt is issued. The bus-off (BOFF) status is reached if TEC > 255 according to CAN specification, changing the MultiCAN module with REC and TEC to the same value 0x1, setting the INIT bit to 1_B, and issuing the BOFF interrupt. The bus-off recovery phase starts automatically. Every time an idle time is seen, REC is incremented. If REC = 0x60, a combined status EWRN+BOFF is reached. The corresponding interrupt can also be seen as a pre-warning interrupt, that the bus-off recovery phase will be finished soon. When the bus-off recovery phase has finished (128 times idle time have been seen on the bus), EWRN and BOFF are cleared, the ALERT interrupt bit is set and the INIT bit is still set.

4.146 [MultiCAN_TC.H003] Message may be discarded before transmission in STT mode

Description

If MOFCRn.STT =1 (Single Transmit Trial enabled), bit TXRQ is cleared (TXRQ=0) as soon as the message object has been selected for transmission and, in case of error, no retransmission takes places.

Therefore, if the error occurs between the selection for transmission and the real start of frame transmission, the message is actually never sent.

Workaround

In case the transmission shall be guaranteed, it is not suitable to use the STT mode. In this case, MOFCRn.STT shall be 0.

4.147 [MultiCAN_TC.H004] Double remote request

Description

Assume the following scenario: A first remote frame (dedicated to a message object) has been received. It performs a transmit setup (TXRQ is set) with clearing NEWDAT. MultiCAN starts to send the receiver message object (data frame), but loses arbitration against a second remote request received by the same message object as the first one (NEWDAT will be set).

When the appropriate message object (data frame) triggered by the first remote frame wins the arbitration, it will be sent out and NEWDAT is not reset. This leads to an additional data frame, that will be sent by this message object (clearing NEWDAT).

There will, however, not be more data frames than there are corresponding remote requests.

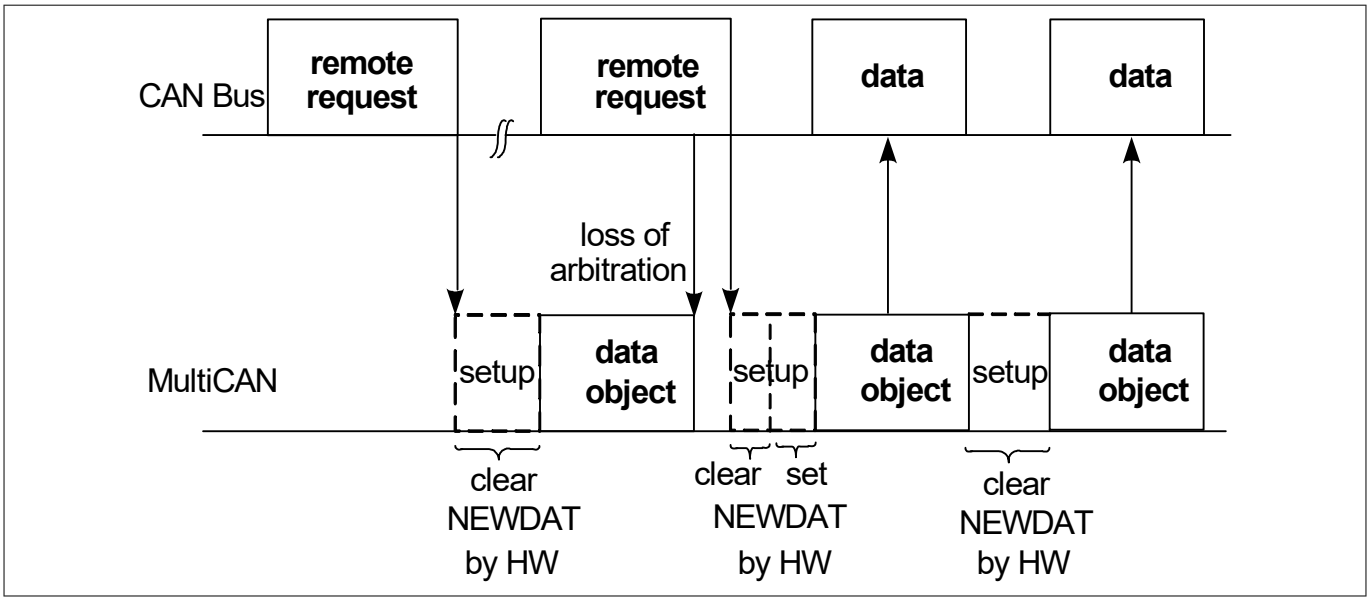

Figure 13 Loss of Arbitration

4.148 [MultiCAN_TC.H007] Oscillating CAN Bus may Disable the CAN Interface

Description

If the connected CAN network is in an unspecified oscillating state for more than 512 cycles this can result in disabling the CAN interface of the device. Enabling the CAN interface again requires then a Power-on Reset.

Recommendation

Please refer to application note AP32264 “DXCPL DAP over CAN Physical Layer” for further information and how this situation can be prevented.

4.149 [MultiCAN_TC.H008] Changes due to CAN FD protocol ISO 11898-1:2015

Description

***Note**: This Application Hint might affect the SFR C Header Definitions. In such cases, SFR usage in the software shall be analyzed within the applications for their correct handling.*

4 Application hints

Specific variants and device steps of the AURIX™ TC2xx family support the CAN FD frame format according to standard version ISO 11898-1:2015. These variants are identified by the feature type code **'N'** as last letter in the device name, for example SAL-TC299TP-128F300**N** or SAK-TC223L-16F133**N**.

***Note**:* *In **TC29x** variants with feature type code 'N', MultiCAN nodes 0..3 support this feature, while MultiCANR nodes don't.*

*In **TC27x** variants with feature type code 'N', all MultiCAN nodes (0..3) support this feature.*

*In **TC26x** variants with feature type code 'N', MultiCAN nodes 0..3 support this feature, while node 4 does not.*

*In **TC23x** variants with feature type code 'N', nodes 0 and 1 in MultiCAN and MultiCAN1 support this feature, while nodes 2 don't.*

*In **TC22x/TC21x** variants with feature type code 'N', all MultiCAN nodes (0..2) support this feature.*

For a summary of the devices and nodes supporting this feature see Table 63 at the end of this text module.

For availability of the variants with this feature see the corresponding "AURIX™ TC2xx Variants / Data Sheet Addendum".

Detailed Description

ISO 11898-1:2015 improves the failure detection capabilities of the ISO11898-1 DIS version 2014. Information about the number of stuff bits in the data field is added to the CRC field. These added bits are called **'Stuff Count'**.

The Stuff Count contains 4 bits, including

- 3 bits gray code to represent the modulo-8 of number of stuff bits in the data field
- and 1 bit for the parity

Since the Stuff Count bits are part of the CRC field, fixed stuff bits will be added before and after the Stuff Count bits. Figure 14 and Figure 15 show the frame format of the ISO 11898-1:2015 CAN FD protocol. There is no change in the classical CAN frame format.

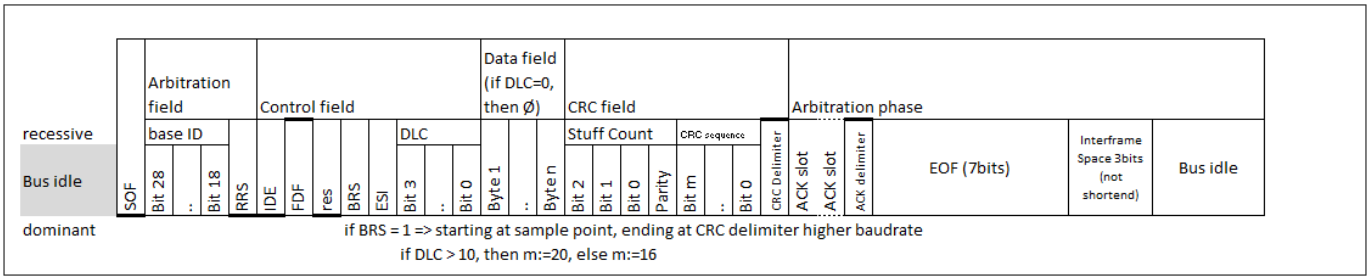

Figure 14 ISO CAN FD 11-bit ID Data Frames

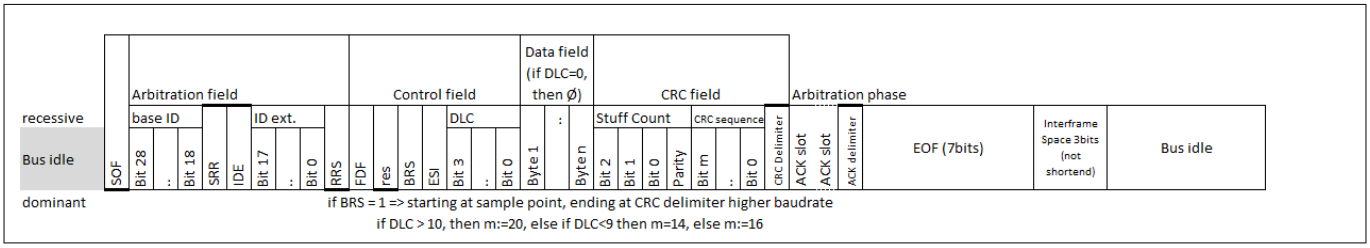

Figure 15 ISO CAN FD 29-bit ID Data Frames

From here on,

- the ISO 11898-1:2015 frame format will be referred to as **ISO** CAN FD format
- the previous frame format will be referred to as **Non-ISO** CAN FD format

***Note**:* *The ISO CAN FD frame format is incompatible with Non-ISO CAN FD frame format.*

4 Application hints

AURIX™ devices (with feature type code 'N') support both ISO and Non-ISO CAN FD formats. The format can be selected by modified functionality of bits NBTR0.15 and NBTR1.15:

Functionality of Bit NBTR0.15

NBTR0.15 is changed from NBTR0.DIV8 (Divide Prescaler Clock by 8) to **NBTR0.NISO**[9] (Non-ISO operation) as shown in Table 60:

Table 60 Functionality of Bit NBTR0.15

Field	Bit	Type	Description
NISO	15	rw	**Non-ISO Operation** If this bit is set, the MultiCAN+ uses the non-ISO CAN FD frame format. This bit is CCE protected. 0_B CAN FD frame format according to ISO 11898-1:2015 (default after reset) 1_B CAN FD frame format non-ISO.

Functionality of Bit NBTR1.15

NBTR1.15 is changed from NBTR1.DIV8 (Divide Prescaler Clock by 8) to **NBTR1.PED**[9] (Protocol Exception Disable) as shown in Table 61:

Table 61 Functionality of Bit NBTR1.15

Field	Bit	Type	Description
PED	15	rw	**Protocol Exception Disable** The protocol exception event is described in the ISO 11898-1:2015 as option. The error frame on the res bit can be controlled with this option. This bit is CCE protected. 0_B Protocol Exception Event is enabled (default after reset). 1_B Protocol Exception Event is disabled.

***Note**: Both NBTR0.NISO and NBTR1.PED are global register bits. This means they affect all the ISO 11898-1:2015 compliant CAN FD nodes in the respective MultiCAN+ module. The former DIV8 function of nodes 0 and 1 is hard-wired to 0_B (i.e. a time quantum lasts (BRP+1) clock cycles).*

The DIV8 function (Divide Prescaler Clock by 8) for all other nodes x (x>1) remains the same, irrespective of the setting of NBTR0.NISO and NBTR1.PED.

Table 62 describes the CAN FD behavior for different configurations of the NBTR0.NISO and NBTR1.PED bits. By default, the CAN FD behaves in compliance with ISO 11898-1:2015 if CAN FD is enabled (bit FDEN = 1_B for corresponding node).

Table 62 Configurations of PED and NISO

PED	NISO	CAN FD Enabled
0	0	Default values - ISO 11898-1:2015 CAN FD compliant
0	1	Non-ISO CAN FD format - same behavior as previous AURIX™ devices
1	0	CAN FD with protocol exception event disabled - ISO 11898-1:2015 CAN FD compliant
1	1	Reserved

[9] The symbolic names NISO and PED are only used for explanation in this context. If desired, the register definition file could be modified.

***Note**: Nodes where FDEN = 0_B will operate using the classical CAN frame format.*

Summary of Devices and Nodes supporting ISO CAN FD

The following table summarizes the nodes of devices with feature type code 'N' which have the ISO 11898-1:2015 CAN FD functionality.

Table 63 AURIX™ TC2xx Devices and Nodes supporting ISO CAN FD

Device / Step	ISO CAN FD supporting nodes	Non-ISO CAN FD supporting nodes
TC29x ≥ BC	MultiCAN - Nodes 0,1,2,3	MultiCANR: Nodes 0, 1
TC27x ≥ DC	MultiCAN - Nodes 0,1,2,3	all nodes support ISO CAN FD
TC26x ≥ BC	MultiCAN - Nodes 0,1,2,3	MultiCAN - Node 4
TC23x[1)] ≥ AC	MultiCAN - Nodes 0,1 MultiCAN1 - Nodes 0,1	MultiCAN - Node 2 MultiCAN1 - Node 2
TC22x ≥ AC	MultiCAN - Nodes 0,1, 2	all nodes support ISO CAN FD
TC21x ≥ AC	MultiCAN - Nodes 0,1, 2	all nodes support ISO CAN FD

1) TC23x Emulation (ED) and ADAS Devices only support Non-ISO CAN FD

4.150 [MultiCAN_TC.H009] Limitation on Secondary Sample Point (SSP) Position (ISO CAN FD nodes only)

Description

***Note**: This Application Hint only applies to ISO CAN FD nodes. For devices and nodes supporting the ISO CAN FD format, see MultiCAN_TC.H008.*

The MultiCAN+ of AURIX™ TC2xx has passed the ISO/DIS 16845-1(E), 2015 CAN Conformance test performed by an external test house C&S group GmbH and the test reports are available. The limitation on the range of SSP position is described in the Conformance test report.

In AURIX™ TC2xx devices, there are two limitations with the Secondary Sample Point (SSP) position for CAN FD with respect to ISO 11898-1, 2015 specification:

1. Granularity of the Transmitter loop delay measurement (only when CAN_FNBTRx.FBRP = 1)

Limitation

The Transmitter loop delay measurement is based on data-phase time quantum ($t_{q(D)}$) and not by minimum time quanta (mtq) or CAN clock period as specified in ISO 11898-1 2015. Hence the granularity of the transmitter loop delay measurement is +1 $t_{q(D)}$ in worst case scenario.

***Note**: According to ISO 11898-1 – 2015, when Transmitter Delay Compensation is enabled (CAN_NTDCR.TDC = 1), then the CAN_FNBTRx.FBRP shall be either 0 or 1.*

Effect

In worst case scenario, the SSP could be delayed by +1 $t_{q(D)}$.

Recommendation

It has to be taken care that the SSP offset (CAN_NTDCR.TDCO) is configured accordingly by including the granularity of the transmitter loop delay measurement of +1 $t_{q(D)}$ in worst case scenario.

2. Range of SSP position (only when CAN_FNBTRx.FBRP = 0)

Limitation

The Secondary Sample Point Position is limited to 31 t_q or 31 mtq (bit-field CAN_NTDCRx.TDCV), when compared to 63 mtq as required by ISO 11898-1, 2015.

***Note**: When CAN_FNBTRx.FBRP = 0, then 1 time-quantum (t_q) = 1 minimum time-quantum (mtq).*

CAN FD applications with fast data baud rate greater than 2 Mbit/s require Fast Baud Rate Prescaler setting CAN_FNBTRx.FBRP = 0 and f_{CAN} at 80 MHz to ensure reliable CAN communication in long networks. In such a scenario, the max SSP position achievable by the TDC is limited to 31 t_q, i.e. 388 ns (31 * 12.5 ns).

Effect

In scenarios where the sum of transmitter loop delay and SSP offset (CAN_NTDCRx.TDCO) is more than 31 time quanta, the SSP value saturates at 31 time quanta, leading to SSP placed (at 31 time quanta) earlier than required.

Recommendation

It has to be taken care to ensure that the sum of transmitter loop delay and SSP offset (CAN_NTDCRx.TDCO) is within the limit of 31 time quanta.

4.151 [MultiCAN_TC.H010] Limitation on maximum SJW Range for CAN FD Data Phase (ISO CAN FD nodes only)

Description

***Note**: This Application Hint only applies to ISO CAN FD nodes. For devices and nodes supporting the ISO CAN FD format, see MultiCAN_TC.H008.*

***Note**: Register names in the text follow the MultiCAN syntax (CAN_FNBTRx, CAN_NBTEVRx). Corresponding registers in MultiCAN1 in TC23x: CAN1_FNBTRy, CAN1_NBTEVRy.*

The MultiCAN+ of AURIX™ TC2xx has passed the ISO/DIS 16845-1(E), 2015 CAN Conformance test performed by an external test house C&S group GmbH and the test reports are available.

ISO 11898-1, 2015 specifies the configuration range of the CAN FD Data phase (re-)synchronization jump width (SJW) as 1-8 $t_{q(D)}$.

In AURIX™ TC2xx devices, the CAN FD Data phase SJW is limited to 1-4 $t_{q(D)}$, as bit-field CAN_FNBTRx.FSJW is 2 bits wide.

Effect

Configuring a MultiCAN+ node for CAN FD communication with CAN FD Data Phase SJW less than required, could result in wrong sampling of the received bit of CAN FD Data Phase, thus causing a Receive Error.

Recommendation

Choose the CAN FD configuration in such a way that

- The period of time-quanta in Arbitration phase is equal to the period of time-quanta in data phase. This can be achieved by configuring CAN_NBTEVRx.BRP = CAN_FNBTRx.FBRP
- CAN_FNBTRx.FSJW = min(CAN_FNBTRx.TSEG2, 3)

By this configuration the effect of limited Data SJW range offered by MultiCAN+ on maximum oscillator tolerance required (as given by conditions described in ISO 11898-1) is minimized.

4.152 [MultiCAN_TC.H011] Transmitter Delay Compensation Behaviour (CAN FD only)

Description

When using Transmitter Delay Compensation consider the following points:

1. The transmitter delay compensation does not take the Fractional Divider into account. This means that the values of CAN_NTDCR.TDCO and CAN_NTDCR.TDCV always correspond to CAN_FDR.DM = 01_B and CAN_FDR.STEP = 1023, even though a different setting of the fractional divider is actually in place. Therefore, it is recommended to use setting DM = 01_B and STEP = 1023 in register CAN_FDR so that the granularity of the transmitter loop delay measurement is depending only on the fast baud rate prescaler (CAN_FNBTRx.FBRP)
2. If $2*f_{CAN} < f_{CLC}$, then the transmitter delay compensation measurement value of the previous measurement may be uploaded to bit-field CAN_NTDCR.TDCV instead of the measured delay of the current message, i.e. the measured delay will appear in bit-field CAN_NTDCR.TDCV with a delay of one CAN message

4.153 [MultiCAN_TC.H012] Delayed time triggered transmission of frames

Description

The value written in the bit-field RELOAD of register NTATTRx(x=0-3), NTBTTRx(x=0-3), NTCTTRx(x=0-3) represents the reload counter value for the timer used for triggered transmission of message objects (Classical CAN or CAN FD frames).

The timer source and the prescaler value is defined in the NTCCRx(x=0-3) register.

Once a value is written to bit-field RELOAD with bit STRT=1 the timer starts counting. This timer counts one value more than the written value in bit-field RELOAD, then it triggers the transmission of a message object.

Effect

The message object transmission is delayed by one counter cycle with respect to the desired count time written in bit-field RELOAD.

Recommendation

In order to transmit a message object at a specific time, when using one of these registers:

- NTATTRx(x=0-3), NTBTTRx(x=0-3), NTCTTRx(x=0-3)

set bit-field RELOAD one value less than the calculated counter value.

4.154 [OCDS_TC.H012] Minimum Hold Time for Inputs OCDS_TGIx

Description

Inputs OCDS_TGIx (x=0..7, depending on device/package type) may be used to trigger the On-Chip Debug System (OCDS) for example for break or interrupt from an external source.

To ensure the external trigger is sampled correctly and not missed, the trigger should be asserted for a minimum of two SPB clock cycles.

4.155 [OCDS_TC.H019] System or Application Reset while OCDS and lockstep monitoring are enabled

Description

After a System or Application Reset the Lockstep Alarm ALMx[0] gets activated if all of the following conditions are met (x = index of CPU with checker core):

1. Lockstep monitoring is enabled by BMI.LCLxLSEN $= 1_B$ for CPUx, AND
2. Debug System is enabled (CBS_OSTATE.OEN = 1_B), AND
3. CPUx Performance Counters are enabled, AND
4. CPUx Clock Cycle Count register CCNT is read

Recommendation

To avoid the unintended ALMx[0] under the conditions described above, either:

- Keep the debug system disabled. OR
- Ensure CPUx Performance Counters are disabled for all CPUs that have lockstep monitoring enabled before executing a System or Application reset. OR
- Use PORST instead of a System or Application reset

4.156 [PACKAGE_TC.H006] Exposed pad dimensions and package outlines for QFP packages - Updates to TC27x Data Sheet

Description

In the scope of the harmonization of the package drawings, the drawings for the LQFP-176 package of the TC27x have been updated. No change of form, fit or function is implied.

The dimensions for the exposed pad are included in the figure.

Furthermore, for the exposed pad, the maximum boundary of the structural corner protrusions to be considered during system design and integration has been added.

This information shall substitute the corresponding information in the TC27x CA-step Data Sheet V1.1, TC27x DB-step Data Sheet V1.2, and TC27x DC-step Data Sheet V1.2.

Package Outlines LQFP-176 for TC27x

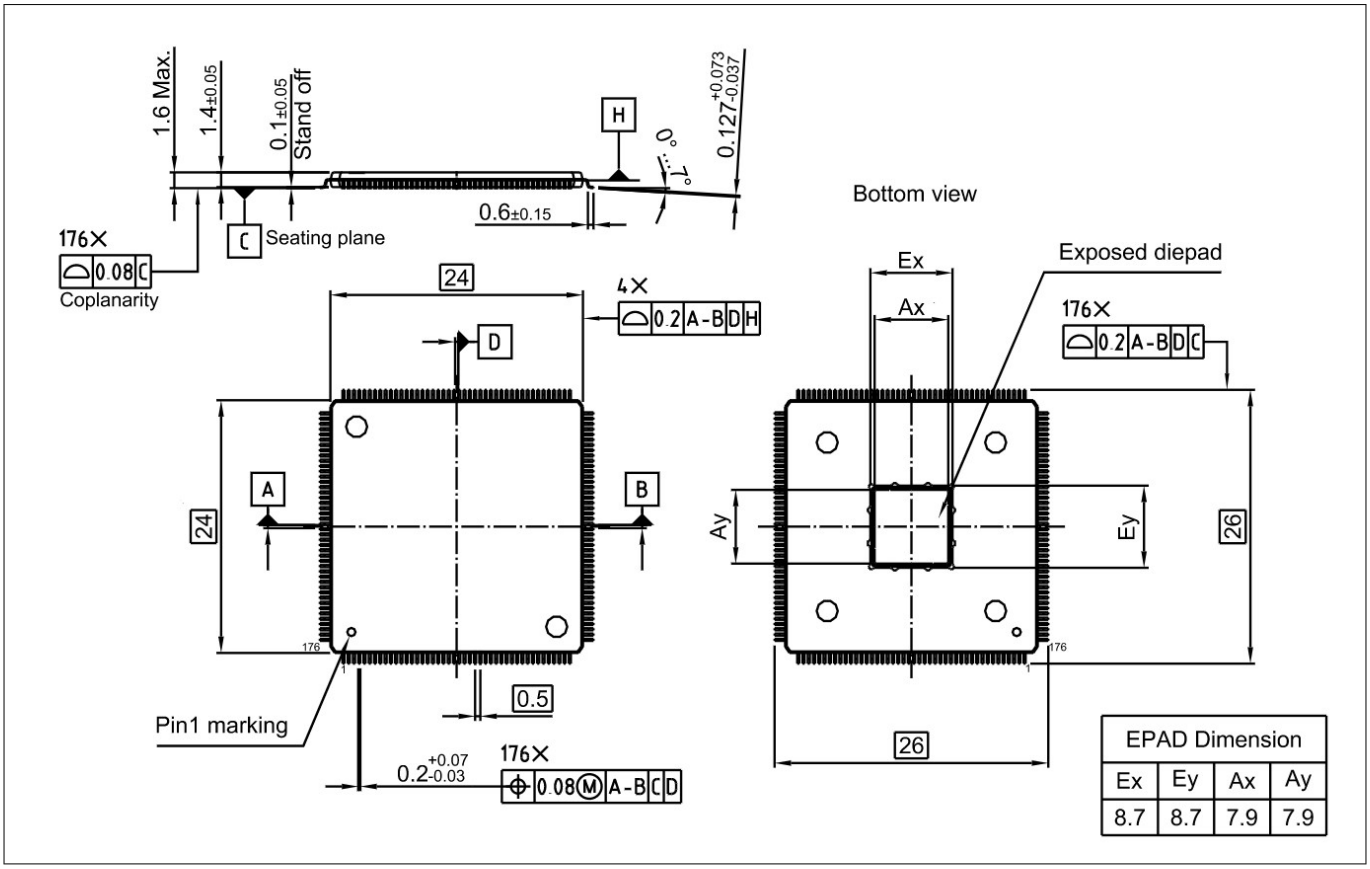

Figure 16 Package Outlines LQFP-176 for TC27x

***Note**: For the exposed pad of the LQFP-176 package of the TC27x, structural corner protrusions have to be considered for purposes of system design and integration with a maximum boundary of 9.4 mm.*

4.157 [PADS_TC.H001] Hysteresis Inactive Function

Description

The following sentence in the first section of chapter “Pad Driver Mode Register” in the User’s Manual is partially incorrect:

“For port lines configured as input (PCx), the PDx fields determines if hysteresis is active or inactive for the input function (hysteresis function is only available for MP, MP+, MPR and LP pads).”

Correction

The correct description is as follows:

For port lines configured as input (PCx), the PDx fields determine if hysteresis is active or inactive for the input function (hysteresis **inactive** function is only available for MP, MP+, MPR and most LP pads). A2, F, and S pads do not support a hysteresis inactive function.

4.158 [PADS_TC.H002] Write Access to Register PMSWCR0 when HWCFG[6] = 0

Description

When option HWCFG[6] = 0 is selected (i.e. default pad behavior is tristate), bit PMSWCR0.TRISTREQ has to be reconfigured to TRISTREQ = 1_B via PMSWCR0.TRISTEN = 1_B with the first write operation to register PMSWCR0 following a power-on.

Otherwise, with TRISTEN = 0_B and TRISTREQ = X_B on the first write to PMSWCR0 after power-on, the pad default behavior (unexpectedly) changes to 'pull-up' with the next warm PORST, system, or application reset assertion/deassertion.

For any subsequent write to PMSWCR0 after power-on, the protection for bit TRISTREQ works as specified (i.e. pad behavior unchanged after write with TRISTEN = 0_B).

***Note**: No special considerations are required when HWCFG[6] = 1, or when PMSWCR0 is not modified.*

Recommendation

When option HWCFG[6] = 0 is selected (i.e. default pad behavior is tristate), ensure to write PMSWCR0.[22:21] = 11_B (i.e. TRISTREQ = 1_B, TRISTEN = 1_B) with the first write operation to register PMSWCR0 following a power-on.

4.159 [PADS_TC.H005] Input function ETHRXCLKA on P11.12 – Additional information

Description

In the current version of the Data Sheet, in Table "Port 11 Functions", for P11.12 the ETH input function ETHRXCLKA is marked in column "Function" as "(Not for productive purposes)".

Additional information

This restriction does no longer apply. This means that P11.12 may be used as ETH input for ETHRXCLKA also in productive systems.

4.160 [PLL_ERAY_TC.H002] Correction in Figure "PLL_ERAY Block Diagram"

Description

The signal originating from block "K2-Divider" in figure "PLL_ERAY Block Diagram" in chapter "ERAY Phase-Locked Loop" of the User's Manual is incorrectly labeled as PLLERAYSTAT.K**1**RDY.

Correction

The correct name of the signal originating from block "K2-Divider" is PLLERAYSTAT.K**2**RDY.

4.161 [PMC_TC.H001] Check for permanent Overvoltage during Power-up

Description

After an initial power-on with a permanent overvoltage condition on either V_{EXT}, V_{DDP3} or V_{DD} supply rails, no overvoltage alarm may be generated by the SMU after configuration of the alarms, as the threshold transition condition has already happened.

However, in case an overvoltage condition was present, it will be indicated by flags OV13, OV33, and OVSWD, respectively, in register EVRSTAT.

Recommendation

Check the OV13, OV33, and OVSWD flags in register EVRSTAT by software at start-up to identify an overvoltage condition.

4.162 [PMC_TC.H002] Description of Register PMSWSTAT

Description

In the description of the Standby and Wake-up Status Flag Register (PMSWSTAT) in the User's Manual, bit PMSWSTAT.16 is erroneously shown as 0_B.

As the reset value of PMSWSTAT.16 = 1_B, the correct description of bit 16 in PMSWSTAT is as shown in Table 64 below:

Table 64 Register PMSWSTAT - Bits 19:16

Field	Bits	Type	Description
Res	16	r	**Reserved** Read as 1
0	19:17	r	**Reserved** Read as 0

4.163 [PMS_TC.H002] Sensitivity to supply voltage ripple during start-up

Description

The internal back-up clock is sensitive to specific power supply voltage disturbance/ripple caused by a voltage ripple intrinsic to DC-DC converters. Specific conditions such as insufficient filtering of the ripple may lead to improper behavior of the start-up scheme of the back-up clock, and thus stuck-at state during the start-up of the microcontroller until this condition is removed.

The acceptable voltage vs. frequency characteristic is portrayed below on the chart:

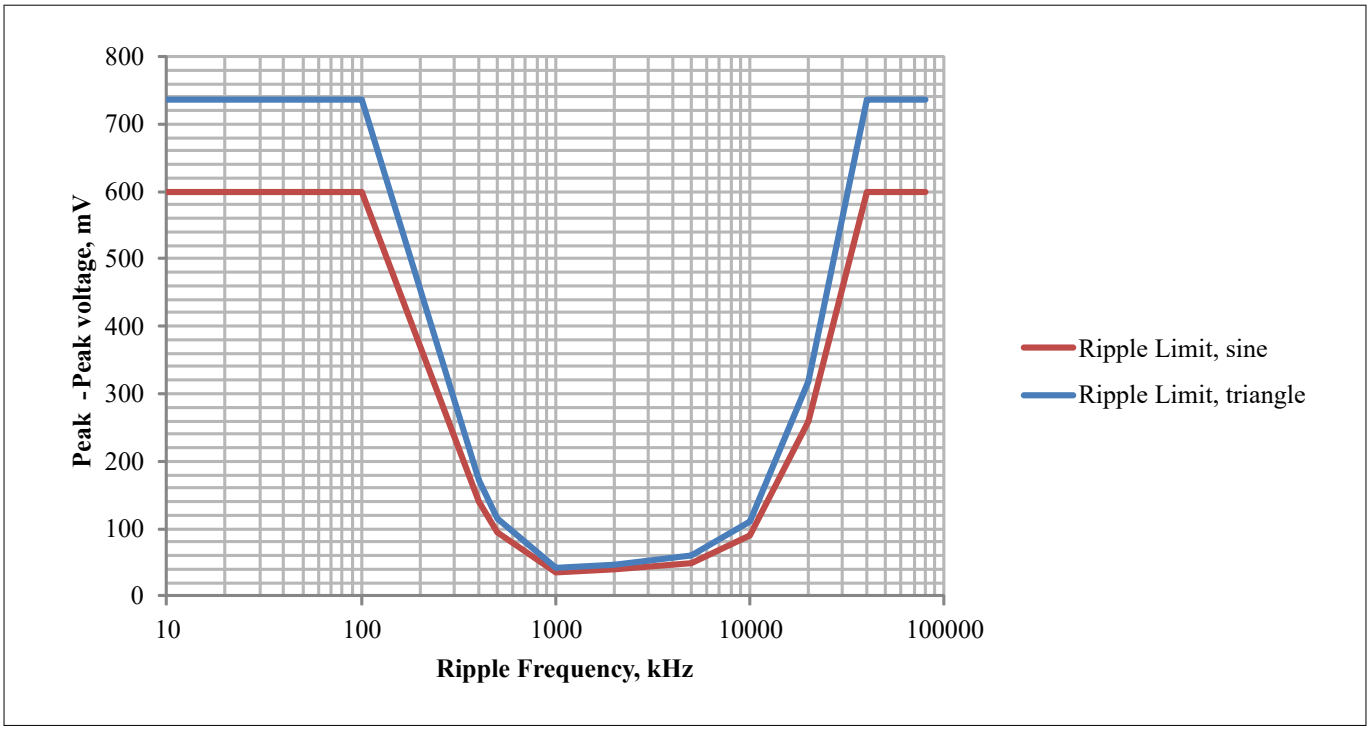

Figure 17 Ripple Voltage vs. Frequency Characteristic

The diagram reflects acceptable ripple level during the cold start of the microcontroller at the respective VDDP3/VEXT/VEVRSB supply of the PMS subsystem, depending on the device and package type, as shown in the following table.

Table 65 Pads/Pins sensitive to supply voltage ripple during start-up

Device	Package	Pad/Pin	Symbol
TC29x	BGA-516	AA16	VEVRSB
TC29x	BGA-416	AD9	VEVRSB
TC29x, TC27x, TC26x	BGA-292	T11	VEVRSB
TC27x, TC26x	QFP-176	69	VEXT
TC26x	QFP-144	59	VEXT
TC23x	BGA-292	T11	VDDP3
TC23x, TC22x, TC21x	QFP-144	69	VDDP3
TC23x, TC22x, TC21x	QFP-100	47	VDDP3
TC22x, TC21x	QFP-80	37	VDDP3

Recommendation 1

Apply an additional ceramic capacitor at the respective VDDP3/VEXT/VEVRSB supply input (at pins specified above) to attenuate the residual ripple of the buck converter. The resonant frequency of the additional filter capacitor shall be chosen in accordance with the amplitude-frequency characteristic given above and the switching frequency of the DC-DC converter in order to provide a proper attenuation in the range of interest.

The amount of ripple voltage can be approximated by $V_{pk\text{-}pk} = I_{load} / (f*C)$ and therefore the necessary nominal value of the blocking capacitance can be estimated as $C = I_{load} / (f*V_{pk\text{-}pk})$

It is recommended to take the I_{load} value as approximately 10 mA for the start-up load at the respective VDDP3/VEXT/VEVRSB domain before the internal regulator starts.

The frequency shall be taken same as the switching frequency of the external DC-DC voltage regulator. For example:

C = (0.010 A) / (10^6 Hz * 0.040 V) = 0.25 * 10^{-6} F

Recommendation 2

Dimension the output LC filter of the external DC-DC converter to meet the limit of the ripple below the specified limit at the switching frequency. The effective value of ripple current flowing in and out of the buffer capacitor is calculated in accordance with standard formulas for the DC-DC buck converters. Selection of the low-ESR buffer capacitor is crucial in such applications, as the ESR value is directly proportional to the voltage drop caused by inductor current ripple.

Recommendation 3

Supply the respective VDDP3/VEXT/VEVRSB rail by an external post LDO power stage.

4.164 [PMS_TC.H008] Interaction of interrupt and power management system - Additional information

Description

- **TC2xx**: The description of steps to enter Idle, Sleep and Standby Mode in chapter “Power Management Overview” of the PMC chapters in the current TC2xx User’s Manuals is not comprehensive in explaining the dependency on pending interrupts as well as received interrupts. Hence, more explanation is provided here.
- **TC3xx**: The description of steps to enter Idle, Sleep and Standby Mode in chapter “Power Management Overview” of the PMS and PMSLE chapters in the current TC3xx User’s Manual is not comprehensive in explaining the dependency on pending interrupts as well as received interrupts. Hence, more explanation is provided here.

For a CPU to enter Idle Mode, it must have no interrupts pending. If it is in Idle Mode it will stay in Idle Mode until one of the specified wake-up events occurs – one of these is to have a pending interrupt.

Any SRN targeting a specific CPU (i.e. TOS set to that CPU), which is enabled, i.e. has SRE set, and has received a trigger event, i.e. has SRR set (whether by a received trigger from a peripheral or a master using the SETR control bit in the SRN) is a pending interrupt. Thus, even if a peripheral is shut down by having its clocks gated off, if it has presented a trigger event to the IR, and the SRE bit for that SRN is set, there will be a pending interrupt to the specified CPU.

It is not necessary for the priority of the pending interrupt to allow it to be taken, nor is it necessary for the CPU to have interrupt servicing enabled. It is possible and valid for Idle Mode to be entered with interrupts disabled, and to only re-enable interrupt acceptance subsequent to resuming execution. Equally, the CPU’s priority may well dictate that the interrupt cannot be serviced immediately on re-enabling interrupts.

There may be some interrupts in a system that a CPU will be required to service and must exit Idle Mode (or Sleep Mode) or prevent entry to Idle Mode (or Sleep or Standby Mode) on their arrival. If one of these interrupts is raised prior to, or just as Idle Mode, Sleep Mode or Standby Mode is requested then that mode will not be entered.

The description for the REQSLP field states

- “In Idle Mode or Sleep Mode, these bits are cleared in response to an interrupt for the CPU, or when bit 15 of the corresponding CPU Watchdog Timer register (bit WDTCPUxSR.TIM[15]) changes from 0 to 1.”

For clarity, this also means, if a write to PMCSRx.REQSLP occurs while the IR has a pending interrupt for CPUx the write data will be ignored and the REQSLP value will remain as 00_B “Run Mode”.

For the system to enter Sleep or Standby Mode by writing to PMCSRx.REQSLP (as opposed through an external low voltage condition), all CPUs must be in Idle Mode. Typically, first other CPUs will be brought into Idle Mode and then the master CPU will be the last to enter to Idle Mode as a transitional state of the request for the system mode Sleep or Standby. Consequently any pending interrupts for any CPU will prevent the entry into Sleep or Standby Mode.

Recommendation

To ensure the transition to a power save mode, for a CPU intended to enter Idle Mode or for a system entering Sleep or Standby mode, all interrupts that are not intended to cause Run Mode to be re-entered or retained, should either have the SRE bit cleared in the respective SRN or be guaranteed to have the SRR bit clear.

- **TC2xx**: If modifying the SRE bit of an SRN, to ensure the new state is reflected in IR arbitration information conveyed to the PMC and CPUs, sufficient time for an arbitration must have elapsed. Hence, a subset of the synchronisation described in subsection “Changing the SRN configuration” of the IR chapter in the corresponding TC2xx User’s Manual is required.
- **TC3xx**: If modifying the SRE bit of an SRN, to ensure the new state is reflected in IR arbitration information conveyed to the PMS and CPUs, sufficient time for an arbitration must have elapsed. Hence, a subset of the synchronisation described in subsection “Changing the SRN configuration” of the IR chapter in the TC3xx User’s Manual is required.

After the last SRN (for CPUx) has been updated

- Read back the last SRN
- Read the LWSRx register

Clearing the SRR bit or disabling the source of the trigger can also be used if there are no timing hazards; i.e. no risk of a trigger being raised just before reconfiguring the peripheral (to not raise triggers), or no risk of an SRN that has had SRR cleared being set again while other SRNs are accessed. If the timing behaviour of these interrupt sources allows them to be disabled at source or in the SRN these are also valid methods. So long as the SRE bit and SRR bit are not both set, there will not be a pending interrupt. If the SRR bits are cleared, after the last SRN is modified there also needs to be a synchronisation step for the IR outputs to reflect the update before the PMCSRx is written.

Once there are no pending interrupts, request the power saving mode by writing to the respective PMCSRx.

***Note**:* ***TC2xx**: There will still be several system clock cycles till the power saving mode is enabled by the PMC during which the CPU will continue to execute instructions.*

***Note**:* ***TC3xx**: There will still be several system clock cycles till the power saving mode is enabled by the PMS during which the CPU will continue to execute instructions.*

To ensure a deterministic boundary for execution to end after the power saving mode request, the write to PMCSRx should be followed by a DSYNC and a WAIT instruction.

4.165 [PMU_TC.H002] Impact of Application Reset on register FLASH0_FCON

Description

Register FLASH0_FCON is described in PMU chapter “Flash Configuration Control” as being reset by Application Reset with reset value 0091 $XXXX_H$ with a footnote adding the information

“[1)] The wait-cycles WSECDF, WSDFLASH, WSECPF and WSPFLASH are changed by the startup after system and power-on resets. **Attention: the configured value is only sufficient for the clock configuration used during startup**. The wait-cycles have to be configured after startup as described in <reference to the PMU section “Configuring Flash Wait Cycles”> before changing to higher clock frequencies.”

In this section the user is informed that after System Reset and Power-On Reset the wait cycles are configured to have a maximum allowed frequency of 100 MHz for f_{FSI} and f_{FSI2}.

In summary this results in the following reset behavior:

- Power-on reset and system reset: both change the wait-cycles to a value sufficient for f_{FSI} and f_{FSI2} at max 100 MHz
- Application reset: changes the wait-cycles to a value not disclosed in the User’s Manual. This value is WSPFLASH=10, WSECPF=2, WSDFLASH=45, WSECDF=2

Recommendation

Consequently after each reset the application software shall write values adapted to the clock configuration as described in the section “Configuring Flash Wait Cycles”.

4.166 [PORTS_TC.H006] Using P33.8 while SMU is disabled

Description

Per default, the SMU is enabled (SMU_CLC = 0x0) and collects the alarms from the safety mechanisms defined by the safety concept. The SMU may optionally use P33.8 to output the Fault Signaling Protocol (FSP), selectable via register SMU_PCTL. To satisfy safety requirements, it is ensured that the pad configuration of this pin is not affected by an application or system reset after the first 0-to-1 transition of bit SMU_PCTL.PCS.

If the SMU is enabled, but is not using P33.8 for the FSP function, this pin may be used as general purpose input/output (GPIO) or alternate function input/output, controlled via the corresponding P33 registers.

However, if the SMU is disabled by software (SMU_CLC.DISR = 1_B, i.e. not clocked), configuration of P33.8 (pull devices, driver settings, selection of alternate function, etc.) requires special considerations as described in the following, otherwise the configuration change may not become effective.

Recommendations

- If P33.8 shall be used as GPIO or alternate function input/output, do not disable the SMU, i.e. keep SMU_CLC = 0x0 (default after reset). In this case, the configuration of P33.8 may be changed by software at any time
- Alternatively, configure P33.8 before the SMU is disabled by software (SMU_CLC.DISR = 1_B). After the SMU is disabled, the configuration of P33.8 can no longer be modified by software
- Alternatively, if the SMU is disabled by software (SMU_CLC.DISR = 1_B, i.e. not clocked), clear bit position 8 at address 0xF003 D364 in the P33 address space once after any reset (Application, System Reset, PORST) before configuring P33.8. Controlling P33.8 as FSP by SMU is possible only once after a reset

***Note**: Write access to address 0xF003 D364 is Safety ENDINIT protected.*

4.167 [PORTS_TC.H008] Emergency Stop for LVDS TX Pads in LVDS Mode

Description

The Emergency Stop function allows to force GPIOs (General Purpose Inputs/Outputs) into a defined state (input with pull-up or High-Z), either via an external signal (EMGSTOPA or EMGSTOPB) or the SMU Port Emergency Stop feature (PES).

However, on pins with LVDSM/LVDSH TX pads, the Emergency Stop function affects only the CMOS driver, not the LVDS driver.

- For **TC29x**, these are P22.[3:0], P21.[5:4], P13.[7:0]
- For **TC27x** and **TC26x**, these are P22.[3:0], P21.[5:4], P13.[3:0]

Thus, for LVDSM/H pads, only when CMOS mode is selected the output is switched off. When LVDS mode is selected the output is not switched off by the Emergency Stop function.

Recommendation

In case these LVDS TX pads are used in LVDS mode, and an Emergency Stop event occurs, switch them to the desired state via software.

4.168 [PORTS_TC.H013] Port 22 Pad Driver Mode 0 Register - Documentation Update

Description

In the current version of the User's Manual

- The reset value for register P22_PDR0 is shown as 0000 3333_H
- Bits 31..16 of register P22_PDR0 (fields PL7..4, PD7..4) are described as read-only (type 'r'), "read as 0 after reset, should be written with 0"

Correction

- The actual reset value for register P22_PDR0 is 3333 3333_H
- Bits 31..16 of register P22_PDR0 (fields PL7..4, PD7..4) are actually implemented as type 'rw', i.e. they can be read and written
- Fields PD7..4 actually control the Pad Driver Mode for Port 22 Pin 4 to 7
- Fields PL7..4 actually control the Pad Level Selection for Port 22 Pin 4 to 7

4.169 [PORTS_TC.H016] Oscillating signal may enable DXCPL and reconfigure the functionality of the port pins P14.0 and P14.1

Description

The port pin P14.1 can be configured as input for different modules such as GTM input, CAN input, FlexRay input or General Purpose Input. In case oscillations are appearing on this input, DXCPL may get enabled unintentionally on P14.0 and P14.1 and disable the module previously assigned to the pins.

Recommendation

Please refer to application note AP32264 "DXCPL DAP over CAN Physical Layer" for further information and how this situation can be prevented.

***Note**: See also MultiCAN_TC.H007 (Oscillating CAN Bus may Disable the CAN Interface).*

4.170 [PSI5_TC.H001] No communication error in case of payload length mismatch

Description

When the payload of a frame is higher than the set payload size PDLxy for channel x and slot y, then neither the CRC error nor any other error flag is reliably set in all cases.

When less data is received than the set payload size PDLxy, there are error flags (NBI) that can handle this scenario.

Recommendation

The payload data received should match the configured payload size PDLxy for channel x and slot y (register/field RCRAx.PDLy).

4.171 [QSPI_TC.H005] Stopping Transmission in Continuous Mode

Description

The QSPI module supports the following mechanisms to (temporarily) suspend its operation:

- Pause by setting bit GLOBALCON.EN = 0_B via software
- Disable by setting bit CLC.DISR = 1_B via software
- Sleep Mode (enabled with CLC.EDIS = 0) requested by hardware
- Suspend Mode requested by hardware (debugger)

These modes and their handling is described in detail in section “Operation Modes” of the QSPI chapter in the User’s Manual.

In **Continuous Mode** , the following specific behavior of QSPI module has to be considered:

- In case the QSPI module is put into **Pause** state by setting bit GLOBALCON.EN = 0_B via software, it continues transmission until the end of the TRAIL phase of the frame with BACON.LAST = 1_B
- In case the QSPI module is put into **Disable**, **Sleep**, or **Suspend** mode, the frame is stopped after the next trailing delay (character n). In case BACON.LAST was not =1_B at that time, transmission continues with character n+2 when operation from Disable/Sleep/Suspend state is resumed, i.e. data loss (character n+1) will occur

Recommendation

Ensure that software does not put the QSPI module into Pause or Disable state (via GLOBALCON.EN or CLC.DISR) while a transmission in Continuous Mode is ongoing.

If Sleep Mode is used in the system, disable acceptance of sleep requests (set CLC.EDIS = 1_B) before starting data transmission in Continuous Mode.

During debugging, ensure that the QSPI is not suspended while it is transmitting in Continuous Mode.

4.172 [QSPI_TC.H006] Corrections to Figures “QSPI - Frequency Domains” and “Phase Duration Control, Overview”

Description

In the current version of the User’s Manual,

- Figure “QSPI - Frequency Domains” erroneously uses the term “f_{PER}” instead of “f_{BAUD2}”, and
- Figure “Phase Duration Control, Overview” erroneously uses the term “T_{PER}” instead of “T_{BAUD2}”

Correction

- $f_{SCLK} = 1/f_{BAUD2}$ in Figure “QSPI - Frequency Domains”, and
- $T_{BAUD2} = 1/f_{BAUD2}$ in Figure “Phase Duration Control, Overview”

4.173 [QSPI_TC.H007] RXFIFO Overflow Bit Behavior in Slave Mode

Description

In slave mode, if no data word has been written to TXFIFO during initialization before the master starts sending data, the error flag corresponding to an RXFIFO overflow (bit STATUS.5) is set to 1_B.

Recommendation

To avoid this RXFIFO overflow event, write (at least) one word to TXFIFO during initialization and after each reset in slave mode. For following transmissions, no data need to be written to TXFIFO to avoid this effect.

4.174 [QSPI_TC.H008] Details of the baud rate and phase duration control - Documentation update

Description

To enhance readability, the last part of the second paragraph in the QSPI chapter “Details of the Baud Rate and Phase Duration Control”, starting with “Variations in the baud rates of the slaves ..”, shall be rephrased as shown below.

For further details see also the formulas in the chapter mentioned above and in the figures in chapter “Calculation of the Baud Rates and the Delays” in the User’s Manual.

Documentation update

Variations in the baud rates of slaves of one module are supported by the ECONz.Q and the ECONz.A/B/C bit-field settings allowing for a flexible bit time variation between the channels in one module.

4.175 [QSPI_TC.H009] Dummy frame required after changing SCLK polarity and phase in three wire mode

Description

When three wire mode is used, and the SCLK polarity (bit ECONz.CPOL) or phase (bit ECONz.CPH) of the master is changed by software, the state of the clock and data signals is not defined before the first data is transmitted.

This may result in wrong data being received or transmitted by the slave.

Recommendation

After the SCLK polarity (bit ECONz.CPOL) or phase (bit ECONz.CPH) is changed by software, transmission of a dummy frame is required. The pad enable shall be after transmission of the dummy frame, such that the slave will not notice the dummy frame.

***Note**: In four wire mode where the slave is controlled by a select signal from the master, this issue has no effect, because the output signals from the master are at the correct levels by the time the slave select signal gets active.*

4.176 [QSPI_TC.H011] Missing information on SLSI misplaced inactivation enable error

Description

Missing information for error interrupt "SLSI misplaced inactivation" in the Status Register.

Recommendation

The documentation will be updated as follows:

- SLSI misplaced inactivation error interrupt is raised when SLSI is deactivated by the master while the data transfer is still ongoing

4.177 [RESET_TC.H002] Unexpected SMU Reset Indication in SCU_RSTSTAT

Description

Under certain conditions the Reset Status Register SCU_RSTSTAT can show an SMU reset indication in addition to the real reset trigger (for example a SW reset).

The explanation of this behavior refers to section “Reset Generation” and following pages in chapter “RCU” of the User’s Manual.

Figure “Reset Overview” shows that all warm resets are executed in a defined sequence. This sequence ensures that first the active CPUs are ramped down, then at 80µs the Flash receives an idle request and at 180µs the reset is executed.

The idle request to the Flash makes it immediately busy, all read requests after this point fail with a bus error. All non-CPU masters (HSM, Ethernet, HSSL, DMA and DAM) however continue operation from 80µs to 180µs. When one of these masters reads the busy Flash, a bus error is signaled to the SMU as alarm ALM3[30] (SRI) and/or ALM3[31] (SPB).

If the SMU is configured to react on this by a reset request, this will be noted in the SCU_RSTSTAT register in addition to the original warm reset.

This applies mainly to the master HSM which fetches its code from PFlash.

Recommendations

- Generally a different alarm handling can be configured in the SMU for the mentioned alarms, for example trigger an NMI trap but not a reset
- When the application detects after reset that SCU_RSTSTAT has an additional SMU reset indication it might ignore it and proceed based on the other reset indication
- In case of SW resets the application can prepare the system just before activating the reset:
  - The non-CPU masters can be disabled or in case of HSM it can be informed about the imminent SW reset and continue execution from RAM
  - The mentioned alarms can be disabled or the alarm reaction can be changed to trigger an NMI trap
  - The SMU module reset can be used to reconfigure the SMU into its initial state in which only watchdog timeout alarms are handled

4.178 [RESET_TC.H003] Usage of the Prolongation Feature for ESR0 as Reset Indicator Output

Description

The ESR0 pin can be used as reset indicator output and in such a case its active low state can be prolonged upon user-configurable selection as described in section “ESRx as Reset Output” of chapter “Reset Control Unit (RCU) in the User’s Manual.

According to this description, an ESR0CNT value of 0 defines “as soon as possible after start of Boot Code execution”, where “as soon as possible” means:

- about 500 µs after cold power-on
- not less than 20 µs after other types of reset

Warning

In case of ESR0CNT = 2, the ESR0 pin will never be released by the device and the user code will never start.

***Note**:* *On the other hand - as explained before - configuring an ESR0CNT value of 1 or 2 would anyhow not be effective as a prolongation time below 20 µs is conceptually unachievable.*

Recommendation

Do not configure ESR0CNT = 2.
If prolongation of about 20 µs or below is needed, configure ESR0CNT = 3 or 0 instead.

4.179 [SCU_TC.H009] LBIST Influence on Pad Behavior

Description

The behavior of the GPIO and ESR0/1 pads during LBIST execution is as follows:

- ESR0 is switched to input direction during LBIST with weak pull-up and pull-down driver disabled (i.e. pad is tri-stated)
- ESR1 is switched to input direction during LBIST with weak pull-down driver enabled
- Other GPIO pins are switched to input direction with weak pull-up devices either stable active or inactive (depending on LBIST user configuration)

4.180 [SCU_TC.H013] Correction to Register References in Chapter “Watchdog Timers”

Description

Some references to register names in chapter “Watchdog Timers” of the User’s Manual are incorrect.
The corrected references and their section headers are listed in **bold** below.

Section Password Access to WDTxCON0

.. To ensure that a CPU fault could not allow a fault to be ignored an option is provided to prevent watchdog unlocking if the Safety Management Unit (SMU) is not in the RUN state. This option may be enabled by bit **WDTxCON1**.UR. If the password is valid and the SMU state meets the requirements of the **WDTxSR**.US bit then WDTxCON0 will be unlocked as soon as the Password Access is completed. ..

Section Timer Operation

.. The parameter divider represents the user-programmable source clock division selected by **WDTxCON1**.IRx, which can be 64, 256 or 16384.

Section Watchdog Timer Registers

- **WDTSCON1** - Safety WDT Control Register 1:
  - References to WDTxCON0 and WDTxSR should be consequently to **WDTSCON0** and **WDTSSR** in the context of WDTSCON1
- **WDTCPUxCON1** - CPUx WDT Control Register 1:
  - References to WDTSCON0 and WDTSSR should be consequently to **WDTCPUxCON0** and **WDTCPUxSR** in the context of WDTCPUxCON1

4.181 [SCU_TC.H014] Reset Value of Bit Field IOCR.PC1 - Control for Pin $\overline{\text{ESR1}}$

Description

The reset value of register SCU_IOCR is documented as 0000 $20E0_H$ in chapter “Reset Control Units” of the User’s Manual, i.e. the reset value of bit-field PC1 = 2_H.
This is not always correct under all circumstances:

The actual SCU_IOCR reset value should be considered as 0000 X0E0$_H$ with the explanations given in the following Documentation Update.

Documentation Update

The reset value of bit-field SCU_IOCR.PC1 is influenced by pin HWCFG6 and bit PMSWCR0.TRISTREQ:

- When a cold reset is activated and HWCFG6=1 then PC1 is reset to 2_H and pin $\overline{ESR1}$ will have input pull-up mode
- If HWCFG6=0 then PC1 is reset to 0_H and $\overline{ESR1}$ will have tri-state mode

PC1 and the $\overline{ESR1}$ reset state can also be configured by software with the PMSWCR0.TRISTREQ bit. PMSWCR0.TRISTREQ is not affected by warm reset or wake-up from standby so the IOCR.PC1 reset value is configured as per the state of the TRISTREQ bit prior to the warm reset.

4.182 [SCU_TC.H027] Bit field INP0 and INP1 in register EICRi - Documentation correction

Description

In the SCU chapter of the current user manual, for settings INP0 = 100_B to 111_B and INP1 = 100_B to 111_B in the description of register EICRi, the last index y of signal TRxy is erroneously shown a 0.

In the description for INP0, the enable bit is erroneously referenced as EIEN(2i) instead of EICRi.EIEN0, and as EIEN(2i+1) instead of EICRi.EIEN1 in the description for INP1.

Documentation correction

The last index y of signal TRxy shall be identical to the OGUy index. The corrected description for INP0 and settings INP0 = 100_B to 111_B and for INP1 and settings INP1 = 100_B to 111_B is shown in the following table.

Table 66 Field INP0 and INP1 in register EICRi (i=0-3) - Correction

Field	Bits	Type	Description
INP0	14:12	rw	**Input Node Pointer** This bit-field determines the destination (output channel) for trigger event (2i) (if enabled by **EICRi.EIEN0**). 100_B An event from input ETL 2i triggers output OGU4 (signal TR(2i) **4**) 101_B An event from input ETL 2i triggers output OGU5 (signal TR(2i) **5**) 110_B An event from input ETL 2i triggers output OGU6 (signal TR(2i) **6**) 111_B An event from input ETL 2i triggers output OGU7 (signal TR(2i) **7**)
INP1	30:28	rw	**Input Node Pointer** This bit-field determines the destination (output channel) for trigger event (2i+1) (if enabled by **EICRi.EIEN1**). 100_B An event from input ETL 2i+1 triggers output OGU4 (signal TR(2i+1) **4**) 101_B An event from input ETL 2i+1 triggers output OGU5 (signal TR(2i+1) **5**) 110_B An event from input ETL 2i+1 triggers output OGU6 (signal TR(2i+1) **6**) 111_B An event from input ETL 2i+1 triggers output OGU7 (signal TR(2i+1) **7**)

***Note**: In the table above, only rows that include corrections are shown.*

4.183 [SCU_TC.H028] ERU configuration changes may lead to ERU reactions

Description

The External Request Unit (ERU) may react on changes of control registers even if there is no edge at its inputs.

For example, if one of the inputs of an input channel x is '1' and this is switched to another input of this channel (by EICRy.EXISz) that is '0', then ERU recognizes an edge if configured for this input channel x and the corresponding EIFR.INTFx is set and the trigger is propagated to the ERU output as configured.

Recommendation

Clear EIFR.INTFx bits after (re-)configuration.

If an ERU reaction is to be suppressed on configuration changes (and you suspect there might be two different levels at the two ERU inputs to be switched), then:

- Clear bits EICRy.RENz, EICRy.FENz without changing EICRy.EXISz (so potential edges are swallowed at the 'Detect Event (edge)' block)
- With a 2nd write access to EICRy set bits EICRy.EXISz as needed without changing the EICRy.RENz, EICRy.FENz
- Wait long enough

  The wait time depends on the ERU input filter setting

  In case the filter is active, the 3rd access to EICRy has to happen after EIFILT.DEPTH * (EIFILT.FILTDIV + 1) SPB (100 MHz) clock cycles, otherwise the edge is still traveling through the filter and has not arrived at the 'Detect Event (edge)' block yet, to be swallowed as intended
- Then with a 3rd write access set EICRy.RENz, EICRy.FENz as needed without changing the EICRy.EXISz

4.184 [SCU_TC.H029] Non-master CPUs can wake-up unexpectedly when exiting from sleep mode

Description

In SLEEP mode, when a wake-up event occurs for the master CPU, the other non-master CPUs might wake-up to RUN state as well.

Expected behavior

Wake-up from SLEEP mode causes the master CPU to transit to RUN mode on the specified wake-up triggers (edges on WDT *MSB*, trap, interrupt, software request). When the master CPU is woken up, then the non-master CPUs should transit from SLEEP mode to IDLE mode.

Observed behavior

In general, the specified behavior is followed by the chip.

- In the corner case where the *MSB* of a non-master WDT is already set (for example during the SLEEP mode), then the corresponding non-master CPU transitions from SLEEP to RUN instead of, from SLEEP to IDLE. This is implemented this way to give the non-master CPU the chance to react before overrun of its WDT counter

Recommendation

In case the non-master CPUx is required to be in IDLE mode after wake-up of the master CPU from SLEEP, then clear the WDTCPUxSR.TIM *MSB* and suspend the WDTCPUx before entering SLEEP so that WDTCPUx MSB is '0' when woken up.

Alternatively, after wake-up from SLEEP, the PMCSRx.REQSLP can be written with "01" to request IDLE for the non-master CPUx.

4.185 [SENT_TC.H002] SENT Nibble Tolerance

Description

The length of a nibble in the SENT protocol determines the value of this nibble. For each value this length can vary, but it has to be at least inside a given range. This range is given by the SENT standard.

- The lower border is nominal_value-(tick_length/2) µs+100 ns
- The upper border is nominal_value+(tick_length/2) µs-**100** ns

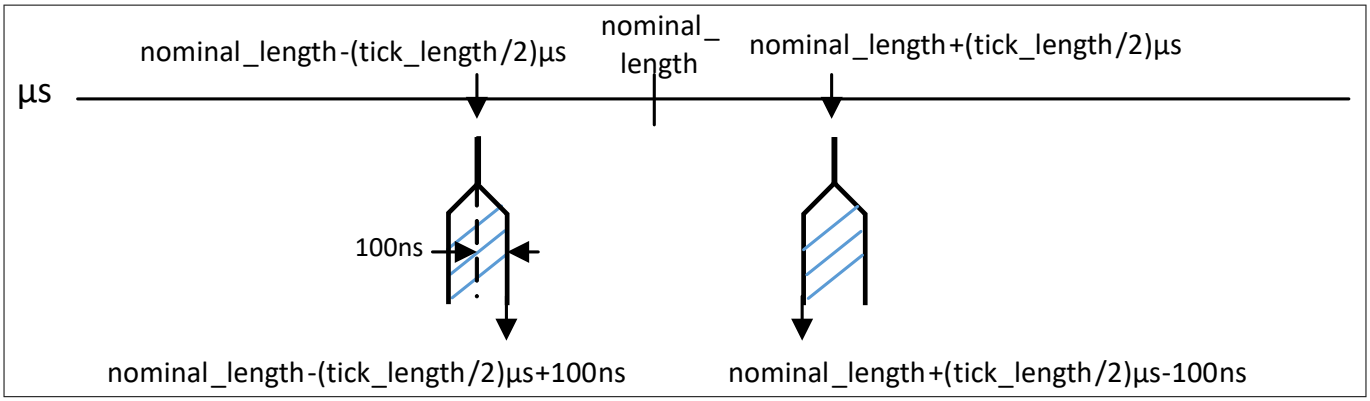

Figure 18 SENT Standard Tolerance

In this design step the range is delimited as follows:

- The lower border is nominal_value - (tick_length/2) µs + 100 ns
- The upper border is nominal_value + (tick_length/2) µs - **145** ns

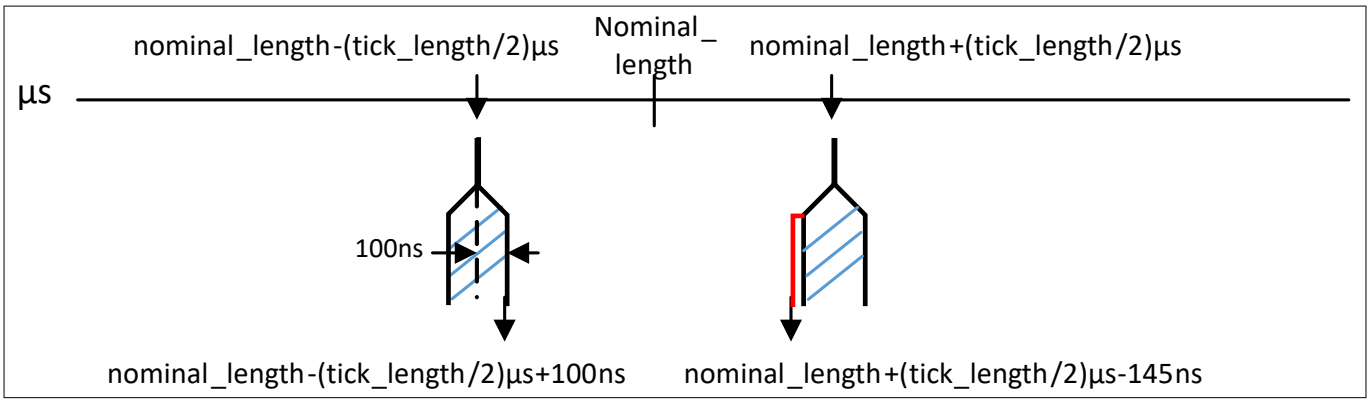

Figure 19 SENT Tolerance of this Design Step

Recommendation

To compensate this 45 ns difference so that there is no deviation from the SENT Standard, use the classified port pins as described in AppNote **AP32286** “Parameter V_{ILSD} for LP and MPx Pads relevant for SENT”.

4.186 [SENT_TC.H003] First Write Access to Registers FDR and TPD after ENDINIT Status Change

Description

Due to an extra registering stage of the ENDINIT signal from the SCU inside the SENT kernel, the behavior of the first write access to SENT registers FDR and TPD protected by the Endinit write protection scheme after an ENDINIT status change is as follows:

- After unlocking protection (ENDINIT change from 1 to 0), if the first access to the SENT module is a write to FDR or TPD, it will still view ENDINIT as locked (value 1). The contents of FDR or TPD is not changed, but no BCU alarm will be generated, as the ENDINIT does not indicate a protected status in case of the access
- By setting protection again (ENDINIT change from 0 to 1), if the first access to the SENT module is a write to FDR or TPD, it will still be effective, i.e., the value will be written. Nevertheless a SMU alarm through BCU will be generated as the protection status is ENDINIT

***Note**: After the first read of any SENT register, or first write to any SENT register, the ENDINIT change will be correctly considered for all following accesses. The CLC, KRST0/1 and KRSTCLR registers (that also have Endinit protection) are not affected at all. An initial value of 0 for ENDINIT is seen by SENT after reset before the first access.*

Recommendation

After a change of the ENDINIT protection status, first perform a read of any SENT register or a write to a non-Endinit-protected SENT register. The second access is then always equipped with correct information of ENDINIT.

4.187 [SENT_TC.H004] Short Serial Message - Figure Correction

Description

In Figure “Short Serial Message, Serial Data Encoding over 16 messages” of the SENT chapter, the arrows originating from bits 2 and 3 of the Status & Comm Nibble are routed incorrectly and must be swapped.

Correction

Figure 20 shows a corrected version of this figure.

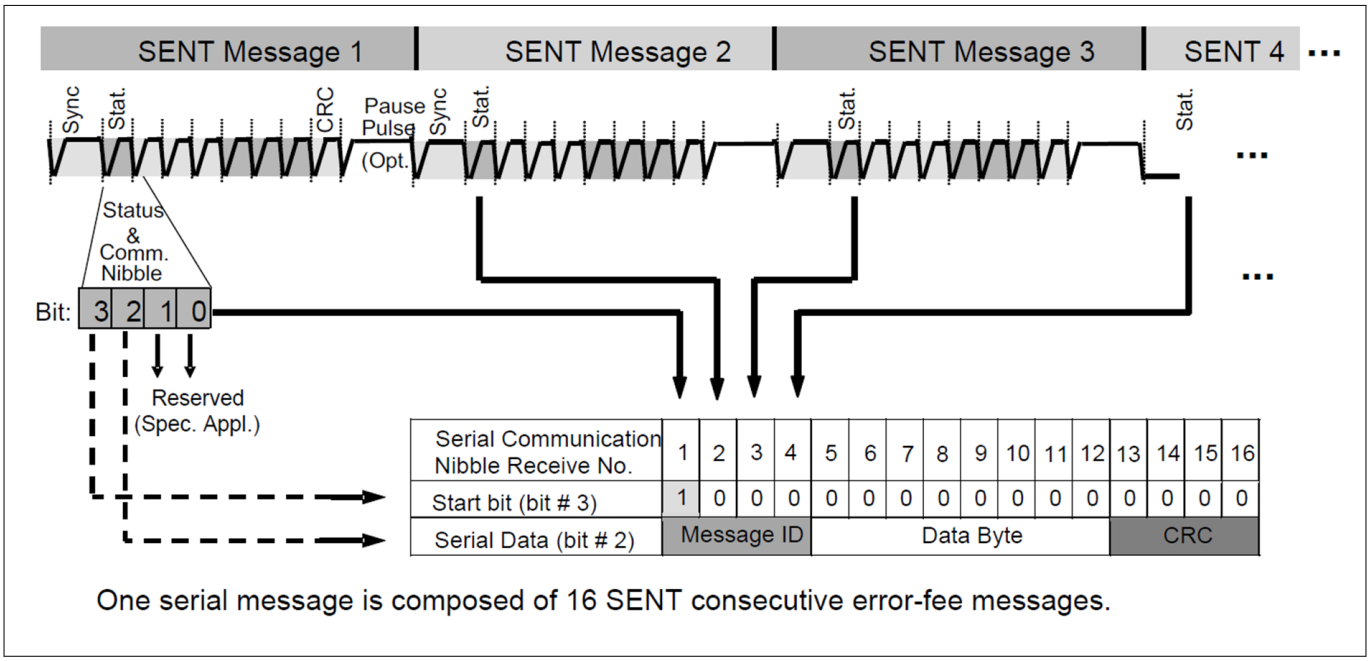

Figure 20 Short Serial Message, Serial Data Encoding over 16 messages

4.188 [SENT_TC.H009] Unexpected NNI error behavior

Description

The NNI interrupt is triggered when the actual number of transmitted nibbles exceeds the expected count predefined in RCRx.FRL. Specifically, when IEP = 0 and no pause pulse is used, NNI interrupt performs as expected. However, when IEP = 1 and a pause pulse is used, the interrupt is not triggered if the number of transmitted nibbles surpasses the expected value by one nibble. In this case, the NNI interrupt is only triggered when the number of nibbles transmitted surpasses the expected value by two or more nibbles.

Recommendation

Due to this issue, SENT messages could be missed. This can be detected by implementing timeout or message rate checking mechanisms.

4.189 [SMU_TC.H001] Write all bit-fields of SMU_PCTL with one write access

Description

When configuring the FSP pin (for example P33.8), all bit-fields (HWDIR, HWEN and PCS) of register SMU_PCTL must be written with the same write access.

Otherwise, when first writing a 1_B to HWEN before writing a 1_B to PCS, the pad configuration will be modified to push/pull configuration before it is latched into field PCFG.

***Note**: When PCS = 1_B, the bit-fields PCFG and PCS are protected against any changes until the next power on reset. HWEN and HWDIR may still be modified by SW, unless locked via register SMU_KEYS.*

4.190 [SMU_TC.H004] Alarm Mapping related to ALM3[9] in ALM3 Group

Description

The VADC incorporated in this device uses clocks derived from f_{SPB}. The fault type “clock out of range” for the VADC is therefore covered by ALM3[7] “SPB clock out of range frequency”.

Previous design steps (for example TC27x Bx, TC26x Ax, TC29x Ax) incorporated a different VADC module (clocked by f_{ADC}) using ALM3[9] to signal faults of f_{ADC}.

However, clock f_{ADC} and its monitor still exist in the present design and are connected to ALM3[9] listed as “ADC clock out of range frequency” alarm in table “Alarm Mapping related to ALM3 group“ of the SMU chapter.

Recommendation

- New software implementations should treat ALM3[9] as “Reserved”, i.e. software should configure the behavior to “No Action”
- Software ported from previous design steps with a VADC module clocked by f_{ADC} may be reused on this device step. However, alarms from ALM3[9] should be ignored

4.191 [SMU_TC.H005] Correction to Figure “SMU Register Map”

Description

The start address “@SMU + 0x0E0” for the SMU System Registers shown in the lower part of figure “SMU Register Map” in the SMU chapter of the User’s Manual is incorrect.

The correct start address is “@SMU + 0x**7E0**”.

Addresses listed in table “Registers Overview” of the SMU chapter are correct.

4.192 [SMU_TC.H006] Description of Bit EFRST in Register SMU_AGC

Description

In the SMU chapter of the User's Manual, the description of the encoding of bit EFRST (Enable FAULT to RUN State Transition) in register SMU_AGC (Alarm Global Configuration) is missing.

The complete description should be as shown in Table 67:

Table 67 Bit EFRST in Register SMU_AGC

Field	Bits	Type	Description
EFRST	29	rw	**Enable FAULT to RUN State Transition** 0_B FAULT to RUN State Transition disabled 1_B FAULT to RUN State Transition enabled See section "**FSP Fault State** " for the usage of this field.

4.193 [SMU_TC.H007] SPB Bus Control Unit (SBCU) Alarm Signalling to SMU

Description

ALM3[31] is dedicated to System Peripheral Bus (SPB) alarms. As described in table "Alarm Mapping related to ALM3 group" in the SMU chapter of the User's Manual, an SPB bus error can result from multiple root causes, including protocol violation, incorrect address, register access protection violation.

More details on the SPB related error conditions can be found in the "On-Chip Bus System" chapter:

The SBCU signals an alarm to the SMU whenever it detects

- a SPB transaction that was finished with a Bus Error (Error Acknowledge)
- an un-implemented Address (no slave responds to a transaction request)
- a SPB transaction that was finished by a Time-out

The alarm signaling to the SMU is independent of the BCU configuration (for example BCU interrupt configuration, BCU debug status).

4.194 [SMU_TC.H010] Clearing individual SMU flags: use only 32-bit writes

Description

The SMU registers shall only be written via 32-bit word accesses (i.e. ST.W instruction), as mentioned in table "Registers Overview" of the SMU chapter in the User's Manual.

If any other instruction such as LDMST or SWAPMSK.W is used to modify only a few bits in the 32-bit register, then this may have the effect of modifying/clearing unintended bits.

Recommendation (Examples in C Language)

- **Example 1**: To clear status flag SF2 in register AG0, use:
  - SMU_AG0.U = 0x0000 0004;
- **Example 2**: To clear status flags EF2 in register RMEF and RMSTS, use:
  - SMU_RMEF.U = 0xFFFF FFFB;
  - SMU_RMSTS.U = 0xFFFF FFFB;

Here the <REGISTER>.U implies writing to the register as an unsigned integer, which normally results in a compiler translation into an ST.W instruction.

Safety Considerations

As long as software uses only 32-bit writes to the SMU registers, there is no risk of malfunction.

In case the software does not use 32-bit writes (and for example uses bit-wise operations such as LDMST instructions instead) – then potentially unintended flags may be written and modified in the SMU registers. Depending on the application, this may potentially have an impact on safety and/or diagnostics.

***Note**: The SMU reaction itself (for example alarm action triggering) is not affected even if the software unintentionally clears additional bits by not using a 32-bit write as recommended.*

4.195 [SMU_TC.H013] Increased Fault Detection for SMU Bus Interface (SMU_CLC Register)

Description

Transient faults can possibly affect the SMU_CLC register and lead to disabling the SMU_core. This unintended switching off of SMU_core cannot be detected if the FSP protocol is not used at all or used in FSP bi-stable mode.

Recommendation

In order to increase the capability of the microcontroller to detect such faults it is recommended to:

- Option 1:
  Use FSP Dynamic dual-rail or Time-switching protocol only, don’t use FSP bi-stable protocol
- Option 2:
  In case FSP protocol is not used at all or Recommendation Option 1 is not possible, the [Application SW] shall read periodically, once per FTTI, the SMU_CLC register to react on unintended disabled SMU

4.196 [SMU_TC.H014] Unintended short pulse on FSP pins in Time switching or Dual-rail mode

Description

Due to an internal synchronization issue, an unintended short pulse of a duration of around 80 ns can be seen on the FSP pins if the FSP pins are configured for Time switching or Dual-rail mode, and one of the following scenarios happens in the SMU state machine:

- Scenario a): transition from START to RUN state
- Scenario b): transition from FAULT to RUN (Fault-Free) state

Recommendation

- Workaround for scenario a):
  - Enable FSP by writing SMU_PCTL register 10 SPB clock cycles (or more) after sending SMU_ReleaseFSP() command
- Assessment for scenario b):
  - The pulse in scenario b), if it occurs, cannot be avoided but has no safety impact as the unintended pulse happens during the transition from fault state to fault-free state. This state transition is not considered as safety relevant

4.197 [SRI_TC.H001] Using LDMST and SWAPMSK.W instructions on SRI mapped peripheral registers (range 0xF800 0000-0xFFFF FFFF)

Description

The LDMST and SWAPMSK.W instructions in the AURIX™ microcontrollers are intended to provide atomicity as well as bit-wise operations to a targeted memory location or peripheral register. They are also referred to as Read-Modify-Write (RMW) instructions.

The bit-manipulation functionality is intended to provide software a mechanism to write to individual bits in a register, without affecting other bits. The bits to be written can be selected through a mask in the instruction. Please refer to the TriCore™ Architecture Manual for further information about these instructions and their formats.

Restrictions for SRI mapped Peripherals

The bit-manipulation functionality is supported only on registers accessed via the SPB bus, and is not supported on the SRI mapped peripheral range, that is address range 0xF800 0000 to 0xFFFF FFFF

The SRI mapped peripheral range includes the following units (if available):

- In **TC2xx**: EBU, PMU0, SRI Crossbar, LMU, DAM, FFT, CPUx SFRs and CSFRs, MCDS, miniMCDS; see table “On Chip Bus Address Map of Segment 15” in chapter “Memory Map”
- In **TC3xx**: DMU, LMU, EBU, DAM, SRI Crossbar, SPU, CPUx SFRs and CSFRs, AGBT, miniMCDS, ...; see table “On Chip Bus Address Map of Segment 15” in chapter “Memory Map”

On the SRI mapped peripherals, usage of these instructions always results in all the bits of a register being written, and not just specific individual bits.

***Note**: The instructions are still executed atomically on the bus – that is, the SRI is locked between the READ and the WRITE transaction.*

4.198 [STM_TC.H001] Effect of kernel reset on interrupt outputs STMIR0/1

Description

The clock ratio $f_{STM} : f_{SPB}$ is determined by the settings of bit-fields STMDIV and SPBDIV in registers CCUCON1 and CCUCON0, respectively.

If $f_{STM} \leq f_{SPB}$, and a kernel reset of the STM module is performed in the same clock cycle where a compare match of the STM with the CMP0 or CMP1 registers occurs, a transition on the interrupt outputs STMIR0 or STMIR1 may occur. This may for example trigger the External Request Unit (ERU), or set the corresponding Service Request flags SRC_STMmSR0.SRR or SRC_STMmSR1.SRR in the Interrupt Router (m = 0, 1, 2, depending on number of CPUs).

***Note**: For $f_{STM} > f_{SPB}$, this effect will not occur.*

Recommendation

If $f_{STM} \leq f_{SPB}$, set bits ICR.CMP0EN = 0_B and ICR.CMP1EN = 0_B to disable the compare match interrupts before performing the STM kernel reset.

4.199 [STM_TC.H002] Access Protection for STM Control Registers

Description

The access protection symbol ‘P’ to indicate Access Enable Register protection is missing in table “Registers Overview - STM Control Registers” of the STM chapter in the User’s Manual for the STM registers CMP0, CMP1, CMCON, ICR, ISCR.

The STM registers CMP0, CMP1, CMCON, ICR, ISCR actually have protection via the Access Enable registers (ACCEN0/1), as shown in the following Table 68.

Table 68 Correction to Table Registers Overview - STM Control Registers

Short Name	Description	Offset Addr.	Access Mode		Reset
			Read	Write	
CMP0	Compare Register 0	30_H	U, SV	U, SV, P	Application
CMP1	Compare Register 1	34_H	U, SV	U, SV, P	Application
CMCON	Compare Match Control Register	38_H	U, SV	U, SV, P	Application
ICR	Interrupt Control Register	$3C_H$	U, SV	U, SV, P	Application
ISCR	Interrupt Set/Clear Register	40_H	U, SV	U, SV, P	Application

4.200 [STM_TC.H003] Suspend control for STMx - Documentation Update

Description

In contrast to the register description of bit OCS.SUS in the STM chapter of the current User's Manual, the suspend functionality of STMx is controlled by signal CPUxSUSOUT of the corresponding CPUx (and not by the signal coming from the OCDS Trigger Switch (OTGS)).

Therefore, the description for bit OCS.SUS in the STM chapter should read:

- "Controls the sensitivity to the suspend signal coming from the CPU (CPUxSUSOUT)"

4.201 [STM_TC.H004] Access to STM registers while STMDIV = 0

Description

If accesses to STM kernel registers are performed while bit-field STMDIV = 0_H in the corresponding CCU Clock Control register (that is, clock f_{STM} is stopped),

- the SPB bus gets locked after the first access until a timeout (defined in BCU Control register field SBCU_CON.TOUT) occurs;
- after the second access the STM slave will answer with RTY (retry) until the STM is clocked again with STMDIV > 0_H

The corresponding CCU Clock Control register including STMDIV is:

- CCUCON1 in **TC2xx**
- CCUCON0 in **TC3xx**

Recommendation

- In **TC2xx**, do not access any STM kernel register while CCUCON1.STMDIV = 0_H
- In **TC3xx**, do not access any STM kernel register while CCUCON0.STMDIV = 0_H

4.202 [TC27xDC_TC.H001] Revision history for datasheet TC27xDC_DS_v12

Description

The datasheet named "TC27xDC_DS_v12", which is available for download from myICP, accidentally includes the revision history for TC27x step DB in chapter 4 (History).

4 Application hints

Except for chapter 4, this datasheet is equivalent to the datasheet named “TC27xDC_DS_v11”, which is also available for download from myICP.

Documentation update

In chapter 4 (History) of the datasheet named “TC27xDC_DS_v12”, the following sentences and titles shall be updated and interpreted for TC27x step DC as listed below:

4. History

Version 0.6 is the first version of the datasheet for TC27x step DB

4.1 Changes from datasheet version 0.6 to 0.7 for step DB

4.2 Changes from datasheet version 0.7 to 1.0 for step DB

4.3 Changes from datasheet version 1.0 for TC27x step DB to datasheet version 1.0 for step DC

The following additional change is included in datasheet version 1.0 for step DC:

- Replace PG-LQFP-176-18 with correct package LF-BGA-292-6 in table 1

4.4 Changes from datasheet version 1.0 for TC27x step DC to datasheet version 1.1 for step DC

4.5 Changes from datasheet version 1.1 for TC27x step DC to datasheet version 1.2 for step DC

Revision history for TC27x step DB included in datasheet for TC27x step DC

Revision history

Document version	Date of release	Description of changes
1.0	2016-08-02	First version for step DC. This device step supports CAN FD frame format according to standard version ISO 11898-1:2015. For details see MultiCAN_TC.H008.
1.1	2017-02-01	• The following text modules have been included in Table 3 (Errata fixed in this step): - FLASH_TC.044 (Repetitive Erase Suspend Requests on Data Flash): only microcode version ≥ v2.3 used in step DC - ADC_TC.P007 (Additional Parameter for Data Sheet: Wakeup Time t_{WU}): see specification of t_{WU} in TC27x DC-Step Data Sheet • New/updated text modules see columns “Change” in Table 4..6 in errata sheet V1.1
1.2	2018-02-23	• Update: new/updated text modules see columns “Change” in tables 4..6 of errata sheet V1.2 • Text modules GTM_TC.H014 and GTM_TC.H015: moved from chapter “Functional Problems” to chapter “Application Hints”; contents unchanged • Removed reference to “GTM-IP Gen1 IFX Errata Sheet” in Table 1 - all GTM errata relevant for this design step are considered in this TC27x errata sheet
1.3	2019-06-24	• Update: new/updated text modules see columns “Change” in tables 4..6 of errata sheet V1.3 • Most of the new/updated DMA_TC.* text modules result from the integration of Information Note No. 028/18 (DMA_TC2xx_EPN), • DMA_TC.061 (DMA Double Buffering Operations) replaces the following text modules: - DMA_TC.029 (DMA Double Buffering Overflow), - DMA_TC.047 (DMA Double Buffering Buffer Switch), - DMA_TC.057 (Double Buffering Overflow Causes Other Channel Corruption)
1.4	2020-11-06	• Update: new/updated text modules see columns “Change” in tables 4..6 of errata sheet V1.4
1.5	2022-07-04	• Update: new/updated text modules see columns “Change” in tables 4..6 of errata sheet V1.5
1.6	2023-08-14	• Update: new/updated text modules see columns “Change” in tables 4..6 of errata sheet V1.6 • Removed: - ASCLIN_TC.012: does not apply to design implementation in AURIX™ family - ASCLIN_TC.H007: does not apply to ASCLIN implementation in TC2xx

Revision history

Document version	Date of release	Description of changes
2.0	2024-06-28	For new and changed errata see also column "Change" in tables 2, 3, and 4. New: • GTM_AI.410, GTM_AI.507, GTM_AI.516, GTM_AI.517, GTM_AI.H519, GTM_AI.522, GTM_AI.H803, HSCT_TC.014, MultiCAN_TC.041, QSPI_TC.H011, SCU_TC.H028, SCU_TC.H029, SENT_TC.H009 Update to latest errata sheet document template (details see below). Following editorial changes were applied to several (not all) errata (examples): • Misspellings, typos, and case sensitivity • Aligned with latest Infineon writing guidelines • Added 'Description' section title when missing • Added 'TM' where missing (e.g. TriCore™) • Standard footnote numbers are incremented over the entire document (and not per erratum). Table footnotes are numbered per table When an erratum is used by different families or devices, the erratum is now identical in all errata sheets. Differences between the different families or devices are clearly highlighted in the erratum. No update of technical content. TC4xx family specific content has been removed: • ADC_TC.068, ADC_TC.H019, ADC_TC.P011, BROM_TC.008, BROM_TC.H003, CCU_TC.H001, CCU_TC.H005, CPU_TC.131, DSADC_TC.H004, DSADC_TC.H010, FlexRay_TC.H002, FPI_TC.H002, GTM_AI.141, GTM_AI.142, GTM_AI.260, GTM_AI.348, GTM_AI.353, GTM_AI.458, GTM_AI.478, GTM_AI.492, GTM_AI.H473, GTM_AI.H481, GTM_AI.H497, GTM_TC.H004, GTM_TC.H007, GTM_TC.H015, GTM_TC.H017, IDD_TC.H001, MTU_TC.016, MTU_TC.H009, MultiCAN_TC.H008, MultiCAN_TC.H010, PADS_TC.P009, PLL_TC.007, PMS_TC.H008, PORTS_TC.002, PORTS_TC.H008, QSPI_TC.017, RTH_TC.H001, SMU_TC.012, SRI_TC.H001, STM_TC.H004 Section 'Severity' is removed from following errata: • FlexRay_AI.104, FlexRay_AI.105, FlexRay_AI.106

Table 69 Errata fixed in this step

Errata	Short description	Change
ADC_TC.P007	Additional Parameter for Data Sheet: Wakeup Time t_{WU}	Fixed[1)]
CCU_TC.002	Clock Monitors - Target Monitoring Frequency Selection	Fixed
CPU_TC.125	Unexpected Address Error Alarms caused by Speculative Access to Out-of-range PMEM Areas	Fixed
FLASH_TC.044	Repetitive Erase Suspend Requests on Data Flash	Fixed
MSC_TC.016	MSC Spikes on Data and Enable Signals	Fixed
MultiCAN_AI.047	Transmit Frame Corruption after Protocol Exception (CAN FD only)	Fixed
PWR_TC.P013	EVR Supply Voltage V_{EXT} Ramp-up	Fixed
SMU_TC.005	Unexpected/Incorrect Reset caused by SMU Alarms	Fixed

1) see specification of t_{WU} in TC27x DC-Step Data Sheet

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Edition 2024-06-28

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-ror1688370667344

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