# TDA38640A OptiMOS iPOL

## 40A Single-voltage Synchronous Buck Regulator with SVID and I2C

## Quality Requirement Category: Industrial

### Features

- Single 5 V to 17 V application or Wide Input Voltage Range from 3.0 V to 17 V with external Vcc
- Output Voltage Range: 0.25 V to 3.04 V with external feedback resistor divider in SVID mode
- Enhanced Fast COT Engine stable with Ceramic output Capacitors and no External Compensation
- Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency
- Programmable Switching Frequency from 400 kHz to 2 MHz in steps of 200 kHz, excluding 1600 kHz
- Monotonic Startup with Selectable Soft-Start Time via SVID or PMBus Commands & Pre-Bias Startup
- Thermally Compensated Internal Over Current Protection with Eight Selectable Settings
- I2C system interface for reporting of Temperature, Voltage, Current & Power telemetry
- Multiple Time Programming (MTP) with up to 14 writes for the USER section
- Digitally programmable load-line without any external components
- 12 V input current sensing is supported without the need of an external interface circuit
- Operating temp: -40 °C < Tj < 125 °C
- Small Size: 5 mm x 6 mm PQFN
- Lead-free, Halogen-free and RoHS2 Compliant with Exemption 7a

### Applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

### Description

The TDA38640A is an easy-to-use, fully integrated and highly efficient dc-dc regulator with Intel SVID and I2C/PMBUs interfaces. The controller utilizes Infineon's fast COT engine which simplifies the design efforts, and achieves faster transient response.

The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38640A a small footprint solution, providing high-efficiency power delivery for low voltage high current applications which may need an SVID interface.

TDA38640A is a versatile regulator, operating with wide input and output voltage range, offering eight programmable switching frequency from 400 kHz to 2 MHz excluding 1600 kHz, and providing eight unique selectable current limits via the PMBUs commands.

It also features important protection functions, like the thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions. The part supports programmable digital dc loadline, providing the customer with an additional tool

to manage the transients for a given rail. The device supports 12 V differential input current sensing (through the pins VINSENP and VINSENM) without the need of external interface circuitry (e.g. pi-sense, etc.) which simplifies the design, reduces complexity, and results in reported current being more consistent and accurate, as it only depends on the internal IC circuitry where the parameters are trimmed for every part to meet specifications.

The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the on-chip memory. The TDA38640A provides extensive OVP, UVP, OCP, OTP & Boot UVLO fault protection. The controller requires the fewest possible external components and results in a simplified Bill of Materials (BOM).

## Table of Contents

# 1 Ordering Information

**Table 1 Ordering Information**

| Sales Part Number | Package Type | Standard Pack Form and Qty | | Orderable Part Number | Part Type |
|---|---|---|---|---|---|
| TDA38640A-aabb | QFN 5 mm x 6 mm | Tape and Reel | 5000 | TDA38640A0000AUMA1 | 40A Generic part – SVID controlled configuration |
| | QFN 5 mm x 6 mm | Tape and Reel | 5000 | TDA38640AaabbAUMA1 | 40A Custom part |

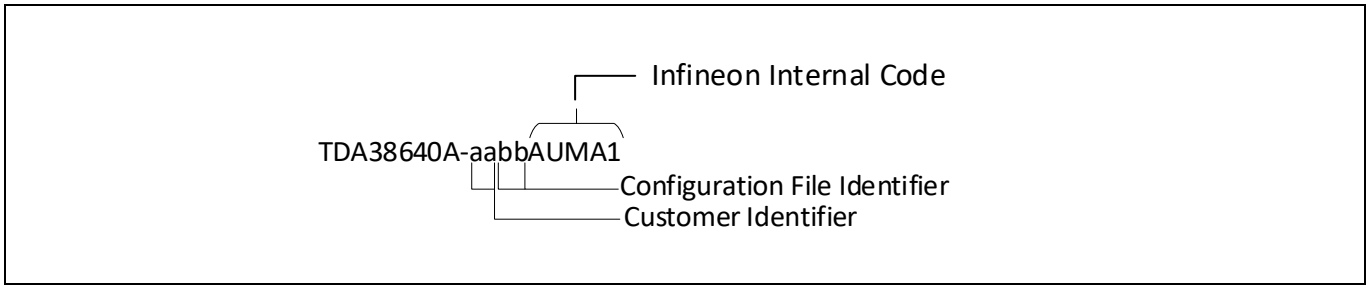



**Figure 1 Orderable Part Number Description**

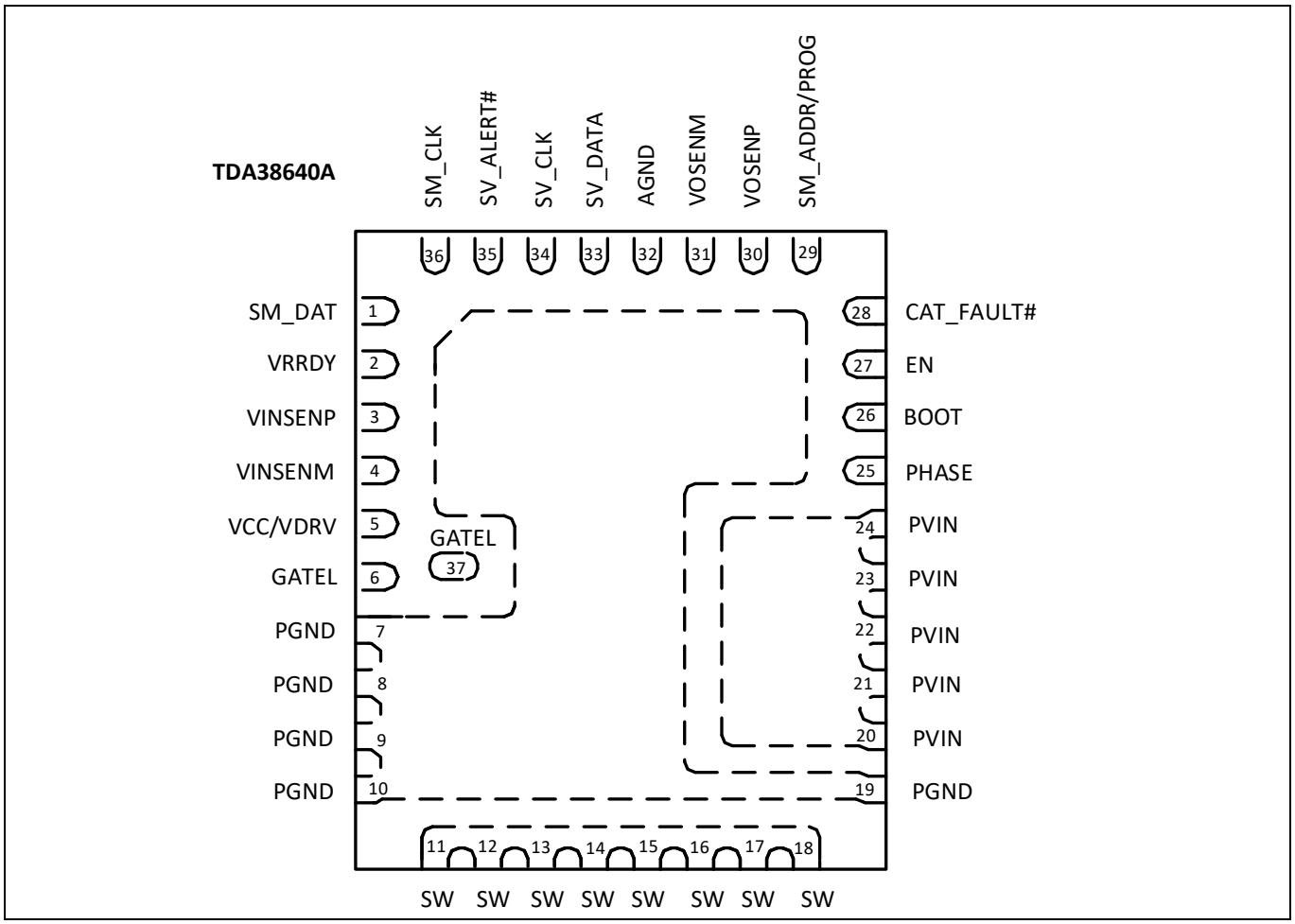



**Figure 2 Package Top View**

# 2 Functional Block Diagram

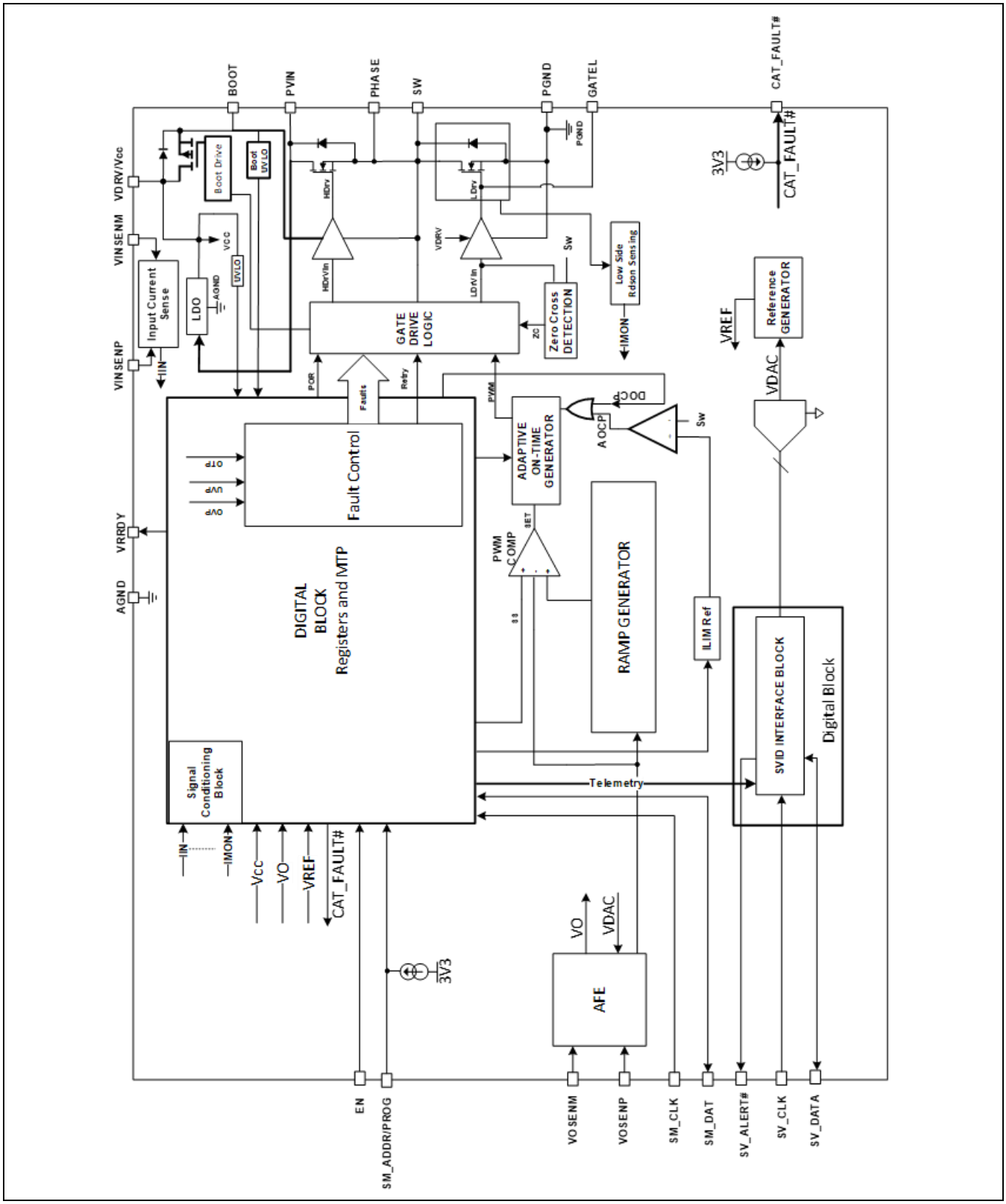



**Figure 3 Block Diagram**

# 3 Typical Application Diagram

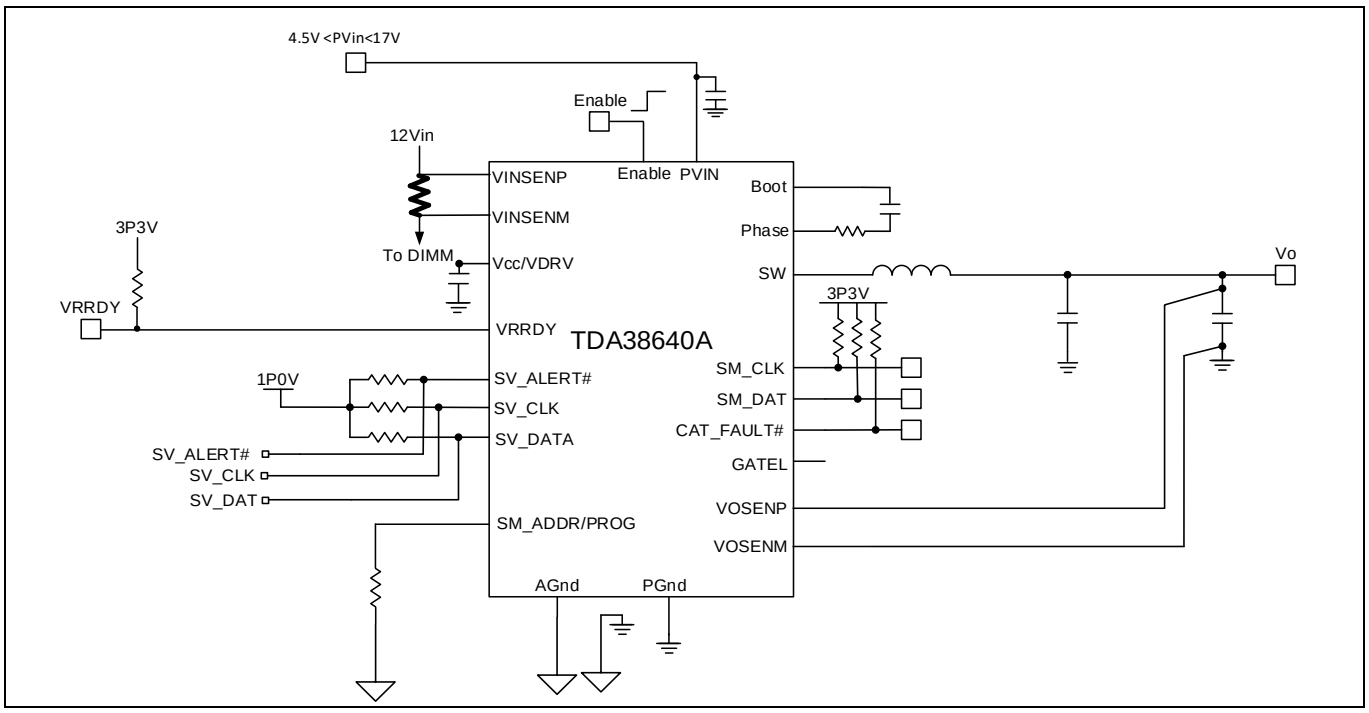



**Figure 4 TDA38640A Basic application circuit with Input Current Sense Enabled (0.25 V ≤ VID ≤ 2.56 V) in SVID Mode**

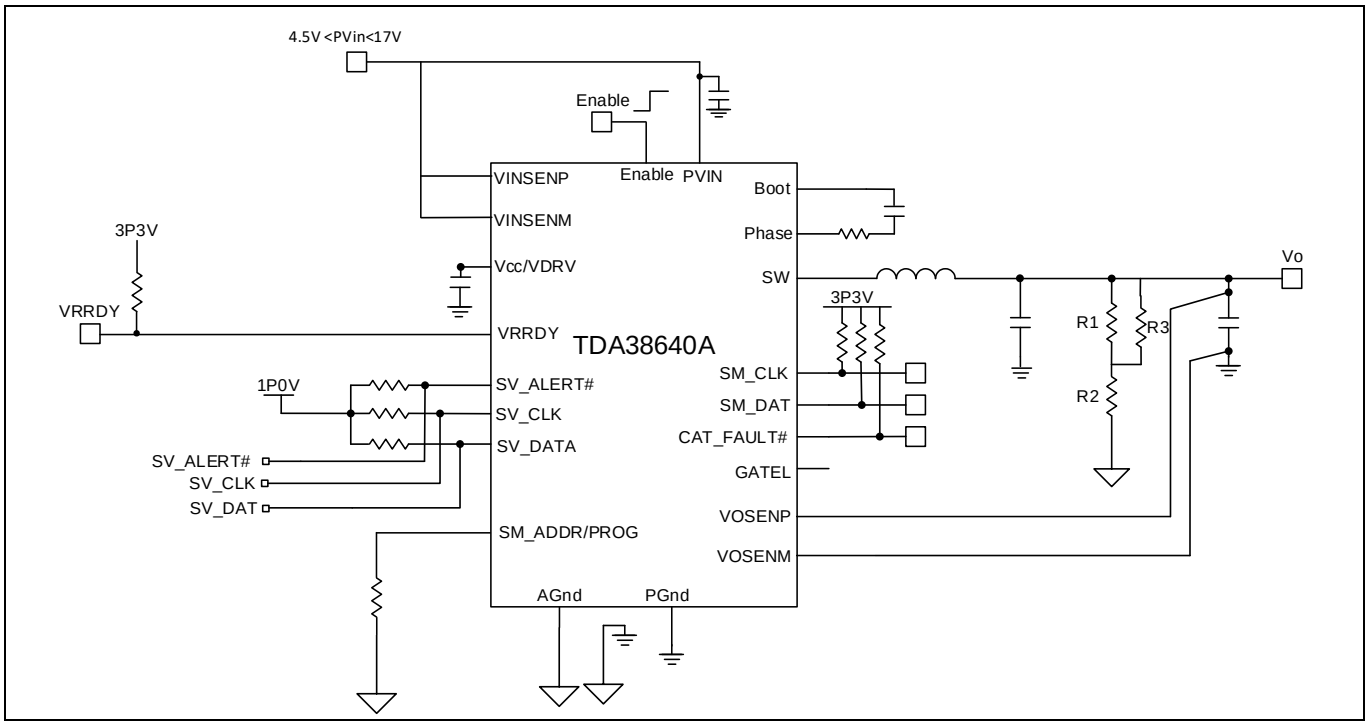



**Figure 5 TDA38640A Application Circuit with Input Current Sense Disabled, VOUT_SCALE_LOOP 1:2 (2.56 V ≤ VID ≤ 3.04 V) in SVID Mode**

# 4 Pin Descriptions

**Table 2 Pin Descriptions**

*Note:*

1. *A - Analog; D- Digital; [I]- INPUT; [O]- OUTPUT; [B]- BI-DIRECTIONAL; [P]- POWER*
2. *Refer to Section 13.9 for more details*

| Pin# | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | SM_DAT | D [B] | I2C bi-directional serial data line. Ground it if not used. |
| 2 | VRRDY | D [O] | Open-drain output that asserts high when the VR has completed soft-start to boot. Pull-up to an external voltage through a resistor. |
| 3 | VINSENP | A [I] | This pin connects to the positive side of the shunt resistor that is used to monitor the input current. Connect to PVIN if not used. |
| 4 | VINSENM | A [I] | This pin connects to the negative side of the shunt resistor that is used to monitor the input current. Connect to PVIN if not used. |
| 5 | Vcc/Vdrv | A [P] | Input bias for the external Vcc voltage and internal driver/output of the internal LDO. A 2.2 uF ceramic capacitor is recommended to use between Vcc and the analog ground (AGND). Connect to external Supply when internal LDO is not used. |
| 6, 37 | GATEL | A [O] | Gate of Low-side FET. The signal on this pin should be used for test purposes only and should not have external components connected to it. Leave it open if not used. |
| 7, 8, 9, 10, 19 | PGND | - | Power Ground. Should be connected to the system's power ground plane. PGND and AGND are internally connected via the lead frame. |
| 11, 12, 13, 14, 15, 16, 17, 18 | SW | A [O] | Switch Node. Connect these pins to an output inductor. |
| 20, 21, 22, 23, 24 | PVin | A [P] | Input supply for the power stage. |
| 25 | Phase | A [O] | Source of High-side FET. Connect a bootstrap capacitor between this pin and Boot pin. A high temperature (x7R) 0.1 uF or greater value ceramic capacitor is recommended. |
| 26 | Boot | A [I] | Supply voltage for the high side driver. Connect this pin to the Phase pin of the regulator through a bootstrap capacitor. For PVin above 14 V, a resistor is recommended in series with the bootstrap capacitor to control the slew rate of the SW node rising edge. |
| 27 | EN | A [I] | Enable pin to turn on and off the IC. Leave it open or ground it when not used. |
| 28 | CAT_FAULT# | D [O] | This is an Active Low open drain output that asserts when a catastrophic fault is detected. Leave it open when not used. |
| 29 | SM_ADDR/PROG | D [I] | I2C Slave Address. A resistor to ground on this pin; points to one of the unique 16 I2C slave devices[2] which needs to be addressed on the board, it does it by adding a fixed offset to |

## Pin Descriptions

| Pin# | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| | | | the I2C base address. The same resistor also defines the specific configuration file that will be loaded from the OTP during power-up. |
| 30 | VOSENP | A [I] | Direct sense output line connected after the switch node inductor. |
| 31 | VOSENM | A [I] | This pin provides the return connection for remote output voltage sensing. It is used as the internal reference voltage by the Analog Front End (AFE). |
| 32 | AGND | - | Signal ground for the internal circuitry. Connect it to the PGND power plane. |
| 33 | SV_DATA | D [B] | Serial VID Data I/O. This is a bi-directional serial line over which the CPU Master issues commands and receives data back. Leave the pin open or Ground it if not being used. |
| 34 | SV_CLK | D [I] | Serial VID Clock Input. Clock input driven by the CPU Master. Leave the pin open or Ground it if not being used. |
| 35 | SV_ALERT# | D [O] | Serial VID ALERT# (INTEL). SV ALERT# is pulled low by the controller to alert the CPU of VR 14/13/12/12.5 status. Leave the pin open if not being used. |
| 36 | SM_CLK | D [I] | Serial Clock Line Input. I2C clock input. The interface is rated to 1 MHz. Ground the pin if not being used. |

# 5 Absolute Maximum Ratings

Stresses higher than those mentioned in Table 3 below may result in permanent damage to the device. These are the absolute stress ratings only and the operation of the device is not recommended or implied at these or any other condition's in excess of those given in the recommended operating ratings in Table 5. Exposure of values over and above the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

**Table 3 Absolute Maximum Ratings**

| Description | Symbol | Values | | | Unit | Note/ Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power Input Voltage | $V_{PVIN}$ | -0.3 | - | 25 | V | Note 3, PVIN Pin |
| Positive Input-Current-Sense voltage | $V_{INSENP}$ | -0.3 | - | 25 | V | Note 3, VINSENP Pin |
| Enable voltage | $V_{EN}$ | -0.3 | - | 25 | V | EN Pin |
| PVIN-PHASE voltage | $V_{PVIN}$ -$V_{PHASE}$ | -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | PVIN-PHASE pin |
| PVIN-Switch Node voltage | $V_{PVIN}$ -$V_{SW}$ | -5 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | PVIN- SW Pin |
| Internal Driver voltage | $V_{DRV}$ | -0.3 | - | 6 | V | Note 3, VCC/VDRV Pin |
| Gate Low Pin voltage | $V_{GATEL}$ | -0.3 | - | 6 | V | GateL Pin |
| BOOT voltage | $V_{BOOT}$ | –0.3 V for 5 ns, -0.3 V dc | - | 29 V dc | V | BOOT Pin |
| | $V_{BOOT}$ - $V_{PHASE}$ | -0.3 | - | 7 V for 5 ns, 6 V dc | V | BOOT – PHASE Pin |
| Switch Node voltage | $V_{SW}$ | -7 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | Switch Node Pin |
| Phase Node voltage | $V_{PHASE}$ | -7 V for 5 ns, -0.3 V dc | - | 34 V for 1 ns, 25 V dc | V | Phase Pin |
| Address/PROG voltage | $V_{SM\_ADDR/PROG}$ | -0.3 | - | 3.6 | V | Note 3, SM_ADDR/PROG Pin |
| Output Positive Sense voltage | $V_{VOSENP}$ | -1.5 V for 5 ns, -0.3 V dc | - | 3.6 | V | Note 3, VOSENP Pin |
| Output Negative Sense voltage w.r.t AGND | $V_{VOSENM}$ | -0.3 | - | 0.3 | V | Note 3, VOSENM Pin |
| Voltage Regulator Ready voltage | $V_{VRRDY}$ | -0.3 | - | 3.6 | V | Note 3, VRRDY Pin |
| Power GND w.r.t Analog GND voltage | $V_{PGND}$- $V_{AGND}$ | -1.5 V for 5 ns , -0.3 dc | - | 1.5 V for 5 ns, 0.3 dc | V | PGND – AGND Pin |
| SVID CLK voltage | $V_{SV\_CLK}$ | -0.3 | - | 3.6 | V | SV_CLK Pin |
| SVID Data voltage | $V_{SV\_DAT}$ | -0.3 | - | 3.6 | V | SV_DAT Pin |
| SVID Alert voltage | $V_{SV\_ALERT\#}$ | -0.3 | - | 3.6 | V | SV_ALERT# Pin |

### Absolute Maximum Ratings

| Description | Symbol | Values | | | Unit | Note/ Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| SM CLK voltage | $V_{SM\_CLK}$ | -0.3 | - | 3.6 | V | SM_CLK Pin |
| SM Data voltage | $V_{SM\_DAT}$ | -0.3 | - | 3.6 | V | SM_DAT Pin |
| Catastrophic Fault voltage | $V_{CAT\_FAULT\#}$ | -0.3 | - | 3.6 | V | CAT_FAULT# Pin |
| Junction Temperature | $T_{Jmax}$ | -40 | - | 150 | °C | - |
| Storage Temperature | $T_{STORAGE}$ | -55 | - | 150 | °C | - |

*Note:*

*3. PGND and AGND pins are connected together*

***Attention: Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

# 6 Thermal Characteristics

**Table 4 Thermal Characteristics**

| Description | Symbol | Values | Test Conditions |
|---|---|---|---|
| Junction to Ambient Thermal Resistance | $\theta_{JA}$ | 19 °C/W | Note 4 |
| Junction to PCB Thermal Resistance | $\theta_{JC\text{-}PCB}$ | 1.1 °C/W | Note 5 |
| Junction to Case Top Thermal Resistance | $\theta_{JC}$ | 24 °C/W | |

*Note:*

4. *Thermal resistance is measured with components mounted on a standard EVAL_TDA38640A_1Vout demo board in free air*
5. *Thermal resistance is based on the board temperature near pin 22*

# 7 Electrical Specifications

**Table 5 Recommended Operating Conditions for Reliable Operation**

| Description | Min | Max | Unit | Note |
|---|---|---|---|---|
| PVin Voltage Range with External Vcc | 3 | 17 | V | Note 6, Note 7 |
| PVin Voltage Range with Internal LDO | 5 | 17 | V | Note 7 , Note 8 & Note 11 |
| Vcc Supply Voltage Range | 4.5 | 5.5 | V | Note 6 , Note 9 |
| Output Voltage Range | 0.25 | 3.04 | V | Note 10 |
| Continuous Output Current Range | | 40 | A | Note 11 |
| Switching Frequency (excluding 1600 kHz) | 400 | 2000 | kHz | Note 12 |
| Operating Junction Temperature | -40 | 125 | °C | |

*Note:*

6. *VCC/VDRV pin is connected to an external bias voltage for PVIN less than 5 V*
7. *A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage not exceeding absolute maximum dc and ac specs. Alternatively, a snubber can be used at SW node to reduce the SW node spike.*
8. *$PV_{in}$ with internal LDO is used. For single-rail applications with the internal LDO and $PV_{in}$ = 5 V-6 V, the internal LDO may enter dropout mode. AOCP limits can be reduced due to the lower VCC voltage.*
9. *The TDA38640A is designed to function with VCC down to 4.5 V, however, electrical specifications such as AOCP limits may be degraded.*
10. *The maximum output voltage is limited by the minimum off-time. For output voltages above 2.56 V, an external feedback resistor divider is needed. The limitation of 3.04 V is valid only in SVID mode, for PMBus mode this goes up to 5.12 V.*
11. *Refer to Section 14.1 for maximum output current rating at different ambient temperatures and OCP threshold tolerance.*
12. *The maximum LDO output current must be limited within 60 mA for operations requiring full operating temperature range of -40 °C ≤ $T_J$ ≤ 125 °C. Thermal De-rating may be needed at an elevated ambient temperature to ensure the junction temperature within the recommended operating range.*

## 7.1 Electrical Characteristics

Unless otherwise specified, these specifications apply over, 5 V ≤ PVin ≤ 17 V, in 0 °C < $T_J$ < 125 °C.
Typical values are specified at Ta = 25 °C.

**Table 6 Electrical Characteristics**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Stage** | | | | | | |
| Top Switch | $R_{ds(on)\_Top}$ | VBoot – Vsw = 5.0 V, IO = 35 A, Tj =25 °C | - | 2.9 | - | mΩ |
| Bottom Switch | $R_{ds(on)\_Bot}$ | Vcc = 5.0 V, IO = 35 A, Tj =25 °C | - | 1.0 | - | |
| Bootstrap Diode Forward Voltage | | I(Boot) = 25 mA | - | 780 | 950 | mV |
| SW Leakage Current | $I_{SW}$ | SW = 0 V, EN = 0 V | - | - | 175 | µA |
| | | SW = 0 V, EN = high, No Switching | - | - | 175 | |
| Dead Band Time | $T_{db}$ | SW Node rising edge, 40 A, Internal LDO, $T_j$=25 °C, Note 13 | - | 10 | - | ns |
| | | SW Node falling edge, 40 A, Internal LDO, Tj = 25 °C, Note 13 | - | 10 | - | |
| **Supply Voltage** | **PVin and External Vcc** | | | | | |
| PVin range (using external VCC = 5V) | | | - | 3 - 17 | - | V |
| External Vcc Range | | | 4.5 | 5 | 5.5 | V |
| **Supply Current** | **Iin** | | | | | |
| PVin Supply Current (standby, LDO) | $I_{in\ (Standby)}$ | EN = Low, No Switching | - | 12 | - | mA |
| PVin Supply Current (dynamic, LDO) | $I_{in\ (Dyn)}$ | EN=High, $F_{sw}$= 800 kHz, PVIN = 12 V, Vout = 1.1 V, Note 13 | - | 48 | - | mA |
| **Digital Inputs** | **VR_ENx (Intel)** | | | | | |
| Input High Voltage | | | 0.70 | - | - | V |
| Input Low Voltage | | | - | - | 0.50 | V |
| Input Impedance | | | - | 1 | - | MΩ |
| **Digital Inputs** | **SV_CLK, SV_DAT** | | | | | |
| Input High Voltage | | | 0.65 | - | - | V |
| Input Low Voltage | | | - | - | 0.45 | V |
| Hysteresis | | | - | 95 | - | mV |
| Input Leakage Current | | SV_CLK = 3.6 V | -1 | - | 1 | µA |
| Pin Capacitance | | See Note 13 | - | - | 4 | pF |
| **Digital Inputs - LVTTL** | **SM_DAT, SM_CLK** | | | | | |
| Input High Voltage | | | 2.31 | - | - | V |

## Electrical Specifications

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Low Voltage | | | - | - | 0.99 | V |
| Input Leakage Current | | SM_CLK = 3.6 V | -1 | - | 1 | µA |
| Pin Capacitance | | See Note 13 | - | - | 4 | pF |
| On Resistance | | I = 20 mA | 4 | - | 13 | Ω |
| **Remote Voltage Sense Inputs** | **VOSENP, VOSENM** | | | | | |
| VOSENP Input Current | | VOSENP = 3.6 V | - | - | 230 | µA |
| | | VOSENP = -0.3 V | -85 | - | - | µA |
| VOSENM Input Current | | VOSENM = 0.3 V | -155 | - | - | µA |
| | | VOSENM = -0.3 V | -200 | - | - | µA |
| Differential Input Voltage Range | | | - | - | 2.56 | V |
| VOSENM Input CM Voltage | | | - | ±300 | - | mV |
| **Input Current Sense Input** | **VINSENP, VINSENM** | | | | | |
| VINSENP Input current | | | - | 200 | - | µA |
| VINSEM Input Current | | | - | - | 5 | µA |
| **Analog Address/Level Inputs** | **SM_ADDR/PROG** | | | | | |
| Output Current | | | - | 15 | - | µA |
| **Open-Drain Outputs–20mA Drive** | **VRRDYx, CAT_FAULT#** | | | | | |
| Output Low Voltage | | I = 20 mA | - | - | 0.3 | V |
| Output Leakage | | $V_{VRRDY}$ = 3.6 V | -5 | - | 5 | µA |
| **Open-Drain Outputs-20mA Drive** | **SV_DAT,SV_ALERT#, SM_DAT** | | | | | |
| Output Low Voltage | | I = 20 mA | - | - | 0.26 | V |
| On Resistance | | I = 20 mA | 4 | - | 13 | Ω |
| Tri-State Leakage | | | -5 | - | 5 | µA |
| **On-Time Timer** | | | | | | |
| Frequency Range (programmable) | | Excluding 1600 kHz and in steps of 200 kHz | 400 | -- | 2000 | kHz |
| Minimum On-Time | | Tj=25 °C, Note 13, PVIN = 12 V, Vo = 0 V, See Note 15 | - | 25 | - | ns |
| Minimum Off-Time | Toff (Min) | Tj=25 °C, VFB=0 V, See Note 13 | - | 150 | - | ns |
| **System Set Point Accuracy (5 mV and 10 mV step mode voltage)** | | | | | | |
| VBOOT Voltage Range | | | Meets Spec | | | V |
| 0.25 V ≤ VID ≤ 0.795 V | | -40 °C ≤ $T_J$ ≤ 125 °C | - | ±10 | - | mV |
| 0.8 V ≤ VID ≤ 0.995 V | | VDD > VID + 200 mV | - | ±8 | - | mV |
| 1.0 V ≤ VID ≤ 2.52 V | | Typ = 3σ, Note 13 & 14 | - | ±1 | - | %VID |
| **VCC LDO Output** | **Vcc** | | | | | |
| Vcc Output Voltage | Vcc | 5.5 V ≤ PVIN ≤ 17 V, when Icc = 50 mA, Cload = 2.2 uF, $T_j$=25 °C | 4.7 | 5.0 | 5.3 | V |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VCC Dropout | Vcc_drop | PVIN = 4.5 V, Icc = 50 mA, Cload = 2.2 uF, $T_j$ = 25 °C | - | 650 | - | mV |
| **Under Voltage Lockout** | | | | | | |
| Vcc_Good Start Threshold | VCC_UVLO_Start | Vcc Rising Trip Level | 3.8 | - | 4.2 | V |
| Vcc_Good Stop Threshold | VCC_UVLO_Stop | Vcc Falling Trip Level | 3.6 | - | 4.0 | |
| Enable-Start-Threshold | Enable_UVLO_Start | ramping up | 0.61 | 0.65 | 0.69 | V |
| Enable-Stop-Threshold | Enable_UVLO_Stop | ramping down | 0.51 | 0.55 | 0.59 | |
| Boot Rising Threshold | BOOT_UVLO_Rising | Boot-Phase Ramping up, Note 13 | 3.7 | 3.85 | 4.0 | V |
| Boot Falling Threshold | BOOT_UVLO_Falling | Boot-Phase Ramping down, Note 13 | 3.5 | 3.65 | 3.8 | V |
| **IMON Reporting Accuracy** | | | | | | |
| IMON Accuracy TDA38640A (40 A) | Imon | Maximum load | - | ±6 | - | % |
| **Over Current Limit** | | | | | | |
| Current Limit Threshold (Valley Current) | $I_{oc}$ | Tj = 25 °C, Vcc = 5.0V | - | 10 | - | A |
| | | | - | 15 | - | |
| | | | - | 20 | - | |
| | | | - | 25 | - | |
| | | | - | 30 | - | |
| | | | - | 40 | - | |
| | | | - | 50 | - | |
| | | | - | 60 | - | |
| Current Limit Threshold Accuracy | | See Note 13 | - | ± 20 | - | % |
| **Over Voltage Protection** | | | | | | |
| | | VID Rising | - | 0.8 | - | V |
| | | | - | 1.0 | - | |
| | | | - | 1.2 | - | |
| | | | - | 1.35 | - | |
| | | | - | 1.5 | - | |
| | | | - | 1.8 | - | |
| | | | - | 2.2 | - | |
| | | | - | 2.85 | - | |
| Output Fixed OVP Threshold Accuracy | | See Note 13 | - | ±5 | - | % |
| Output Relative OVP Threshold (programmable) | | Relative to VID in steps of 50 mV in VOUT_SCALE_LOOP 1:1 mode | 50 | - | 400 | mV |
| Output Relative OVP Threshold Accuracy | | Relative to VID in steps in VOUT_SCALE_LOOP 1:1 mode | - | ± 50 | - | mV |
| **Under Voltage Protection** | | | | | | |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Relative UVP Threshold (programmable) | UVP_Vth | Relative to VID in steps of 50 mV in VOUT_SCALE_LOOP 1:1 mode | 50 | - | 400 | mV |
| Output Relative UVP Threshold Accuracy | | Relative to VID in steps; in VOUT_SCALE_LOOP 1:1 mode | - | ± 50 | - | mV |
| **I2C and Reporting** | | | | | | |
| Bus Speed | | Normal | - | 100 | - | kHz |
| | | Fast | - | 400 | - | kHz |
| | | High-Speed | - | 1000 | - | kHz |
| Output Voltage Resolution | | Note 15 and 16 | - | 0.625, 0.977, 1.953, 3.906 | - | mV |
| Output Voltage Filter Rate | | | - | 8 | - | kHz |
| Output Voltage Update Rate | | | - | 379 | - | kHz |
| Highest Reported Vout | | VOUT_SCALE_LOOP =1:1 | - | - | 2.56 | V |
| Vout Reporting Accuracy | | -40 °C - 125 °C (Tj), 4.5 V < Vcc < 5.5 V, 0.25 ≤ VID ≤ 0.5; VOUT_SCALE_LOOP in 1:1 mode | -2 | - | 2 | % |
| | | -40 °C - 125 °C (Tj), 4.5 V < Vcc < 5.5 V, 0.5<VID ≤ 2.52; VOUT_SCALE_LOOP in 1:1 mode | -1 | - | 1 | % |
| Iout Resolution | | | - | 0.0625 | - | A |
| Iout Filter Rate | | | - | 8 | - | kHz |
| Iout Update Rate | | | - | 379 | - | kHz |
| Iout Digital Monitoring Range | | | - | | 64 | A |
| Iout Reporting Accuracy (PMBus) | | 0 °C-125 °C, 4.5V<Vcc<5.5V 0 A ≤ Iout ≤ 40 A 0.25 V ≤ Vout ≤ 2.52 V, Note 15 | - | ±6 | - | % |
| Temperature Resolution | | | - | 1 | - | °C |
| Temperature Filter Rate | | | - | 4 | - | kHz |
| Temperature Update Rate | | | - | 189 | - | kHz |
| Temperature Monitoring Range | | | -40 | - | 125 | °C |
| Temperature Reporting Accuracy | | See Note 13 | - | ±1 | - | °C |
| Thermal Shutdown | | See Note 13 | - | 140 | - | °C |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Shutdown Hysteresis | | See Note 13 | - | 20 | - | ℃ |
| Input Power Resolution | | | - | 0.5 | - | W |
| Input Power Reporting Range | | | - | - | 1024 | W |
| Input Power Filter Rate | | | - | 8 | - | kHz |
| Input Power Update Rate | | | - | 379 | - | kHz |
| Input Power Accuracy | | A 4-terminal 1 mΩ (1 % accurate) shunt is used, Note 15 | - | ±3 | - | % |

*Note:*

13. *Guaranteed by design and not tested in production*
14. *Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*
15. *Guaranteed by Bench Characterization at Room Temperature and not tested in production*
16. *Actual output is limited by the resolution of the internal DAC*

# 8 Typical Efficiency and Power Loss Curves

## 8.1 $PV_{in}$ = 12 V, $F_{sw}$ = Varying

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate efficiency and dashed lines are showing power loss.

**Table 7 Inductors for PVin=12 V, Fs = varying**

| Vout (V) | Lout (nH) | P/N | Frequency(kHz) | DCR (mΩ) | Inductor Size (mm³) |
|---|---|---|---|---|---|
| 1.1 (Ext. Vcc) | 100 | L101247A-100L | 600 | 0.125 | 10 x 6.4 x 12 |
| | | | 800 | | |
| | | | 1000 | | |

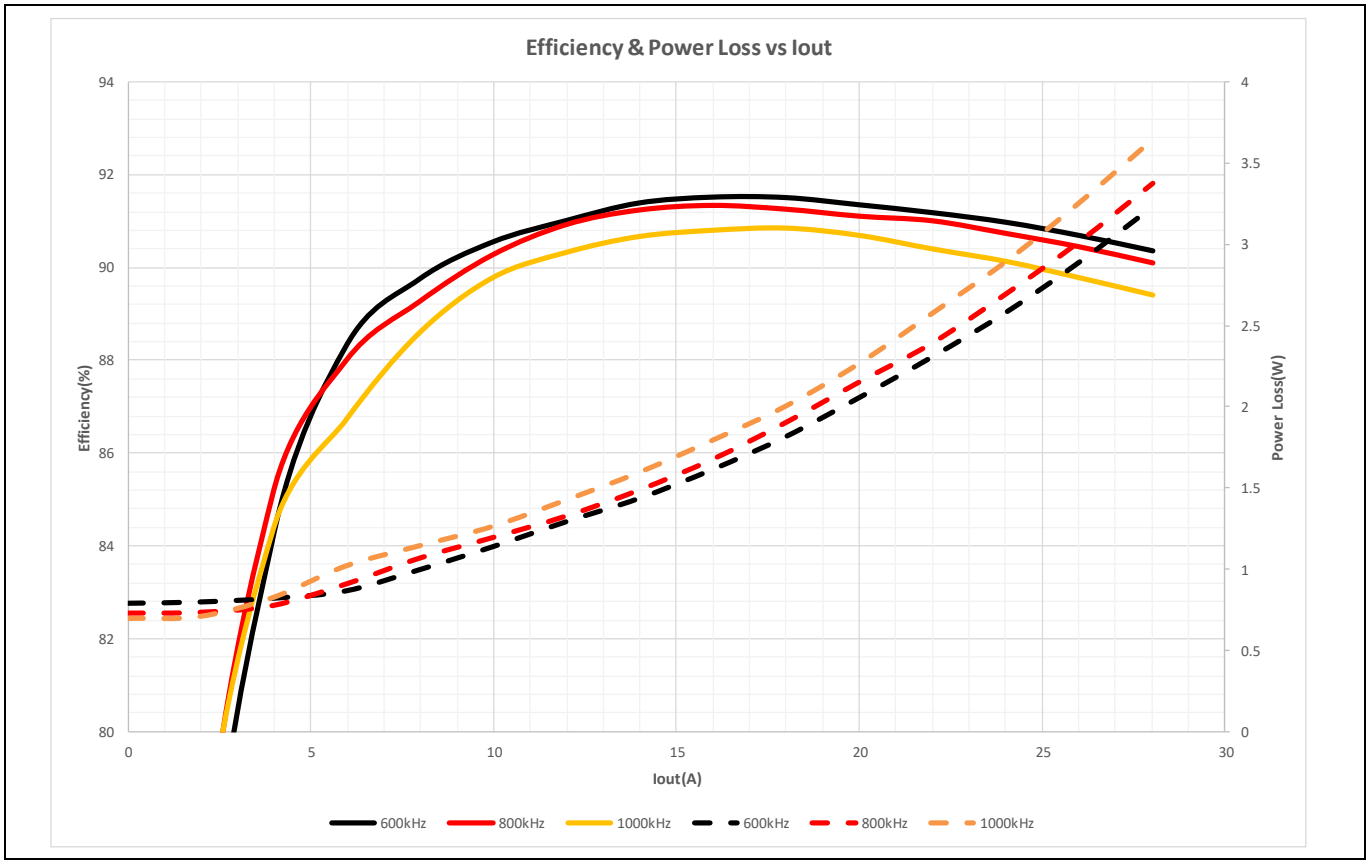



**Figure 6 Typical efficiency and power loss curves, $PV_{in}$ = 12 V, $F_{sw}$ = Varying**

## 8.2 $PV_{in}$ = 12 V, $F_{sw}$ = 800 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate efficiency and dashed lines are showing power loss.

**Table 8 Inductors for PVin=12 V, Fsw = 800 kHz**

| Vout (V) | Lout (nH) | P/N | Frequency(kHz) | DCR (mΩ) | Inductor Size (mm³) |
|---|---|---|---|---|---|
| 1.1 (Ext. Vcc) | 100 | L101247A-100L | 800 | 0.125 | 10 x 6.4 x 12 |
| 1.1 (Int. Vcc) | | | | | |

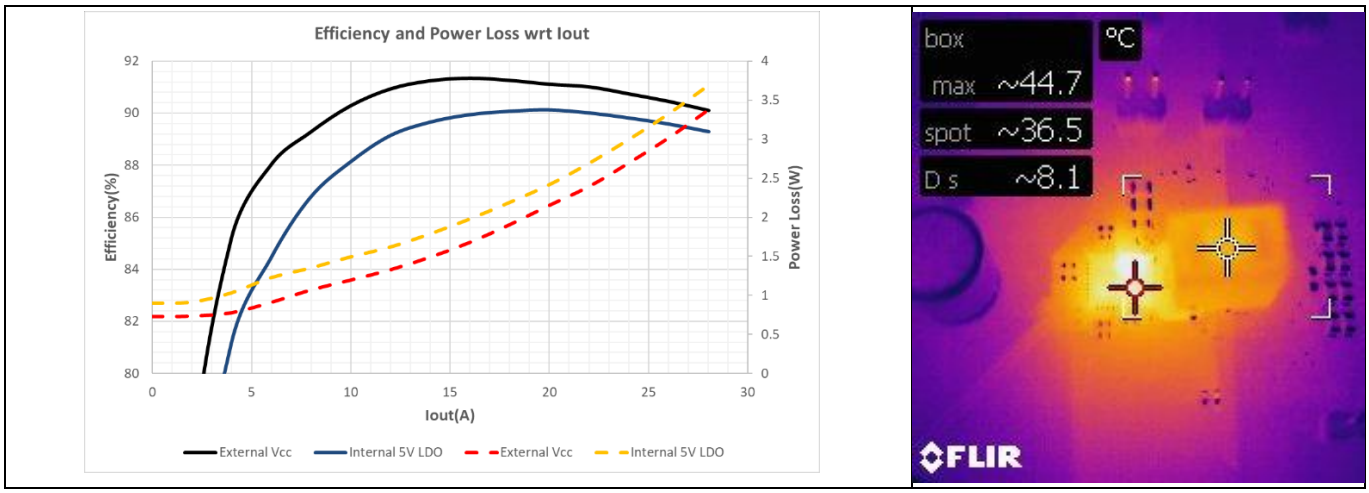



**Figure 7 Typical efficiency & power loss curve plus thermal image at full load of 28 A with Internal LDO, $PV_{in}$ = 12 V, $F_{sw}$ = 800 kHz**

## 8.3 $PV_{in}$ = Varying, $F_{sw}$ = 1000 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate efficiency and dashed lines are showing power loss.

**Table 9 Inductors for PVin=Varying, Fsw = 1000 kHz**

| Vout (V) | Lout (nH) | P/N | PVIN(V) | DCR (mΩ) | Inductor Size (mm³) |
|---|---|---|---|---|---|
| 1.1 (Int. Vcc) | 100 | L101247A-100L | 10.8 | 0.125 | 10 x 6.4 x 12 |
| | | | 12 | | |
| | | | 13.2 | | |

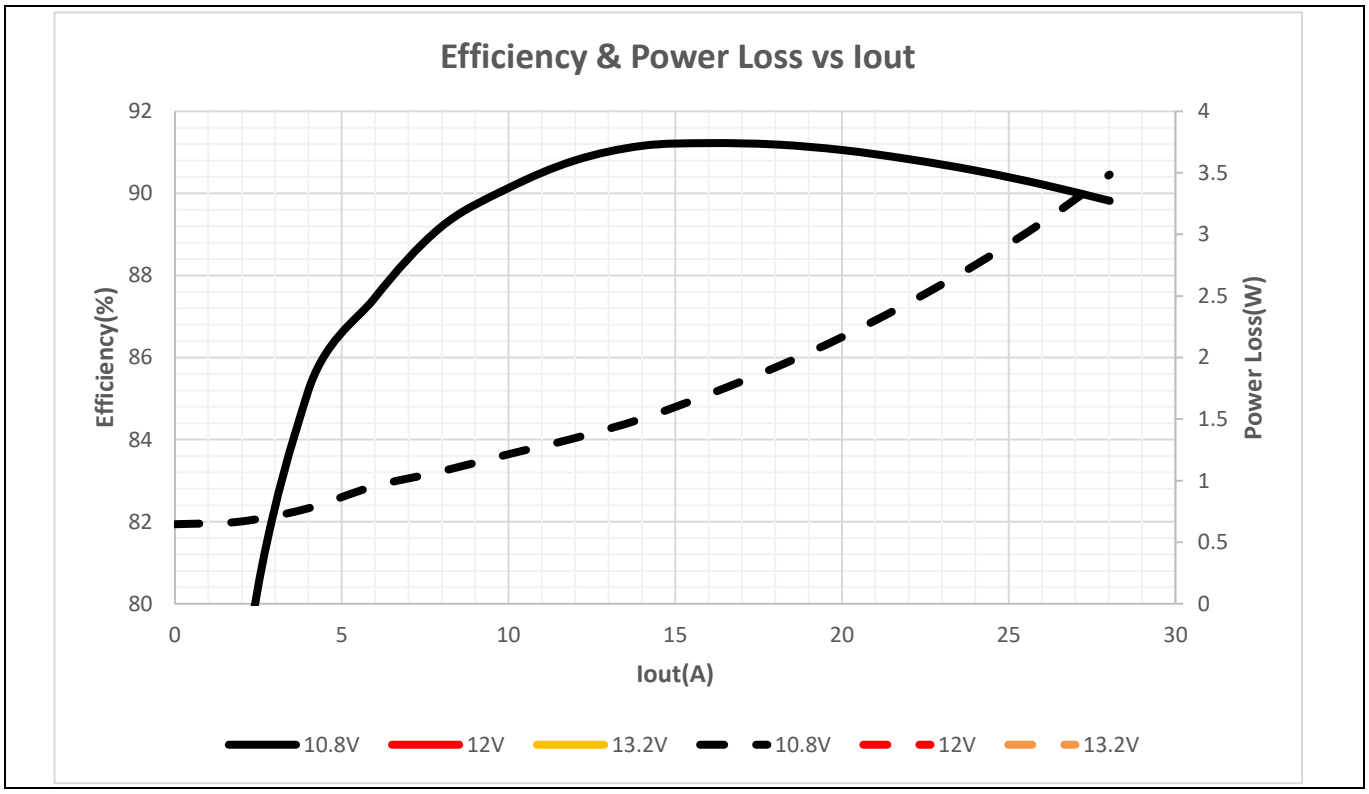



**Figure 8 Typical efficiency and power loss curves, $PV_{in}$ = Varying, $F_{sw}$ = 1000 kHz**

# 9 Thermal De-rating curves

This test is done on a DB356 Rev 2 Evaluation Board for TDA38640A. It is an 8-layer board with 1 oz inner Cu layers and 2 oz on the top and bottom layer. FR4 material and the size of the eval board is 105 mm x 133 mm.

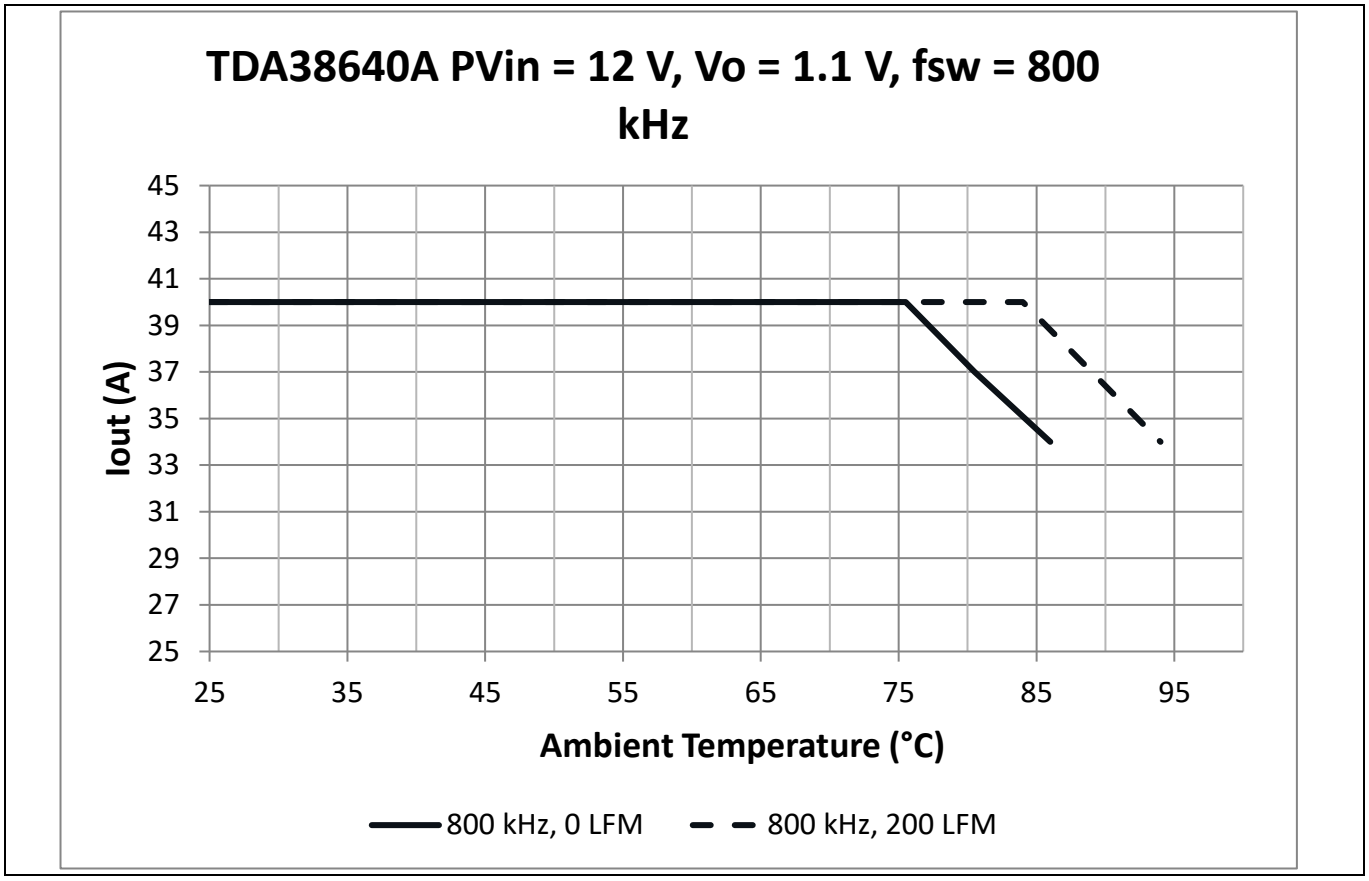



**Figure 9 Thermal de-rating curves, $PV_{in}$ = 12 V, $V_{out}$=1.1 V, $f_{sw}$ = 800 kHz, VCC = Internal LDO**

# 10 $R_{DS(on)}$ of MOSFET Over Temperature

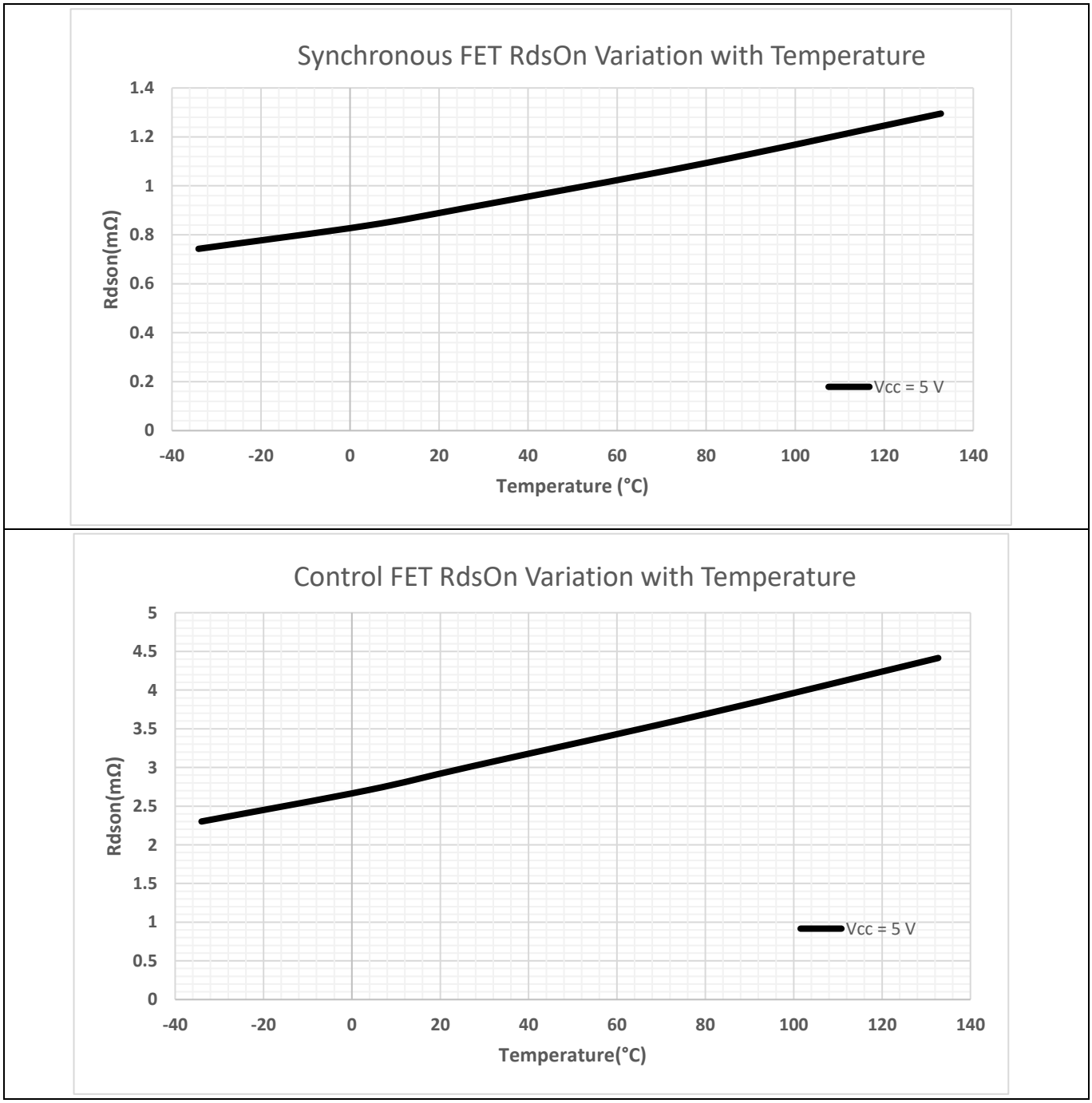
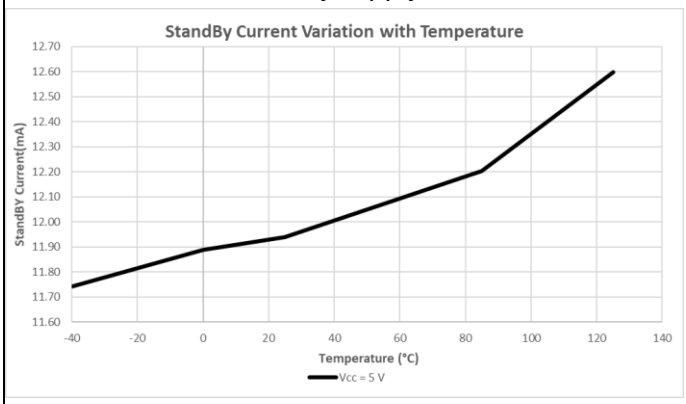


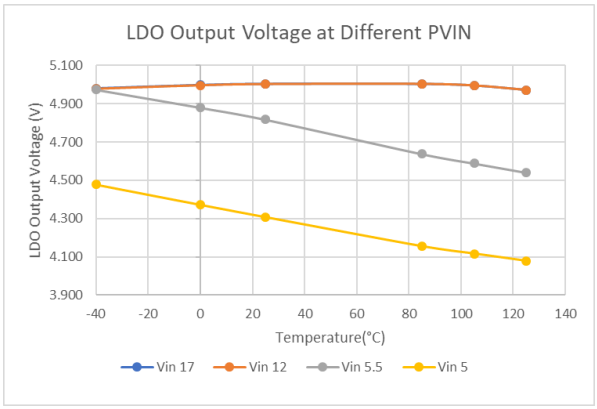

**Figure 10 RDS(on) of MOSFETs over Junction Temperature**

# 11 Typical operating characteristics (-40 °C ≤ $T_j$ ≤ +125 °C)

PVIN standby supply current




LDO output voltage, Icc = 60 mA




Enable Start and Stop Thresholds

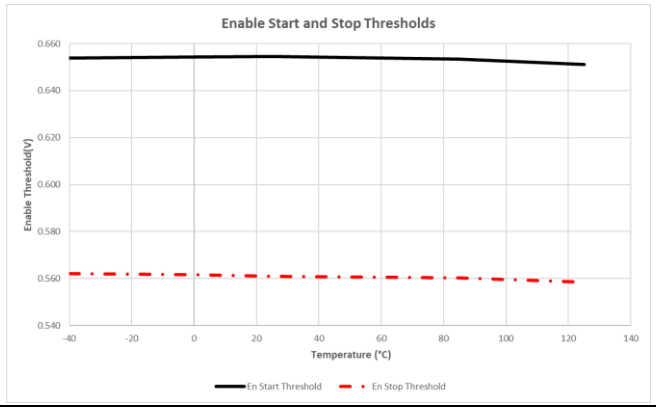



**Figure 11 Typical operating characteristics (set 1 of 2)**

## Typical operating characteristics (-40 C ≤ Tj ≤ +125 C)

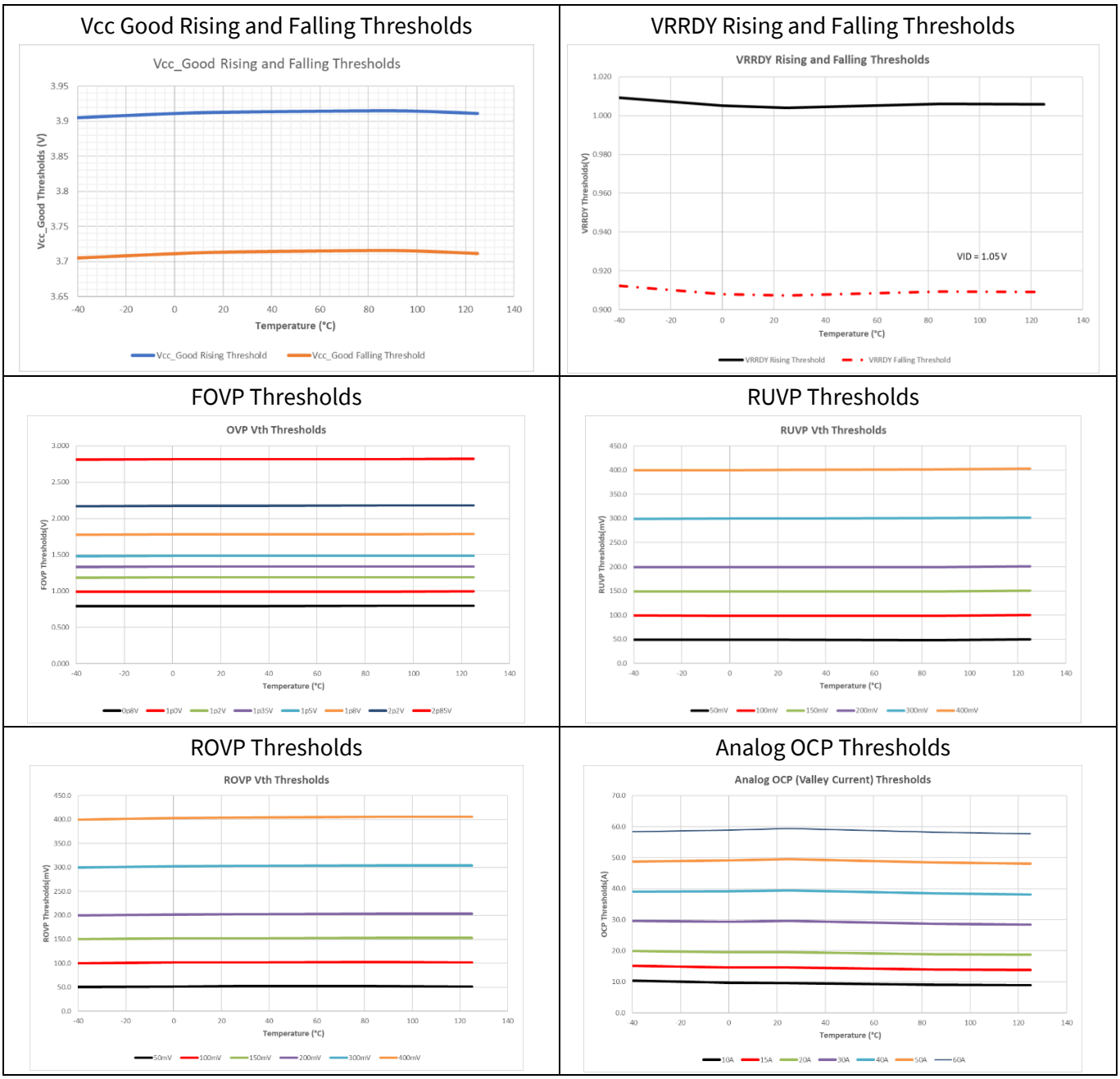



**Figure 12 Typical operating characteristics (set 2 of 2)**

# 12 General Description

The TDA38640A is an easy-to-use, fully integrated, and highly efficient dc-dc regulator optimized to convert a 12 V input supply to a voltage level required by high performance microprocessors and DDR memory. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38640A a small footprint solution, providing high-efficient power delivery. Using a fast Constant On-Time (COT) control scheme simplifies the design efforts and achieves fast control response. The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the on-chip memory.

## 12.1 Intel Operating Mode

The TDA38640A can be used for Intel® VR12, VR 12.5, VR13, VR14, IMPVP8 designs and DDR Memory without significant changes to the Bill of Materials (BOM). The required mode is selected in MTP and the pin-out, VID table and other relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory different PWM controllers.

## 12.2 PMBUS Operating Mode

The TDA38640A can be used in PMBUS mode. The required mode is selected in MTP using GUI using the register 0x44[15]. In PMBUS mode, the output voltage is controlled by the PMBUS VOUT_COMMAND command. The VOUT_COMMAND resolution can be set to 0.625 mV/lsb, 0.977 mV/lsb, 1.953 mV/lsb, or 3.906 mV/lsb. The output DAC resolution is 1.25 mV/lsb. The resolution is user-programmable via a configuration file. See Table 20 for a full list of all supported PMBUS commands. Please refer to App Note AN_2203_PL12_2204_184108 for more information.

## 12.3 Multiple Time Programming Memory

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Check (CRC) validation on each power up. The controller will not start up in the event of a CRC error.

The TDA38640A-xxxx allows up to 13 unique configurations to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. In addition, the TDA38640A also allows loading of multi-image (up to 13 consecutive) configuration files and automatic selection of a unique file after power-up based on the resistor value at the SM-ADDR/PROG pin and the pointer (0x0000[13:8]). There are registers available in the CNFG section of the register map which allow the user the capability to set the starting point for a multi-image (register 0x0000[13:8]) and number of images as part of the multi-image config file (register 0x0000[3:0]). TDA38640A can be programmed successfully for an application up to 13 times for a single image config file. Please refer to AN_2308_PL12_2308_163442 Programming Guide v1.1 for details on programming the part.

The user still has access to all the possible I2C slave addresses by setting the address through address registers This requires the address offset capability of the SM_ADDR/PROG pin to be disabled by setting the bit 0x42[6] to 1. Thus, the base address register 0x40[14:8] for I2C and 0x40[6:0] for PMBus will represent the effective slave address for the device. In this case the SM_ADDR/PROG effectively becomes just the PROG pin used for selecting the correct config file for an application. For example, for an effective 7-bit I2C address of 14h the register 0x40[14:8] should be set to 14h. The second method for choosing the effective slave address is using the base address in register 0x40 and adding the offset selected by the SM_ADDR/PROG pin. The pin configuration limits the offset capability available for an application, as shown in Table 13.

## 12.4 Voltage Sense

Inorder to obtain output voltages in the range of 2.56V to 3.04V, an external feedback resistor divider is needed and needs to operate in VOUT_SCALE_LOOP 1:2 mode. In applications that require high Vout set point accuracy, a resistor in parallel to top resistor of the divider need to be connected as shown in Figure 5. The Value of the resistor is calculated as follows:

$$\text{Rtop} = \frac{\text{Vo}-\text{Vfb}}{\left(\frac{\text{Vfb}}{\text{R2}}+\frac{\text{Vfb}}{13570}-\frac{1.2}{20000}\right)}$$

Where
R1 is the top resistor of the divider
R2 is the bottom resistor of the divider
Req= Effective value of R1 and R3 in parallel
Vo=Target Output Voltage
Vfb= VOSENSP = Vo/2
R1, R2=499 Ohms (recommended)

$$\text{R3} = \frac{\text{R1xReq}}{\text{R1}-\text{Req}}$$

For given feedback resistor values Vout is calculated as follows:

$$\text{Vout} = \text{Vfb}\left(1+\frac{\text{Req}}{\text{R2}}+\frac{\text{Req}}{13570}\right)-1.2\text{x}\frac{\text{Req}}{20000}$$

Suggested values of R1 anf R3 are as follows:

| Target Vout (V) | R1, R2 (Ohms) | R3 (kOhms) |
|---|---|---|
| 2.56 | 499 | 37.4 |
| 3.04 | 499 | 29.1 |

## 12.5 I2C & PMBus Interface

An I2C or PMBus interface is used to communicate with the TDA38640A. This two-wire serial interface consists of clock and data signals and operates as fast as 1 MHz. The bus provides read & write access to the internal registers for configuration, and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, a base address for TDA38640A is programmed into the MTP. The unique slave address for the device is a combination of the base address in the device register plus the offset generated by the SM_ADDR/PROG pin (depending on the resistor value connected to the pin). Alternatively, this can be achieved by programming the effective I2C address into the base address register and disabling the SM_ADDR/PROG pin offset functionality via bit 0x42[6] in the USER section.

To protect customer configuration and information, the I2C and PMBus interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers.

Refer to the PMBus Command Codes in Table 20 for more information. One can access the non-PMBus registers (I2C register) via the MFR_REG_ACCESS(D0h) PMBus Command. More information is available in the PMBus Commands document. Setting the base address for PMBus, 0x40[6:0], to zero disables the PMBus interface. If the

I2C base address, 0x40[14:8], register is set to 0, the device is forced into test mode. All registers at this address are protected by the i2c_pmb_addr_lock register 0xD4[2]. Please refer to the App note AN_2203_PL12_2204_210835 for more information on the register map.

## 12.6 Infineon XDP Designer GUI

The Infineon XDP Designer GUI provides the designer with a comprehensive design environment that includes input settings, output settings, telemetry, PMBus interface, and SVID settings. With these tools, a designer can monitor and set real-time system configuration settings for fault thresholds and output behavior. The XDP Designer GUI allows real-time design monitoring of key parameters such as output current and power, input current and power, efficiency, temperature, and faults. Figure 13 and Figure 14 show the GUI home screen and design tools with the available parameter windows. The GUI is available to download from Infineon website as part of the Toolbox utility.

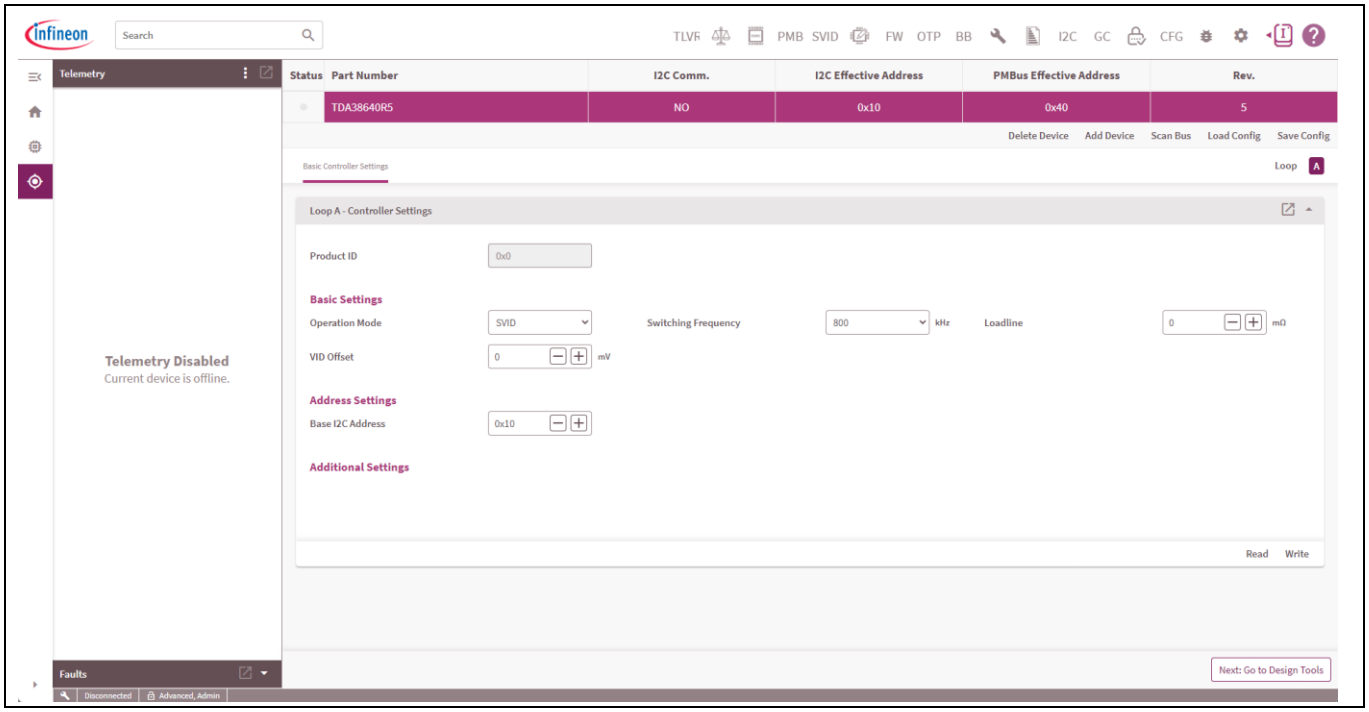



**Figure 13 Snapshot of the XDP Designer GUI Home screen for TDA38640A working in Offline Mode**

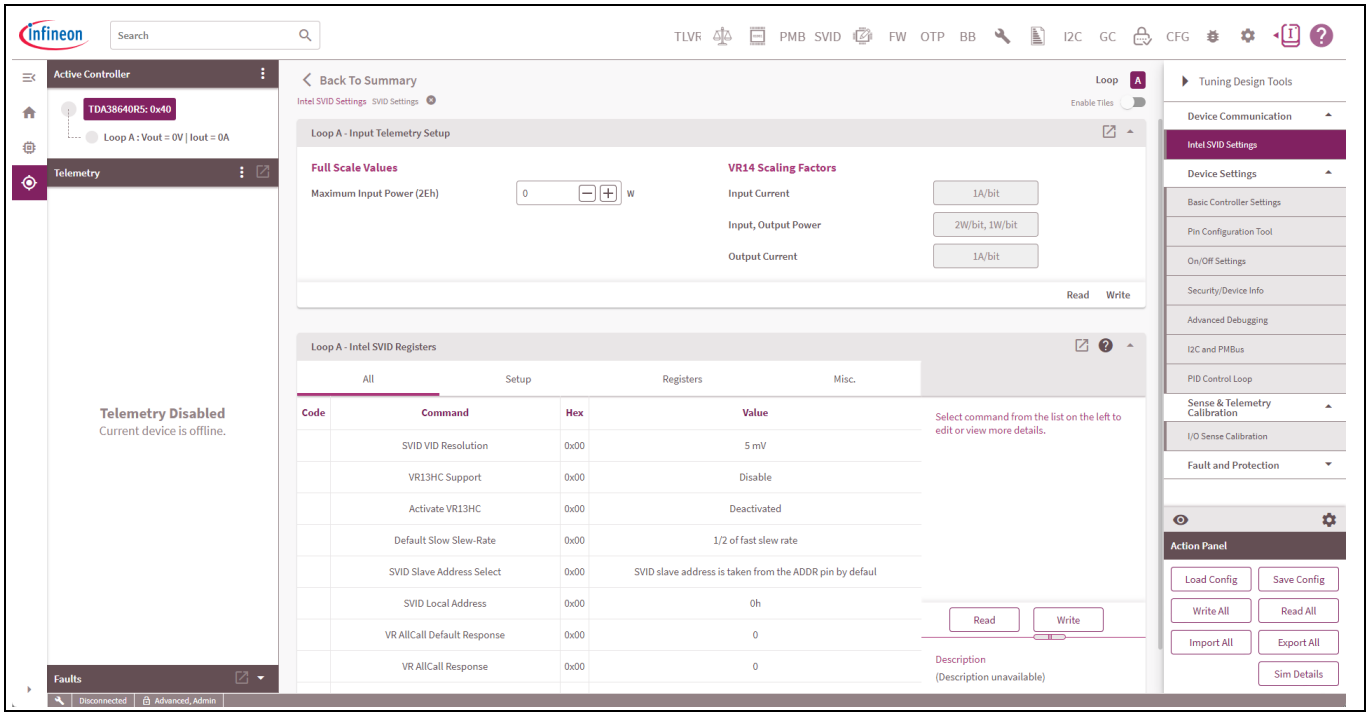



**Figure 14 Snapshot of the XDP Designer GUI Design Tools for TDA38640A working in Offline Mode**

## 12.7 Programming

Once a design is complete, the XDP Designer GUI produces a configuration file. These configurations files can be saved and loaded. Infineon does not recommend loading a new config file and programming the device while the device is operating to produce an output voltage. Please refer to programming guide AN_2204_PL12_2308_163442 for more details.

## 12.8 Real-time Monitoring

The TDA38640A can be accessed through the use of PMBus Command codes (described in Table 20), to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power and temperature of the IC.

# 13 Theory of Operation

## 13.1 Start up Configuration

TDA48640A operation is controlled by OTP configuration stored in NVM, then loaded into working registers during initialization.

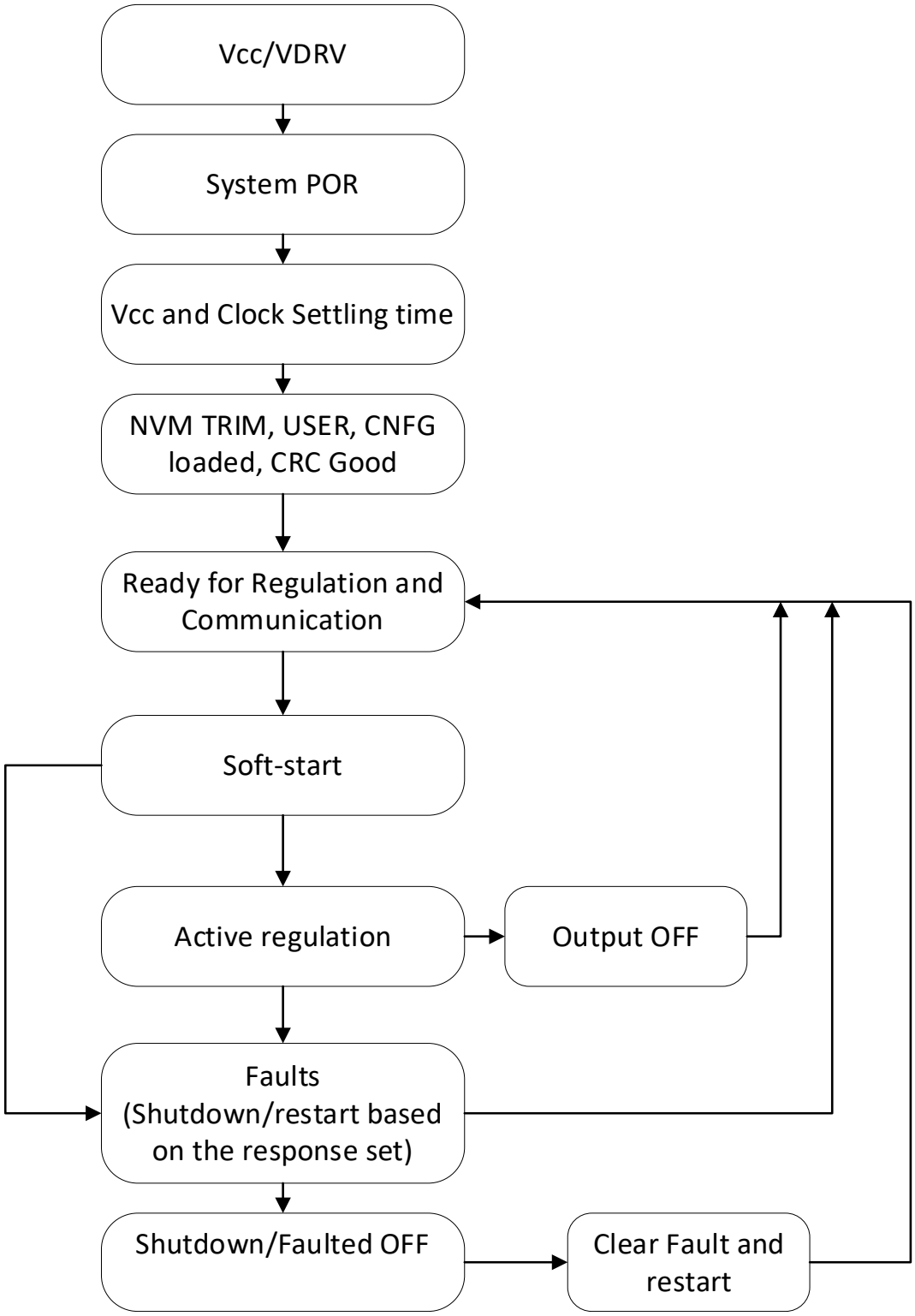



**Figure 15 State Machine**

### 13.1.1 Power on and Initialization

The on-chip regulator operates from the Vcc/VDRV and generates an internal +1.2 V voltage. TDA38640A operation is initialized by an internal threshold-based power-on reset circuit. To ensure no sensitive analog measurements is executed prior to Vcc/VDRV supply is settled, the controller provides a delay which extends the “System POR” state between power-on reset and entering the NVM Load state. This delay is used to ensure internal analog circuitry settles before making any precision measurements. After this, Trim and Config images are loaded from NVM to working registers. While waiting for the Trims to take effect, current sources are enabled at all pins that have external resistors (SM_ADDR/PROG). The resulting voltages are read through the low-speed ADC and latched. If Trim and Config CRC matches, User configuration is loaded from NVM to the working registers CRC check is carried out to validate the data in these registers. If the calculated CRC does not match the CRC stored in the NVM, CRC error is flagged and next sequences in ther start up are terminated. If there is a CRC match, the part continues with the start up sequence. The device starts switching once part is ready for regulation and communication and enable signal is pulled high. When the contents of the NVM are being loaded into the working registers the PWM outputs are held in high impedance (Hi-Z) state.

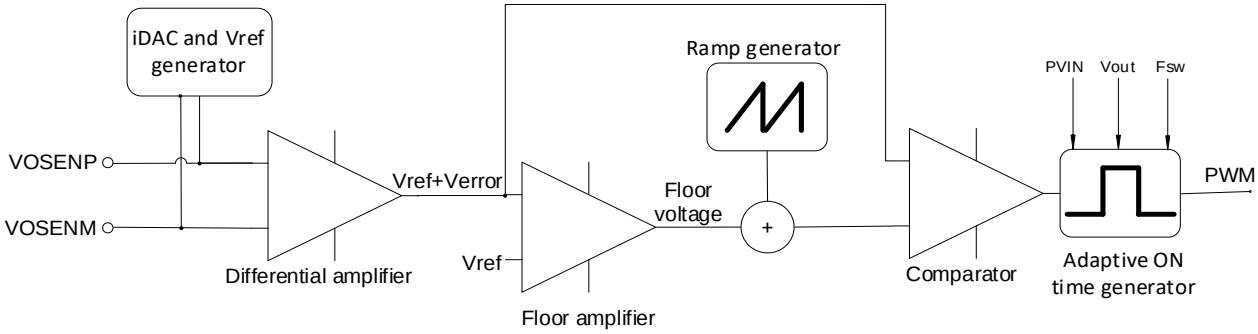
### 13.1.2 Soft-Start

In PMBus mode, the controller will wait for a programmable period of time specified by TON_DELAY before ramping up the output voltage. Prior to entering the active regulation state, the controller performs a controlled, monotonic ramp of the voltage output based on time specified by TON_RISE. This acts as a Soft-Start and is performed by actively regulating the output voltage while digitally ramping up a reference voltage to its final target value.

In SVID mode, the rise time is determined by the default slow slew rate specified by Intel and may be programmed to a fraction of the fast slew rate. The device uses 2.5 mV/us by default. It should be noted, however, that if Vboot is 0, the output voltage does not ramp until the CPU issues a voltage setting command at either the fast slew rate or slow slew rate specified by the CPU.

### 13.1.3 Active Regulation

During active regulation, the output voltage is applied as a feedback voltage alongwith Vref to a differential amplifier. Vref is proporatinal to the set Vout. The error voltage produced by differential amplifier is added to the Vref and fed to a floor amplifier. The difference between this input and Vref is amplified by floor amplifier to generate a floor voltage. The floor amplifier helps improve the transient response and Vout accuracy. Floor voltage and the ramp signal are added together and applied to the comparator and compared against error voltage. The resultant output is fed to Adaptive ON time generator. This block generates PWM signal of pseudo constant frequency. The Adaptive ON Time generator turns the PWM ON for a fixed duration based on the PVIN, Vout and Fsw. The PWM OFF time is determined by the set Fsw and output load. The output is regulated at the set level until the output is commanded OFF, Fault occurs, or POR is deasserted.



### 13.1.4 Shutdown

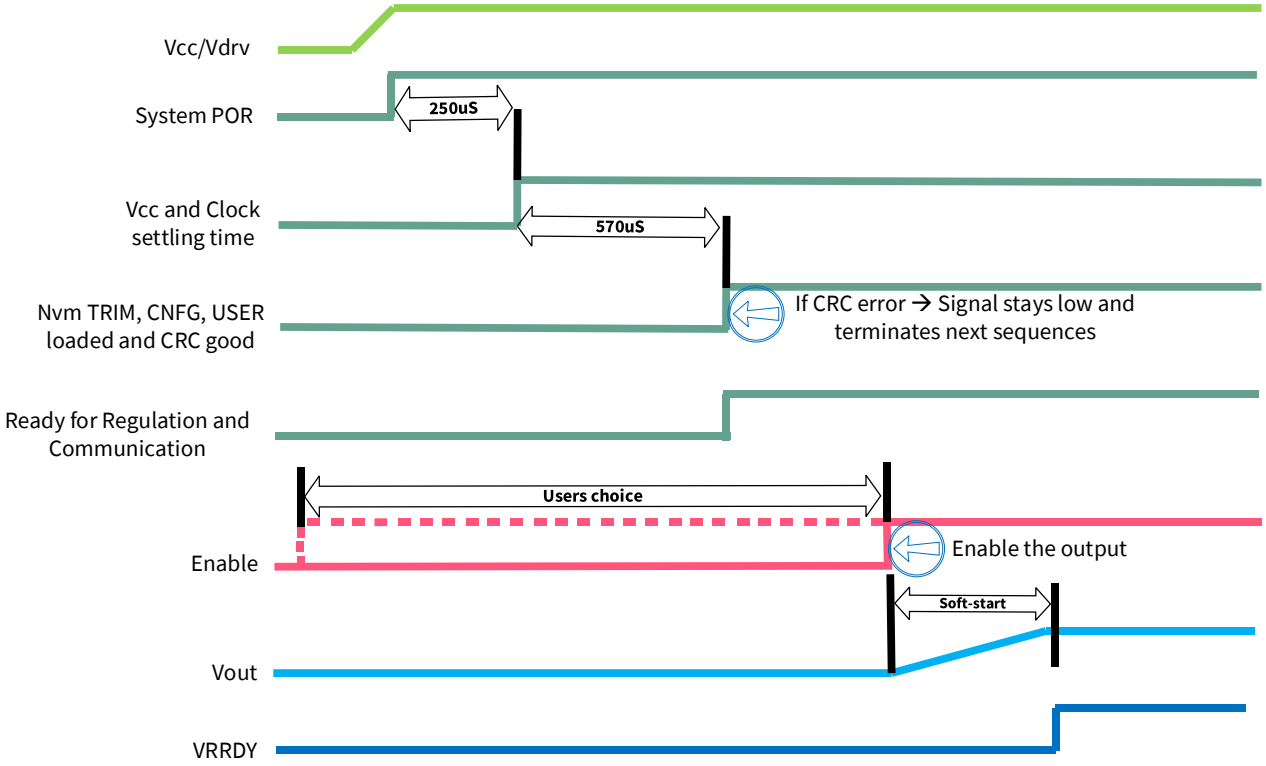
The shut-down state can be entered from either soft-start or active regulation states through user intervention such as Enable being pulled low or through a detected fault including OTP, OCP, UVP, OVP, VIN fault etc.

In PMBus mode, the output may be set to shutdown after a delay specified by TOFF_DELAY and at a ramp down rate specified by TOFF_FALL. The range for this programmable delay is 0ms to 127 ms, and the resolution is 1 ms. Further, in this mode, the soft stop time is limited to 1 ms. The programmable turn off delay only applies in PMBus™ mode. Alternatively, the output may be shutdown as fast as possible by stopping the switching. The response to Enable being pulled low is determine by the settings in ON_OFF_CONFIG register.

In SVID mode, the output voltage decays down to zero.

In the event of shutdown due to fault, the part will execute a fault response based on the fault response set in the configuration of the part.

### 13.1.5 Startup Sequence




## 13.2 Operating Mode

The TDA38640A changes its functionality based on the user-selected operating mode, allowing one device to be used for multiple applications without significant BoM changes. This greatly reduces the user's design cycles and time-to-market (TTM).

The functionality for each operating mode is completely configurable by simple selections in MTP. The mode configuration is shown in Table 10. The mode can be selected based on the I2C register 0x44[12:8], this is the protocol- id register which selects the Intel Mode for which the device is being used.

**Table 10 Mode Selection**

| Mode | Description |
|---|---|
| VR14 | Intel® VR14 (Selected via MTP) |

| Mode | Description |
|---|---|
| VR13 | Intel® VR13 (Selected via MTP) |
| VR12.X | Intel® VR12.X (Selected via MTP) |

## 13.3 Pre-bias startup

The TDA38640A is able to start up into a pre-charged output. The part supports prebias level of Vout setting or lower for VOUT_SCALE_LOOP 1:1 application. The part supports prebias level of half of Vout setting or lower for VOUT_SCALE_LOOP 1:2 application.

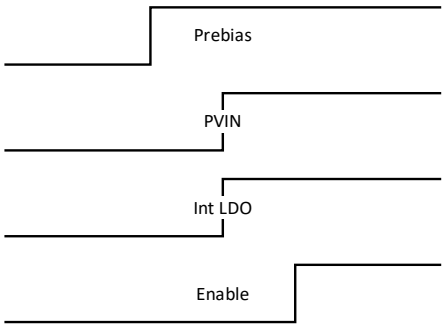
For proper start up in prebias mode, following conditions must be fulfilled:

- The “power down analog circuit when the output is not enabled” feature is disabled (set register 0x6C value to 0xF240)
- Register 0x0064[11], d2a_enable_prebias is set to 1
- PVIN Slew rate is lower than 25V/mS
- Prebias source is current limited to 1A

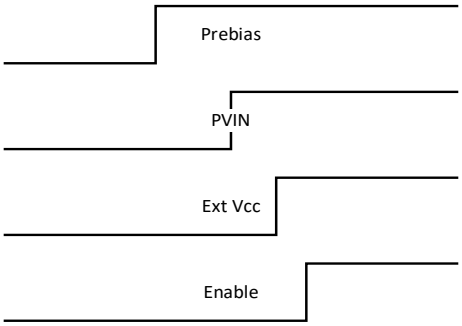
  Based on whether Vcc is supplied externally or an internal LDO is used, the required power-up sequences are shown in Figure 16 below

In applications that do not follow the above prebias operation requirements, the part may go into a protection mode when powered up with prebias condition. In most cases the part recovers from then fault upon cycling of EN. In applications that use external Vcc to power the part, and PVIN needs to be cycled OFF and ON after the first power up, please use the sequences shown in case 3 and 4 below.

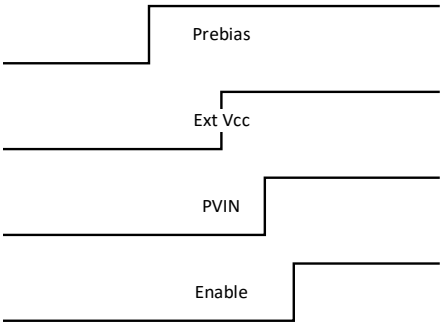
Device Startup with Internal LDO




Device Startup with External Vcc (Case 1)




Device Startup with External Vcc (Case 2)




Device Startup with External Vcc then PVIN is cycled (Case 3)

Device Startup with External Vcc then PVIN is cycled (Case 4)

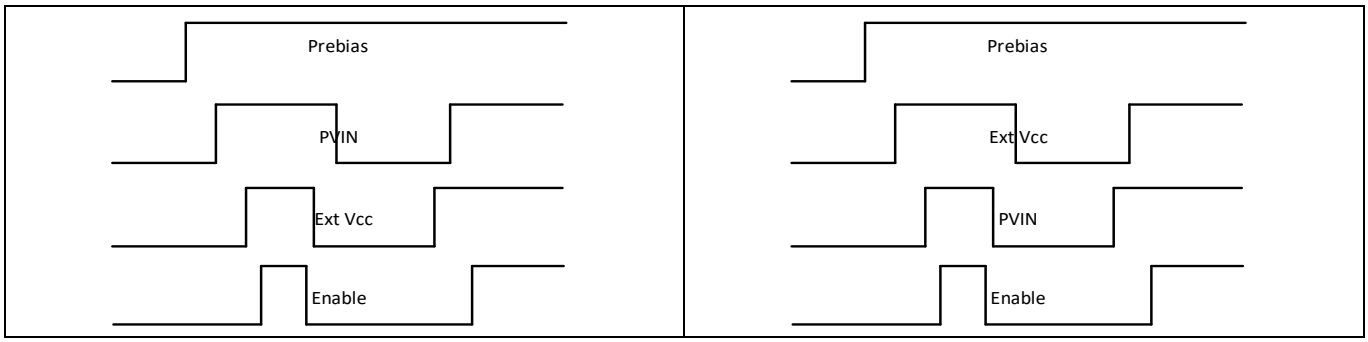



**Figure 16 Device power-on sequence with pre-bias.**

## 13.4 Internal Low-Dropout (LDO) Regulator

The TDA38640A has an integrated low-dropout LDO regulator, to provide the bias voltage for internal circuitry. When the Vcc UVLO start threshold and the enable voltage is above the Enable threshold, the soft-start sequence starts. When using the internal LDO for a single rail operation, PVIN internally acts as an input to the LDO block. To save the power losses on the LDO, an external bias voltage can be used by connecting it to the VCC/LDO pin. Additionally, it is recommended to set 0x64[3] to 0, this disables the internal LDO operation, otherwise the LDO will back feed into PVIN.

When using external Vcc with PVIN pin voltage still below 1.4 V, there is a leakage path from the external Vcc pin to the PVIN pin via the LDO current limiter circuit. A maximum of 200 µA current may flow through this path. The leakage doesn't affect the functionality and reliability of the part. Figure 17 illustrates the possible configurations of VCC/LDO, and PVIN pin.

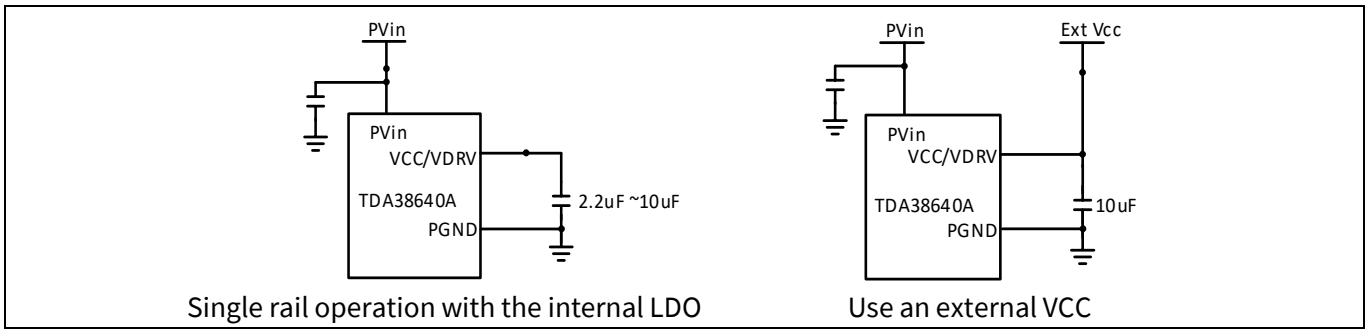



**Figure 17 Configuration of using the internal LDO or an external VCC.**

## 13.5 Enable (EN) Pin

The EN pin controls the on/off status of the TDA38640A. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts.

The EN pin can be configured in four ways. Three of them are as shown in Figure 18. Configuration one is an external logic signal. The second possible configuration derives the enable signal from the PVin voltage by a resistive divider, $R_{EN1}$ and $R_{EN2}$. The third one is a direct connection of EN to the PVIN pin. This is useful in space constrained applications. The fourth configuration is control via PMBus register 0x204[7:0] using the PMBus communication. TDA38640A utilizes the PMBus ON_OFF_CONFIG command in combination with OPERATION command, register 0x202[7:0], to control the enable digitally. Using this, a preference between hardware or software enable may be established. More information is available in the PMBUs app note AN_2203_PL12_2204_184108.

If not used the EN pin may be left floating. There is an internal 1 MΩ pull down in the IC.

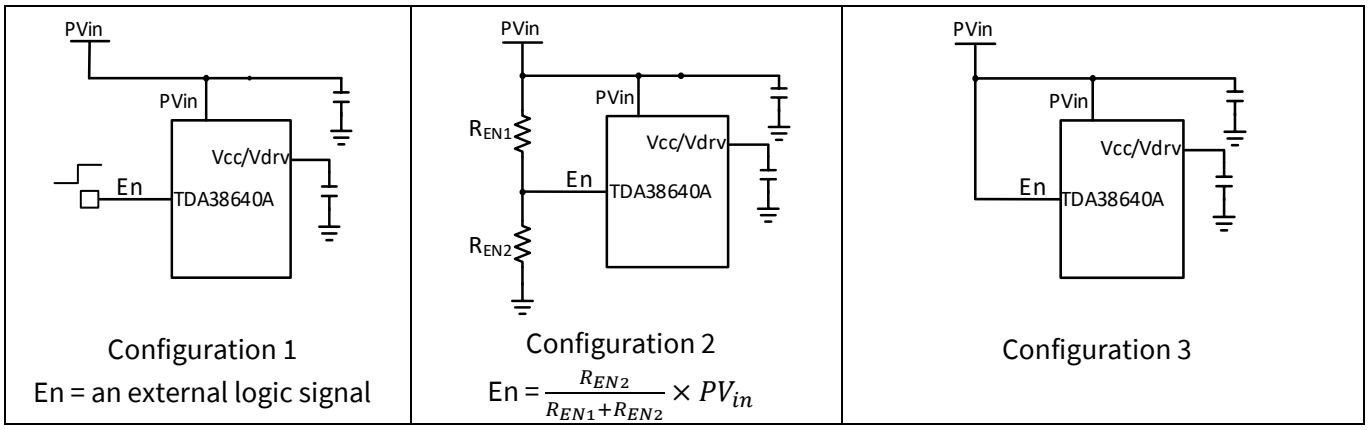



**Figure 18 Enable Configurations**

## 13.6 Switching Frequency and FCCM/DEM Operation

TDA38640A offers two operation modes: Forced Continuous Conduction (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38640A always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripples. In DEM, the synchronous FET is turned off when the inductor current is close to zero, which reduces the switching frequency and improves the efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected by bit 0x5A [1]. Value 1 for this bit programs the device to operate in FCCM mode. Value 0 programs for DEM. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new configuration, EN or VCC voltage needs to be cycled.

The TDA38640A offers eight programmable switching frequencies, $f_{sw}$, from 400 kHz to 2 MHz excluding 1600 kHz, by editing the PMBus register, 0x266[16:0], using the I2C lines. Based on the selected $f_{sw}$, the TDA38640A generates the corresponding on-time of the Control FET for a given $PV_{in}$ and $V_o$, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{f_{sw}}$$

Where $f_{sw}$ is the desired switching frequency. During the operation, the TDA38640A monitors $PV_{in}$ and $V_o$, and can automatically adjust the on-time to maintain the pre-selected $f_{sw}$. With the increase of the load, the switching frequency can increase to compensate for the power losses. Therefore, the TDA38640A has a pseudo constant switching frequency.

Using the FREQUENCY_SWITCH PMBus command, the switching frequency may be programmed between 400 kHz and 2 MHz in steps of 200kHz except 1600kHz.

## 13.7 Intel Mode

When the power-on sequence is initiated, and with VBOOT set to > 0 V, the output voltage will ramp to its configured boot voltage and assert VRRDY. The slew rate to VBOOT is programmed per VID_FAST/VID_SLOW commands.

If Vboot = 0 V, the VR will stay at 0 V and will not soft-start until the CPU issues a VID command to the loop. In VR13 mode, as soon as the IC is ready for SVID communication, SV_ALERT# will be asserted with Vboot = 0 V.

### 13.7.1 Intel Boot Mode

The TDA38640A Vboot voltage is fully programmable in MTP to the range specified in the Intel VID tables. Table 11 and Table 12 show the Intel VID tables for 5 mV and 10 mV VID steps respectively.

### 13.7.2 Intel SVID Interface

The TDA38640A implements a fully compliant Intel® VR 13, VR12, VR 12.5, and VR14 Serial VID (SVID) interface. This is a 3-wire interface between an Intel processor & VR that consists of clock, data and alert# signals.

The TDA38640A implements all the required SVID registers and commands per Intel specifications. For the selected Intel mode, the TDA38640A also implements most of the optional commands and registers with very few exceptions. The Intel CPU is able to detect and recognize the extra functionality that the TDA38640A provides and thus gives the Intel® VR 14/13/12/12.5 CPU unparalleled ability to monitor and optimize its power.

The SVID address of the TDA38640A defaults to 0. This address can be re-programmed in MTP. An address lock function prevents accidental overwrites of the address.

The pseudo-code below illustrates the MTP address programming:

```
# unlock the address register to write, then lock
Set Address_lock_bit=0
Write new SVID address
```

### 13.7.3 All Call SUPPORT

All Call for each loop of TDA38640A can be configured in following ways:

- 0E and 0F.
- 0E only.
- 0F only.
- No All Call

TDA38640A can be configured to be used as VR for CPU which is All Call 0F or Memory which is All Call 0E.

### 13.7.4 VR13 Operation

VR 13 mode is selectable via MTP bit (0x44[12:8]). The boot voltage in VR 13 mode is configured in the boot register. In VR 13 mode, the boot voltage can be configured in 5 mV steps or 10 mV steps.

### 13.7.5 VR14 Operation

VR 14 mode is selectable via MTP bit (0x44[12:8]). The boot voltage in VR 14 mode is configured in the boot register. In VR 14 mode, the boot voltage can be configured in 5mV steps) or 10mV steps.

### 13.7.6 Set Work Point

TDA38640A supports SVID Set WP command to Set VID voltage for all rails through all call address. When processor asserts a Set WP command, all the rails of the VR settle to the corresponding new set-voltage encoded in WP registers. Slew rate and power state of all the rails are identical during a set work point operation.

**Table 11 Intel 5mV VID Table (VR14 and VR13)**

| VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| FF | 1.52 | DA | 1.335 | B5 | 1.15 | 90 | 0.965 | 6B | 0.78 |
| FE | 1.515 | D9 | 1.33 | B4 | 1.145 | 8F | 0.96 | 6A | 0.775 |
| FD | 1.51 | D8 | 1.325 | B3 | 1.14 | 8E | 0.955 | 69 | 0.77 |

| VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| FC | 1.505 | D7 | 1.32 | B2 | 1.135 | 8D | 0.95 | 68 | 0.765 |
| FB | 1.5 | D6 | 1.315 | B1 | 1.13 | 8C | 0.945 | 67 | 0.76 |
| FA | 1.495 | D5 | 1.31 | B0 | 1.125 | 8B | 0.94 | 66 | 0.755 |
| F9 | 1.49 | D4 | 1.305 | AF | 1.12 | 8A | 0.935 | 65 | 0.75 |
| F8 | 1.485 | D3 | 1.3 | AE | 1.115 | 89 | 0.93 | 64 | 0.745 |
| F7 | 1.48 | D2 | 1.295 | AD | 1.11 | 88 | 0.925 | 63 | 0.74 |
| F6 | 1.475 | D1 | 1.29 | AC | 1.105 | 87 | 0.92 | 62 | 0.735 |
| F5 | 1.47 | D0 | 1.285 | AB | 1.1 | 86 | 0.915 | 61 | 0.73 |
| F4 | 1.465 | CF | 1.28 | AA | 1.095 | 85 | 0.91 | 60 | 0.725 |
| F3 | 1.46 | CE | 1.275 | A9 | 1.09 | 84 | 0.905 | 5F | 0.72 |
| F2 | 1.455 | CD | 1.27 | A8 | 1.085 | 83 | 0.9 | 5E | 0.715 |
| F1 | 1.45 | CC | 1.265 | A7 | 1.08 | 82 | 0.895 | 5D | 0.71 |
| F0 | 1.445 | CB | 1.26 | A6 | 1.075 | 81 | 0.89 | 5C | 0.705 |
| EF | 1.44 | CA | 1.255 | A5 | 1.07 | 80 | 0.885 | 5B | 0.7 |
| EE | 1.435 | C9 | 1.25 | A4 | 1.065 | 7F | 0.88 | 5A | 0.695 |
| ED | 1.43 | C8 | 1.245 | A3 | 1.06 | 7E | 0.875 | 59 | 0.69 |
| EC | 1.425 | C7 | 1.24 | A2 | 1.055 | 7D | 0.87 | 58 | 0.685 |
| EB | 1.42 | C6 | 1.235 | A1 | 1.05 | 7C | 0.865 | 57 | 0.68 |
| EA | 1.415 | C5 | 1.23 | A0 | 1.045 | 7B | 0.86 | 56 | 0.675 |
| E9 | 1.41 | C4 | 1.225 | 9F | 1.04 | 7A | 0.855 | 55 | 0.67 |
| E8 | 1.405 | C3 | 1.22 | 9E | 1.035 | 79 | 0.85 | 54 | 0.665 |
| E7 | 1.4 | C2 | 1.215 | 9D | 1.03 | 78 | 0.845 | 53 | 0.66 |
| E6 | 1.395 | C1 | 1.21 | 9C | 1.025 | 77 | 0.84 | 52 | 0.655 |
| E5 | 1.39 | C0 | 1.205 | 9B | 1.02 | 76 | 0.835 | 51 | 0.65 |
| E4 | 1.385 | BF | 1.2 | 9A | 1.015 | 75 | 0.83 | 50 | 0.645 |
| E3 | 1.38 | BE | 1.195 | 99 | 1.01 | 74 | 0.825 | 4F | 0.64 |
| E2 | 1.375 | BD | 1.19 | 98 | 1.005 | 73 | 0.82 | 4E | 0.635 |
| E1 | 1.37 | BC | 1.185 | 97 | 1 | 72 | 0.815 | 4D | 0.63 |
| E0 | 1.365 | BB | 1.18 | 96 | 0.995 | 71 | 0.81 | 4C | 0.625 |
| DF | 1.36 | BA | 1.175 | 95 | 0.99 | 70 | 0.805 | 4B | 0.62 |
| DE | 1.355 | B9 | 1.17 | 94 | 0.985 | 6F | 0.8 | 4A | 0.615 |
| DD | 1.35 | B8 | 1.165 | 93 | 0.98 | 6E | 0.795 | 49 | 0.61 |
| DC | 1.345 | B7 | 1.16 | 92 | 0.975 | 6D | 0.79 | 48 | 0.605 |
| DB | 1.34 | B6 | 1.155 | 91 | 0.97 | 6C | 0.785 | 47 | 0.6 |
| 46 | 0.595 | 37 | 0.52 | 28 | 0.445 | 19 | 0.37 | 0A | 0.295 |
| 45 | 0.59 | 36 | 0.515 | 27 | 0.44 | 18 | 0.365 | 09 | 0.29 |
| 44 | 0.585 | 35 | 0.51 | 26 | 0.435 | 17 | 0.36 | 08 | 0.285 |
| 43 | 0.58 | 34 | 0.505 | 25 | 0.43 | 16 | 0.355 | 07 | 0.28 |
| 42 | 0.575 | 33 | 0.5 | 24 | 0.425 | 15 | 0.35 | 06 | 0.275 |

| VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| 41 | 0.57 | 32 | 0.495 | 23 | 0.42 | 14 | 0.345 | 05 | 0.27 |
| 40 | 0.565 | 31 | 0.49 | 22 | 0.415 | 13 | 0.34 | 04 | 0.265 |
| 3F | 0.56 | 30 | 0.485 | 21 | 0.41 | 12 | 0.335 | 03 | 0.26 |
| 3E | 0.555 | 2F | 0.48 | 20 | 0.405 | 11 | 0.33 | 02 | 0.255 |
| 3D | 0.55 | 2E | 0.475 | 1F | 0.4 | 10 | 0.325 | 01 | 0.25 |
| 3C | 0.545 | 2D | 0.47 | 1E | 0.395 | 0F | 0.32 | 00 | 0 |
| 3B | 0.54 | 2C | 0.465 | 1D | 0.39 | 0E | 0.315 | | |
| 3A | 0.535 | 2B | 0.46 | 1C | 0.385 | 0D | 0.31 | | |
| 39 | 0.53 | 2A | 0.455 | 1B | 0.38 | 0C | 0.305 | | |
| 38 | 0.525 | 29 | 0.45 | 1A | 0.375 | 0B | 0.3 | | |

**Table 12 Intel 10mV VID Table (VR14 and VR13)**

| VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| FF | 3.04 | DC | 2.69 | B9 | 2.34 | 96 | 1.99 | 73 | 1.64 |
| FE | 3.03 | DB | 2.68 | B8 | 2.33 | 95 | 1.98 | 72 | 1.63 |
| FD | 3.02 | DA | 2.67 | B7 | 2.32 | 94 | 1.97 | 71 | 1.62 |
| FC | 3.01 | D9 | 2.66 | B6 | 2.31 | 93 | 1.96 | 70 | 1.61 |
| FB | 3.00 | D8 | 2.65 | B5 | 2.30 | 92 | 1.95 | 6F | 1.60 |
| FA | 2.99 | D7 | 2.64 | B4 | 2.29 | 91 | 1.94 | 6E | 1.59 |
| F9 | 2.98 | D6 | 2.63 | B3 | 2.28 | 90 | 1.93 | 6D | 1.58 |
| F8 | 2.97 | D5 | 2.62 | B2 | 2.27 | 8F | 1.92 | 6C | 1.57 |
| F7 | 2.96 | D4 | 2.61 | B1 | 2.26 | 8E | 1.91 | 6B | 1.56 |
| F6 | 2.95 | D3 | 2.60 | B0 | 2.25 | 8D | 1.90 | 6A | 1.55 |
| F5 | 2.94 | D2 | 2.59 | AF | 2.24 | 8C | 1.89 | 69 | 1.54 |
| F4 | 2.93 | D1 | 2.58 | AE | 2.23 | 8B | 1.88 | 68 | 1.53 |
| F3 | 2.92 | D0 | 2.57 | AD | 2.22 | 8A | 1.87 | 67 | 1.52 |
| F2 | 2.91 | CF | 2.56 | AC | 2.21 | 89 | 1.86 | 66 | 1.51 |
| F1 | 2.90 | CE | 2.55 | AB | 2.20 | 88 | 1.85 | 65 | 1.50 |
| F0 | 2.89 | CD | 2.54 | AA | 2.19 | 87 | 1.84 | 64 | 1.49 |
| EF | 2.88 | CC | 2.53 | A9 | 2.18 | 86 | 1.83 | 63 | 1.48 |
| EE | 2.87 | CB | 2.52 | A8 | 2.17 | 85 | 1.82 | 62 | 1.47 |
| ED | 2.86 | CA | 2.51 | A7 | 2.16 | 84 | 1.81 | 61 | 1.46 |
| EC | 2.85 | C9 | 2.50 | A6 | 2.15 | 83 | 1.80 | 60 | 1.45 |
| EB | 2.84 | C8 | 2.49 | A5 | 2.14 | 82 | 1.79 | 5F | 1.44 |
| EA | 2.83 | C7 | 2.48 | A4 | 2.13 | 81 | 1.78 | 5E | 1.43 |
| E9 | 2.82 | C6 | 2.47 | A3 | 2.12 | 80 | 1.77 | 5D | 1.42 |
| E8 | 2.81 | C5 | 2.46 | A2 | 2.11 | 7F | 1.76 | 5C | 1.41 |
| E7 | 2.80 | C4 | 2.45 | A1 | 2.10 | 7E | 1.75 | 5B | 1.40 |

| VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) | VID (Hex) | Voltage (V) |
|---|---|---|---|---|---|---|---|---|---|
| E6 | 2.79 | C3 | 2.44 | A0 | 2.09 | 7D | 1.74 | 5A | 1.39 |
| E5 | 2.78 | C2 | 2.43 | 9F | 2.08 | 7C | 1.73 | 59 | 1.38 |
| E4 | 2.77 | C1 | 2.42 | 9E | 2.07 | 7B | 1.72 | 58 | 1.37 |
| E3 | 2.76 | C0 | 2.41 | 9D | 2.06 | 7A | 1.71 | 57 | 1.36 |
| E2 | 2.75 | BF | 2.40 | 9C | 2.05 | 79 | 1.70 | 56 | 1.35 |
| E1 | 2.74 | BE | 2.39 | 9B | 2.04 | 78 | 1.69 | 55 | 1.34 |
| E0 | 2.73 | BD | 2.38 | 9A | 2.03 | 77 | 1.68 | 54 | 1.33 |
| DF | 2.72 | BC | 2.37 | 99 | 2.02 | 76 | 1.67 | 53 | 1.32 |
| DE | 2.71 | BB | 2.36 | 98 | 2.01 | 75 | 1.66 | 52 | 1.31 |
| DD | 2.70 | BA | 2.35 | 97 | 2.00 | 74 | 1.65 | 51 | 1.30 |
| 50 | 1.29 | 3E | 1.11 | 2C | 0.93 | 1A | 0.75 | 08 | 0.57 |
| 4F | 1.28 | 3D | 1.10 | 2B | 0.92 | 19 | 0.74 | 07 | 0.56 |
| 4E | 1.27 | 3C | 1.09 | 2A | 0.91 | 18 | 0.73 | 06 | 0.55 |
| 4D | 1.26 | 3B | 1.08 | 29 | 0.90 | 17 | 0.72 | 05 | 0.54 |
| 4C | 1.25 | 3A | 1.07 | 28 | 0.89 | 16 | 0.71 | 04 | 0.53 |
| 4B | 1.24 | 39 | 1.06 | 27 | 0.88 | 15 | 0.70 | 03 | 0.52 |
| 4A | 1.23 | 38 | 1.05 | 26 | 0.87 | 14 | 0.69 | 02 | 0.51 |
| 49 | 1.22 | 37 | 1.04 | 25 | 0.86 | 13 | 0.68 | 01 | 0.50 |
| 48 | 1.21 | 36 | 1.03 | 24 | 0.85 | 12 | 0.67 | 00 | 0 |
| 47 | 1.20 | 35 | 1.02 | 23 | 0.84 | 11 | 0.66 | | |
| 46 | 1.19 | 34 | 1.01 | 22 | 0.83 | 10 | 0.65 | | |

## 13.8 Program Pin (SM_ADDR/PROG)

A resistor to ground on this pin sets both a fixed I2C slave address offset and selects a configuration from the 14 possible config files in the OTP during power-up. All parts sent from factory have a default config image programmed in it. The user can program a maximum of 13 config images. As shown in Table 13, the SM_ADDR pin selects an offset based on the resistor connected to the SM_ADDR/PROG pin. This pin also selects a configuration from the 13 possible config files from a multi image config file during power-up.

The pin programming allows the address offset adjust capability from 0 to 12 for a 13 image multi config file. It allows address offset adjust capability from 0 to 15 for single image config file. The most recently programmed CONFIG image will be loaded from the OTP irrespective of the pin programmed address offset when single image config file is programmed. For multi-image application, the table above shows the CONFIG image that will be loaded from the OTP based on the pin programmed address offset. The address offset from this pin can be disabled by setting register i2c_disable_addr_offset(0x42[6]) to 1. In this mode the effective address is determined by the register value in i2c_device_addr(0x40[6:0]) and pmb_device_addr(0x40[6:0]). This is helpful when address offset need to be 13, 14 or 15 which is otherwise not possible with multi-image config application when i2c_disable_addr_offset(0x42[6]) is set to 0.

**Table 13 SM_ADDR/PROG Pin with the consecutive images starting from Config 0 at location 0**

| Resistor to GND (kΩ) | SM_ADDR function: Offset selection from the base address | PROG function: Config selection (For single -image Config) | PROG pin: Config selection (For Multi-image Config) | Programmability for single and multi-image config file |
|---|---|---|---|---|
| SHORT | 0 | Most recently programmed CONFIG | CONFIG0 | Please refer to section 12 for single image and multi-image programming details |
| 5.62 | 1 | | CONFIG1 | |
| 9.53 | 2 | | CONFIG2 | |
| 14 | 3 | | CONFIG3 | |
| 21 | 4 | | CONFIG4 | |
| 30.1 | 5 | | CONFIG5 | |
| 36.5 | 6 | | CONFIG6 | |
| 43.2 | 7 | | CONFIG7 | |
| 51.1 | 8 | | CONFIG8 | |
| 61.9 | 9 | | CONFIG9 | |
| 75 | 10 | | CONFIG10 | |
| 88.7 | 11 | | CONFIG11 | |
| 105 | 12 | | CONFIG12 | |
| 127 | 13 | | Not supported | |
| 147 | 14 | | | |
| FLOAT | 15 | | | |

## 13.9 Load-line

TDA38640A offers digital load line which can be set via configuration registers, without any need for external components. The load line can be programmed from 0 to 10 mΩ at a resolution of 19.53 µΩ using the VOUT_DROOP command 0x250[15:0]. The range and resolution of the VOUT_DROOP may be increased by using the bit loadline_range_sel 0x6A [6] to 0 to 50 mΩ at a resolution of 100 µΩ. In addition to this, the bandwidth of the digital load line is also programmable from 30 kHz to 500 kHz in steps of 30 kHz by using 4 bits of register 0x6A [3:0].

## 13.10 Output Voltage Differential Sensing

The TDA38640A VSEN and VRTN pins are connected across the output capacitors near the load to provide true differential remote voltage sensing with high common-mode rejection. Fast COT control compares the output voltage to a floor voltage combined with an internal ramp signal. When Vout drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vout with a reference voltage. As shown in Figure 19, the output sense pins VOSENP and VOSENM are connected across the output capacitors.

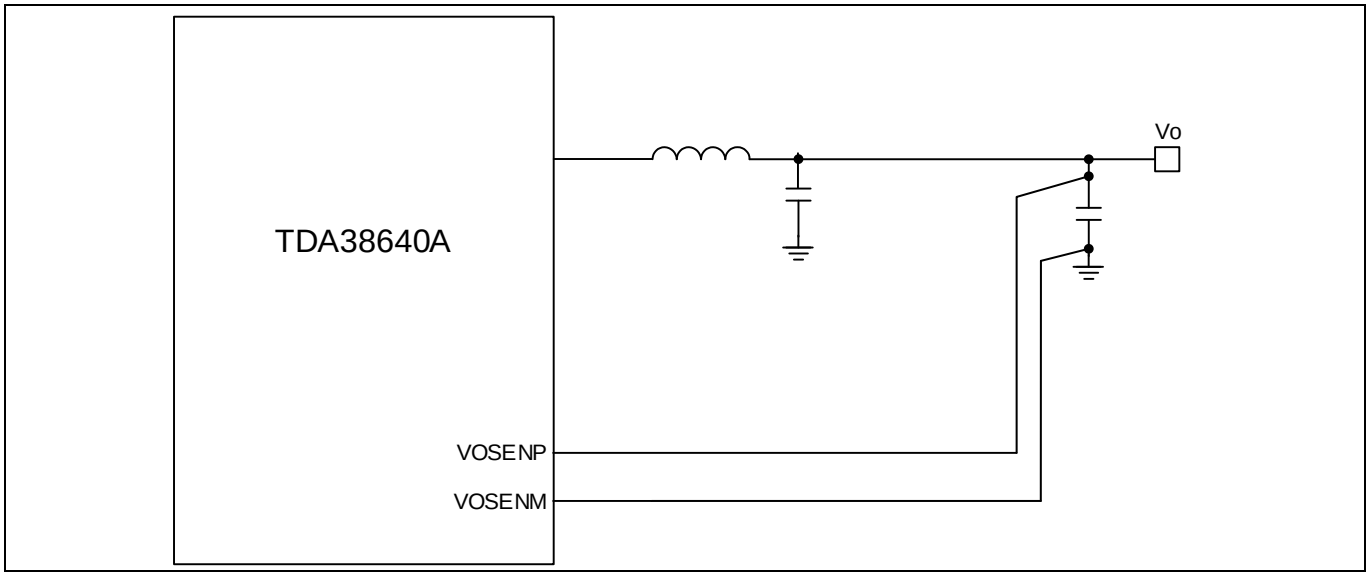



**Figure 19 Output voltage sensing connections**

## 13.11 Input Current Sensing

The TDA38640A can measure input current using a measured value from a shunt resistor and/or calculate it using other known variables. The input current sense mode is controlled by the register iin_sense_mode, with options outlined in Table 14.

**Table 14 Register iin_sense_mode options.**

| Value | Mode |
|---|---|
| 3, 2 | Calculated and external resistor sense |
| 1 | External resistor sense |
| 0 | Calculated |

The “lossless input current estimation” scheme can accurately calculate the actual input current as it knows the value of output current, output voltage, input voltage and pulse width of each phase. This eliminates the need for a dedicated shunt. The IINSEN pin also simplifies board layout by eliminating additional components. It is recommended to use the value 1 for register iin_sense_mode when utilizing this feature in the part for input current sensing. The pins VINSENP and VINSENM should be tied to PVIN and the register ,iin_sense_mode, should set to 0 if the feature needs to be disabled for a particular rail in an application.

Register iin_rsense_value controls the external resistor value used for sensing. There is also offset and gain correction that is provided to the user via the iin_offset_user (0x66[13:8]) and iin_gain_user (0x66[7:4]) registers respectively.

Table 15 summarizes the usable external resistor values from iin_rsense_value (0x66[3:0]).

Figure 20 shows the generic application circuit for input current sensing in a typical application.

**Table 15 Usable external input current sense resistors, from register iin_rsense_value.**

| Value | Threshold | Value | Threshold |
|---|---|---|---|
| 11-15 | 10 mΩ | 5 | 4 mΩ |
| 10 | 9 mΩ | 4 | 3 mΩ |
| 9 | 8 mΩ | 3 | 2 mΩ |

| Value | Threshold | Value | Threshold |
|---|---|---|---|
| 8 | 7 mΩ | 2 | 1 mΩ |
| 7 | 6 mΩ | 1 | 0.5 mΩ |
| 6 | 5 mΩ | 0 | 0.2 mΩ |

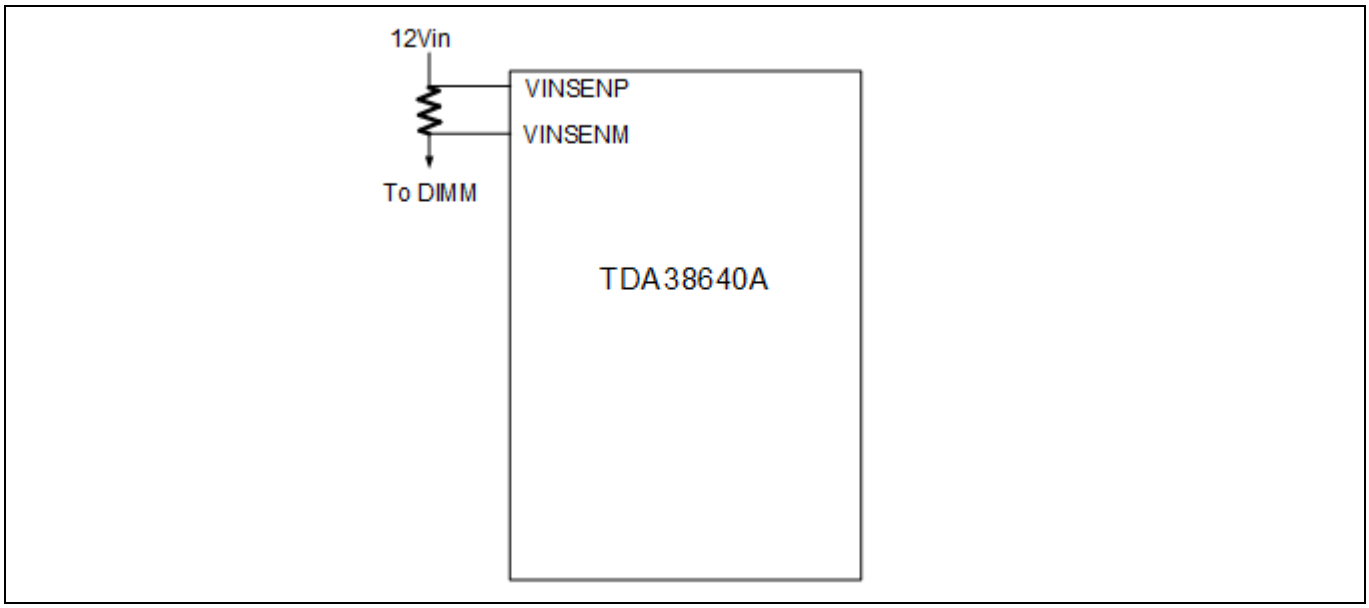



**Figure 20 Input current sensing using external shunt**

## 13.12 CAT_FAULT# and VRRDY

TDA38640A supports CAT_FAULT functionality. This is an additional indication of a fault which the system can use to take an action. CAT_FAULT is an open drain output and is pulled high to 3.3 V in the system. In case of a fault, this active low signal is asserted. The conditions under assertion are shown below in Table 16. The functionality is further defined in the VR14 PWM document. CAT_FAULT# is asserted for a high side short during startup. The CAT_FAULT# signal is not asserted for any other fault during startup. To reset CAT_FAULT# when external Vcc is used, PVIN must be cycled below 4V. For rails which uses internal LDO, a PVIN cycle is needed to reset CAT_FAULT#.

VRRDY is Intel's equivalent of PGOOD. The electrical characteristics for the signal are defined in detail in the Intel VR14 PWM document. It is an open drain output pulled up to 3.3 V. When the power-on sequence is initiated, and with VBOOT set to > 0V, the output voltage will ramp to its configured boot voltage and assert VRRDY.

**Table 16 VRRDY and CAT_FAULT# Response to Faults**

| Type of Fault | VRRDY Pin Functionality | CATFLT# Pin Functionality | Device Behavior after event |
|---|---|---|---|
| OVP | This pin is de-asserted | This pin is asserted | Latched Shutdown |
| OCP | This pin is de-asserted | This pin is asserted | Latched Shutdown |
| UVP | This pin is de-asserted | This pin is asserted | Latched Shutdown |
| Boot UVLO | This pin is de-asserted | This pin is asserted | Latched Shutdown |
| Vcc UVLO | This pin is de-asserted | This pin is asserted | Latched Shutdown |
| OTP | This pin is de-asserted | This pin is asserted | Latched Shutdown |

# 14 Faults and Protection

## 14.1 Over Current Protection (OCP)

The TDA38640A has two levels of OCP protection: Analog OCP (AOCP) and Digital OCP (DOCP). The AOCP current limit is based on valley inductor current, whereas the DOCP is based on average current information. AOCP is a fast fault response and should be set to a value that prevents failure of the device.

The scheme allows reconstruction of the inductor current from the voltage sensed across the Sync FET $R_{DS(on)}$. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting.

The AOCP fault protection circuit also uses the voltage sensed across the $R_{DS(on)}$ of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the over current threshold and does not depend on the ADC or reported current. The current limit scheme uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Synchronous MOSFET. As a result, the over current trip threshold remains almost constant over temperature.

The TDA38640A AOCP can be accessed via three bits in the register map (aocp_thresh_sel [0:2]). The digital OCP (DOCP) is available via the PMBus register IOUT_OC_FAULT_LIMIT, and the response is decided by IOUT_OC_FAULT_RESPONSE. Available responses are shutdown, retry 6 times and latch off, or retry indefinitely. The indication of the fault is available in the STATUS_IOUT register in PMBus.

AOCP shall be enabled during soft-start and normal operation including FCCM and DEM modes. When AOCP threshold is exceeded, the low side MOSFET will continue to stay on for the remaining cycle and the following high side pulse will be ignored to allow inductor relaxation (pulse skipping). If an AOCP condition is detected on the rising edge of a PWM pulse, the high side will still be blocked from turning on and the pulse will be skipped. The high side will continue to be ignored if the current remains above the AOCP threshold. When current falls below the AOCP threshold, the following high-side pulse will be enabled. The Vout under AOCP is determined by the overload on the output and that determines if the VRRDY gets de-asserted or the UVP protection is triggered as a result of AOCP.

Current signal for the DOCP protection is passed through a 5.5KHz filter, before being compared with the IOUT_OC_FAULT_LIMIT threshold. Hence the response of the DOCP circuit is slower than AOCP due to the averaging of the current signal by the filter. The DOCP threshold operating point can be calibrated by IOUT_ CAL _GAIN and IOUT_ CAL _OFFSET. Because of the averaging of the current signal, DOCP is more accurate than AOCP. It is recommended to set AOCP higher than DOCP as AOCP may get triggered earlier than DOCP and may result in drop in output voltage when both AOCP and DOCP are set to same value. When the Digital OCP is triggered using the Analog OCP threshold, using the bit docp_from_aocp, 0x60[3], a 10-count counter is implemented to count 10 AOCP events, then a signal is sent to the digital block to perform the programmed response. The counter is reset after 3 consecutive non-OCP events. The count occurs at the valley of the current. Note that COT switching frequency will decrease when skipping pulses. Figure 21 is an example AOCP response.

Cycle-by-cycle OCP response allows the TDA38640A to fulfill a brief high current demand, such as a high inrush current during the startup. The Output slew rate and the output capacitance will affect the AOCP during startup. At higher output voltages with no-load, a higher slew rate or a higher output capacitance can trigger AOCP at startup. The TON_RISE time should be increased or reduce output capacitance to avoid false triggering of AOCP.

The AOCP is activated when EN voltage is above its threshold. During AOCP events, the valley of the inductor current is regulated around the AOCP limit. But during the first switching cycle when the AOCP is tripped, the valley of the inductor current can drop slightly below the AOCP limit due to cycle skipping. It should be noted that AOCP events do not pull the VRRDY signal low unless the output voltage eventually drop below the Under-Voltage Protection (UVP) threshold and trigger UVP. The response is also shown in Figure 21.

The OCP limits are thermally compensated. The corresponding output dc current can be calculated as follows:

$$I_{out\_OCP} = I_{LIM} + \frac{\Delta i_L}{2}$$

Where: $I_{out\_OCP}$ = Output dc current when AOCP is tripped. $I_{LIM}$ = AOCP limit, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current.

To avoid inductor saturation during AOCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{LIM\_max} + \Delta i_L$$

Where: $I_{sat}$ is the inductor saturation current and $I_{LIM\_max}$ is the maximum spec of the AOCP limit.

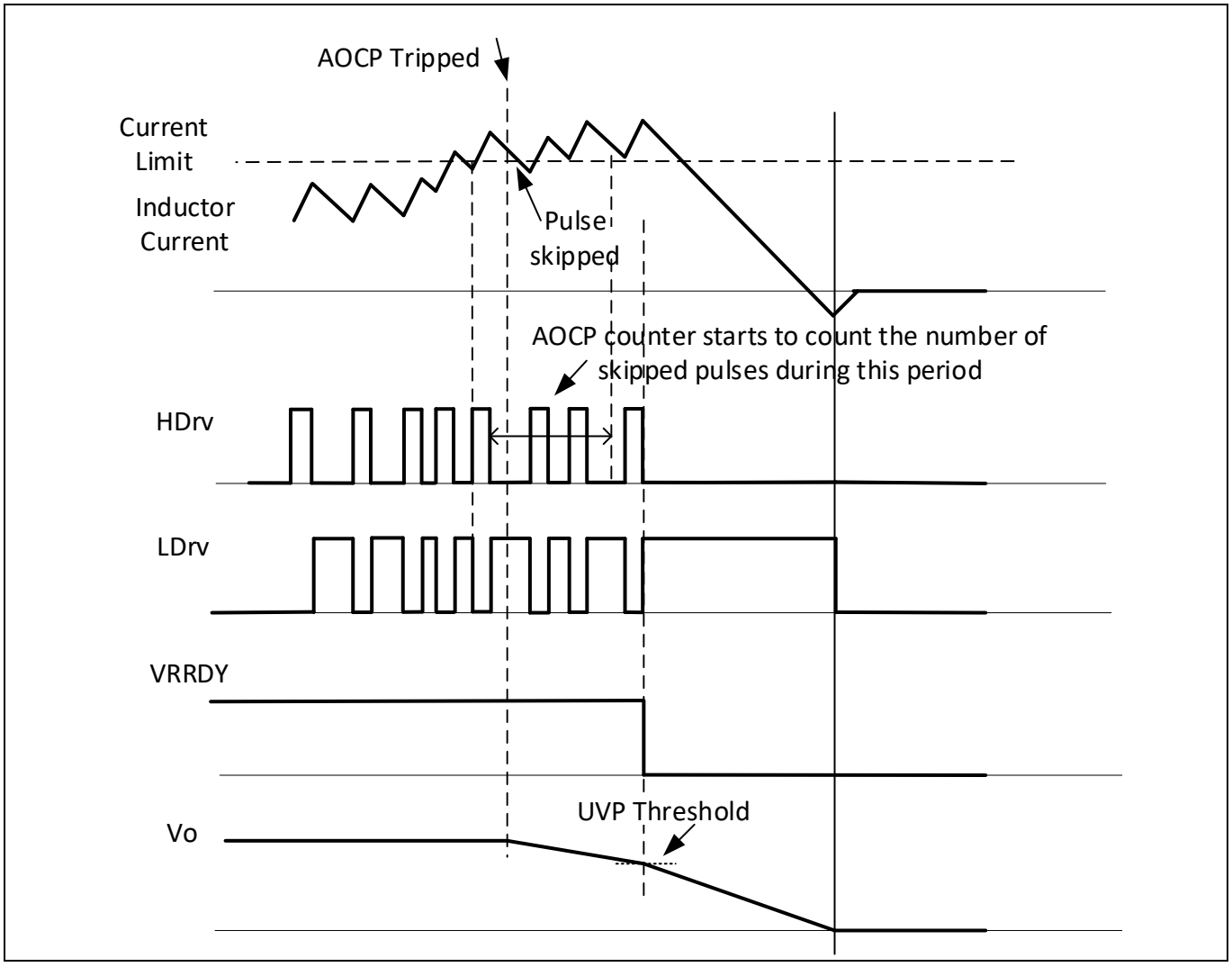



**Figure 21 AOCP response timing diagram.**

## 14.2 Output Under Voltage Protection (UVP)

The TDA38640A UVP response is a relative limit configurable from 50 mV to 400 mV in steps of 50 mV. The limit is programmed via the VOUT_UV_FAULT_LIMIT PMBus command, and the response is programmed via the VOUT_UV_FAULT_RESPONSE command. There is also the option to program the UVP Limit for the part by accessing the I2C register in the common regmap space. The UVP threshold is enabled using the relative_uvp_thresh_en (0x5E [15]) bit and the levels are set by the relative_uvp_thresh [2:0] (0x5E [10:8]) bits.

Possible responses are ignore, shutdown, and retry indefinitely. The relative UVP may be disabled using the disable_relative_UVP(0x60[14]) bit.

When the UVP fault is triggered, a flag is raised and low-side FET is turned ON to drag down the output. The Vout setting is changed to 0V with a slew rate of 30mV/uS to drag the output to 0V as soon as possible. After that both MOSFETs are tri-stated as long as the Vout stays below 0.25V. The part is started again by either cycling the Vcc voltage or the EN signal to the part.

If the response is set to retry, a user defined timer (1 ms to 8 ms in steps of 1 ms) is started as soon as the UVP fault is triggered and the output is tri-stated. At the end of the timer the output is checked against a fixed level of 250 mV. If the output is below this voltage the startup sequence is initiated or else the timer is reset and the output tri-state continues (both the MOSFET's are tri-stated).

There are options for UVP protection to be lifted during voltage transitions (Vboot, DVID up and/or down) using the register bits blank_uv_sel [1:0]. The options for this register are outlined in Table 17.

**Table 17 Optional UVP blanking via register blank_uv_sel (0x60[11:10]).**

| sel | Description |
|---|---|
| 3 | blank UV faults during DVID up or down (including Vboot) |
| 2 | blank UV faults during DVID up (including Vboot) |
| 1 | blank UV faults during Vboot |
| 0 | no UV fault blanking |

## 14.3 Over Voltage Protection (OVP)

The OVP response is divided into two parts: Fixed OVP (FOVP) and Relative OVP (ROVP). The Fixed OVP is typically used for startup, all DVIDs, and when EN is low. ROVP covers all other situations during operation. Figure 22 depicts an example of when FOVP and ROVP are utilized.

The FOVP has 8 distinct levels (0.8 V, 1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.2 V, and 2.85 V) with VOUT_SCALE_LOOP in 1:1 mode. The levels are 2x in 1:2 mode. It is programmable via fixed_ovp_thresh [2:0] in configuration register 0x60. The response to an OVP event is programmed via the VOUT_OV_FAULT_RESPONSE command. OVP can have four responses: ignore, shutdown, and retry n (max 6) times after n (defined by PMBus) seconds before latching and retry forever. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50 mV using the I2C register relative_ovp_thresh [2:0] (0x5e [14:12]). The OVP fault can also be blanked by using the bits [13:12] of register 0x60 in common regmap space. Please refer to Table 18 for more details. The PMBUs commands could be over-ridden by using the relative_ovp_thresh_en (0x5e [15]) bit to over-ride the PMBUs commands.

**Table 18 Optional OVP blanking via blank_ov_sel(0x60[13:12])**

| sel | Description |
|---|---|
| 3 | blank OV faults during DVID up or down (including Vboot) |
| 2 | blank OV faults during DVID up (including Vboot) |
| 1 | blank OV faults during Vboot |
| 0 | no OV fault blanking |

When the output triggers an FOVP event, the OVP flag is set, the low side switch is turned ON and the high side switch is turned OFF. The low side switch is turned ON till the output voltage is dragged down to the set FOVP threshold. The output voltage then decreases to zero with its natural decay.

When the output triggers an ROVP event, the VID set point is moved to 0 V at a controlled slew rate of 30 mV/uS and the OVP flag is set. Next, the low side switch is turned ON and the high side is turned OFF. This allows the output to discharge until VID set point reaches zero or Vout catches up with the VID set point at which point the low side and high side switched turn ON and OFF as required to maintain the output at the VID set point. How fast the output voltage discharges during this event is determined by the by the output voltage, output capacitance and output inductor. This determines if the output voltage indeed is dragged down to zero by the end of the controlled VID ramp down. At the end of the ramp, if the output is not already dragged down to zero, the output voltage will decrease to zero with its natural decay.

Please refer to the relative OVP and UVP thresholds table under register 5E[10:8] of the register map app note AN_2204_PL12_2204_183614 for more information on how to set these thresholds for VOUT_SCALE_LOOP 1:1 and VOUT_SCALE_LOOP 1:2.

The picture below shows and example of how ROVP and RUVP work during DVID changes in conjuction with blank settings mentioned above. In this example, the ROVP is blanked during the DVID down and Vboot

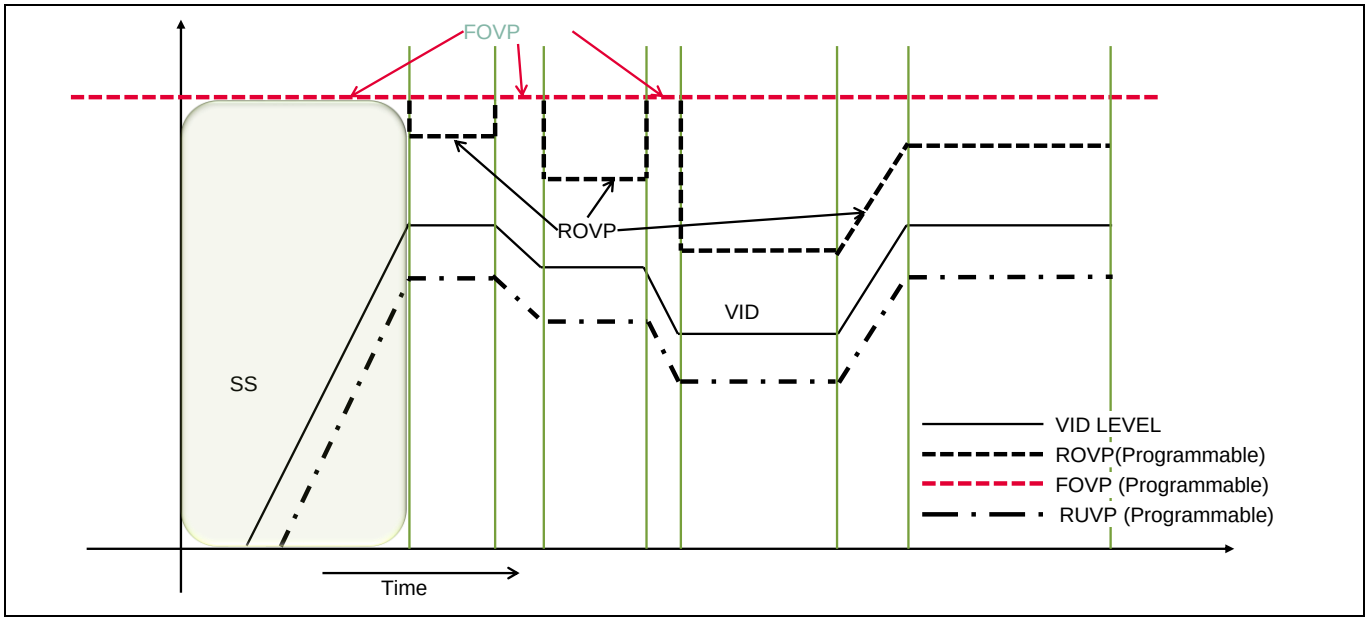



**Figure 22 OVP and RUVP example diagram. Note the situations in which FOVP takes over from ROVP.**

## 14.4 Over Temperature Protection (OTP)

Temperature protection is programmable via the OT_FAULT_LIMIT, OT_WARN_LIMIT, and OT_FAULT_RESPONSE PMBus registers. The TDA38640A supports three responses: ignore, shutdown, and retry indefinitely. The fault is non-latching.

An OTP event is triggered when the device temperature reaches the OT_FAULT_LIMIT. The switching output is tri-stated and the output discharges, while staying biased with the internal LDO on. With the output off, the device cools until reaching the OT_WARN_LIMIT, and if set to retry, the device will hiccup with potential of pre-biased startup.

## 14.5 Boot Under Voltage Lockout (UVLO)

The voltage from the BOOT pin to PHASE pin is monitored on the TDA38640A. If the UVLO Boot lower threshold violation is detected within the PWM cycle, the event is counted and a fault is asserted after 10 violations. After 3 consecutive cycles without a UVLO BOOT event (above the lower threshold during the PWM cycle), the counter

resets. To clear the fault, Vcc or EN has to be cycled. The Boot UVLO fault is in the fail_code_sticky register. This protection can be disabled by setting the bit drv_uvlo_boot_dis (0x006C[10]) to 1.

## 14.6 Minimum On - Time and Minimum Off - Time

The minimum on-time refers to the shortest time for Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38640A to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in the Section 7.1. Otherwise the resulting switching frequency may be lower than the desired target. The following formula could be used to check for the minimum on-time requirement.

$$\frac{V_0}{kf_{sw} \times V_{in}} > \max\ spec\ of\ T_{on(\min)}$$

Where $f_{sw}$ is the desired switching frequency, and *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure the design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in the Section **6**, which can be calculated as shown below.

$$\frac{V_{in} - V_0}{kf_{sw} \times V_{in}} > \max\ spec\ of\ T_{off(\min)}$$

Where $f_{sw}$ is the desired switching frequency, and *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure the design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

## 14.7 High-Side Short (HSS) Detection

The TDA38640A offers high-side FET short detection. The phase pin is monitored when the low-side FET is active. HSS monitoring happens both at startup and during normal operation. In an HSS event, the HSS threshold is reached and both VRRDY and CAT_FAULT# pins are asserted. In the case of an HSS event during startup, the response is communicated via the CAT_FAULT# pin. Once the HSS threshold is reached, the low-side FET is turned on and the switching stops. There is no current reporting during this time. The fault is sticky and only clears when either the VCC or EN signal is cycled. This protection can be disabled by setting the bit drv_hss_det_dis (0x006C[11]) to 1.

# 15 Fault Communication

The TDA38640A supports OCP, OVP, UVP, OTP, BOOT UVLO, and Vcc UVLO via telemetry.

## 15.1 I2C Slave Addressing

The TDA38640A simultaneously supports I2C and PMBus through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different I2C addresses. Once the address of the TDA38640A is set, it can be locked to protect it from being overridden. Optionally, a resistor can be tied to the SM_ADDR/PROG pin to generate an offset as shown in Table 19 .

As an example, setting a base 7-bit I2C address of 28h with a resistor offset of +15 sets the 7-bit I2C address to 37h. There is an option to disable the offset functionality on the SM_ADDR pin by using the i2c_disable_addr_offset (0x42[6]) bit from commmon regmap space. When the address offset bit is enabled an offset is added to the base address for i2c depending upon the resistor connected to the SM_ADDR/PROG pin.

**Table 19 Disable Offset Options (0x42[6])**

| Enable I2C_use_addr_offset bit | I2C Address Offset |
|---|---|
| 0 | enabled |
| 1 | disabled |

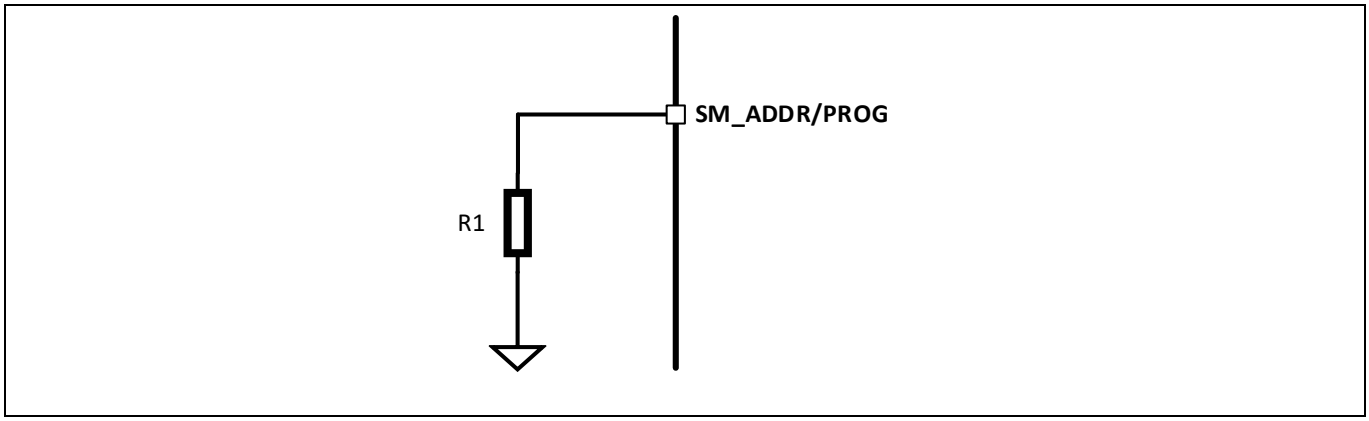



**Figure 23 SM-ADDR/PROG Pin Components**

## 15.2 Real-Time Telemetry

TDA38640A provides real-time accurate measurement of input voltage, input current, output voltage, output current temperature, output power, and input power over the I2C interface. Output voltage is calculated based upon the VID setting and the result is reported through the I2C. In the SVID domain, the TDA38640A supports output voltage, output current, input voltage, input current, and input power telemetry.

## 15.3 I2C Protocol

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 24 shows the I2C format employed by the TDA38640A.

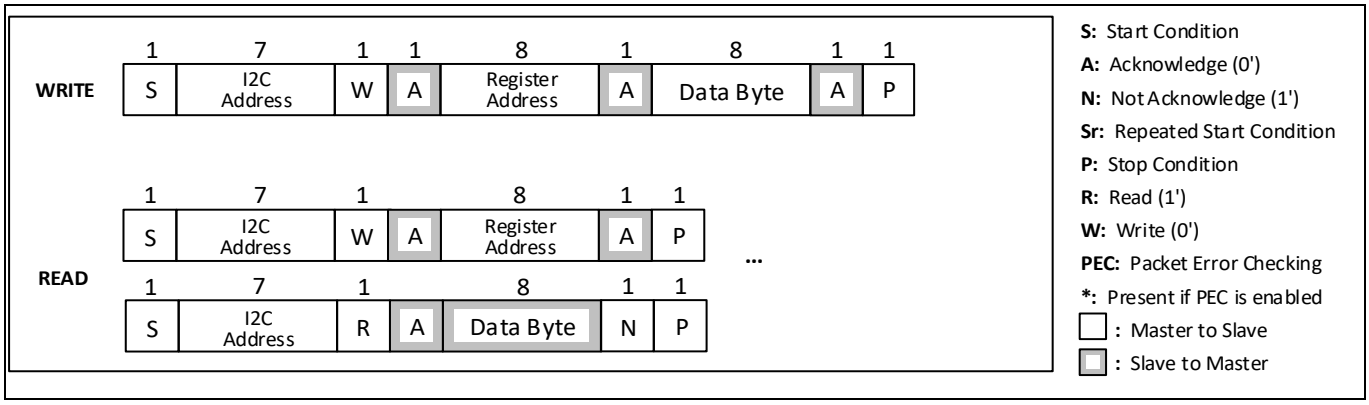



**Figure 24 I2C Format**

## 15.4 PMBus Commands Supported

Table 20 lists all the PMBus commands which are supported by the device.

**Table 20 PMBus Commands Supported**

| I2C Register Address | COMMAND | PMBus PROTOCOL | PMBus COMMAND CODE | DESCRIPTION |
|---|---|---|---|---|
| 0x200 | PAGE | Read/Write Byte | 00h | Allows access of each loop via paging. |
| 0x202 | OPERATION | Read/Write Byte | 01h | Enables or disables the output and controls margining. Ignores OVP on Margin High, UVP on Margin Low. |
| 0x204 | ON_OFF_CONFIG | Read/Write Byte | 02h | Configures the combination of CONTROL pin and OPERATION command needed to turn the unit on and off. |
| 0x206 | CLEAR FAULTS | Send Byte | 03h | Clear contents of Fault registers |
| 0x20A | PAGE_PLUS_WRITE | Write Block | 05h | Set the PAGE within a device, send a command, and send the data for the command in one packet. |
| 0x20C | PAGE_PLUS_READ | Block Read | 06h | Set the PAGE within a device, send a command, and read the returned data by the command in one packet |
| 0x220 | WRITE_PROTECT | Read/Write Byte | 10h | Protects from overwriting the configuration files and modes accidentally |
| 0x222 | STORE_DEFAULT_ALL | Send Byte | 11h | Instructs the device to copy the entire contents of the configuration registers to the NVM |
| 0x224 | RESTORE_DEFAULT_ALL | Send Byte | 12h | Reloads the OTP |
| 0x22A | STORE_USER_ALL | Send Byte | 15h | Stores the user OTP section |
| 0x22C | RESTORE_USER_ALL | Send Byte | 16h | Reloads the user OTP section |
| 0x232 | CAPABILITY | Read Byte | 19h | Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz |
| 0x236 | SMBALERT_MASK | Block Write/ Block Read Process Call | 1Bh | Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register |

| | | | | |
|---|---|---|---|---|
| | | | | to be masked in the low byte, the bit to be masked in the High byte. |
| 0x240 | VOUT_MODE | Read/Write Byte | 20h | Sets the format for VOUT related commands.<br>Linear mode, -8, -9, and -12 exponents supported. |
| 0x242 | VOUT_COMMAND | Read/Write Word | 21h | Sets the voltage to which the device should set the output. Format according to VOUT_MODE. Resolution is 5mV when the IC Vout is configured with a load line. Resolution is 5mV or 0.625 mV when the IC is configured without a load line. |
| 0x248 | VOUT_MAX | Read/Write Word | 24h | Sets an upper limit on the output voltage the unit can command. Format according to VOUT_MODE. |
| 0x24A | VOUT_MARGIN_HIGH | Read/Write Word | 25h | Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE. |
| 0x24C | VOUT_MARGIN_LOW | Read/Write Word | 26h | Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE. |
| 0x24E | VOUT_TRANSITION_RATE | Read/Write Word | 27h | Sets the rate at which the output changes voltage due to VOUT_COMMAND or OPERATION commands. |
| 0x250 | VOUT_DROOP | Read/Write Word | 28h | Allows the user to set the load-line value in resolution of 5/256 Ω. Exponent is 1 |
| 0x252 | VOUT_SCALE_LOOP | Read/Write Word | 29h | Used to account for any external attenuation network on VOUT sense feedback and provide correct VOUT reporting. |
| 0x256 | VOUT_MIN | Read/Write Word | 2Bh | Sets a lower limit on the commanded output voltage. Format according to VOUT_MODE |
| 0x266 | FREQUENCY_SWITCH | Read/Write Word | 33h | Sets the switching frequency in kHz per table found in user note UN0047. Exp = 0, 1 |
| 0x26A | VIN_ON | Read/Write Word | 35h | Sets the value of the input voltage at which the unit should begin power conversion. Exp = -1. |
| 0x26C | VIN_OFF | Read/Write Word | 36h | Sets the value of the input voltage at which the unit, once operation has started, should stop power conversion. Exp = -1. |
| 0x270 | IOUT_CAL_GAIN | Read/Write Word | 38h | Used to calibrate the output current's gain |
| 0x272 | IOUT_CAL_OFFSET | Read/Write Word | 39h | Used to null out any offsets in the output current sensing circuitry. Exp = 2. |
| 0x280 | VOUT_OV_FAULT_ LIMIT | Read/Write Word | 40h | Returns the value of the output voltage, measured at the sense or output pins, that causes an output over voltage fault. |
| 0x282 | VOUT_OV_FAULT_ RESPONSE | Read/Write Byte | 41h | Instructs the device on what action to take in response to an output over voltage |

| | | | | |
|---|---|---|---|---|
| | | | | fault. Only shutdown and ignore are supported. |
| 0x288 | VOUT_UV_FAULT_ LIMIT | Read/Write Word | 44h | Returns the value of the output voltage, measured at the sense or output pins, that causes an output undervoltage fault. |
| 0x28A | VOUT_UV_FAULT_ RESPONSE | Read/Write Byte | 45h | Instructs the device on what action to take in response to an output undervoltage fault.<br>Only shutdown and ignore are supported. |
| 0x28C | IOUT_OC_FAULT_ LIMIT | Read/Write Word | 46h | Sets the value of the output current, in amperes, that causes the over current detector to indicate an over current fault condition. Set by writing this command in Linear format with a -1 exponent. |
| 0x28E | IOUT_OC_FAULT_ RESPONSE | Read/Write Byte | 47h | Instructs the device on what action to take in response to an output over current fault.<br>Only C0h (shutdown immediately), F8h (hiccup forever), and D8 (hiccup 3 times) are supported. |
| 0x29E | OT_FAULT_LIMIT | Read/Write Word | 4Fh | Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over temperature fault. Exp = 0. |
| 0x2A0 | OT_FAULT_RESPONSE | Read/Write Byte | 50h | Instructs the device on what action to take in response to an over temperature fault. Only shutdown and ignore are supported. |
| 0x2A2 | OT_WARN_LIMIT | Read/Write Word | 51h | Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over temperature Warning alarm. Exp = 0. |
| 0x2AA | VIN_OV_FAULT_LIMIT | Read/Write Word | 55h | Sets the value of the input voltage that causes an input over voltage fault. Exp = -4. |
| 0x2AC | VIN_OV_FAULT_RESPONSE | Read/Write Byte | 56h | Instructs the device on what action to take in response to an input over voltage fault. Only shutdown and ignore are supported. |
| 0x2BC | POWER_GOOD_ON | Read/Write Word | 5Eh | Sets the output voltage at which an optional POWER_GOOD signal should be asserted. Format according to VOUT_MODE. |
| 0x2BE | POWER_GOOD_OFF | Read/Write Word | 5Fh | Sets the output voltage at which an optional POWER_GOOD signal should be negated. Format according to VOUT_MODE. |
| 0x2C0 | TON_DELAY | Read/Write Word | 60h | Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Exp = 0. |
| 0x2C2 | TON_RISE | Read/Write Word | 61h | Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exp = 0. |

| | | | | |
|---|---|---|---|---|
| 0x2C8 | TOFF_DELAY | Read/Write Word | 64h | Sets the time (in ms) from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exp = 0. |
| 0x2CA | TOFF_FALL | Read/Write Word | 65h | Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. The TOFF_FALL is limited to 1ms. Exp = 0. |
| 0x2F0 | STATUS_BYTE | Read/Write Byte | 78h | Returns 1 byte where the bit meanings are:<br>Bit <7> Reserved<br>Bit <6> Output off (due to fault or enable)<br>Bit <5> Output over voltage fault<br>Bit <4> Output over current fault<br>Bit <3> Input under voltage fault<br>Bit <2> Temperature fault<br>Bit <1> Communication/Memory/Logic fault<br>Bit <0>: None of the Above |
| 0x2F2 | STATUS_WORD | Read/Write Word | 79h | Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are:<br>Bit <7> Output high or low fault<br>Bit <6> Output over current fault<br>Bit <5> Input voltage or current fault.<br>Bit <4> MFR_SPECIFIC<br>Bit <3> POWR GOOD#<br>Bit <2:0> Not Supported |
| 0x2F4 | STATUS_VOUT | Read/Write Byte | 7Ah | Bit <7> Output over voltage Fault<br>Bit <6> Not Supported<br>Bit <5> Not Supported<br>Bit <4> Output Undervoltage Fault<br>Bit <3> VOUT_MAX Warning<br>Bit <2:0> Not Supported |
| 0x2F6 | STATUS_IOUT | Read/Write Byte | 7Bh | Bit <7> Output over current Fault<br>Bit <6> Not Supported<br>Bit <5> Output over current Warning<br>Bit <4:0> Not Supported |
| 0x2F8 | STATUS_INPUT | Read/Write Byte | 7Ch | Bit <7> Input over voltage Fault<br>Bit <6:0> Not Supported |
| 0x2FA | STATUS_TEMPERATURE | Read/Write Byte | 7Dh | Bit <7> Over temperature Fault<br>Bit <6> Over temperature Warning<br>Bit <5:0> Reserved |
| 0x2FC | STATUS_CML | Read/Write Byte | 7Eh | Returns 1 byte where the bit meanings are: |

| | | | | |
|---|---|---|---|---|
| | | | | Bit <7> Invalid or unsupported command<br>Bit <6> Invalid or unsupported data<br>Bit <5> PEC fault<br>Bit <4:2> Reserved<br>Bit <1> Other communication fault not listed here<br>Bit <0> Reserved |
| 0x310 | READ_VIN | Read Word | 88h | Returns the input voltage in Volts |
| 0x312 | READ_IIN | Read Word | 89h | Returns the input current in Amperes |
| 0x316 | READ_VOUT | Read Word | 8Bh | Returns the output voltage in the format set by VOUT_MODE |
| 0x318 | READ_IOUT | Read Word | 8Ch | Returns the output current in Amperes |
| 0x31A | READ_TEMPERATURE_1 | Read Word | 8Dh | Returns the addressed loop NTC temperature in degrees Celsius |
| 0x32C | READ_POUT | Read Word | 96h | Returns the output power in Watts |
| 0x32E | READ_PIN | Read Word | 97h | Returns the input power in Watts |
| 0x330 | PMBUS_REVISION | Read Byte | 98h | Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2(draft) |
| 0x332 | MFR_ID | Block Read/Write<br>Byte count = 2 | 99h | The MFR_ID is set to IF (Hex 4946) unless programmed differently in the USER registers of the controller. |
| 0x334 | MFR_MODEL | Block Read/Write<br>Byte count = 2 | 9Ah | The MFR_MODEL is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR_Model command returns the value in the USER register for MFR_MODEL. |
| 0x336 | MFR_REVISION | Block Read/Write<br>Byte count = 2 | 9Bh | The MFR_REVISION is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR_REVISION command returns the value in the USER register for MFR_REVISION. |
| 0x35A | IC_DEVICE_ID | Block Read | ADh | Returns a 1-byte code with the following values:<br>A6h = TDA38640A |
| 0x35C | IC_DEVICE_REV | Block Read | AEh | The IC revision that is stored inside the IC |
| 0x382 | MFR_VENDOR_INFO_1 | Read Word,<br>Byte count = 2 | C1h | Returns the product_id and silicon revision |
| 0x384 | MFR_VENDOR_INFO_2 | Read/Write Word<br>Byte count = 2 | C2h | Available for vendor use |
| 0x3A0 | MFR_REG_ACCESS | Block Read/Write<br>Process call | D0h | Read/Write I2C registers |

## 15.5 11-BIT Linear Data Format

Monitored parameters use the Linear Data Format (Figure 25) encoding into 1 Word (2 bytes), where:

$$Value = Y * 2^{N}$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

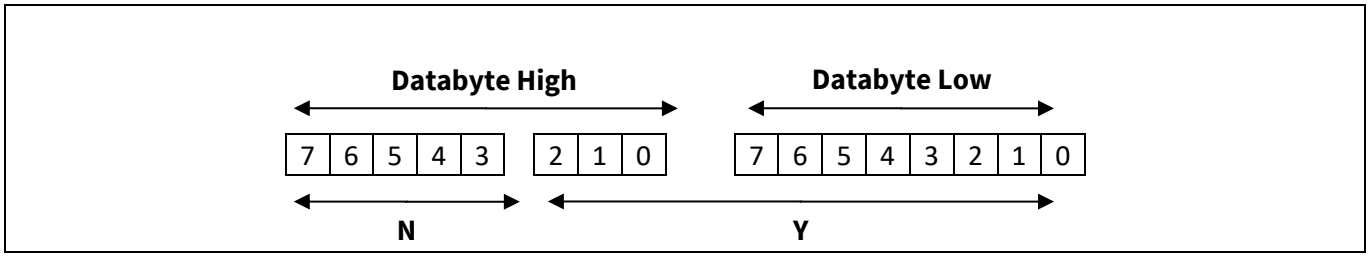



**Figure 25 11-Bit Linear Data Format**

## 15.6 16-BIT Linear Data Format

This format is only used for VOUT related commands (READ_VOUT, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, POWER_GOOD_ON, and POWER_GOOD_LOW):

$$Value = Y * 2^{N}$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

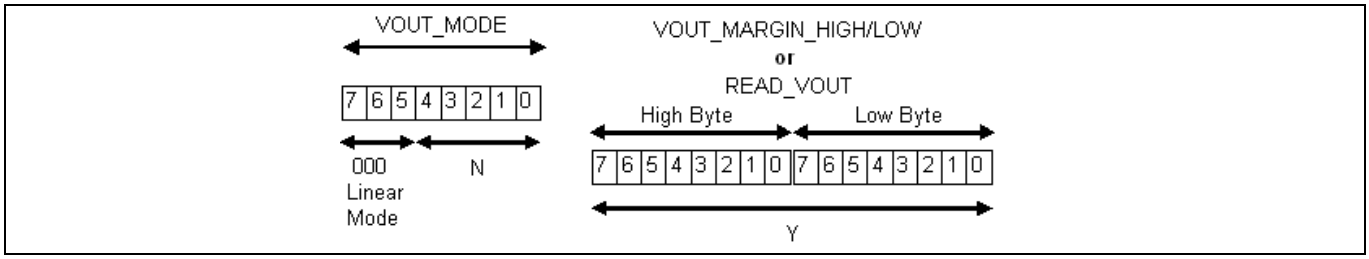



**Figure 26 16-BIT Linear Data Format**

## 15.7 SVID Registers

A list of all the SVID registers is given in Table 21. SVID registers supported by the TDA38640A in VR12.5, VR13, and VR13.HC mode conform to VR12.5, VR13, and VR13.HC specifications respectively.

**Table 21 SVID Registers**

| Register Address | Register Name | Access | VR12.5 Mode | VR13 Mode | VR14 Mode |
|---|---|---|---|---|---|
| 00 | Vendor ID | RO | Supported | Supported | Supported |
| 01 | Product ID | RO | Supported | Supported | Supported |
| 02 | Product Revision | RO | Supported | Supported | Supported |
| 03 | Product Date Code | - | Not Supported | Not Supported | Not Supported |
| 04 | Lot Code | - | Not Supported | Not Supported | Not Supported |
| 05 | Protocol ID | RO | Supported | Supported | Supported |
| 06 | Capability | RO | Supported | Supported | Supported |

| Register Address | Register Name | Access | VR12.5 Mode | VR13 Mode | VR14 Mode |
|---|---|---|---|---|---|
| 07 | Step Size | RO | Not Supported | Not Supported | Not Supported |
| 07 | Vendor Use | RW | Not Supported | Not Supported | Not Supported |
| 08 | Bias VID Table | RO | Not Supported | Not Supported | Not Supported |
| 09 | VIDOMAX_H_CAPA | RO | Not Supported | Not Supported | Supported |
| 0A | VIDOMAX_L | RO | Not Supported | Not Supported | Supported |
| 0B | VIN_FULLSCALE_H | RO | Not Supported | Not Supported | Not Supported |
| 0C | VIN_FULLSCALE_L | RO | Not Supported | Not Supported | Not Supported |
| 0D | VOUT_FULLSCALE_H | RO | Not Supported | Not Supported | Supported |
| 0E | VOUT_FULLSCALE_L | RO | Not Supported | Not Supported | Supported |
| 0F | ALLCALL_ACT | RW | Not Supported | Not Supported | Supported |
| 10 | Status_1 | RO | Supported | Supported | Supported |
| 11 | Status_2 | RO | Supported | Supported | Supported |
| 12 | Temperature | RO | Supported | Supported | |
| 13 | PMIC_GLOBAL_ST | RO | Not Supported | Not Supported | Not Supported |
| 14 | LASTREAD | RO | Not Supported | Not Supported | Supported |
| 15 | IOUT_H | RO | Supported | Supported | Supported |
| 16 | VOUT_H | RO | Supported | Supported | Supported |
| 17 | VR Temperature | RO | Supported | Supported | Supported |
| 18 | Output Power | RO | Supported | Supported | Supported |
| 19 | Input Current | RO | Not Supported | Not Supported | Not Supported |
| 1A | Input Voltage | RO | Not Supported | Not Supported | Not Supported |
| 1B | Input Power | RO | Not Supported | Not Supported | Not Supported |
| 1C | Status 2 Last Read | RO | Supported | Supported | Supported |
| 1D | PARERR_CNT | RO | Not Supported | Not Supported | Not Supported |
| 1E | CFG_FILE_ID | RO | Not Supported | Not Supported | Supported |

| Register Address | Register Name | Access | VR12.5 Mode | VR13 Mode | VR14 Mode |
|---|---|---|---|---|---|
| 1F | Future Command | - | Not Supported | Not Supported | Not Supported |
| 20 | ICC IN Max | RO | Not Supported | Not Supported | Not Supported |
| 21 | ICC Max | RO | Supported | Supported | Supported |
| 22 | Temp Max | RO | Not Supported | Supported | Supported |
| 23 | DC_LL | RO | Not Supported | Not Supported | Not Supported |
| 24 | SR_Fast | RO | Supported | Supported | Supported |
| 25 | SR_Slow | RO | Supported | Supported | Supported |
| 26 | Vboot | RO | Supported | Supported | Supported |
| 27 | VR Tolerance | - | Not Supported | Not Supported | Not Supported |
| 28 | Current-Offset | RW | Not Supported | Not Supported | Not Supported |
| 29 | Temperature Offset | RW | Not Supported | Not Supported | Not Supported |
| 2A | Slow Slew Rate Select | RW | Not Supported | Supported | Supported |
| 2B | PS4 Exit Latency | RO | Not Supported | Not Supported | Supported |
| 2C | PS3 Exit Latency | RO | Not Supported | Not Supported | Supported |
| 2D | Enable to Ready | RO | Not Supported | Not Supported | Supported |
| 2E | Pin Max | RO | Not Supported | Not Supported | Not Supported |
| 2F | Pin Alert Threshold | RW | Not Supported | Not Supported | Not Supported |
| 30 | $V_{OUT}$ Max | RW | Supported | Supported | Supported |
| 31 | VID Setting | RW | Supported | Supported | Supported |
| 32 | Pwr State | RW | Supported | Supported | Supported |
| 33 | Offset | RW | Supported | Supported | Supported |
| 34 | Multi VR Config | RW | Supported | Supported | Supported |
| 35 | MAIN_ADDR_PTR | RW | Not Supported | Not Supported | Not Supported |
| 36 | DC_LL_FINE | RO | Not Supported | Not Supported | Not Supported |
| 37 | Future Command | - | Not Supported | Not Supported | Not Supported |
| 38 | Future Command | - | Not Supported | Not Supported | Not Supported |

| Register Address | Register Name | Access | VR12.5 Mode | VR13 Mode | VR14 Mode |
|---|---|---|---|---|---|
| 39 | Future Command | - | Not Supported | Not Supported | Not Supported |
| 3A | Work Point 0 | RW | Not Supported | Supported | Supported |
| 3B | Work Point 1 | RW | Not Supported | Supported | Supported |
| 3C | Work Point 2 | RW | Not Supported | Supported | Supported |
| 3D | Work Point 3 | RW | Not Supported | Supported | Supported |
| 3E | Work Point 4 | RW | Not Supported | Not Supported | Not Supported |
| 3F | Work Point 5 | RW | Not Supported | Not Supported | Not Supported |
| 40 | Work Point 6 | RW | Not Supported | Not Supported | Not Supported |
| 41 | Work Point 7 | RW | Not Supported | Not Supported | Not Supported |
| 42 | IVID1-VID | RW | Not Supported | Not Supported | Not Supported |
| 43 | IVID1-I | RW | Not Supported | Not Supported | Not Supported |
| 44 | IVID2-VID | RW | Not Supported | Not Supported | Not Supported |
| 45 | IVID2-I | RW | Not Supported | Not Supported | Not Supported |
| 46 | IVID3-VID | RW | Not Supported | Not Supported | Not Supported |
| 47 | IVID3-I | RW | Not Supported | Not Supported | Not Supported |
| 50 | HIGH_PWR | RO | Not Supported | Not Supported | Supported |
| 51 | PWRSTATE_SUP | RO | Not Supported | Not Supported | Supported |
| 52 | PHSHED_SUP | RO | Not Supported | Not Supported | Supported |
| 53 | PHSHED_ACT | RW | Not Supported | Not Supported | Supported |
| 54 | NEGVREN_SUP | RO | Not Supported | Not Supported | Supported |
| 55 | NEGVREN_ACT | RW | Not Supported | Not Supported | Supported |
| 56 | DIGOUT_STATUS | RO | Not Supported | Not Supported | Not Supported |

| Register Address | Register Name | Access | VR12.5 Mode | VR13 Mode | VR14 Mode |
|---|---|---|---|---|---|
| 57 | WP_SLEW_0 | RW | Not Supported | Not Supported | Supported |
| 58 | WP_SLEW_1 | RW | Not Supported | Not Supported | Supported |
| 59 | WP_SLEW_2 | RW | Not Supported | Not Supported | Not Supported |
| 5A | WP_SLEW_3 | RW | Not Supported | Not Supported | Not Supported |
| 5B | WP_SLEW_TT | RW | Not Supported | Not Supported | Supported |
| 60 | CAL_CAPABILITY | RO | Not Supported | Not Supported | Not Supported |
| 61 | CAL_REQUEST | WT | Not Supported | Not Supported | Not Supported |
| 62 | CAL_IMAG_A | RW | Not Supported | Not Supported | Not Supported |
| 63 | CAL_IMAG_B | RW | Not Supported | Not Supported | Not Supported |
| 64 | CAL_STATUS | RO | Not Supported | Not Supported | Not Supported |
| 70 | EXP_ACCURACY | RO | Not Supported | Not Supported | Not Supported |
| 71 | IOUT_L | RO | Not Supported | Not Supported | Not Supported |
| 72 | VOUT_L | RO | Not Supported | Not Supported | Not Supported |
| 73 | POUT_L | RO | Not Supported | Not Supported | Not Supported |
| 74 | IIN_L | RO | Not Supported | Not Supported | Not Supported |
| 75 | VIN_L | RO | Not Supported | Not Supported | Not Supported |
| 76 | PIN_L | RO | Not Supported | Not Supported | Not Supported |
| 77 | PSYS_CR_LVL_L | RW | Not Supported | Not Supported | Not Supported |
| 78 | PSYS_W2_LVL_L | RW | Not Supported | Not Supported | Not Supported |
| 79 | PSYS_W1_LVL_L | RW | Not Supported | Not Supported | Not Supported |
| 7A-BF | RESERVED | | Not Supported | Not Supported | Not Supported |
| C0-FF | VENDOR_RESERVED | RW | Not Supported | Not Supported | Not Supported |

# 16 Design example

In this section, an example is used to explain how to design a buck regulator with the TDA38640A. The design specifications are given below.

- $PV_{in}$ = 12 V (±10%)
- $V_o$ = 1.0 V
- $I_o$ = 40 A
- $V_o$ ripple voltage = ±1% of $V_o$
- Load transient response = ± 3% of $V_o$ with a step load current = 9 A and slew rate = 30 A/µs

## 16.1 Enabling the TDA38640A

The TDA38640A has a precise Enable threshold voltage, the Enable feedback resistor, $R_{EN1}$ and $R_{EN2}$, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN(max)}$ is the maximum spec of the EN-start-threshold as defined in the Absolute Maximum Ratings table. For $PV_{in\ (min)}$ =10.8 V, select $R_{EN1}$=49.9 kΩ and $R_{EN2}$> 3.4 kΩ. Suggested value is $R_{EN2}$=7.5 kΩ.

## 16.2 Programming the Switching Frequency and Operation Mode

The TDA38640A has very good efficiency performance and is suitable for high switching frequency operation. In this case, 800 kHz is selected to achieve a good compromise between efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. The 800 kHz switching frequency and FCCM operation can be selected via register bits.

## 16.3 Selecting Input Capacitors

Without input capacitors, the pulse current of Control MOSFET is provided directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and cause potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Where $I_{RMS}$ is the RMS value of the input capacitor current. $I_o$ is the output current and D is the Duty Cycle. For $I_o$ = 40A and $D_{(max)}$ = 0.09, the resulting RMS current flowing into the input capacitor is $I_{rms}$ = 11.6 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1 - D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1 - D))}$$

Where $\Delta PV_{in}$ is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistance of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For $I_o$ = 40 A, $f_{sw}$ = 800 kHz, ESR = 3 mΩ, and $\Delta PV_{in}$ = 240 mV, $C_{in(min)}$ > 32 µF. To account for the de-rating of ceramic capacitors under a bias voltage, 10 x 22 µF/0805/25 V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

## 16.4 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease with an increase in temperature. It is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (PV_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $PV_{in(max)}$ = Maximum input voltage; $\Delta iL_{max}$ = Maximum peak-to-peak inductor ripple current; $OCP_{max}$ = maximum spec of the OCP limit as defined in Section 14.1, and $I_{sat}$ = inductor saturation current. In this case, select inductor L =150 nH to achieve $\Delta iL_{max}$ = 25% of $I_{omax}$. The $I_{sat}$ should be no less than 56 A.

## 16.5 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the $V_o$ ripple requirement, $C_o$ should satisfy the following criterion.

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where $\Delta V_{or}$ is the desired peak-to-peak output ripple voltage. For $\Delta iL_{max}$= 7.5 A, $\Delta V_{or}$ =20 mV, $f_{sw}$ = 800 kHz, $C_o$ must be larger than 59 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where $\Delta V_{OL}$ is the allowable $V_o$ deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the $C_o$ that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e. $\Delta V_{OL}$= 30 mV, $\Delta I_{o(max)}$ = 9 A), select $C_o$ = ~600 µF. For more accurate estimation of $C_o$, simulation tool should be used to aid the design.

## 16.6 Output Voltage Programming

Output voltage can be programmed with register bits and modified with PMBus or SVID commands, depending on chosen operating mode.

## 16.7 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for the bootstrap capacitor placed between PHASE and BOOT. For applications requiring $PV_{in}$ equal to or above 14 V, a small resistor of 1 - 2 Ω should be used in series with the BOOT pin to ensure the maximum SW node spike voltage does not exceed 20 V.

## 16.8 PVIN, and VCC/LDO bypass Capacitor

Please see the recommendation in 13.4 on the internal LDO. A 10 µF MLCC is selected for the VCC/LDO bypass capacitor and a 4.7 µF MLCC is selected for the PVIN bypass capacitor.

## 16.9 Design Recommendations

Listed below are the design recommendations for an application utilizing TDA38640A.

- A 0 Ω resistor should be connected between Vcc and Vdrv
- A 100 Ω minimum load resistor should be connected across the output
- The GL pin should be floating. It is available for testing purpose only
- Pin 19 should be grounded
- AGND and PGND should be shorted with minimum possible impedance
- Add a 1 µF or a 2.2 µF 0402 ceramic cap across PVIN and PGND for high frequency decoupling
- Check the sequence of PreBias, PVIN, VCC/VDRV and EN to meet the recommended sequence
- Check for proper selection of remote and local sense resistors.
- The LDO output should not be used to power external devices

# 17 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors Vcc/VDRV bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from TDA38640A power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vo. The bypass capacitor shared by VCC and VDRV should be terminated to PGND.
- Place a boot strap capacitor near the TDA38640A BOOT and PHASE pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noises
- On the TDA38640A demo board, AGND pin is connected to the exposed PGND pad with a copper trace.
- Via holes can be placed on PVin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Output voltage sensing in TDA38640A is done differentially using the VOSENP and VOSENM pins.
    - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high-frequency bypass capacitor of 0.1 µF or higher.
    - The ground connection of the remote sensing signal must be terminated at VOSENM pin.
    - The Vo connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VOSENM pin for output voltages greater than 2.5 V.
    - Shield the pair of remote sensing lines with ground planes above and below
    - Do **NOT** connect VOSENM pin and AGND pin in this configuration
- VINSENM and VINSENP lines have to be routed differentially and they should be shielded with ground planes from above and below
- For routing the SVID lines Intel's guidance on the spacing and length of the lines allowed (maximum) should be followed. One should also pay attention to the matching resistors and the pull-up requirements when routing these lines to multiple SVID slaves. All of this information is available in the Intel VR14 PWM spec document.
- The En pin and configuration pins including SM_ADDRS/PROG should be terminated to a quiet ground. On the TDA38640A standard demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

More information about the layout is found in the USER guide for the Eval Board for TDA38640A. For more information on it please get in touch with the respective Sales team member

## 17.1 PCB Metal and Component Placement

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to the "Recommendationd for Board Assembly of Infineon Integrated Packages without Lead" Application note https://ecmpub.infineon.com/dctm-publish/ecmdata/tech_0460/Z8F80291788.pdf.

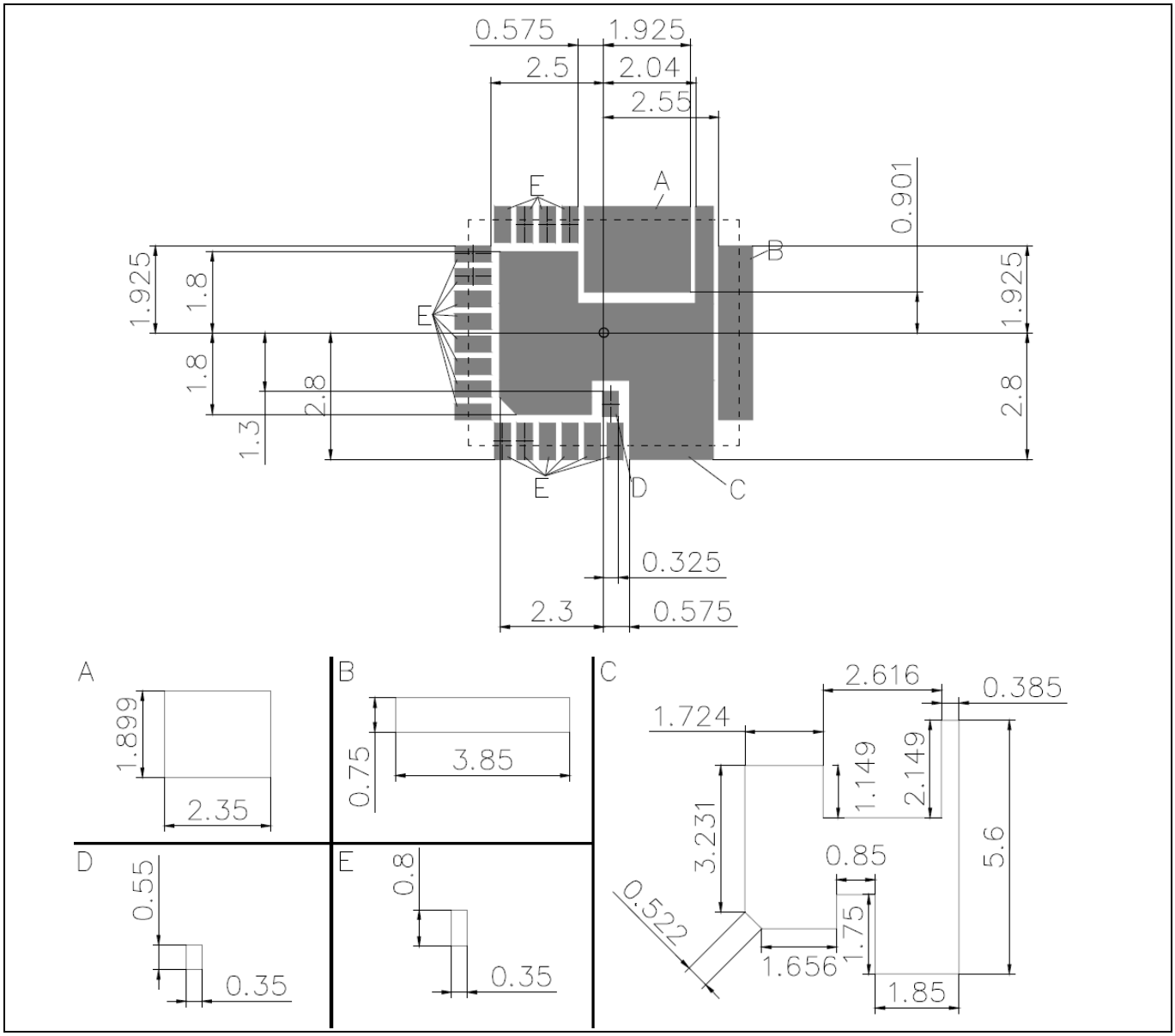



**Figure 27 PCB metal pad sizing and spacing (all dimensions in mm)**

## 17.2 Solder Resist

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1 mm in X & Y.) When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025 mm on each edge, (i.e. 0.05 mm in X&Y,) in order to accommodate any layer to layer misalignment. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

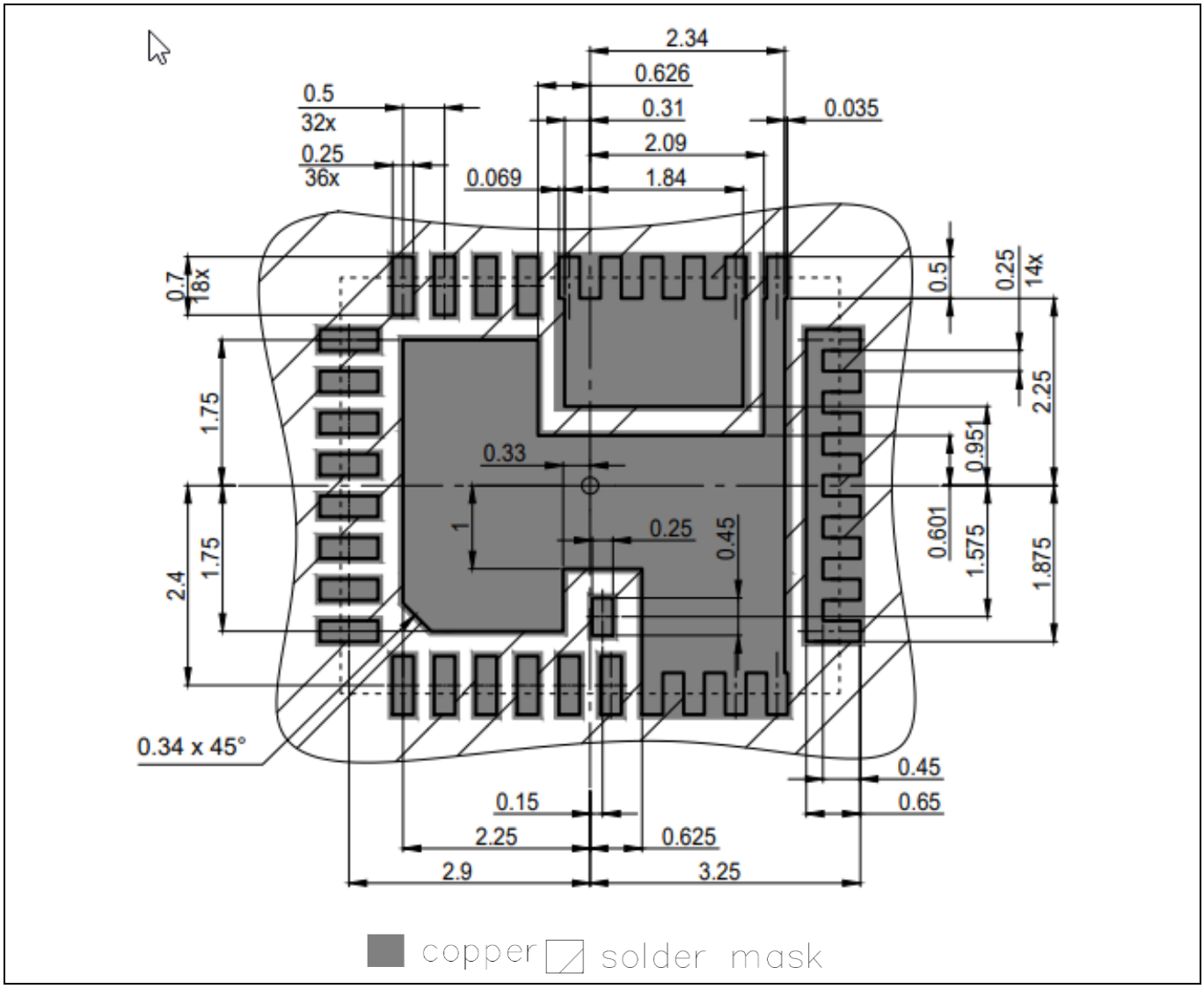



**Figure 28 Solder resist**

## 17.3 Stencil Design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results.

A recommended stencil design is shown in Figure 29. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

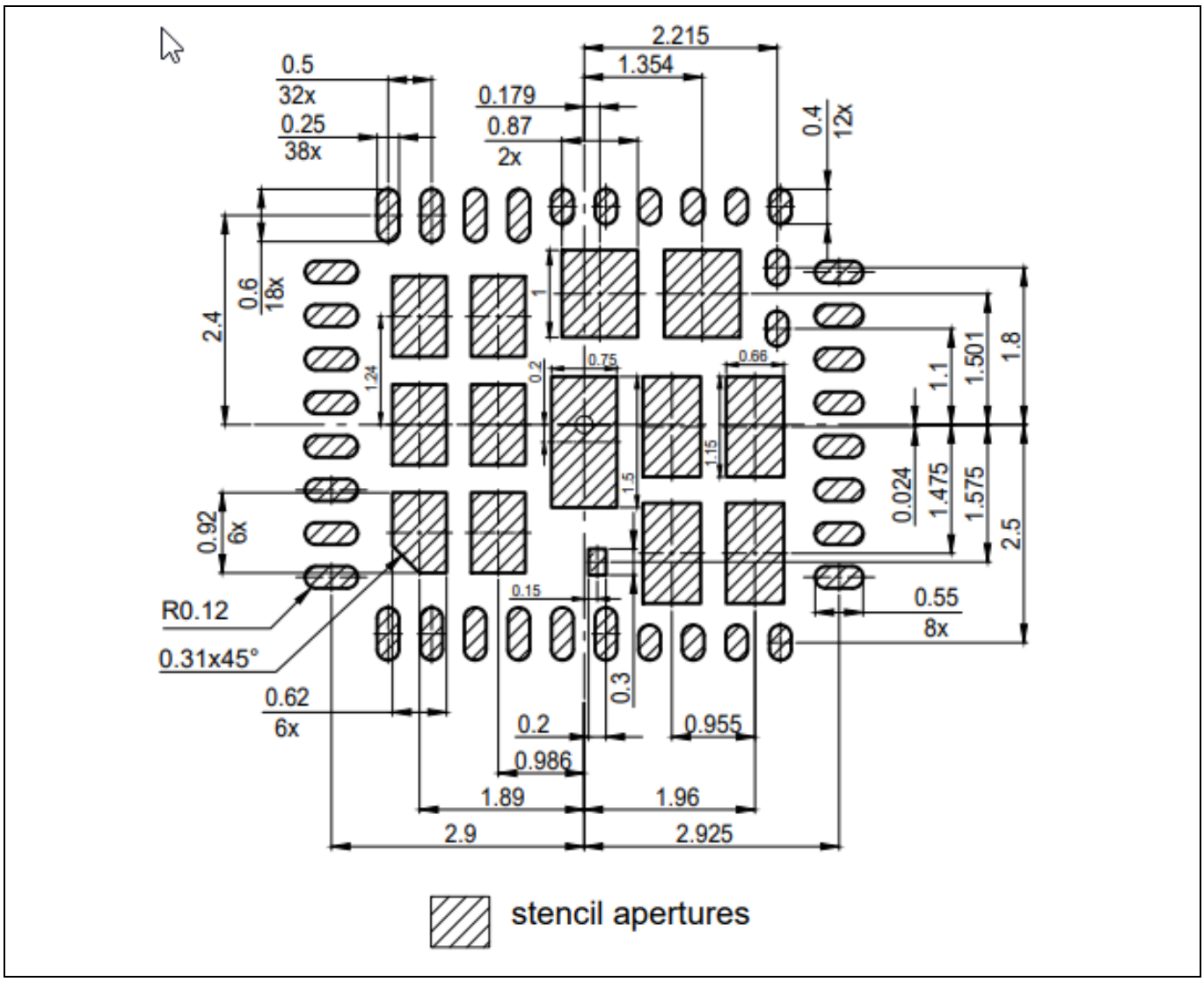



**Figure 29 Stencil pad size and spacing (all dimensions in mm)**

# 18 Package

## 18.1 Marking Information

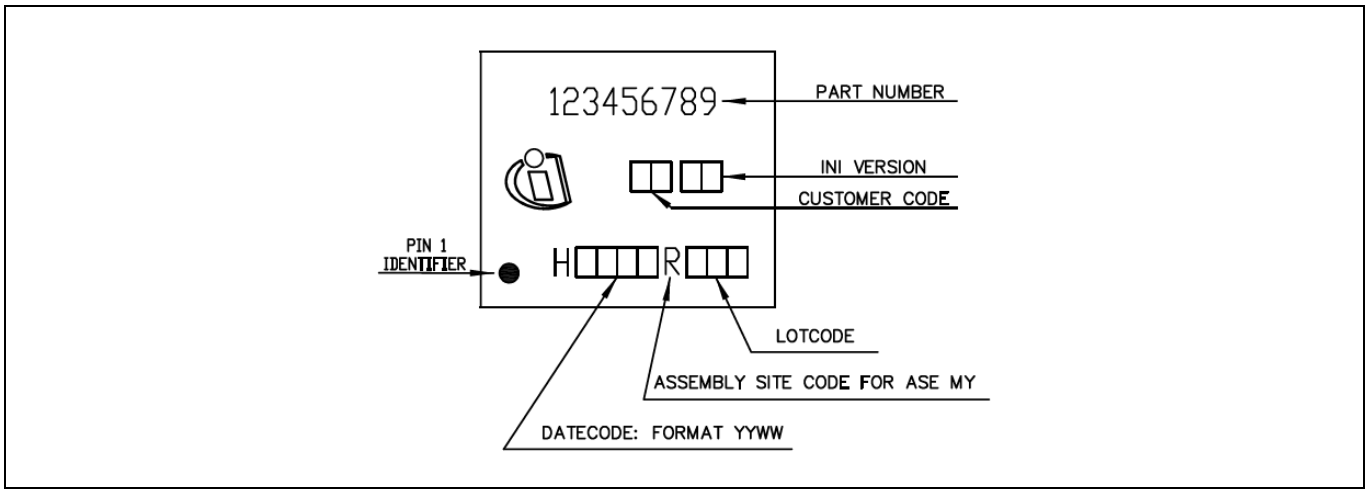



**Figure 30 Package Marking**

## 18.2 Dimensions

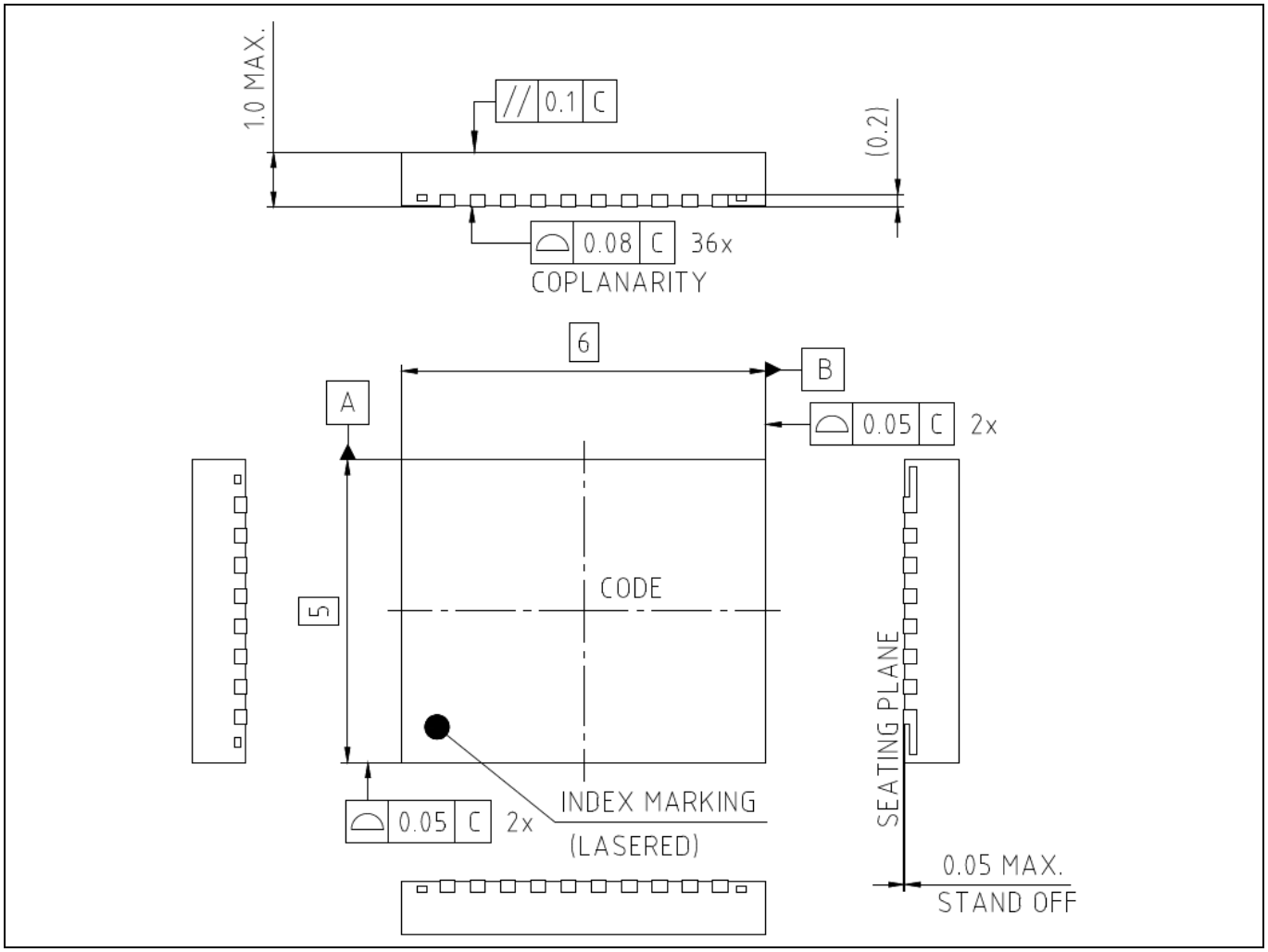
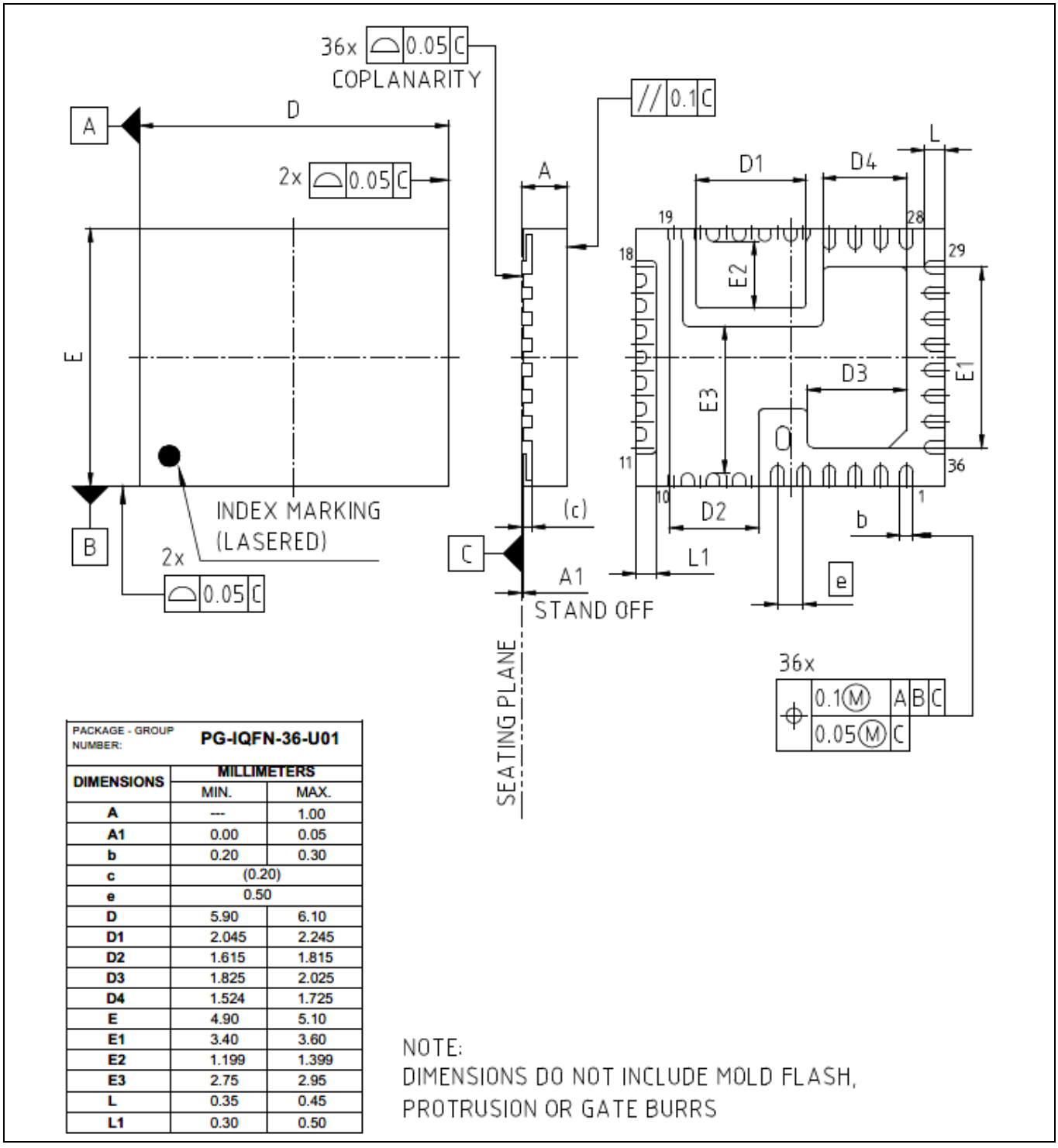



**Figure 31 Package view**




| PACKAGE - GROUP NUMBER: | PG-IQFN-36-U01 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | --- | 1.00 |
| A1 | 0.00 | 0.05 |
| b | 0.20 | 0.30 |
| c | (0.20) | |
| e | 0.50 | |
| D | 5.90 | 6.10 |
| D1 | 2.045 | 2.245 |
| D2 | 1.615 | 1.815 |
| D3 | 1.825 | 2.025 |
| D4 | 1.524 | 1.725 |
| E | 4.90 | 5.10 |
| E1 | 3.40 | 3.60 |
| E2 | 1.199 | 1.399 |
| E3 | 2.75 | 2.95 |
| L | 0.35 | 0.45 |
| L1 | 0.30 | 0.50 |

**Figure 32 Package Dimensions in mm**

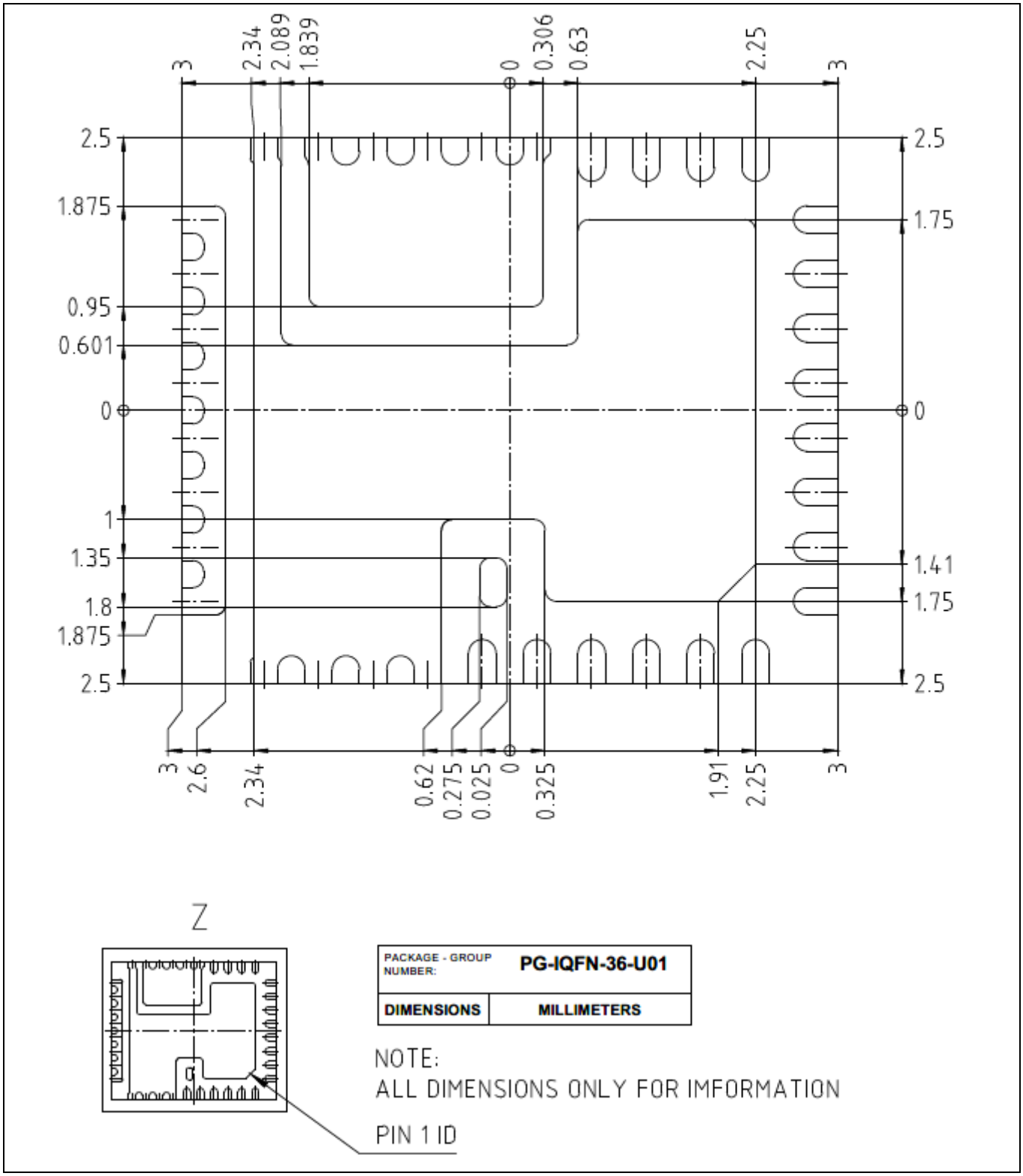



**Figure 33 Package Dimensions- Pad Layout**

## 18.3 Tape and Reel Information

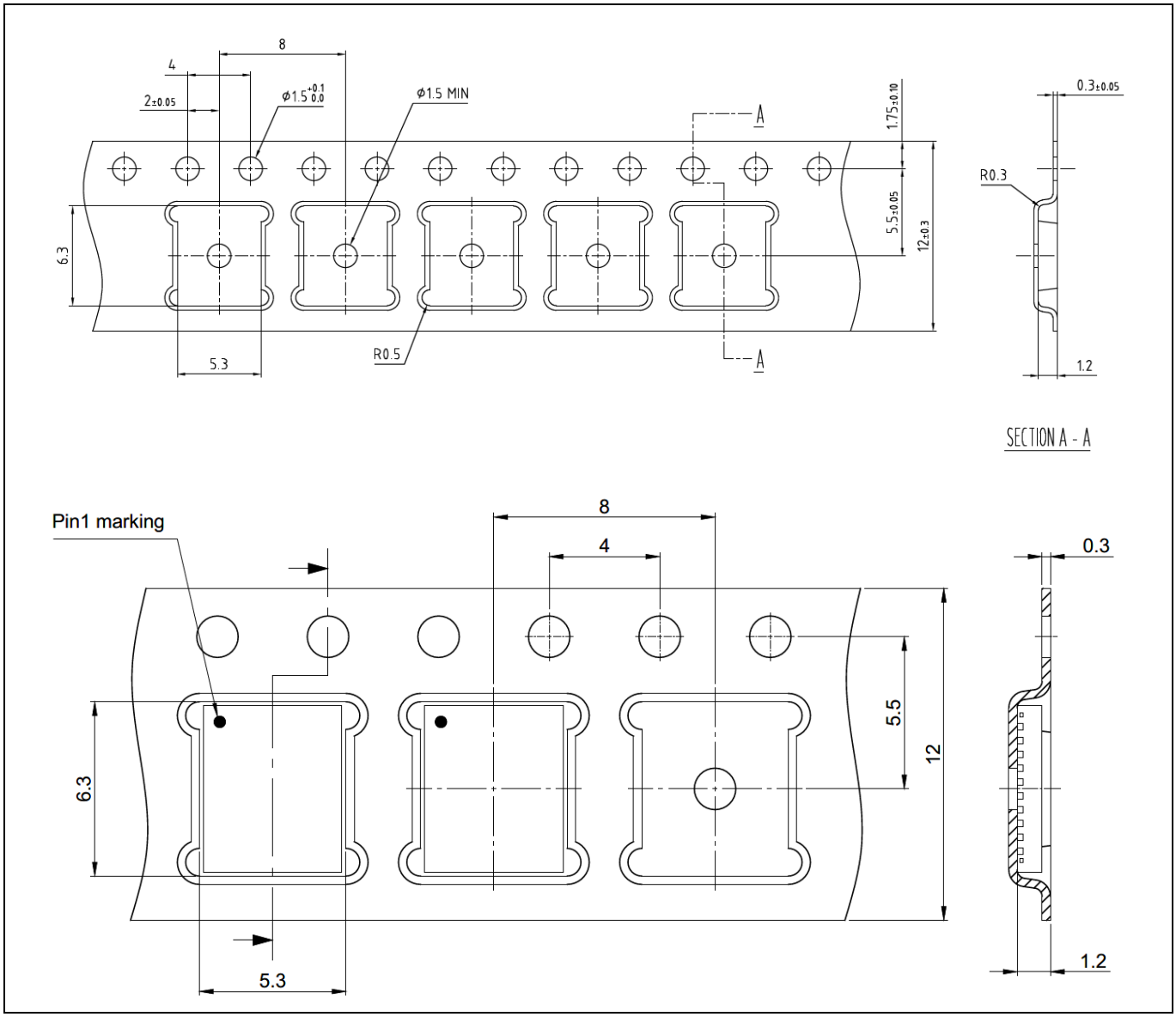



**Figure 34 Pin 1 orientation in the Tape & reel**

# 19 Environmental Qualifications

**Table 22**

| | | | |
|---|---|---|---|
| **Qualification Level** | | **Industrial** | |
| **Moisture Sensitivity** | | 5 x 6 mm QFN Package | JEDEC Level 2 @ 260°C |
| **ESD** | **Human Body Model** | ANSI/ESDA/JEDEC JS-001, Class 2 (2000 V to < 4000 V) | |
| | **Charged Device Model** | ANSI/ESDA/JEDEC JS-002, Class C3 (≥ 1000 V) | |
| **RoHS2 Compliant** | | This product follows EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU(RoHS) and contains Pb according RoHS exemption 7a, Lead in high melting temperature type solders | |

## Revision History

TDA38640A

### Revision 2024-07-09, Rev. 2.1

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2024-04-29 | Release of final |
| 2.1 | 2024-07-09 | Update EC table – Improved UVP and OVP accuracy Updated table 13 – Changes to SM_ADDR/PROG pin operation Updated Device_ID address in Table 20 Updated section 13.5 Enable – EN cycling not required after VBOOT UVLO |



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