TDA38807

6 A synchronous Buck regulator

Features

- Wide Input Voltage Range: 4 V to 16 V with internal bias and 2.7 V to 16 V with external VCC (3.3 V)
- Precision Reference Voltage (0.9 V +/- 0.5%)
- Stable with Ceramic Output Capacitors
- No External Compensation
- Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency
- Selectable Switching Frequency from 600 kHz, 1100 kHz, and 2 MHz
- Programmable Soft-Start Time with a minimum of 1.5 ms & Enhanced Pre-Bias Start-Up
- Voltage Tracking with External Reference Input
- Programmable Over Current Protection Limit with Internal Thermal Compensation
- Enable input with Voltage Monitoring Capability
- Power Good Output
- Latch-off OCP, UVP, Thermal Shutdown and OVP
- Operating Temp: -40 °C < T_j < 125 °C
- Small Size: 2 mm x 3 mm QFN-14
- Lead-free, Halogen-free and RoHS Compliant

Potential applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The TDA38807 is a 6 A fully integrated and highly efficient DC - DC Buck regulator. It uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast control response during the transients while maintaining excellent line and load regulation. It can operate over a wide range of input voltage (2.7 V to 16 V) using an external bias supply.

TDA38807 is a versatile regulator, offering switching frequency selectable from 600 kHz, 1.1 MHz and 2 MHz, programmable current limit and soft-start time with a minimum of 1.5 ms, Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM) operation. The TDA38807 supports voltage tracking with an external reference input. It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage, under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions. The TDA38807 is available in a standard QFN-14 (2mm x 3mm) package and is able to operate over a wide temperature range (-40 °C < Tj < 125 °C).

Table of contents

1 Ordering Information

1. Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
TDA38807	QFN-14	Tape and Reel	3000	TDA38807XUMA1

TDA38807 ——

A1 — Designator

Packing type	Tape & Reel
Moisture protection packing	Dry
Packing size	330 mm

UM —

Halogen Free	Yes
RoHS compliant	Yes
Total lead free	Yes

X —

PGND VCC

14 13

PGND 1

MODE 12

SW 2

SW 11

VIN 3

BST 10

CS 4

PGOOD 9
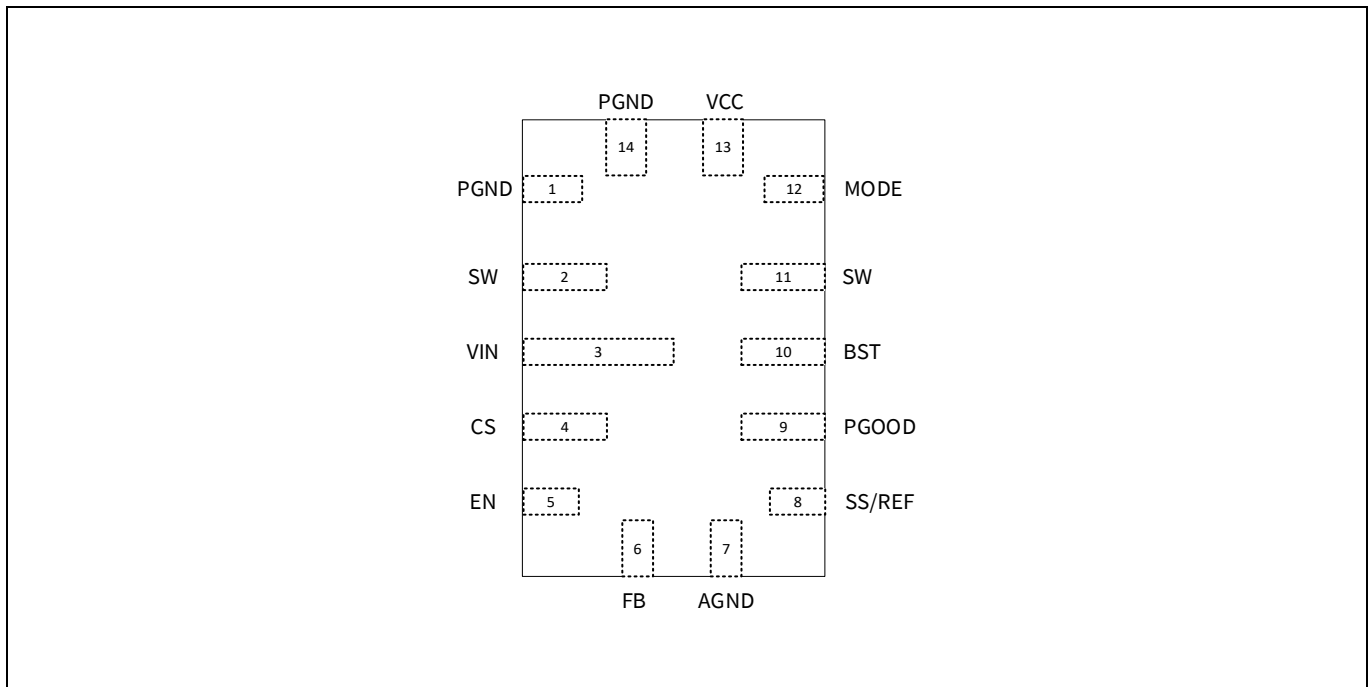
EN 5

SS/REF 8

6 7

FB AGND

Figure 1 Package Top View – TDA38807
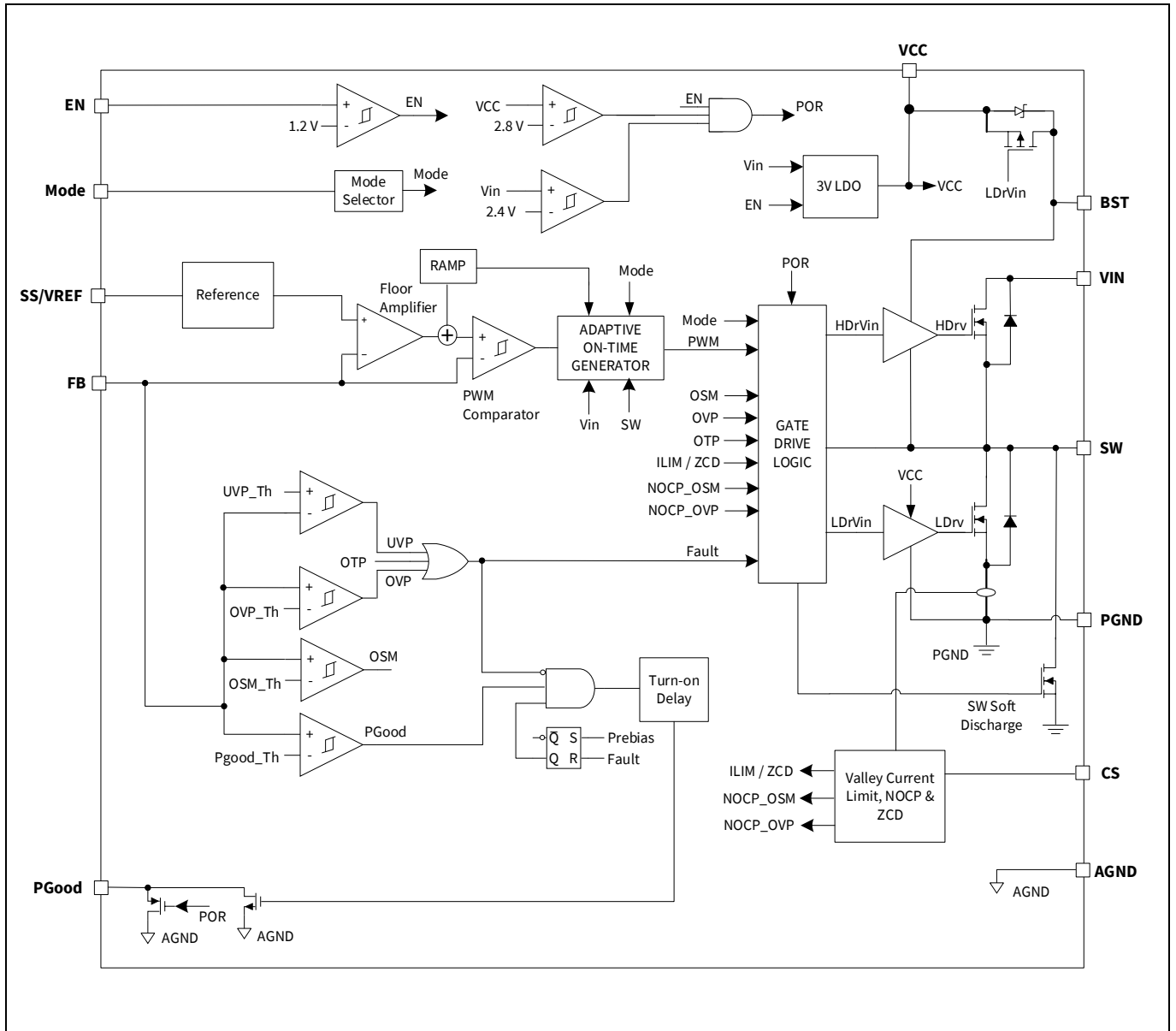
2 Functional Block Diagram

Figure 2   Block Diagram

3 Typical Application Diagram

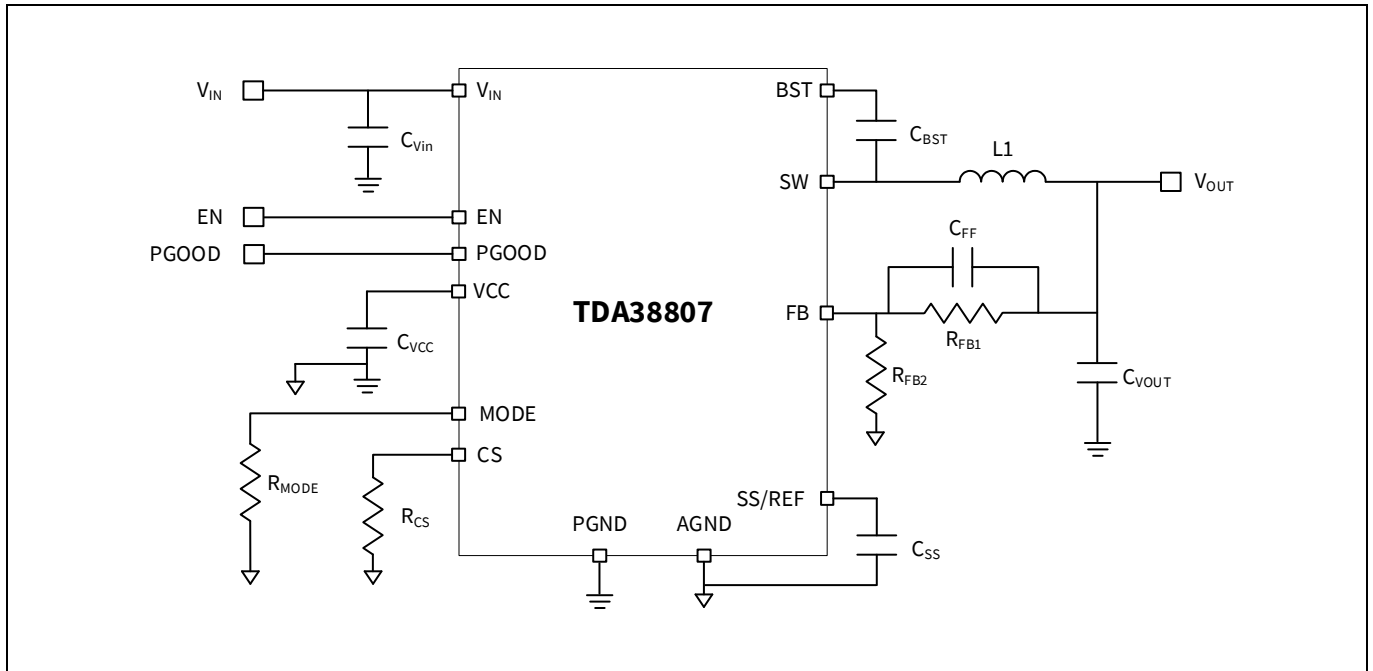**Figure 3** TDA38807 application circuit

4   Pin Descriptions

Note: *I = Input, O = Output*

Pin#	Pin Name	I/O	Type	Pin Description
1,14	PGND	-	Ground	System ground. PGND is the reference ground return. For this reason, care must be taken in PCB layout. Use wide PCB traces to make the connection.
2,11	SW	O	Power	Switch Node output. Connect SW to the inductor and bootstrap capacitor. SW is driven up to the V_{IN} voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.
3	VIN	I	Power	Input voltage. V_{IN} supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Place decoupling capacitors close to VIN and PGND. Use wide PCB traces to make the connection.
4	CS	I	Analog	Current Limit; connect a resistor to AGND to set the current limit trip point.
5	EN	I	Analog	Enable; EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator, drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN Pin.
6	FB	I	Analog	Feedback; An external resistor divider from the output to AGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces. Place a feed-forward capacitor (C_{FF}) between output and FB to optimize load transient response.
7	AGND	-	Ground	Signal Ground for the control circuit. AGND and PGND must be connected on PCB with a single ground connection.
8	SS/REF	I	Analog	Input pin for external reference to support voltage tracking. Decouple with a ceramic capacitor as close to SS/REF pin possible. The capacitance of this capacitor also determines the soft-start time.
9	PGOOD	O	Analog	Power good output. This is an open-drain signal. A pull-up resistor (connected to a DC voltage) is required to indicate high if the output voltage is within regulation. There is about 1 ms delay from FB ≥ 92.5% of V_{REF} to PGOOD pull-high.
10	BST	I	Analog	Supply voltage for the high side driver. Connect this pin to the SW pin through a bootstrap capacitor.
12	MODE	I	Analog	Operation mode selection. Program MODE to select FCCM, DEM, and the operating switching frequency.
13	VCC	I/O	Power	Internal 3V LDO output. The driver and control circuits are powered from this voltage. Decouple with a minimum 2.2 µF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.

TDA38807
6 A synchronous Buck regulator
Absolute maximum ratings

5 Absolute maximum ratings

Absolute maximum ratings

Description	Min	Max	Unit	Conditions
VIN	-0.3	18	V	Note **1**
VCC	-0.3	4.0	V	Note **1**
EN	-0.3	18	V	
SW to PGND	-0.3 (dc), -5 V for 5 ns	VIN (dc) 25 V for 5 ns	V	Note **1**
VIN to SW	-0.3 (dc), -5 V for 5 ns	VIN (dc) 25 V for 5 ns	V	Note **1**
BST to PGND	-0.3 V(dc)	V_{SW} + 4.0 V	V	Note **1**
BST to SW	-0.3	4.0	V	
PGND to AGND	-0.3	0.3	V	
CS, FB, PGOOD, MODE, SS/REF to AGND	-0.3	4.0	V	Note **1**
Junction Temperature Range	-40	150	°C	
Storage Temperature Range	-55	150	°C	

Note:

1. *PGND and AGND pin are connected together.*

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal Characteristics

6.1 Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	32.2 °C/W	Note **2**
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	20 °C/W	Note **2**
Junction to Case Top Thermal Resistance	θ_{JC}	36.8 °C/W	Note **3**

Note:

2. *Simulated using TDA38807 evaluation board (Dimensions: 3in. x 3.15in., 4 Layer FR-4 PCB).*
3. *Simulated standalone thermal characteristics. Measured between junction and center on the package top.*

7 Electrical specifications

7.1 Recommended operating conditions

Description	Min	Max	Unit	Note
VIN Voltage Range with External VCC	2.7	16	V	Note **4**
VIN Voltage Range with Internal LDO	4	16	V	
VCC Supply Voltage Range	3.12	3.6	V	
Output Voltage Range	0.9	5.5	V	
Continuous Output Current Range		6	A	
OCP Limit (Valley)		6.6	A	
Peak current		8	A	
Switching Frequency	600	2000	kHz	
Operating Junction Temperature	-40	125	°C	

Note:

4. *External bias voltage is connected to VCC pin.*

7.2 Electrical characteristics

Note: *Unless otherwise specified, the specifications apply over, VIN = 12V, in -40 °C < T_j < 125 °C. Typical values are specified at T_a = 25 °C.*

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	Rds(on)_Top	$V_{BST} - V_{SW}$ = 3.0 V, I_O = 3A, T_j = 25 °C		25.7		mΩ
Bottom Switch	Rds(on)_Bot	VCC = 3.0 V, Io = 3A, T_j = 25 °C		9.9		
SW float voltage	Vsw	EN = 0 V			400	mV
		EN = high, No Switching			400	mV
DeadBand Time	Tdb	SW node rising edge, Note **7**		1.2		ns
		SW node falling edge, Note **7**		6		
Supply Current						
VIN Supply Current (standby)	Iin (standby)	EN = Low, No Switching, T_j = 25 °C		2.7	10	µA
VIN Supply Current (static)	Iin (static)	EN = 2 V, No Switching, T_j = 25 °C		1.05	1.2	mA
Soft Start						
Soft Start Sourcing current	Iss_source	SS = 0 V		16		µA
Soft Start Sinking current	Iss_sink	SS = 1 V		6.8		µA
Minimum SS time	Tss_min	C_{SS} = 1nF, T_j = 25 °C	1	1.5	2	ms
Feedback Voltage						
Feedback Voltage	Vfb			0.9		V
Accuracy		0°C < T_j < 85 °C, Note **5**		0.5		%
		-40 °C < T_j < 125 °C, Note **5**		1		
On-Time Timer Control						
On-Time	Ton	Mode = VCC, Vin=12V, Vout=1.8V, DEM, Fsw = 1100 kHz, Note **6**	130	144	160	ns
		Mode = GND, Vin=12V, Vout=1.8V, FCCM, Fsw = 1100 kHz, Note **6**				
		Mode = 243 kΩ, Vin=12V, Vout=1.8V, DEM, Fsw = 2000 kHz, Note **6**	75	84	95	
		Mode = 30.1 kΩ, Vin=12V, Vout=1.8V, FCCM, Fsw = 2000kHz, Note **6**				
		Mode = 121 kΩ, Vin=12V, Vout=1.8V, DEM, Fsw = 600 kHz, Note **6**	233	259	285	
		Mode = 60.4 kΩ, Vin=12V, Vout=1.8V, FCCM, Fsw = 600 kHz, Note **6**				
Minimum On-Time	Ton (min)	V_{FB} = 0V, Fsw = 1100 kHz		23		ns

Electrical specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum Off-Time	Toff (min)	V_{FB} = 500 mV, V_O = 5V, V_{IN} = 5.5V, F_{SW} = 1100KHz, FCCM Mode, No Load		184		ns
VCC LDO Output						
Output Voltage	Vcc		2.88	2.99	3.12	V
VCC load regulation		Icc = 25 mA, SS/Vref=0V		0.5		%
Short Circuit Current limit	Ishort	4 V ≤ Vin ≤ 16 V		260		mA
Foldback current limit	Ifoldback	Vin = 4 V, Tj = 25C, Note **7**		14		mA
Under Voltage Lockout						
VIN UVLO Rising Threshold	VINUVLO-Rise	Vcc_ext = 3.3 V	2.1	2.4	2.7	V
VIN UVLO Falling Threshold	VINUVLO-Fall	Vcc_ext = 3.3 V	1.55	1.8	2.15	V
VCC-Start Threshold	Vcc_UVLO_Start	VCC Rising Trip Level	2.65	2.8	2.95	V
VCC-Stop Threshold	Vcc_UVLO_Stop	VCC Falling Trip Level	2.35	2.5	2.65	
Enable-Start-Threshold	En_UVLO_Start	ramping up	1.15	1.2	1.3	V
Enable Hysteresis	En_hysteresis			0.21		
Input Impedance	R_{EN}		500	1050	1800	kΩ
Soft shutdown discharge FET	R_{ON_DISCH}	Note **7**		75		Ω
Over Current Limit						
Current Limit Threshold	Vcs		1.15	1.2	1.25	V
ICS to IOUT ratio	Gcs	Iout >= 2A	36	40	44	µA/A
Negative current limit	NOCP_OSM			-3		A
	NOCP_OVP			-3		A
Output OVP and UVP						
OVP Trip Threshold	OVP_Vth	FB Rising	113	116	119	% Vref
OSM Rising Threshold	OSM_Vth_Rising			104		
OSM Falling Threshold	OSM_Vth_Falling			102		
UVP Trip Threshold	UVP_Vth	FB Falling	77	80	83	
Power Good		VPG (upper)				
Pgood Turn on Threshold	VPG (Upper)	FB Rising	89.5	92.5	95.5	% Vref
Pgood Turn off Threshold	VPG (Lower)	FB Falling	77	80	83	
		OVP Condition	113	116	119	

Electrical specifications

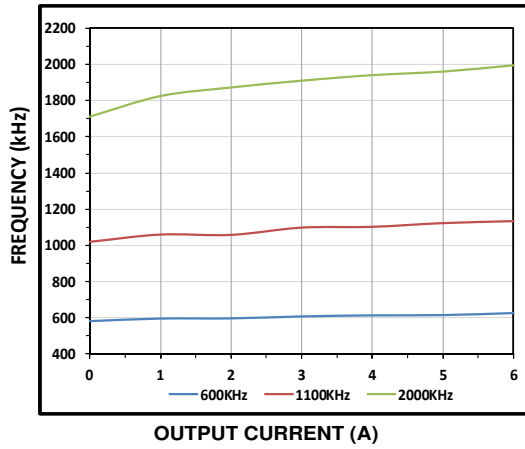| Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pgood Voltage Low	VPG (low)	IPG = 10 mA, Powered ON			100	mV
		VIN = VCC = 0 V, IPG = 2 mA, Rpull-up ≥2 kΩ to 3.3 V		0.49	0.65	V
Pgood Turn on Delay	VPG (on)_Dly	FB Rising, see VPG (upper)	0.7	1	1.3	ms
Pgood Leakage Current		PG = 3.3 V			10	µA
Thermal Shutdown						
Thermal Shutdown		Note **7**		150		°C

Note:

5. *Hot and cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*

6. *Ton is trimmed so that the target switching frequency of 1100 kHz is achieved at around 3 A load current for a 12Vin and 1.8Vout operation.*

7. *Guaranteed by construction and not tested in production.*

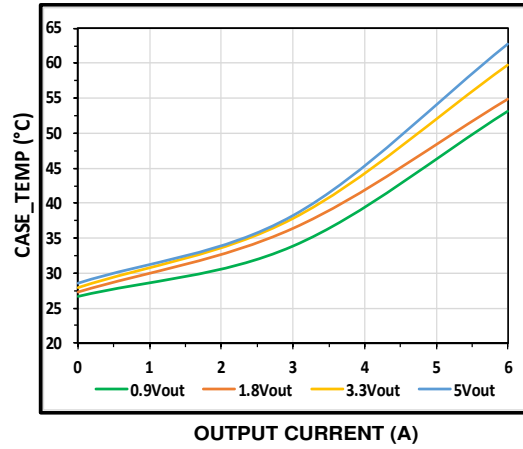# 8   Typical Efficiency and Performance Characteristics

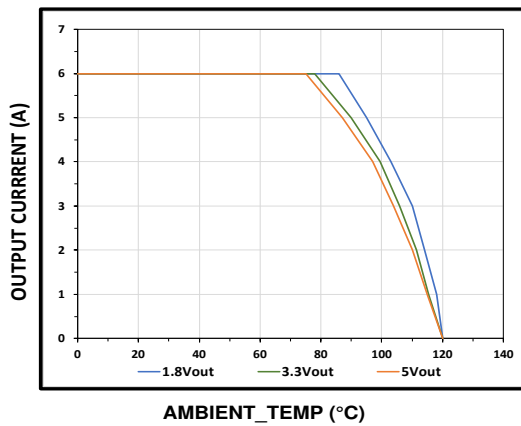*Note:*   *VIN = 12V, VOUT = 1.8V, Fsw = 1.1MHz, L = 1µH, TA = +25°C, unless otherwise Specified*

Efficiency
DEM

Efficiency
FCCM

Efficiency
FCCM, 1µH

Load Regulation

Power Loss
DEM

Power Loss
FCCM

Typical Efficiency and Performance Characteristics
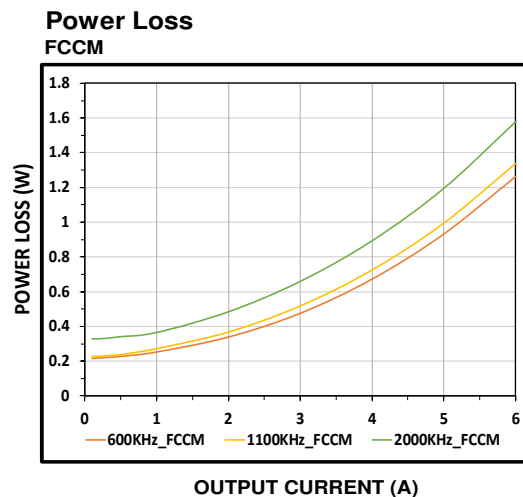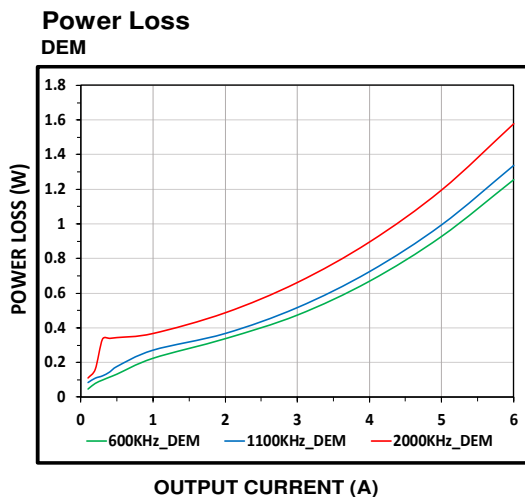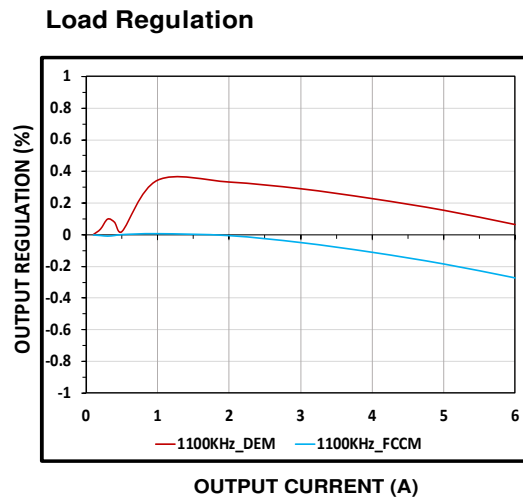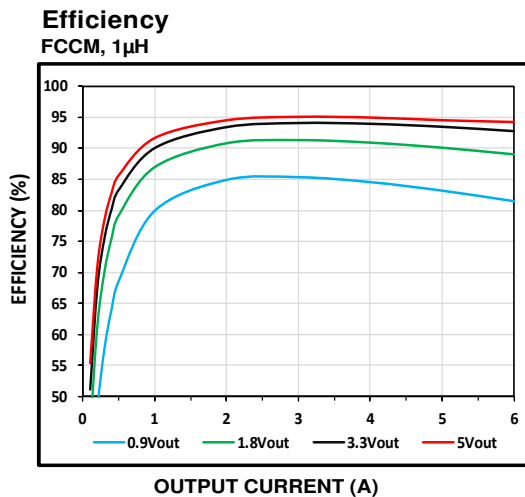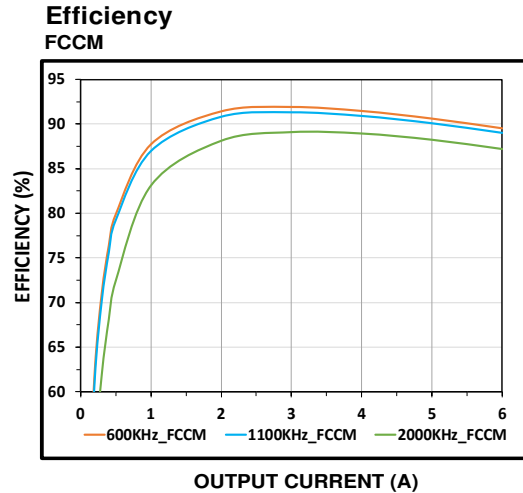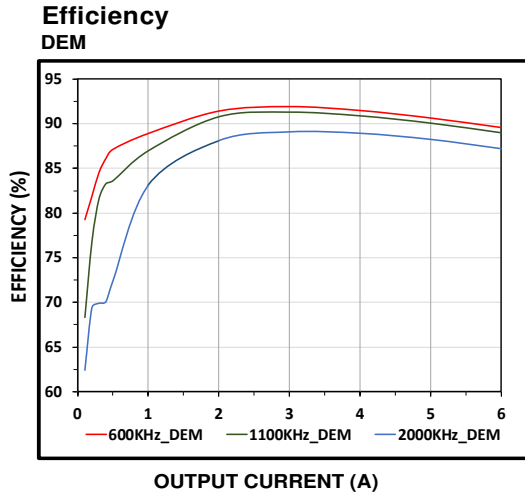
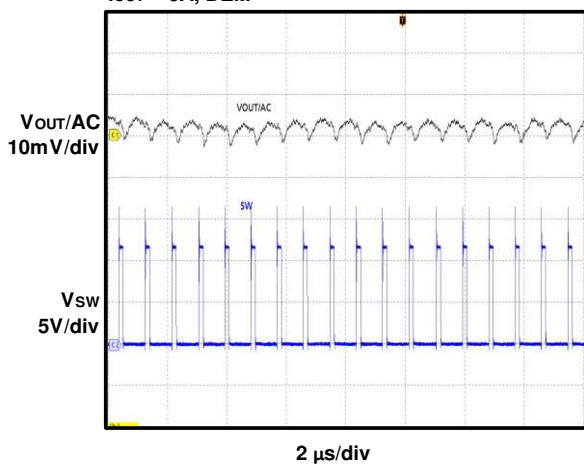### Switching Frequency vs Output Current

Thermal
No Air-Flow

Thermal Derating

Steady State
I_OUT = 0A, DEM
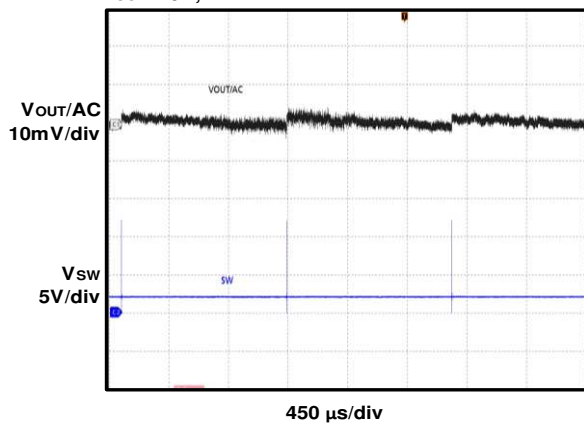
450 µs/div

Steady State
I_OUT = 0.5A, DEM

2 µs/div

Steady State
I_OUT = 6A, DEM

2 µs/div

Steady State
I_{OUT} = 0A, FCCM

2 µs/div

Steady State
I_{OUT} = 6A, FCCM

2 µs/div

Load Transient
I_{OUT} = 0A-3A, 2.5A/µs, DEM

200 µs/div

Load Transient
I_{OUT} = 0A-3A, 2.5A/µs, FCCM

200 µs/div

Power-Up through EN
I_{OUT} = 0A, DEM

2 ms/div
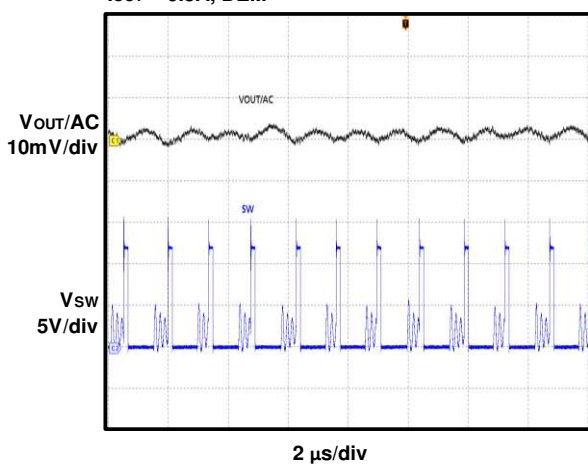
Power-Up through EN
I_{OUT} = 6A, DEM
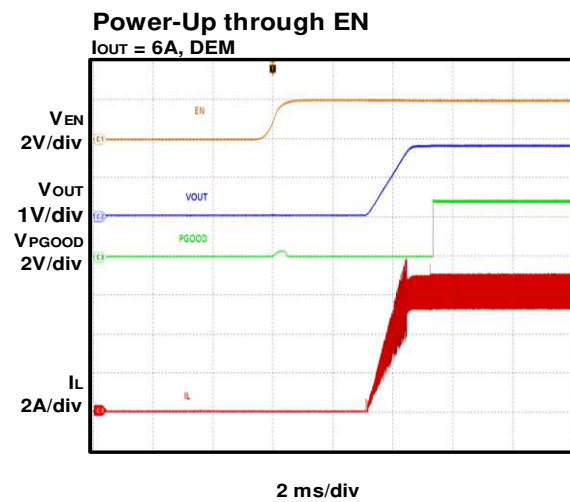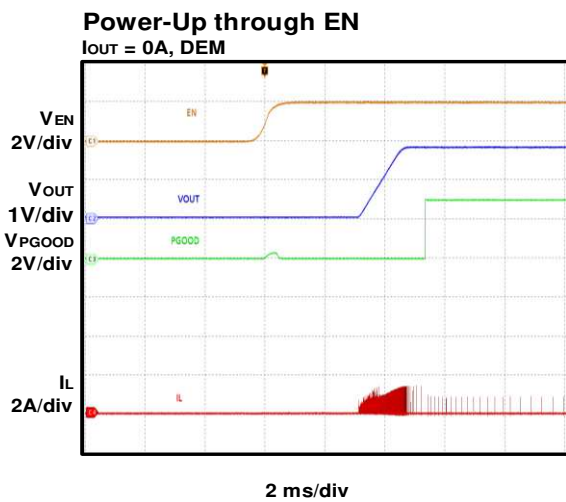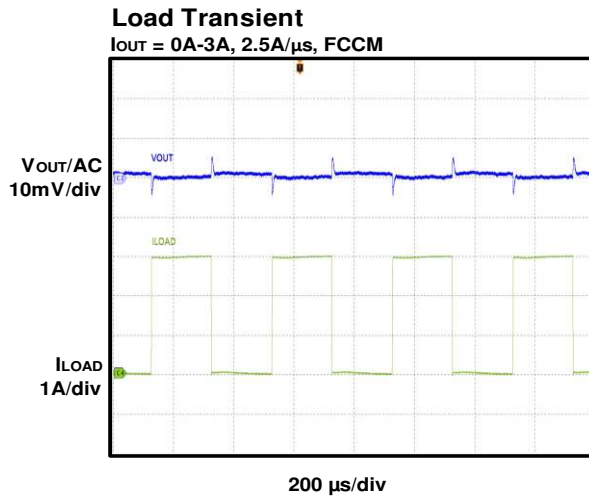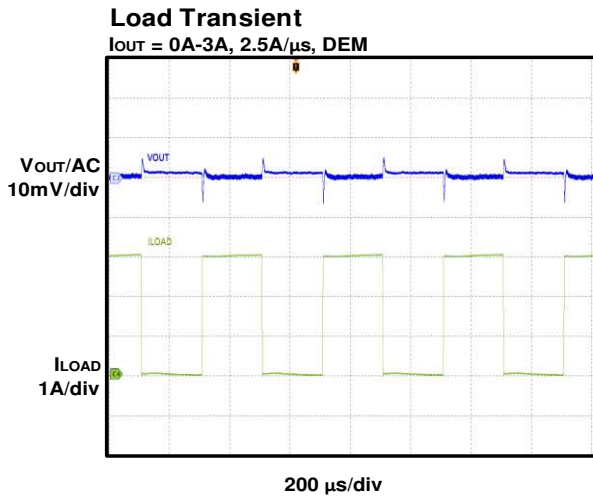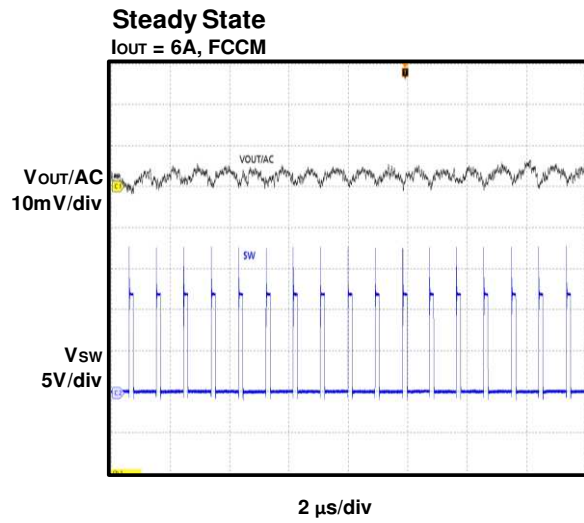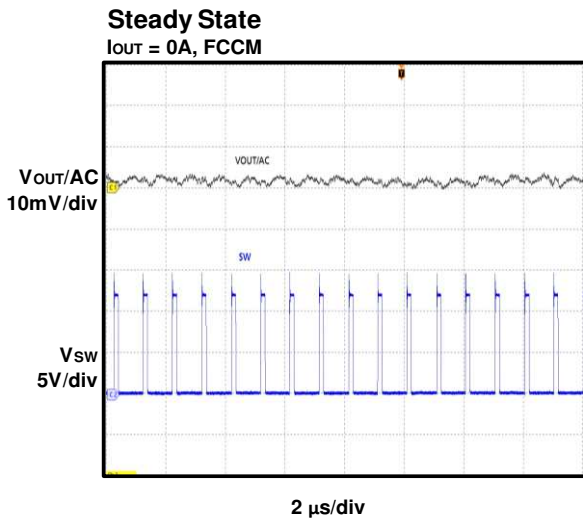
2 ms/div

Power-Up through EN
I_{OUT} = 0A, FCCM
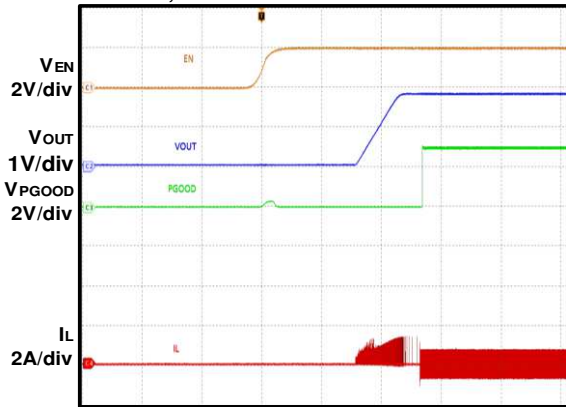
2 ms/div

Power-Up through EN
I_{OUT} = 6A, FCCM
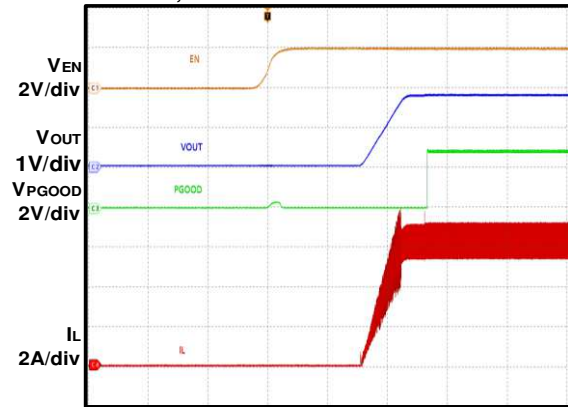
2 ms/div

Power-Down through EN
I_{OUT} = 0A, DEM
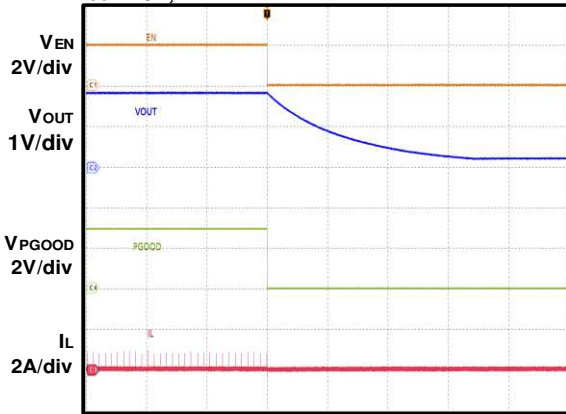
10 ms/div

Power-Down through EN
I_{OUT} = 6A, DEM
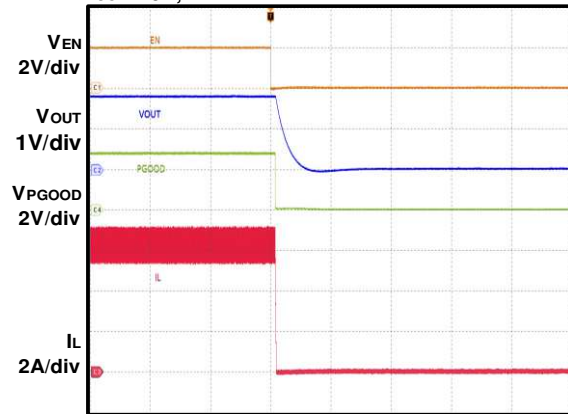
200 µs/div

Power-Down through EN
I_{OUT} = 0A, FCCM
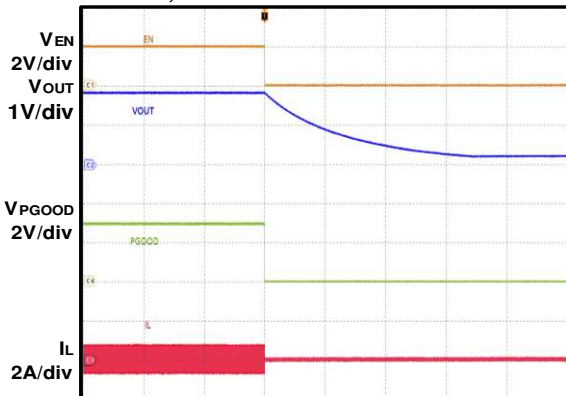
10 ms/div

Power-Down through EN
I_{OUT} = 6A, FCCM

200 µs/div

Typical Efficiency and Performance Characteristics

Pre-Bias Start-Up
DEM, No Load
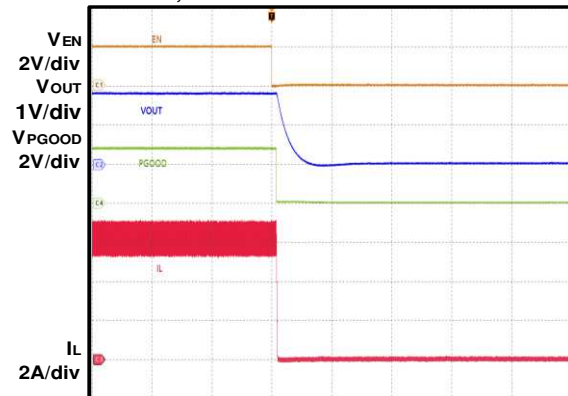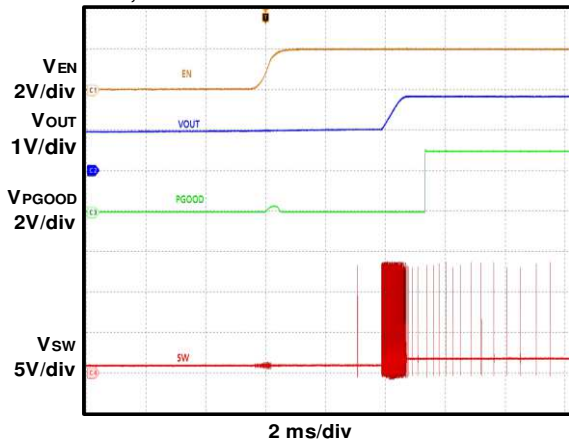
2 ms/div

Pre-Bias Start-Up
FCCM, No Load
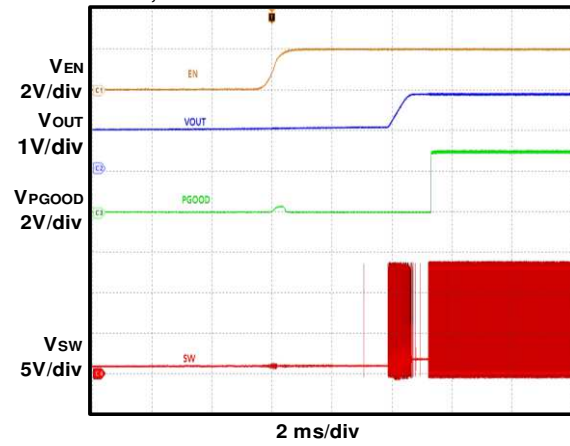
2 ms/div

Over-Current Protection
DEM
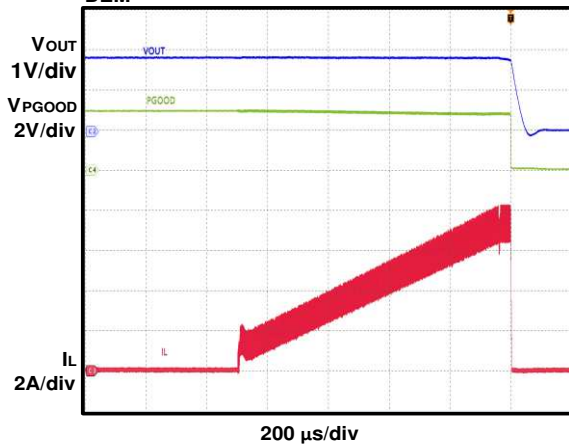
200 μs/div

Over-Current Protection
FCCM

200 μs/div

OSM Operation
DEM

40 ms/div

OSM Operation
FCCM

20 ms/div

Typical Efficiency and Performance Characteristics
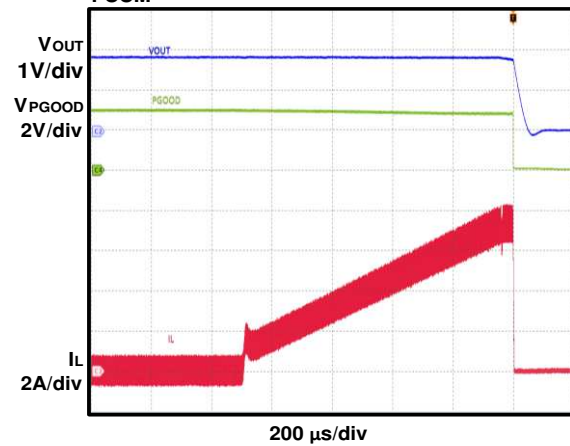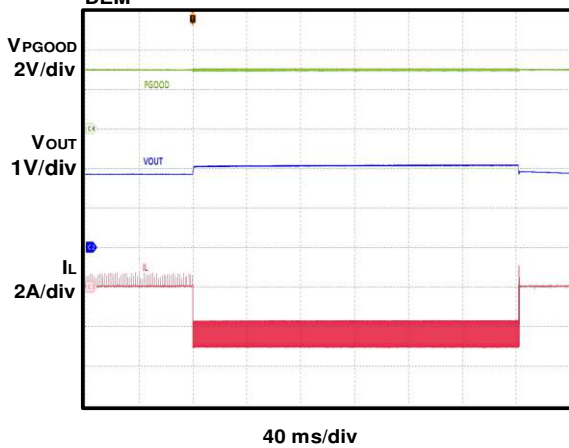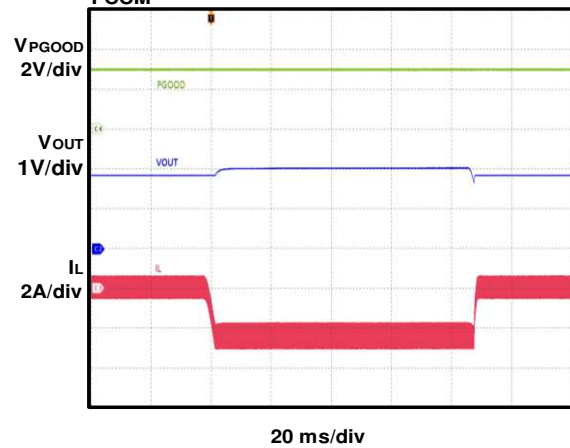
Over-Voltage Protection
DEM
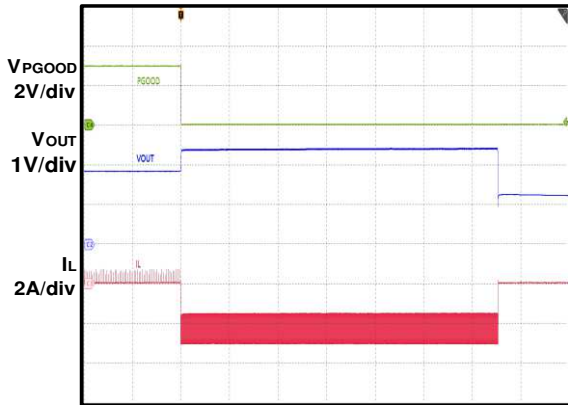
40 ms/div

Over-Voltage Protection
FCCM

40 ms/div

TDA38807
6 A synchronous Buck regulator
Theory of operation
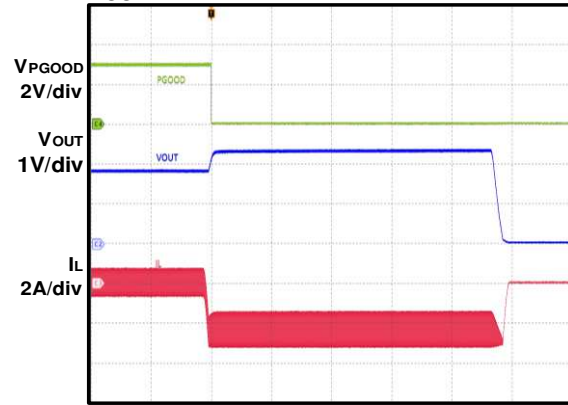
9 Theory of operation

9.1 Fast Constant On-Time Control

The TDA38807 features a proprietary fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize the design effort. Fast COT control compares the output voltage, V_{OUT}, to a floor voltage combined with an internal ramp signal. When V_{OUT} drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vout with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves the Vout regulation.

9.2 FCCM and DEM Operation

The TDA38807 offers two operation modes: Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38807 always operates as a synchronous buck converter with a pseudo-constant switching frequency leading to small output voltage ripple. In DEM, the synchronous FET is turned off when the inductor current is close to zero, reducing the switching frequency and improving efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected with the MODE pin, as shown in **Table 1**. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new MODE configuration, EN or VCC voltage must be cycled.

9.3 Pseudo-Constant Switching Frequency

The TDA38807 offers three programmable switching frequencies, F_{SW}, from 600 kHz to 2 MHz, by connecting an external resistor from the MODE pin to AGND. Based on the selected F_{SW}, the TDA38807 generates the corresponding on-time of the Control FET for a given V_{IN} and V_{OUT}, as shown by the formula below.

$$T_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}$$

Where F_{SW} is the desired switching frequency. During operation, the TDA38807 monitors V_{IN} and V_{OUT}, and can automatically adjust the on-time to maintain the pre-selected F_{SW}. As load current increases, the switching frequency can increase to compensate for power losses.

Table 1 lists the configurations for MODE pin. In this table, E96 resistor with ±1% tolerance is used. To load a new MODE configuration, EN or VCC voltage must be cycled.

Table 1   Configuration of Mode Pin

MODE pin	Freq (kHz)	Mode
AGND	1100	FCCM
30.1 kΩ to AGND	2000	
60.4 kΩ to AGND	600	
VCC	1100	DEM
243 kΩ to AGND	2000	
121 kΩ to AGND	600	

9.4 Enable

EN pin controls the on/off state of the TDA38807. An internal Under Voltage Lock-Out (UVLO) circuit monitors the EN voltage. When the EN voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts. The EN pin can be configured in three ways, as shown in **Figure 4** Enable Configurations. With configuration 2, the EN signal is

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derived from the VIN voltage by a resistor divider, R_{EN1} and R_{EN2}. By selecting different divider ratios, users can program a UVLO threshold for the bus voltage. This is a very desirable feature because it prevents the TDA38807 from operating until VIN is higher than a desired voltage level. For some space-constrained designs, the EN pin can be directly connected to VIN without using the external resistor divider, as shown in Configuration 3. The EN pin should not be left floating. A pull-down resistor in the range of tens of kilohms is recommended.
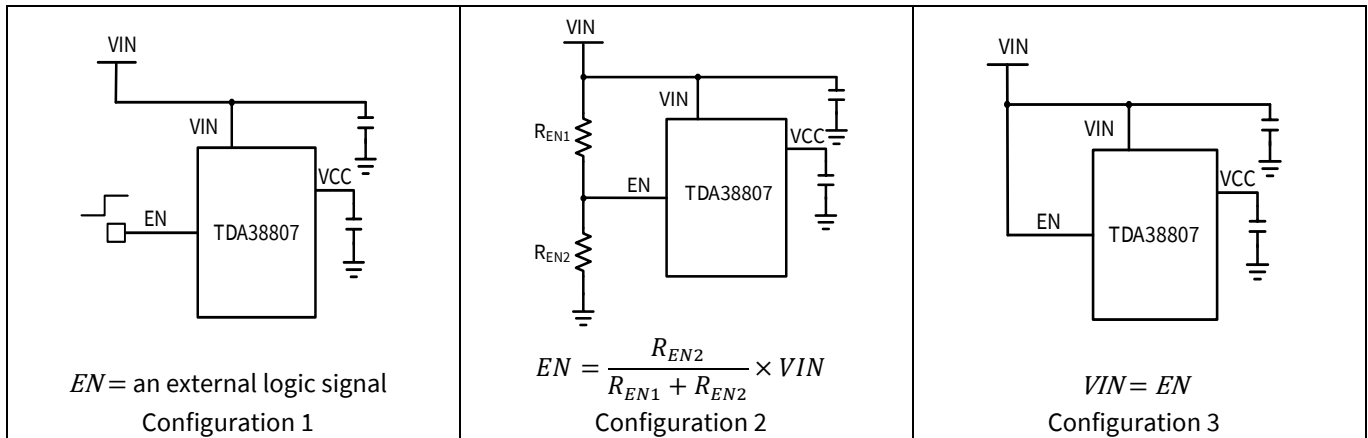

EN = an external logic signal
Configuration 1

$$EN = \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \times VIN$$

Configuration 2

$VIN = EN$
Configuration 3

Figure 4   Enable Configurations

9.5   Soft-start

The TDA38807 has an internal digital soft start to control the output voltage rise and to limit the current surge at start-up. To ensure proper start-up, the soft-start sequence initiates when the EN and VCC voltages rise above their respective thresholds. When EN and VCC rise above the threshold, the part does not soft start for 400 µs (typical) where it reads the MODE pin and any external reference voltage applied on SS/VREF pin. Then the internal soft start signal linearly rises from 0 V to 0.9 V in a defined time duration. The soft-start time does not change with the output voltage. During soft start, the TDA38807 operates in DEM until 1 ms after the output voltage ramps above the PGood turn-on threshold. The TDA38807 has a minimum soft start time of 1.5 ms. A longer soft start time can be set by adding capacitance between SS/VREF and GND. The soft start capacitance required can be calculated using,

$$C_{SS}\ (nF) = \frac{t_{SS}\ (ms) \times 10\mu A}{0.9\ (V)}$$

where, C_{SS} is recommended to be a minimum of 3.3 nF.

9.6   Pre-bias Start-up

The TDA38807 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When the TDA38807 starts up with a pre-biased output voltage, both control FET and Sync FET are kept OFF until the SS/REF voltage exceeds the FB voltage.

9.7   Voltage Tracking and External Reference

The TDA38807 supports voltage tracking and external reference voltage with the use of SS/REF pin. When no external voltage is sensed on the SS/REF pin, the part will use the internal reference voltage (0.9 V). When an external reference voltage is connected between SS/REF and AGND, it acts as reference for the output voltage. The feedback (FB) voltage follows this external voltage signal.

During the power on delay, a detection circuit senses the voltage on the SS/REF pin. Right before this sensing occurs, an internal 120 Ω resistor tries to discharge the voltage on SS/REF pin for 100 µs. The discharge circuit

makes sure that any left-over energy in the SS/REF capacitor is not detected as the voltage reference. The detection circuit senses the SS/REF voltage 40 µs after the discharge circuit is turned off. If the detection circuit senses the voltage on the SS/REF pin to be higher than 90% of internal reference, it will use the SS/REF pin voltage as the new reference for PGood, V_{OUT} OVP and UVP thresholds. The part powers up using internal soft start and PGood is high 1 ms after FB pin reaches the rising threshold. If the detection circuit senses the SS/REF voltage to be lower than 90% of internal reference, it will use the internal reference voltage for the PGood, V_{OUT} OVP and UVP thresholds. For soft start, FB follows the slower one among the internal soft start or external SS/REF pin. Once the PGood is high, the reference voltage is transitioned from the internal reference to the voltage on SS/REF pin.

During startup, the SS/REF voltage must reach a minimum voltage equal to the internal reference (0.9 V) to ensure proper operation. After soft start is complete and Pgood is high, the SS/REF input signal can be in the range of 0.4 V to 1.2 V. The slew rate of the track voltage must be limited to 1 mV/us. To overdrive the SS/REF during normal operation, the external source must be able to sink more than 10 µA of current when the external reference is lower than the internal reference. Or it should be able to source a current more than 6 µA when the external reference is higher than internal reference.

During ramping down of the external track voltage down to zero, the PGood goes low after the SS/REF pin voltage reaches 100 mV. While tracking below 100 mV, the part would enter a latch off OVP and would require an EN or V_{CC} recycle to power back up.

(a) Startup sequence with voltage tracking

(b) Startup sequence with external reference
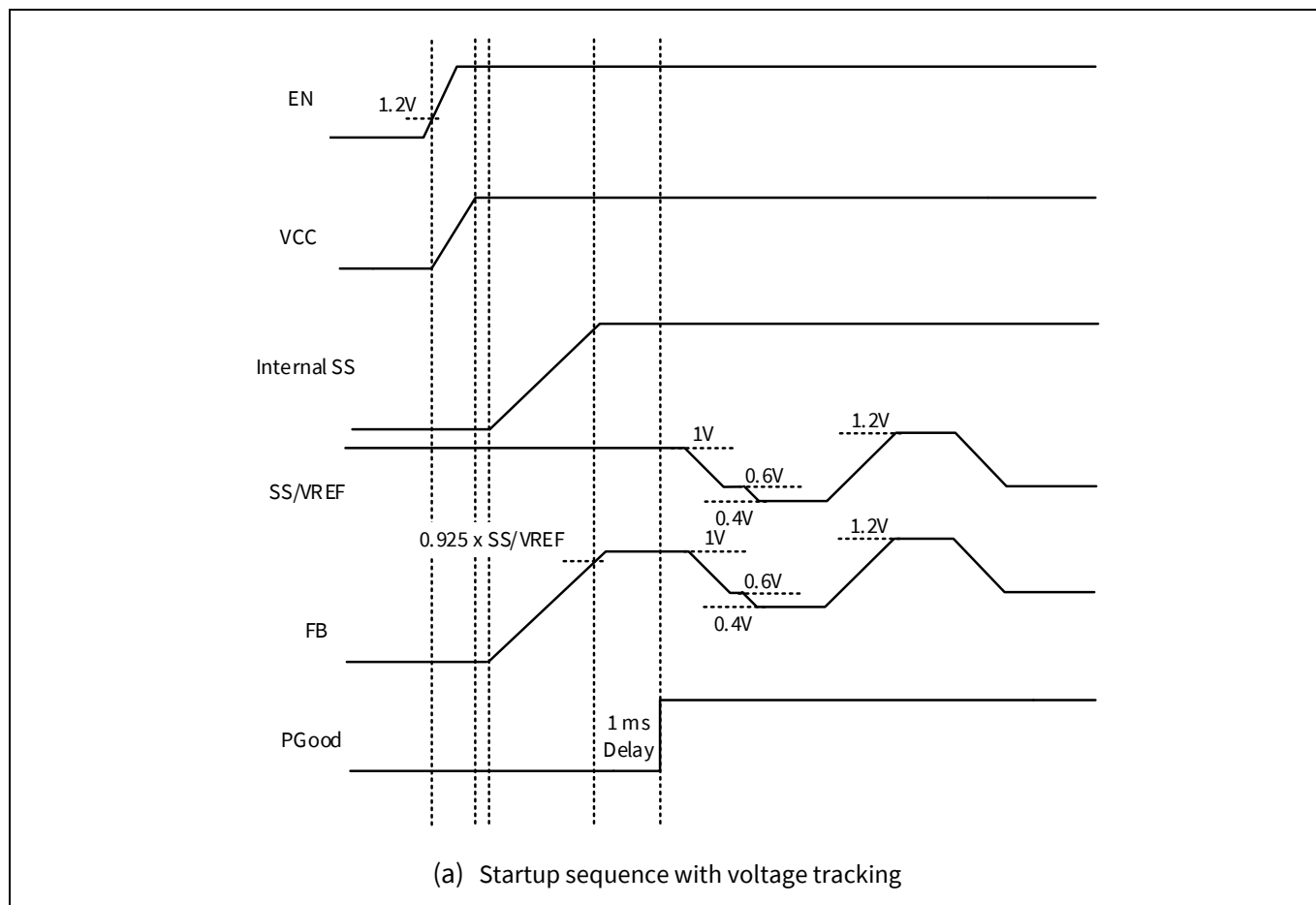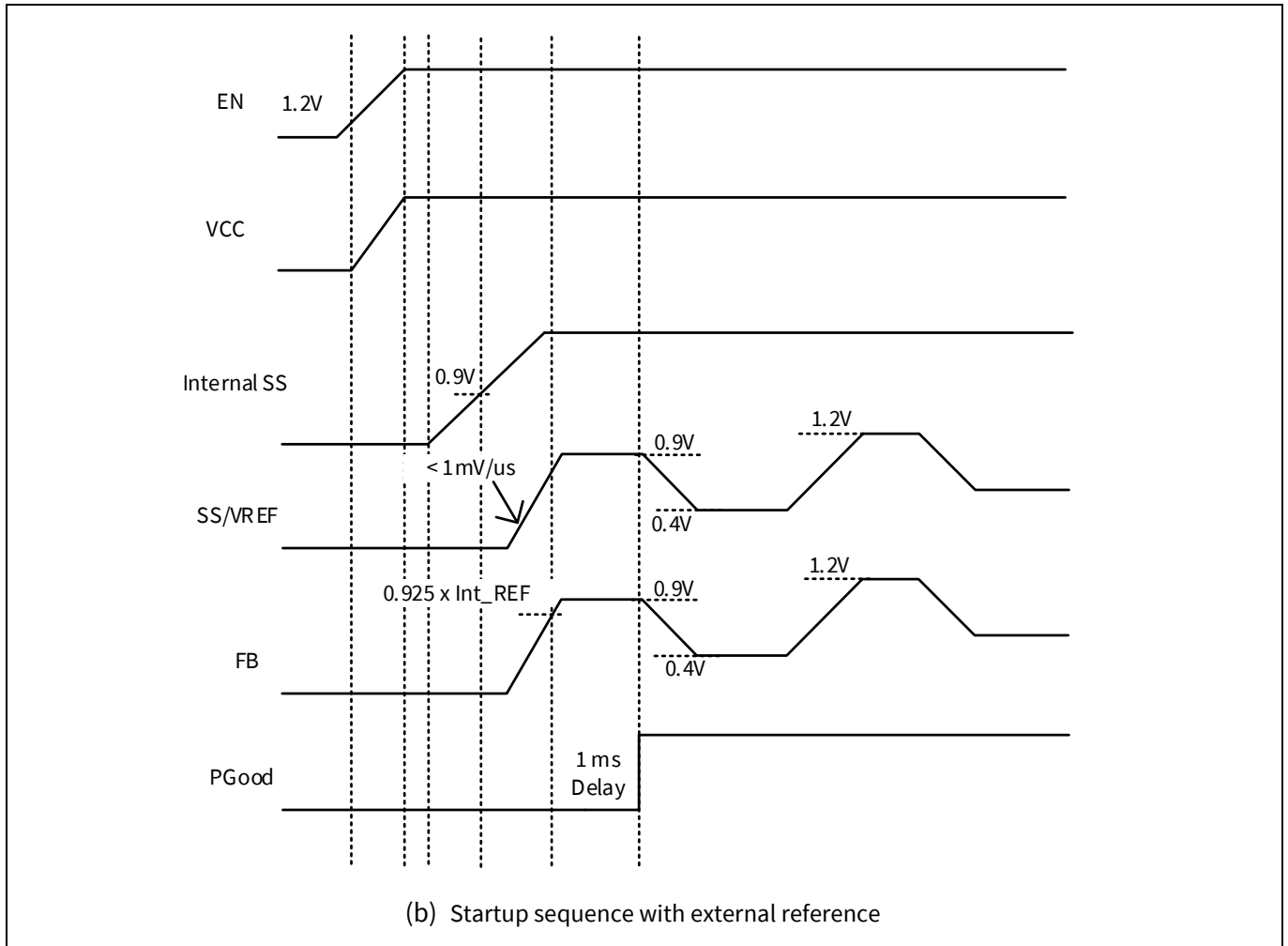
Figure 5 **Startup sequence with voltage tracking and external reference**

9.8 Internal Low-Dropout (LDO) Regulator

The TDA38807 has an integrated low-dropout (LDO) regulator, providing the bias voltage for the internal circuitry. To minimize standby current, the internal LDO is disabled when the EN voltage is pulled low. VIN pin is the input of the LDO. To save power losses on the LDO, an external bias voltage can be used by connecting directly to the VCC pin. **Figure 6** illustrates the configuration of VCC, and VIN pin for internal LDO and external Vcc operation.
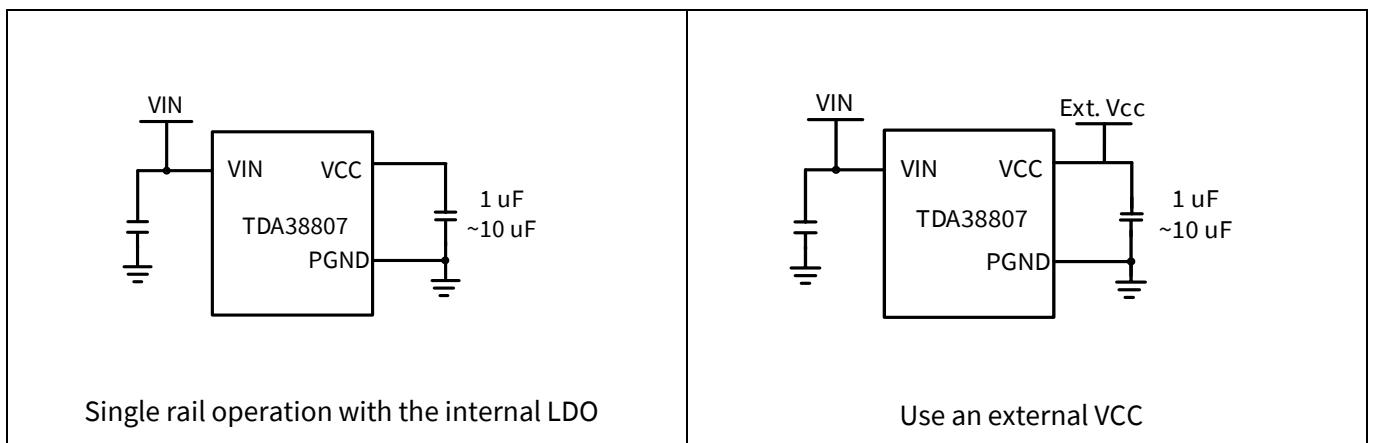
Figure 6 **Configuration of using the internal LDO or an external VCC**

Section **7.1** specified the recommended operating voltage range of VIN and VCC pin under different configurations. The following design guidelines are recommended when configuring the VCC.

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- Place a bypass capacitor to minimize the disturbance on the VCC pin.
- For both operation using the internal LDO and external Vcc, a 1 uF~10 uF low ESR ceramic capacitor is required to be placed close to the VCC with reference to PGND.

The internal LDO has two current limits, i.e., a short circuit current limit and a foldback current limit. Foldback current limit is much lower than the short circuit current limit. The transition between the two limits is based on the VCC UVLO rising and falling thresholds. During startup, the LDO ramps up with the foldback current limit. Once the LDO voltage is above the VCC UVLO rising threshold, it transitions to the short circuit current limit. In case of short on LDO, the current is limited to short circuit current limit until the LDO voltage drops below the VCC UVLO falling threshold. Beyond which, the fold back current limit is enabled. These two limits help protect the LDO during any fault conditions.

9.9 Current Sense (CS) and Over Current Protection (OCP)

During the ON time of the Synchronous MOSFET, the inductor current is sensed and mirrored to CS pin with the ratio of G_{CS}. By using an external resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The Control MOSFET is only allowed to turn on when the V_{CS} voltage is below the internal OCP voltage threshold V_{CS} (During the ON state of Synchronous MOSFET) to limit the SW valley current cycle-by-cycle. The resistor R_{CS} can be calculated as below.

$$R_{CS}(\Omega) = \frac{V_{CS}}{G_{CS} \times \left(I_{LIM} - \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times F_{SW}} \right) \right)}$$

Where, Vcs is 1.2 V, GCS = 40 µA/A, and ILIM is the desired DC current limit.

OCP latch response is active 3 ms after the device is enabled. Once it is active, if the device detects over current condition for consecutive 40 cycles, or if the FB drops below under voltage protection (UVP) threshold, the device latches off the Control MOSFET immediately, and PGOOD flags low. The device will restart into a soft start when Vin, EN or Vcc is cycled.

9.10 Under Voltage Protection (UVP)

Under Voltage Protection (UVP) provides additional protection during OCP fault or other faults. UVP protection is enabled when the soft-start reference rises above 160 mV. UVP circuitry monitors FB voltage. When FB is below the UVP threshold for 5 µs (typical), an undervoltage trip signal is triggered. PGood is pulled low after a delay of ~2 µs. The part continues to switch for ~5 µs after PGood is pulled low. Then, the Control MOSFET is latched OFF and the Synchronous MOSFET is turned off after ZCD (zero crossing detection) is detected. Also, the SS/VREF capacitor is discharged. The device will restart into a soft start when VIN, EN or VCC is cycled.

9.11 Output Voltage Discharge

The device enters output voltage discharge mode when it is disabled through EN. Both Control and Synchronous MOSFETs are latched OFF. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch ON resistance of the FET is about 75 Ω. Once FB voltage drops below 10% of SS/VREF, the discharge FET is turned OFF.
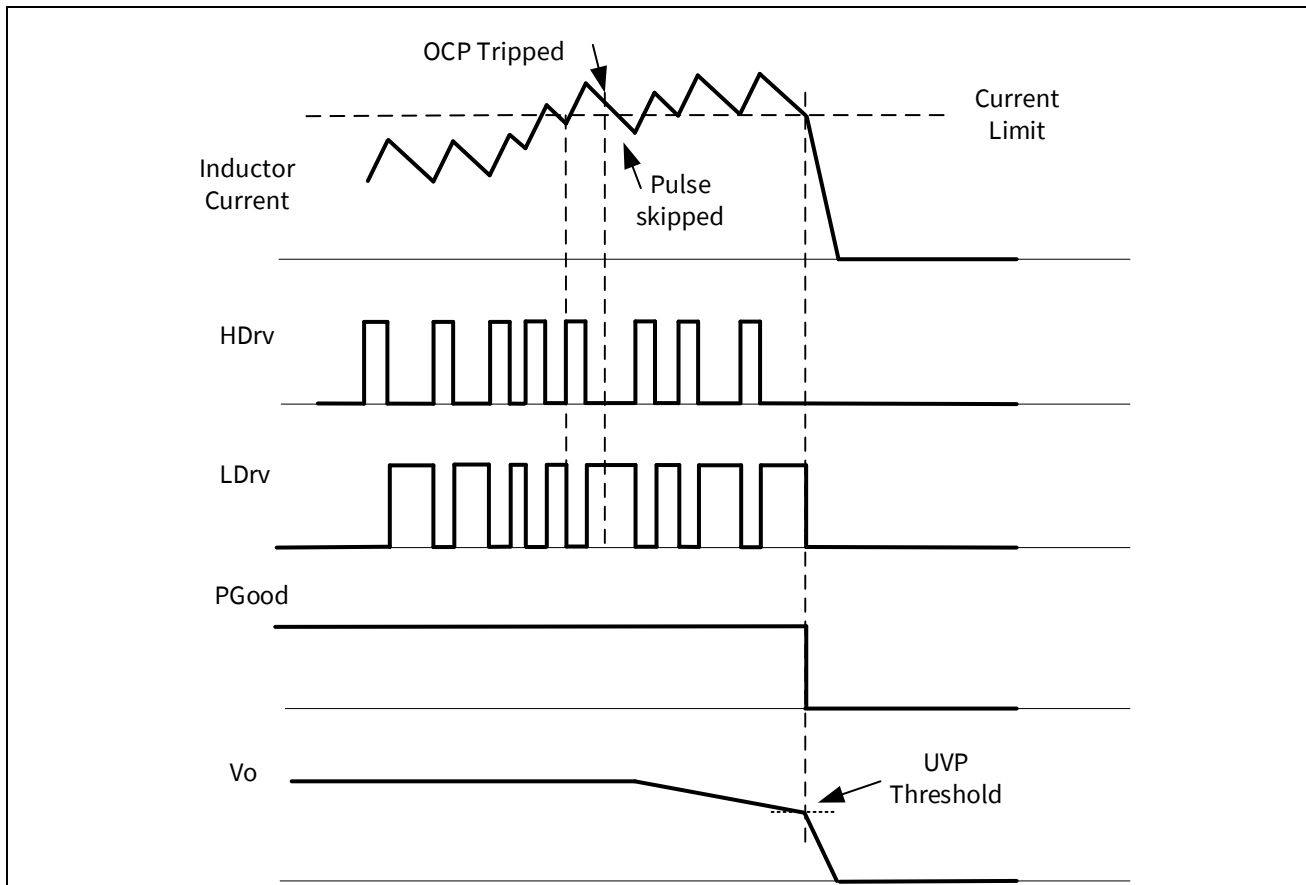
Figure 7   **Cycle-by-cycle OCP response**

9.12   Output Sinking Mode (OSM)

When the FB voltage is higher than 104% SS/VREF voltage but is below the OVP threshold, it triggers Output Sinking Mode. During OSM operation, the Synchronous MOSFET remains ON to discharge the output until it hits the -3 A negative current limit (NOCP_OSM). When it hits -3A limit, the Synchronous MOSFET is turned OFF and Control MOSFET is turned ON for TON time. Then the Control MOSFET is turned OFF and Synchronous MOSFET is turned back ON. The device keeps this operation until the FB drops below 102% SS/VREF. Once FB drops below 102% SS/VREF, the device exits OSM.

9.13   Over Voltage Protection (OVP)

The OVP comparator becomes active after the SS/VREF voltage reaches 0.9 V. TDA38807 has a Latched OVP response, i.e., when OVP is triggered, the Control FET remains latched off until either VCC voltage or the EN signal is cycled.

Over Voltage Protection (OVP) is achieved by comparing the FB voltage to an OVP threshold voltage. When the FB voltage exceeds the OVP threshold, an over voltage trip signal is asserted after 2 μs (typical) delay. The Control MOSFET is latched OFF and PGood flags low. The Synchronous MOSFET remains ON to discharge the output until it hits the -3 A negative current limit (NOCP_OVP). When it hits -3A limit, the Synchronous MOSFET is turned OFF and Control MOSFET is turned ON for TON time. Then the Control MOSFET is turned OFF and Synchronous MOSFET is turned back ON. This operation is repeated until the FB voltage drops below 50% of the SS/VREF voltage. When FB voltage drops below 50% of the reference voltage, Synchronous MOSFET is turned OFF if the part is operating in DEM. If operating in FCCM, it repeats the switching behavior (Synchronous MOSFET turned ON until the NOCP limit is hit, then turn OFF Synchronous MOSFET and turn control MOSFET ON for TON time) until FB is discharged to 10% of the reference voltage. After that Control MOSFET stays latched OFF. If ever the FB rises above the OVP threshold in this state, the response is repeated.

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9.14 Negative Over Current Limit (NOCP)

The TDA38807 offers negative over current limit protection. When the device detects the current in the synchronous MOSFET is at the negative current limit, it turns off the Synchronous MOSFET to limit the negative current. Under normal operation or in the case of an OSM event, the negative current is limited at -3 A. In the case of an OVP event, the negative current is limited at - 3A
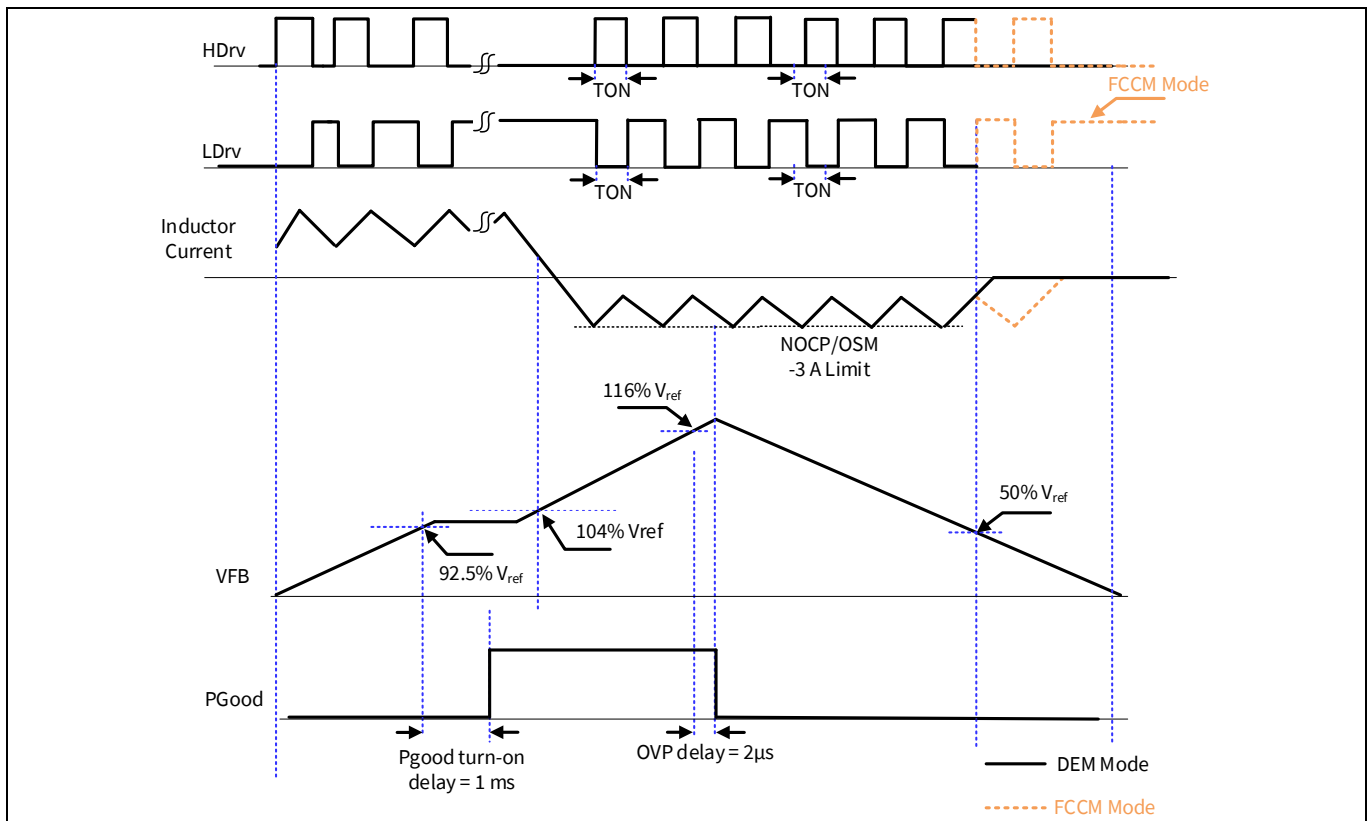

Figure 8 Over voltage protection response and PGood behavior

9.15 Over Temperature Protection (OTP)

Temperature is monitored internally on TDA38807. When the temperature exceeds the over temperature threshold, OTP circuitry turns off the Control MOSFET immediately and the Synchronous MOSFET is turned off after ZCD (zero crossing detection) is detected. Also, the SS/VREF capacitor is discharged. Restart is initiated when VIN, EN or VCC is cycled.

9.16 Power Good (PGood) Output

The PGood pin is the open drain of an internal NFET and must be externally pulled high through a pull-up resistor. The PGood signal is high when three criteria are satisfied:

1. EN signal and VCC voltage are above their respective thresholds.

2. No over voltage or over temperature faults occur.

3. V_{OUT} is within regulation.

To detect if V_{OUT} is in regulation, the PGood comparator continuously monitors FB voltage. When FB voltage ramps up above the upper threshold, the PGood signal is pulled high after 1 ms. When FB voltage drops below the lower threshold or rises above the OVP threshold, the PGood signal is pulled low. **Figure 7** and **Figure 8** illustrate the PGood response. During start-up with a pre-biased output voltage, the PGood signal is held low

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before the first PWM is generated and is then pulled high with 1 ms delay after FB voltage rises above the PGood threshold.

A 10 kΩ or higher pull-up resistor is needed for a PGood bias voltage of 3.3V to maintain the PGood signal at logic low (below 0.7 V) when VIN = VCC = 0 V

9.17 Minimum ON - Time and Minimum OFF - Time

The minimum on-time refers to the shortest time for the Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38807 to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in Section **7.2**. Otherwise, the resulting switching frequency may be lower than the desired target. The following formula should be used to check for the minimum on-time requirement.

$$\frac{V_{OUT}}{k \times F_{SW} \times V_{IN}} > \max \ spec \ of \ T_{ON(\min)}$$

Where F_{SW} is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in Section **7.2**, which can be calculated as shown below.

$$\frac{V_{IN} - V_{OUT}}{k \times F_{SW} \times V_{IN}} > \max \ spec \ of \ T_{OFF(\min)}$$

Where F_{sw} is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

9.18 Selection of Feedforward Capacitor and Feedback Resistors

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.9 V. The divider ratio is set to provide 0.9 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Recommended feedback resistors values is from 1kΩ to 20kΩ.

A small MLCC capacitor, Cff, is preferred in parallel with the top feedback resistor, RFB1, to provide extra phase boost and to improve the transient load response. The value of Cff is recommended to be 10 pF to 1nF. For higher output voltage, lower cff capacitor value is recommended.

10 Design Example

In this section, an example is used to demonstrate how to design a buck regulator with the TDA38807.The design specifications are given below:

- VIN = 12 V (±10 %)
- V_o = 1.8 V
- I_o = 6 A
- V_o ripple voltage = ±1 % of V_o
- Load transient response = ± 3 % of V_o with a step load current = 3 A and slew rate = 2.5 A/µs

10.1 Enabling the TDA38807

The TDA38807 has a precise Enable threshold voltage, which can be used to implement a higher UVLO on the input bus voltage by connecting the EN pin to VIN with a resistor divider, as shown in Configuration 2 of **9.4**. The Enable feedback resistor, R_{EN1} and R_{EN2}, can be calculated as follows.

$$VIN_{(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{VIN_{(\min)} - V_{EN(\max)}}$$

Where $V_{EN\,(\max)}$ is the maximum spec of the Enable-start-threshold as defined in Section **7.2**. For VIN $_{(\min)}$ = 10 V, select R_{EN1} = 49.9 kΩ and R_{EN2} = 7.5 kΩ.

10.2 Selecting Input Capacitors

Without input capacitors, the pulse current of the Control MOSFET is provided directly from the input supply. Due to the impedance of the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{VIN}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current, and D is the Duty Cycle. For I_o = 6 A and $D_{(\max)}$ = 0.15, the resulting RMS current flowing into the input capacitor is I_{rms} = 2.14 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1 - D) \times D}{f_{sw} \times (\Delta VIN - ESR \times I_o \times (1 - D))}$$

Where ΔVIN is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistance of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For Io = 6 A, fsw = 1100 kHz, ESR = 2 mΩ, and VIN = 120 mV, Cin(min) > 6.33 µF. Ensure to account for the derating of ceramic capacitors under a bias voltage while selecting capacitors to satisfy $C_{in(min)}$

condition. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

10.3 Inductor Selection

The inductor is selected based on output power, operating frequency, and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency, and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease with increasing temperature. It is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relations:

$$L = (V_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{V_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $VIN_{(max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; OCP_{max} = maximum spec of the OCP limit as defined in Section **7.2**; and I_{sat} = inductor saturation current. In this case, select inductor L = 1 µH to achieve ΔiL_{max} = 23% of I_{omax}. The I_{sat} should be no less than 7.64 A for V_{cs} = 1.25V, R_{cs} = 5kΩ, where OCP_{max} is the valley current.

10.4 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_o ripple requirement, C_o should satisfy the following criterion:

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For ΔiL_{max} = 1.39 A, ΔV_{or} = 18 mV, f_{sw} = 1100 kHz, C_o must be larger than 8.77 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion:

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable V_o deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the C_o that is calculated above as a starting point, and then optimize the design based on bench measurement. In this case, to meet the transient load requirement (i.e. ΔV_{oL}= 54 mV, $\Delta I_{o(max)}$ = 3 A), select C_o = ~46 µF. For more accurate estimation of C_o, simulation tools should be used to aid the design.

10.5 Output Voltage Programming

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.9 V. The divider ratio is set to provide 0.9 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Select R_{FB1} = 10 kΩ and R_{FB2} = 10 kΩ, to achieve V_o = 1.8 V.

10.6 Feedforward Capacitor

A small MLCC capacitor, C_{ff}, can be placed in parallel with the top feedback resistor, R_{FB1}, to improve the transient response. With Lo = 1uH, Co = 220 µF and R_{FB1} = 10 kΩ, C_{ff} = ~470 pF. C_{ff} can be further optimized based on bench testing of transient load response.

10.7 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between SW and BOOT.

10.8 VCC bypass Capacitor

A 2.2 µF MLCC is recommended for the VCC/LDO bypass capacitor and a 2.2 µF MLCC is selected for the VIN bypass capacitor.

10.9 Pgood Resistor

The recommended value for Pgood resistor is 10 kΩ and above. 10 kΩ resistor is selected for the Pgood resistor.

10.10 SS/Vref Capacitor

Soft start can be programmed with an external capacitor at SS/Vref pin. The calculation of the soft start capacitor is shown below.

$$C_{SS}\ (nF) = \frac{t_{SS}\ (ms) \times 10\mu A}{0.9\ (V)}$$

For 2.2ms soft start, 25nF of capacitor has to be connected between SS/Vref to AGND. Minimum value of 3.3nF capacitor value is recommended between SS/Vref pin to AGND.

10.11 Current Sense Resistor

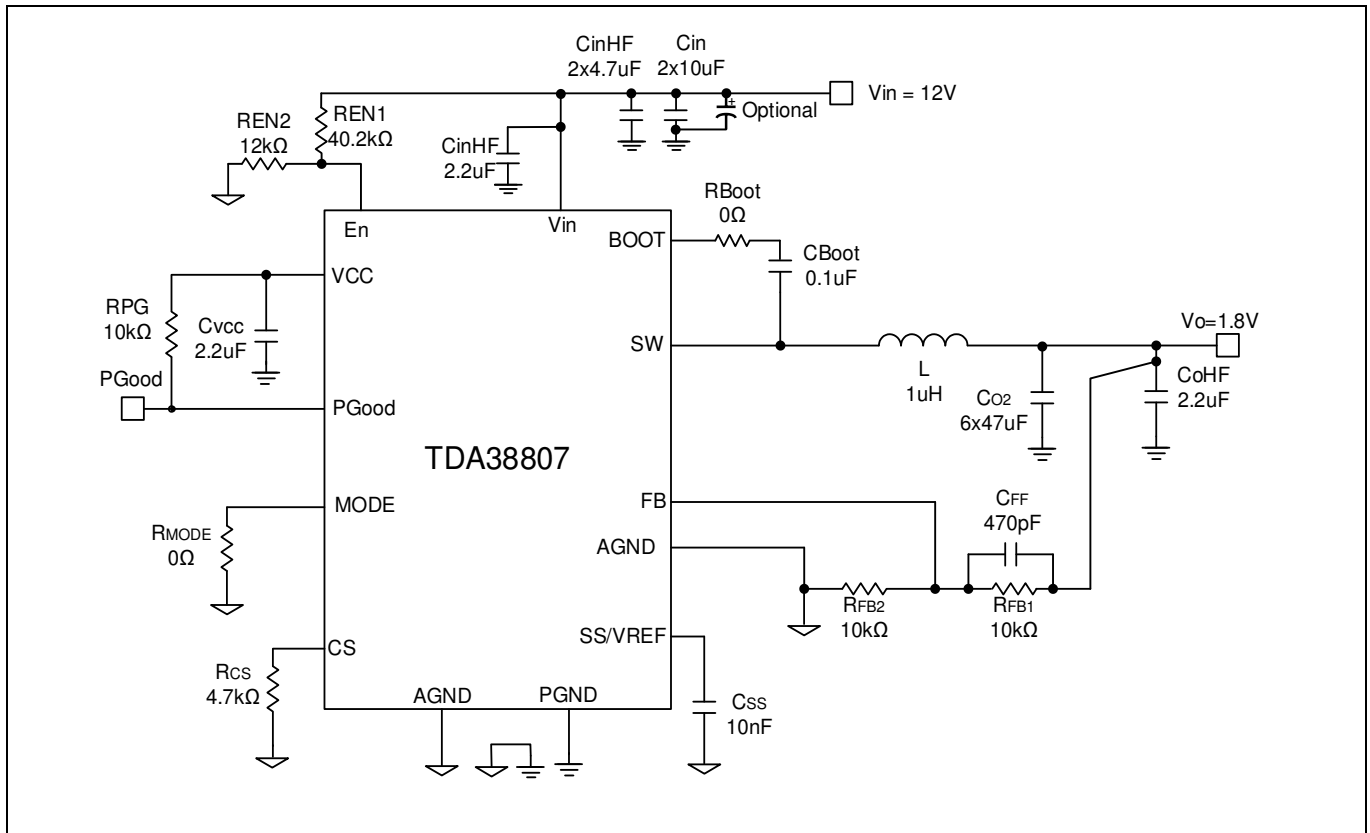Following equation is used to calculate current sense resistor.

$$R_{CS}(\Omega) = \frac{V_{CS}}{G_{CS} \times \left(I_{LIM} - \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times F_{SW}} \right) \right)}$$

where, V_{CS} is 1.2 V, G_{CS} = 40 µA/A, and ILIM is the desired DC current limit.
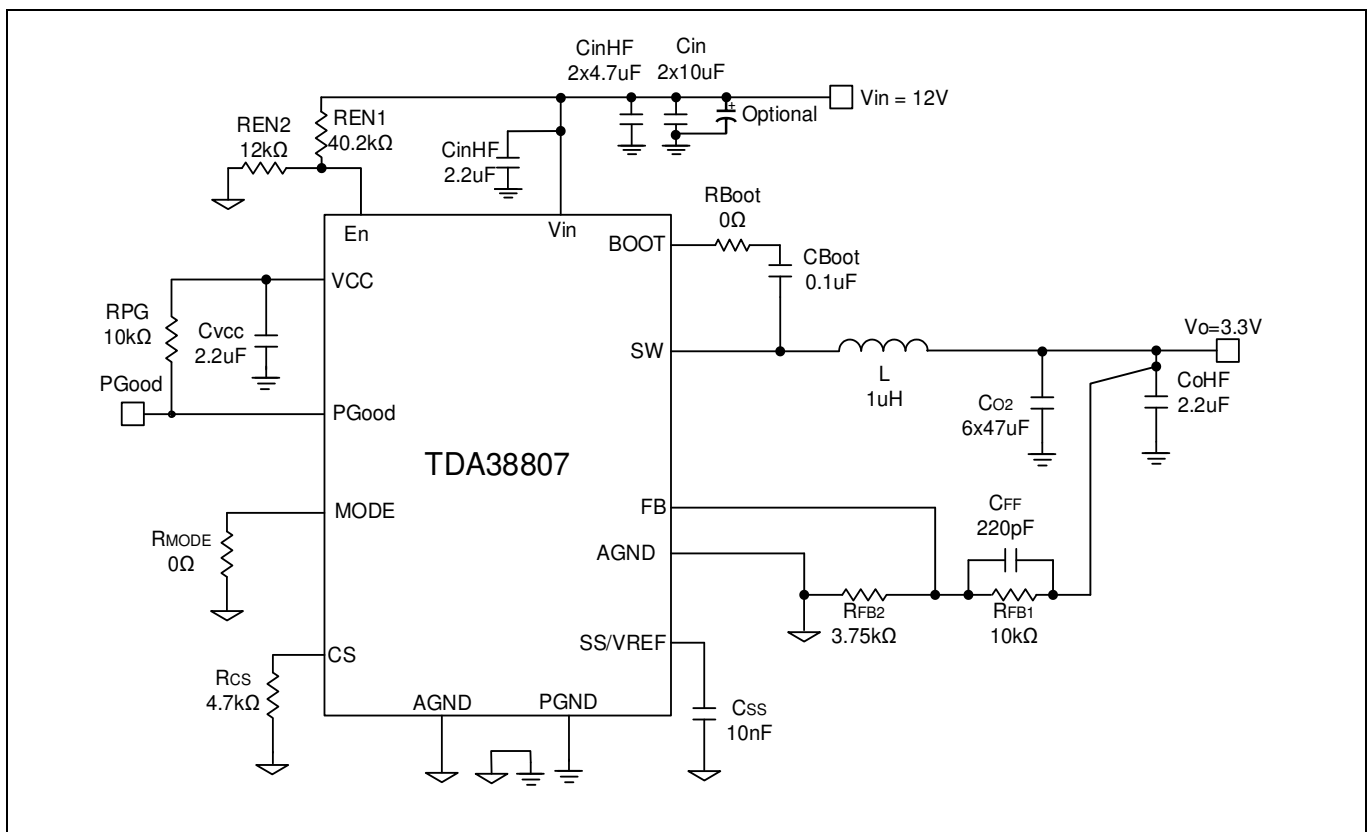
4.7kΩ resistor is selected for 6.6A current limit.
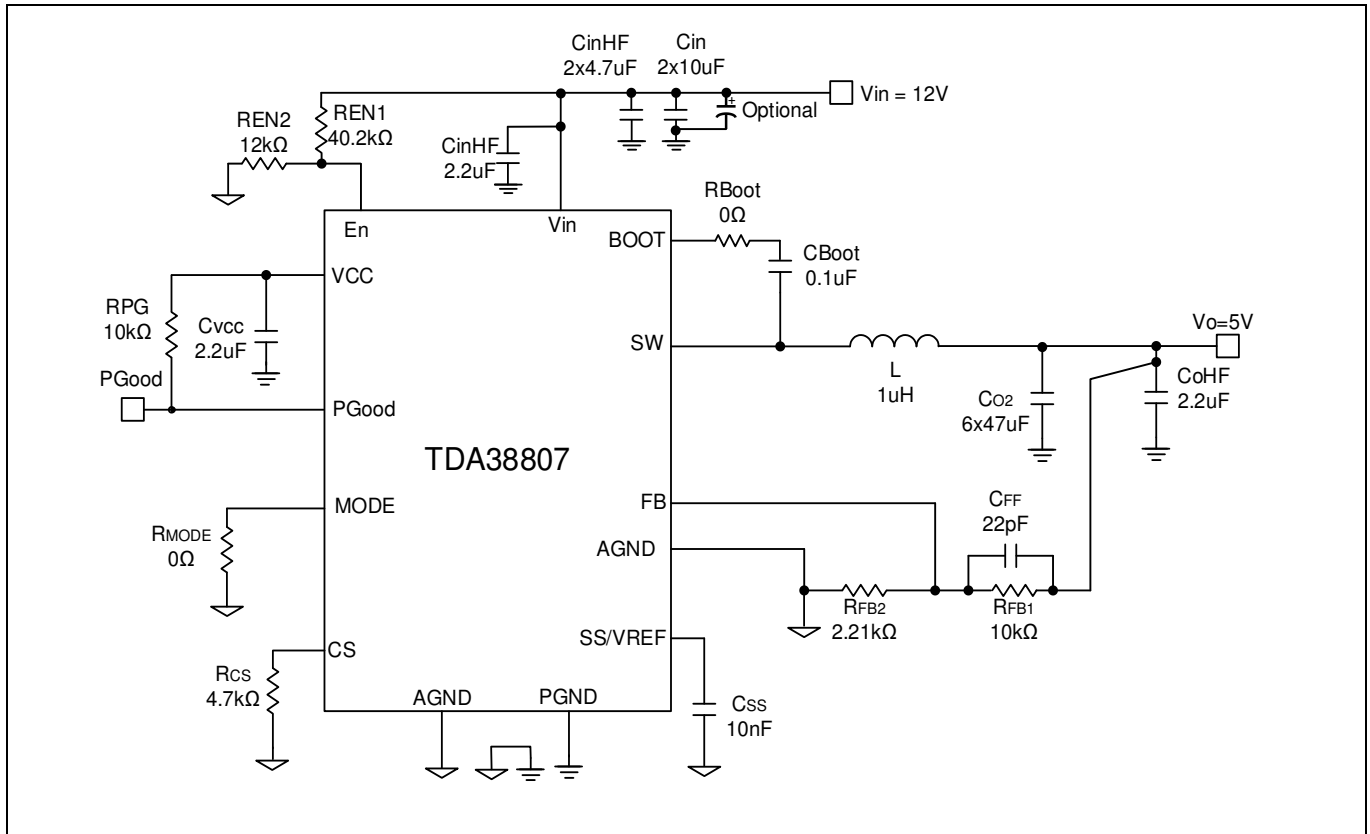
11 Application Information

11.1 Application Diagram for Vout = 1.8V

11.2 Application Diagram for Vout = 3.3V

11.3 Application Diagram for Vout = 5V

12 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, VIN and VCC bypass capacitors, should be placed near the corresponding pins as close as possible.

- Place bypass capacitors from TDA38807 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vout. The bypass capacitor shared by VCC should be terminated to PGND.

- Place a boot strap capacitor near the TDA38807 BST and SW pin as close as possible to minimize the loop inductance.

- SW node copper should only be routed on the top layer to minimize the impact of switching noise.

- Connect AGND pin to the PGND pad through a single point connection, using a wider trace. Keep the trace length to minimum and place it right underneath the AGND and PGND pins.

- Via holes can be placed on VIN and PGND pads to aid thermal dissipation.

- Wide copper polygons are desired for VIN and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.

- The EN pin and configuration pins including SS/VREF, MODE, and CS should be terminated to a quiet AGND.
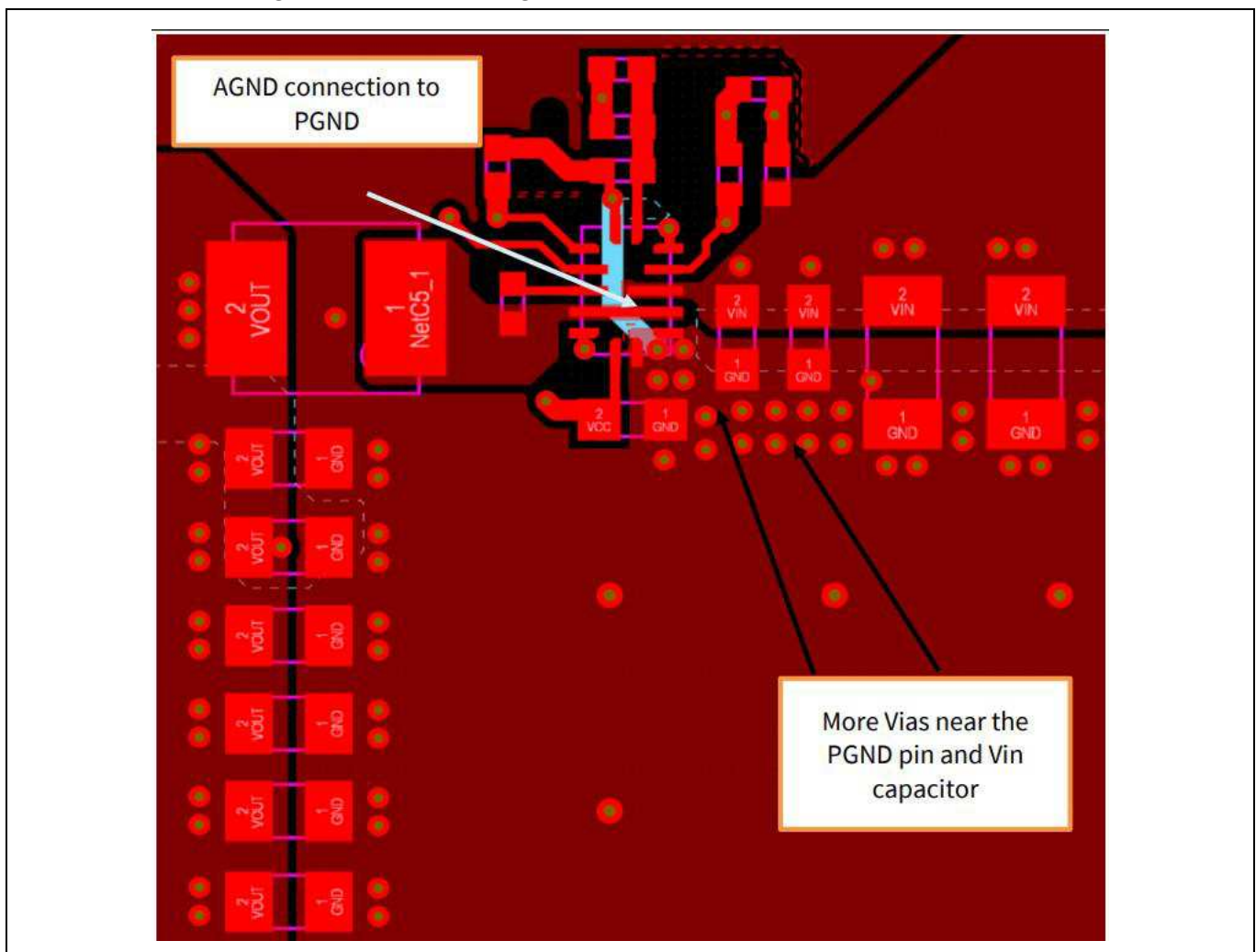

Figure 9   Layout Diagram

Layout Recommendations

Following figures illustrate the PCB layout design of the TDA38807 standard demo board.
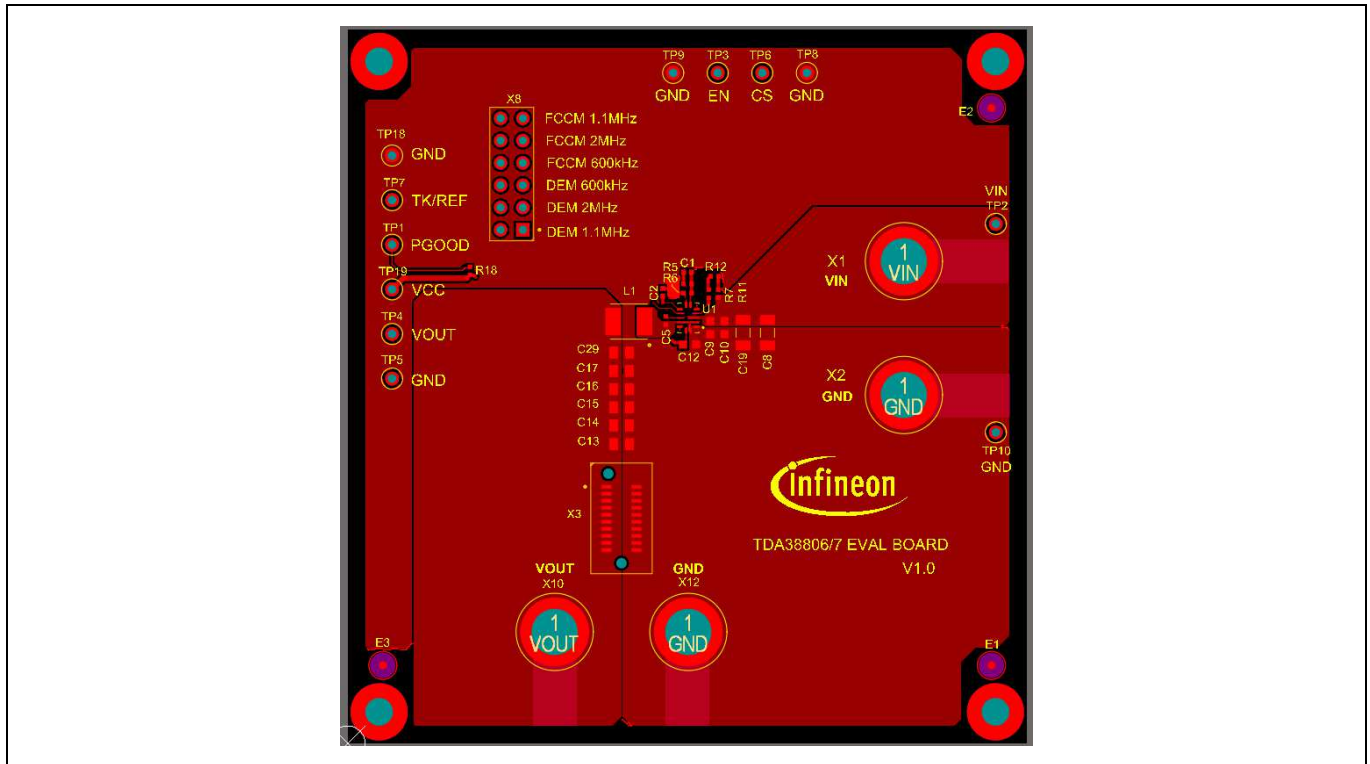
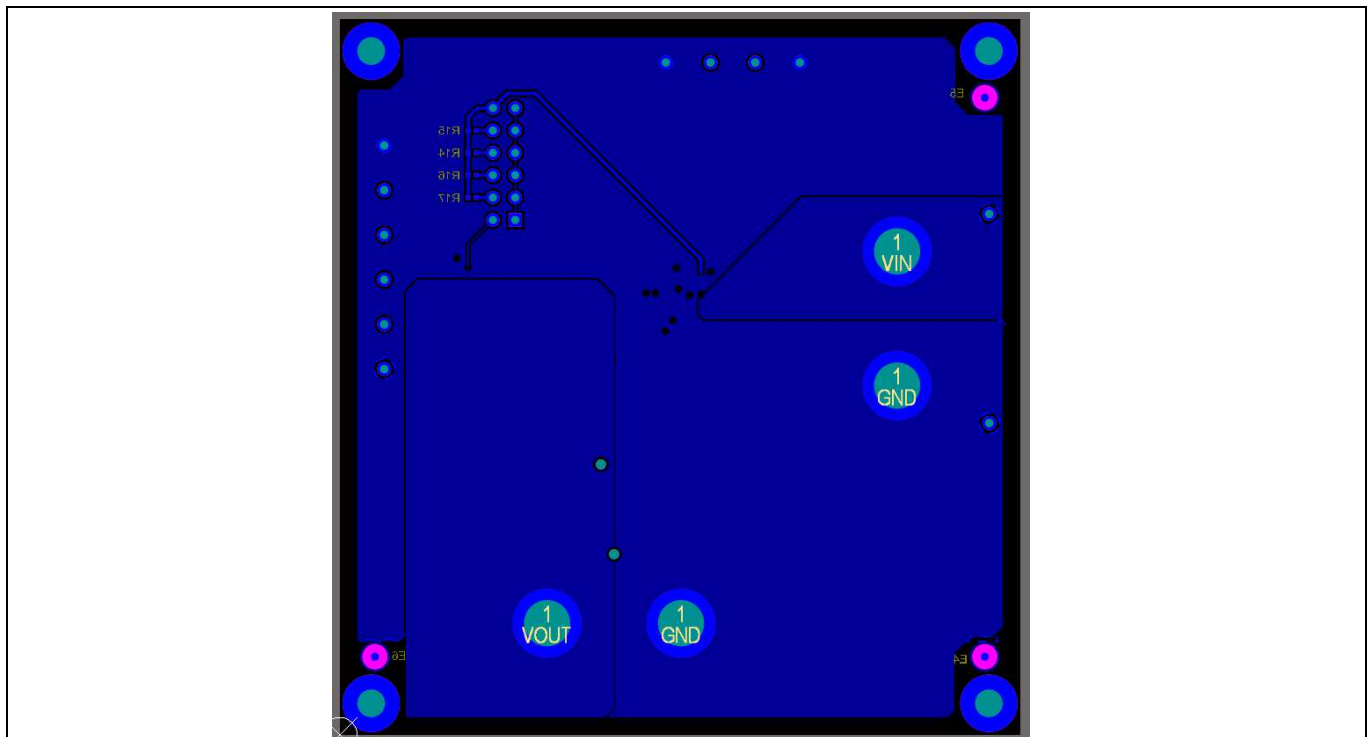**Figure 10   TDA38807 Demo Board – Top Layer**

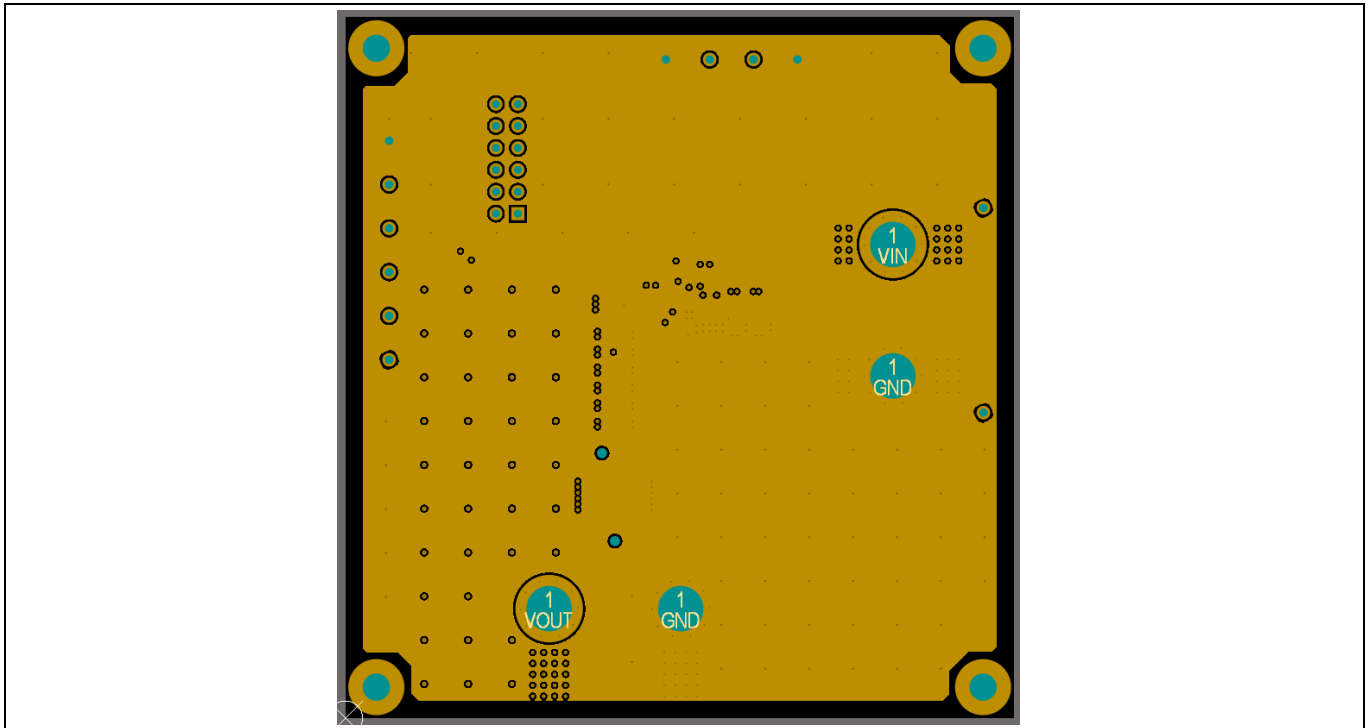**Figure 11   TDA38807 Demo Board – Bottom Layer**

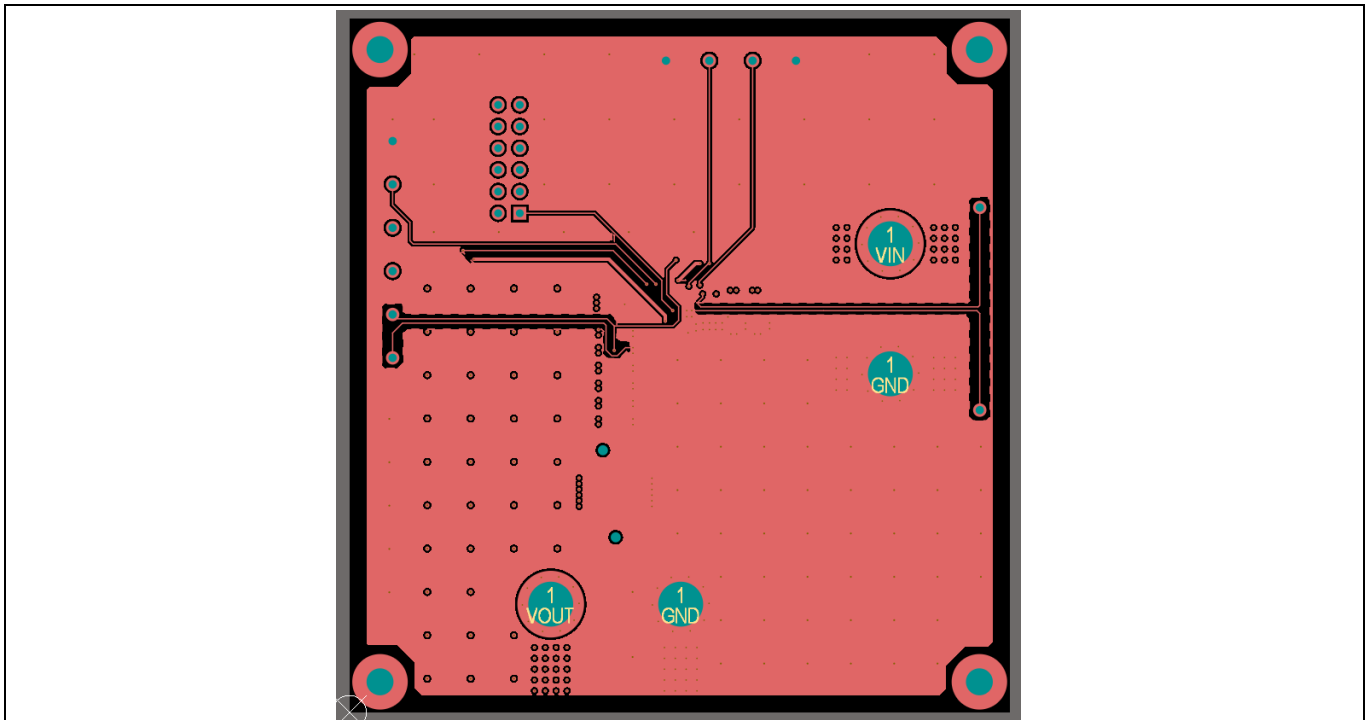**Figure 12   TDA38807 Demo Board – 2nd Layer**

Figure 13   TDA38807 Demo Board – 3rd Layer

12.1 Solder mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. QFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist between the smaller signal lead areas is at least 0.15 mm wide due to the high x/y aspect ratio of the solder mask strip.

12.2 Stencil design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010"). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008"), with suitable reductions, give the best results. A recommended stencil design is shown below. This design is for a stencil thickness of 0.127 mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.
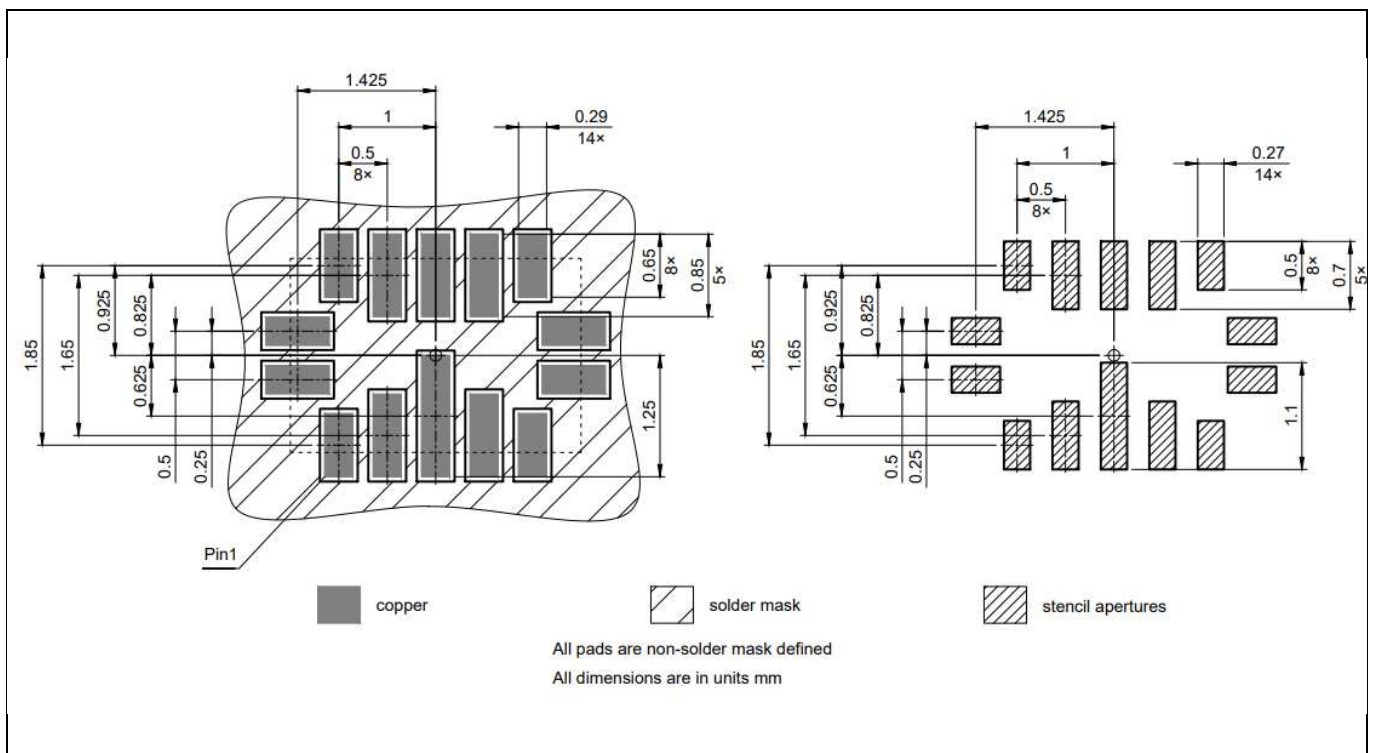

Figure 14   PCB metal, solder mask, and Stencil - pad size and spacing

13 Package

This section includes marking, mechanical and packaging information for the TDA38807.

13.1 Marking Information

Dot: - Pin1 identifier
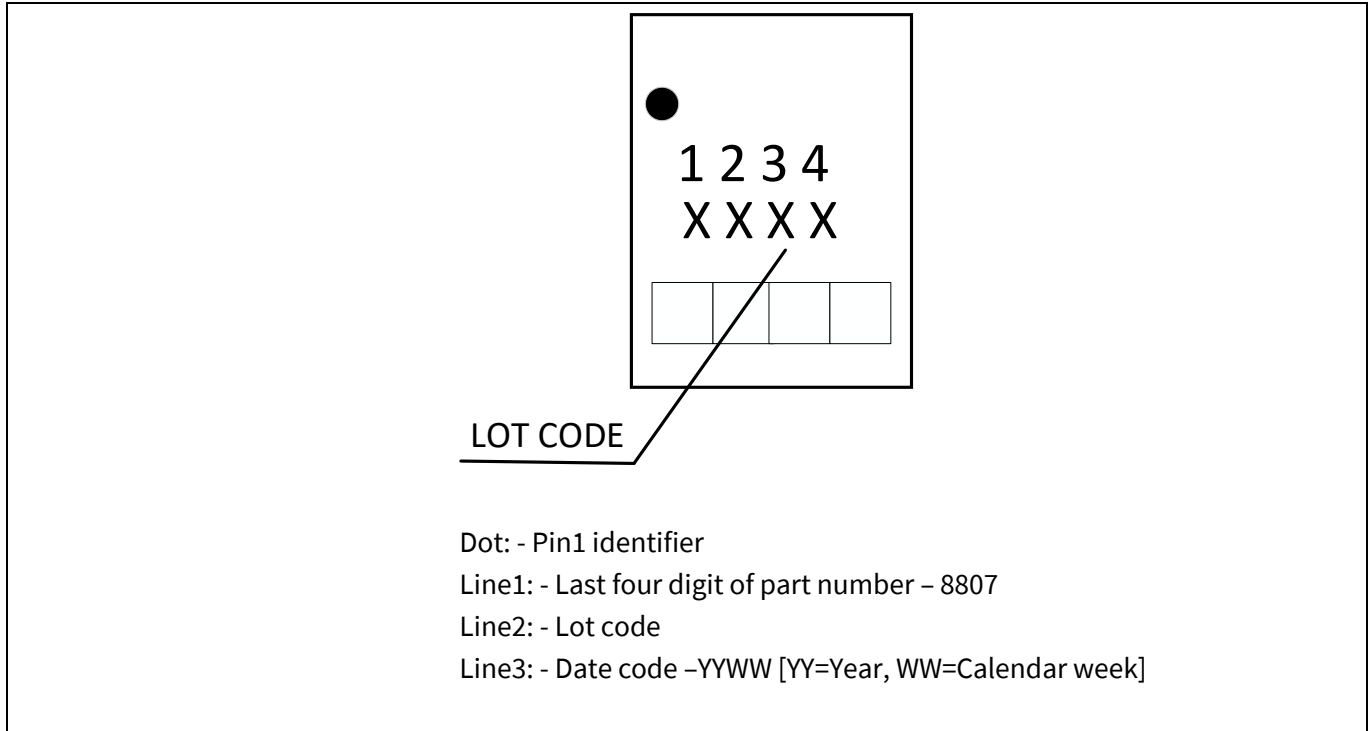
Line1: - Last four digit of part number – 8807

Line2: - Lot code

Line3: - Date code –YYWW [YY=Year, WW=Calendar week]

Figure 15   Package Marking

13.1 Dimensions
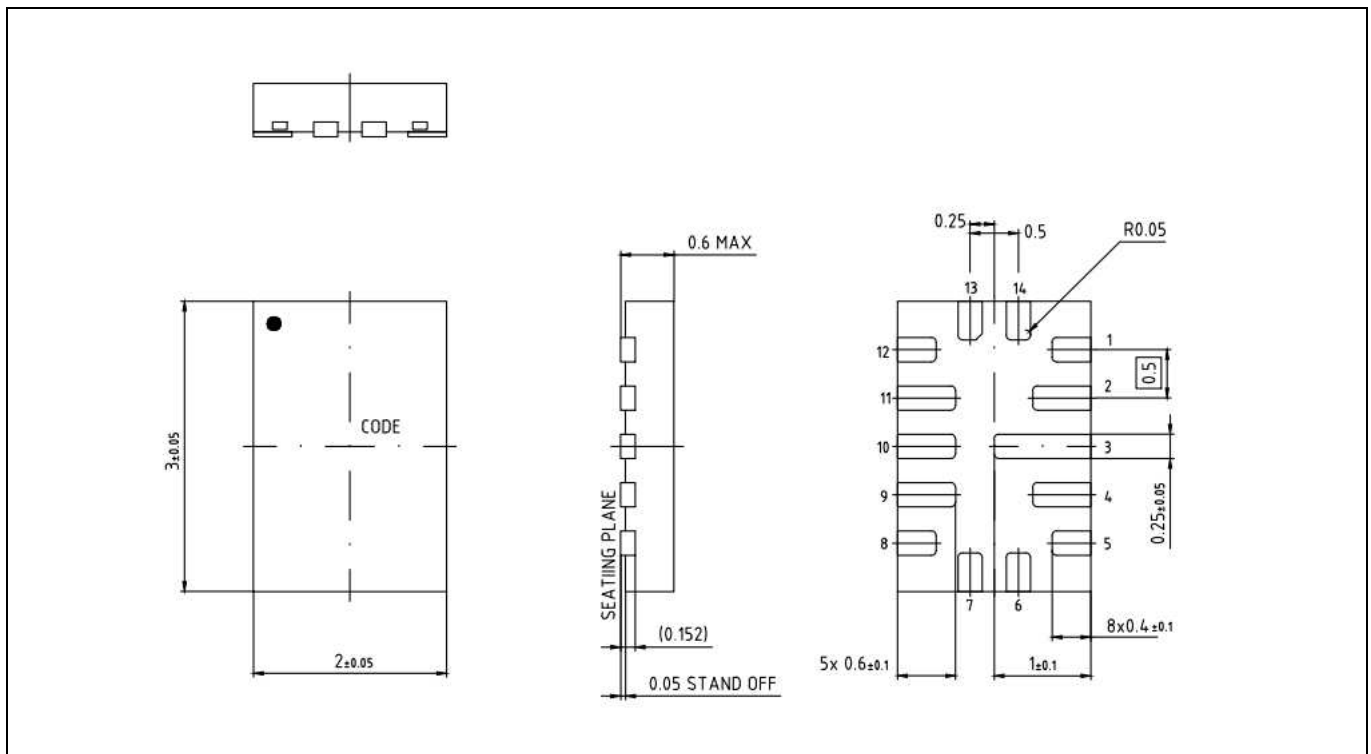
Figure 16   Package Dimensions (all dimensions in mm)

13.2   Tape and Reel information

All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [◁⊕]
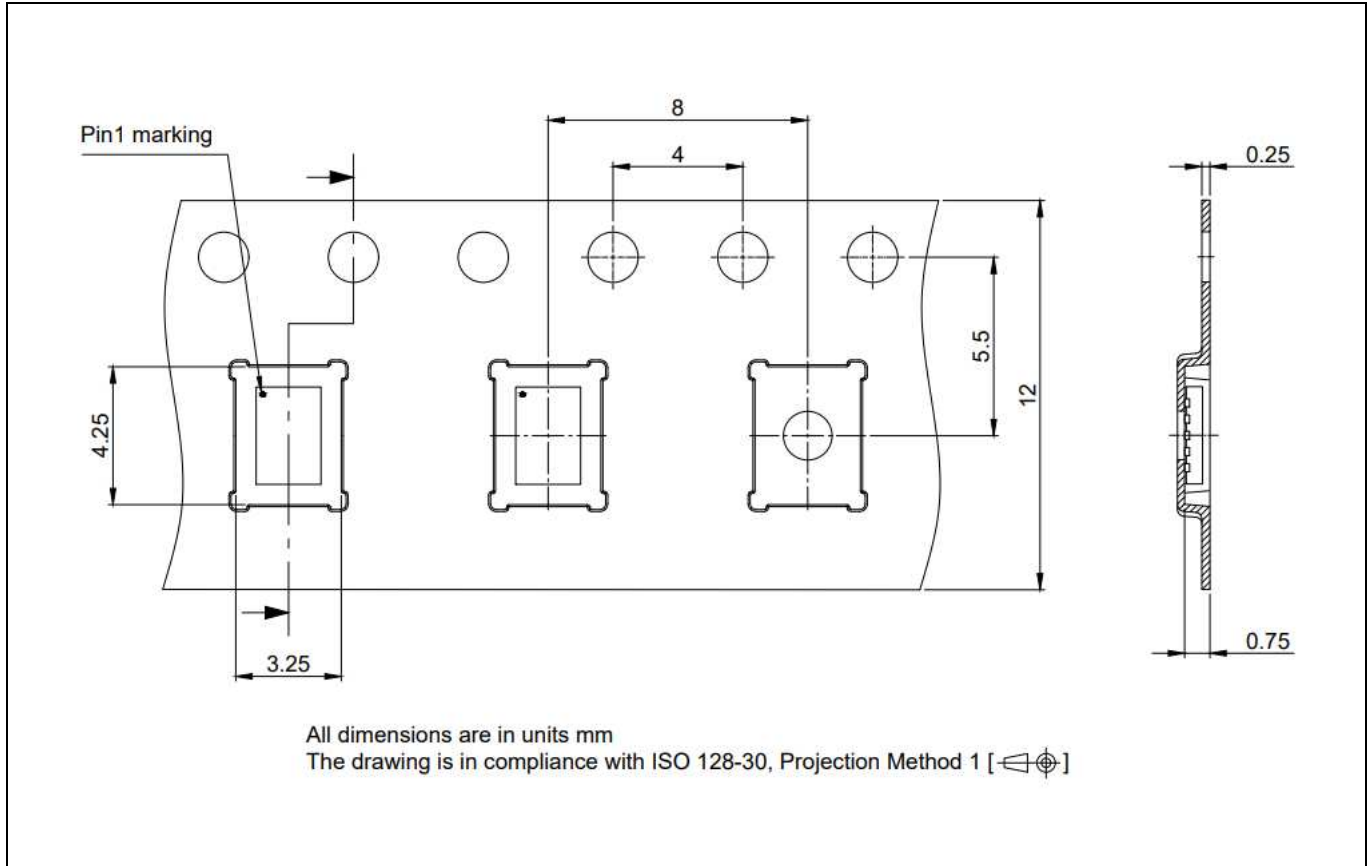
14   Environmental Qualifications

Qualification Level	Industrial	
Moisture Sensitivity	QFN Package	JEDEC Level 2 @ 260 ℃
ESD Human Body Model	ANSI/ESDA/JEDEC JS-001, 2 (2000V to < 4000V)	
Charged Device Model	ANSI/ESDA/JEDEC JS-002, C3 (≥ 1000V)	
RoHS Compliant	Yes	

Revision History

TDA38807

Revision: 2024-03-19, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-07	Release of final version
2.1	2024-03-19	Added VDS Maximum specification for the High side MOSFET Updated the Global condition of Vin for the EC table Updated the IC dimensions Updated the IC Marking

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