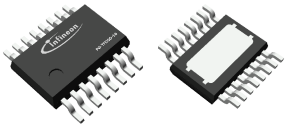
LITIX™ Basic+

Features



- Single channel device with integrated and protected output stage (current sink), optimized to drive LEDs
- High output current up to 400 mA
- Possibility to offload power consumption via low cost external resistor to allow maximum current driving capability (Power Shift)
- Fault management supports both 1-fail-all-OFF and 1-fail-all-ON
- Analog output current control input to adjust the output current
- Open load (OL), short to battery (SC) and thermal shutdown protections
- Intelligent fault management: up to 10 devices can share a common error network with only one external resistor
- Thermal derating function via external NTC resistor

Potential applications

- Cost effective "stop"/"tail" function with shared and separated LEDs per function
- Automotive light functions like turn indicators, position, fog, stop/tail, DRL and side markers
- Animated light functions like sequential indicator and "welcome/goodbye" functions
- Interior lighting functions like ambient lighting, illumination and dash board lighting
- LED indicators for industrial applications and instrumentation

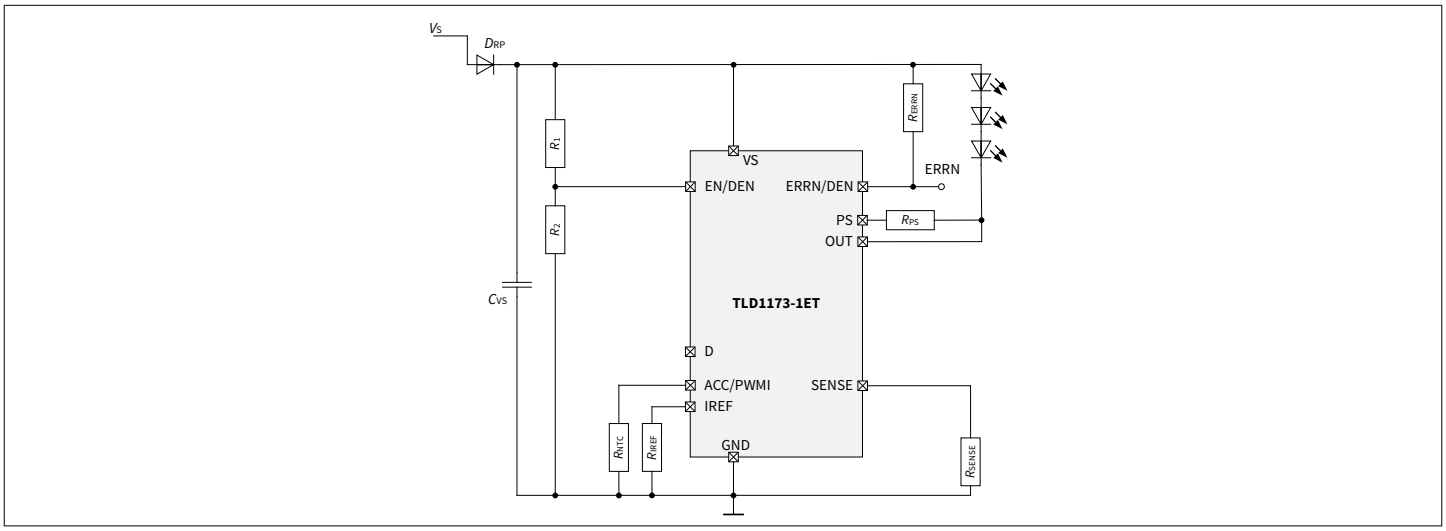
Product validation

Product validation according to AEC-Q100, Grade 1.

Qualified for automotive applications.

Description

The TLD1173-1ET is a single channel low-side driver IC with integrated and protected output stage. It is designed to control LEDs with a current up to 400 mA as linear current sink (LCS). The power shift feature allows the device to reach maximum current driving capability by offloading power consumption to an external low cost resistor. Along with its integrated diagnostic features, it offers a simple and reliable solution compared to discrete solutions. The diagnostic features and thermal derating via external NTC resistor provide a reliable solution for high current applications. The configurable fault management allows up to 10 and more devices to share the same error network and to be combined in applications with other LITIX™ LED drivers, such other LITIX™ Basic+ products and LITIX™ TLD7002-16ES.



Product type	Package	Marking
TLD1173-1ET	TFDSO-16	117

Table of contents

1 Product description

Table 1 Product summary

Parameter	Symbol	Values
Operating voltage	$V_{S(func)}$	5.5 V - 18 V
Extended operating voltage	$V_{S(ext)}$	4.5 V - 36 V
Maximum load current	$I_{SENSE(max)}$	400 mA
Output current accuracy	$V_{SENSE(reg)}$	±4% with V_{SENSE} = 400 mV
Current consumption in sleep mode	$I_{VS(sleep, max)}$	3 µA
Maximum current consumption during fault	$I_{VS(fault, ERRN)}$	850 µA
Maximum dropout voltage	$V_{DR,CS(max)}$	0.6 V

2 Block diagram

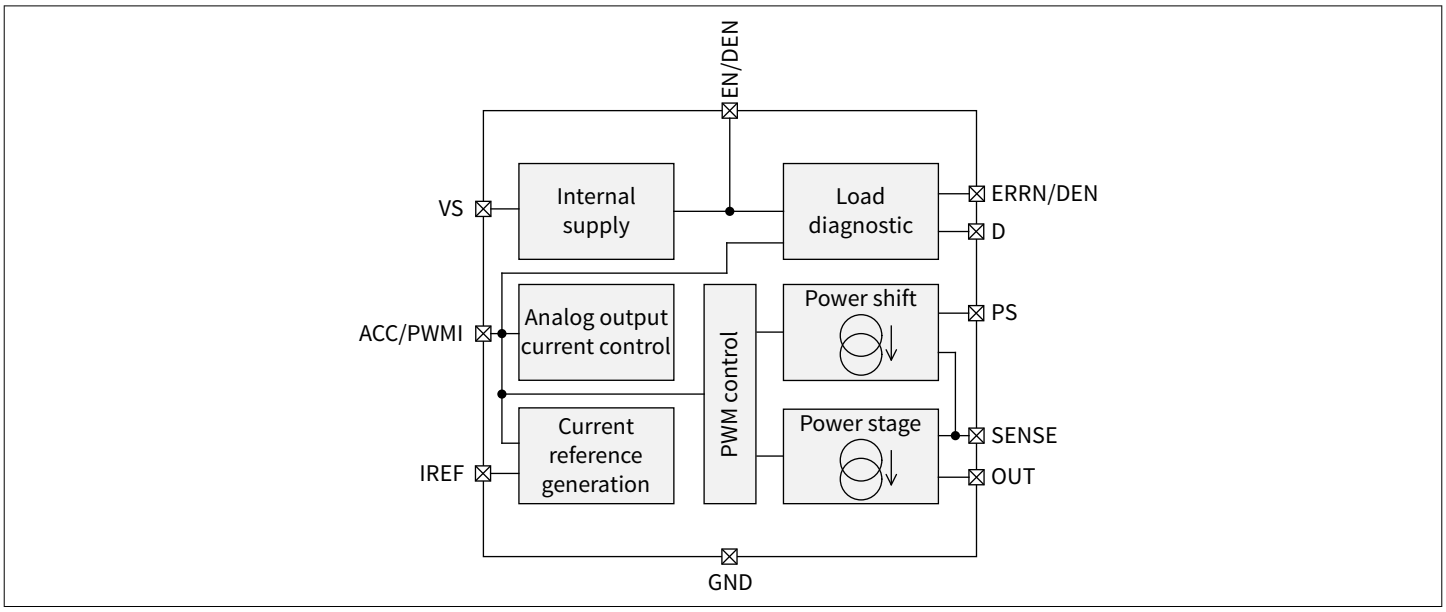


Figure 1 TLD1173-1ET Block diagram

3 Pin configuration

3.1 Pin assignment

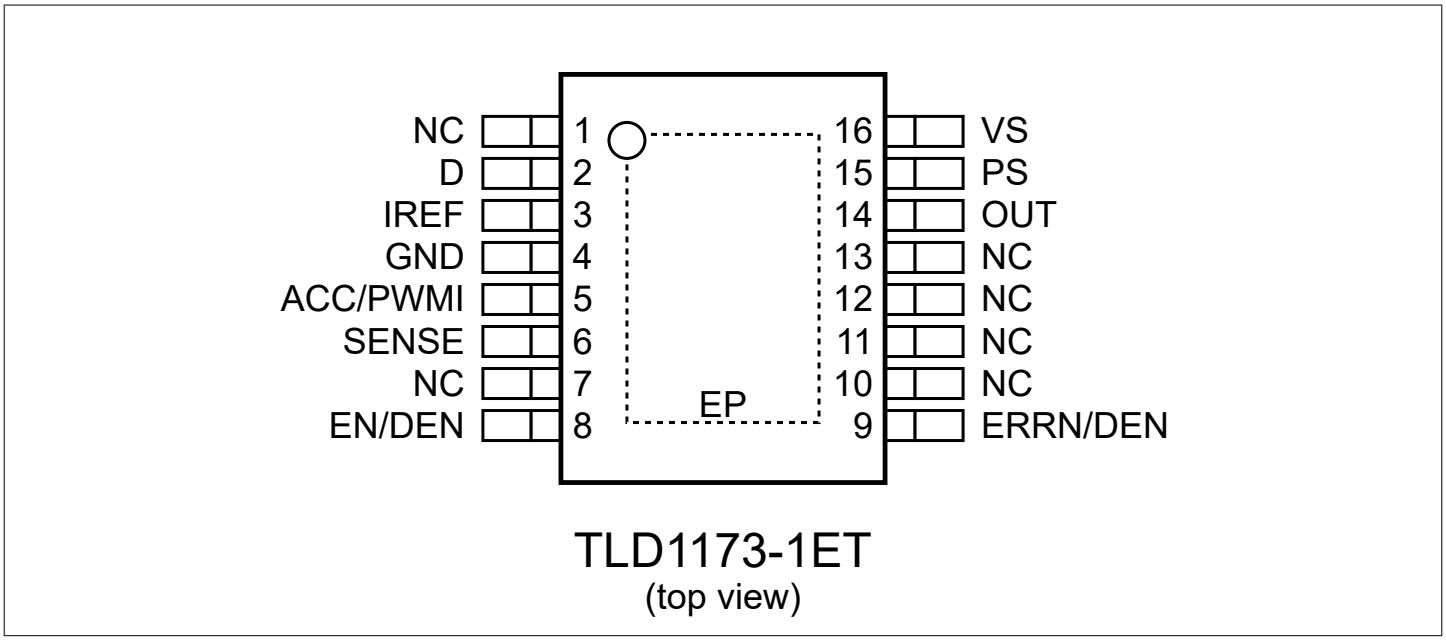


Figure 2 PG-TFDSO-16

3.2 Pin definitions and functions

Table 2 Pin definitions and functions

Pin	Symbol	Function
16	VS	**Power supply voltage** Battery supply input
4	GND	**Ground** Ground potential. Connect externally close to the chip
8	EN/DEN	**Output enable and diagnosis control input** Connect to V_S via a resistor divider to enable OUT control and diagnosis capability
9	ERRN/DEN	**ERROR flag I/O and diagnosis control input** Open drain, active low. Connect to V_S via pull-up resistor for ERROR flag capability only otherwise connect to V_S via a resistor divider to enable diagnosis capability
6	SENSE	**Sense input** Connect to low ohmic accurate sense resistor
14	OUT	**Channel output pin** Open drain linear current sink. Connect to the target load
15	PS	**Power shift** Connect to external power resistor

(table continues...)

Table 2 (continued) Pin definitions and functions

Pin	Symbol	Function
2	D	**Disable/delay error input** Connect to a capacitor, leave open or connect to GND depending on the required diagnostic management
5	ACC/PWMI	**Analog current control and PWMI input pin** Connect to external low power resistor or apply a desired reference voltage to adjust the output current. Connect to external NTC to apply thermal derating. It is possible also to connect to an external open drain PWM controller
3	IREF	**Current reference generation** Connect to an external accurate low power resistor to generate a current reference
1,7,10, 11,12,13	NC	**Not connected** Leave these pins open
Exposed pad	EP	**Exposed pad** Used only for thermal dissipation purpose. Connect externally to GND close to the chip

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

[1] $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	PRQ-32
EN/DEN voltage	$V_{EN/DEN}$	-0.3	–	40	V	–	PRQ-55
Output voltage	V_{OUT}	-0.3	–	40	V	–	PRQ-56
Power shift voltage	V_{PS}	-0.3	–	40	V	–	PRQ-59
Sense voltage	V_{SENSE}	-0.3	–	0.9	V	–	PRQ-63
ERRN/DEN voltage	$V_{ERRN/DEN}$	-0.3	–	40	V	–	PRQ-61
D voltage	V_D	-0.3	–	5.5	V	–	PRQ-175
ACC/PWMI voltage	$V_{ACC/PWMI}$	-0.3	–	5.5	V	–	PRQ-64
IREF voltage	V_{IREF}	-0.3	–	5.5	V	–	PRQ-176
Temperatures							
Junction temperature	T_{J_ABS}	-40	–	150	°C	–	PRQ-39
Storage temperature	T_{STG}	-55	–	150	–	–	PRQ-40
ESD robustness							
ESD robustness all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	ESD robustness, Human Body Model “HBM” according to AEC Q100-002	PRQ-53
ESD robustness all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	ESD robustness, Charged Device Model “CDM” according to AEC Q100-011 Rev.D	PRQ-41
ESD robustness corner pins (CDM)	$V_{ESD(CDM)\ CR}$	-750	–	750	V	ESD robustness, Charged Device Model “CDM” according to AEC Q100-011 Rev.D	PRQ-54

1) Not subject to production test, specified by design

***Note**:* *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

Table 4 Functional range

$T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage for operating range	$V_{S(func)}$	5.5	–	18	V	–	PRQ-33
Extended supply voltage for operating range	$V_{S(ext)}$	4.5	–	36	V	–	PRQ-71
Currents							
Channel output current	$I_{SENSE(func)}$	5	–	400	mA	–	PRQ-224
Power dissipation							
Max. static and dynamic power dissipation	P_{max}			1.5	W	T_A = 85°C and R_{thJA} = 42 K/W	PRQ-419
Temperatures							
Junction temperature	$T_{J(func)}$	-40	–	150	°C	–	PRQ-72

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. Within the Extended Operation range, parameters deviations are possible. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

4.3 Thermal resistance

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org*

Table 5 Thermal resistance

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to top	Ψ_{JTOP}	–	8	–	K/W	1)	PRQ-34
Junction to case	R_{thJC}	–	8	–	K/W	2)	PRQ-49
Junction to ambient 1s0p board	R_{thJA1}	–	64	–	K/W	3) T_A = 85°C	PRQ-48
Junction to ambient 2s2p board	R_{thJA2}	–	42	–	K/W	4) T_A = 85°C	PRQ-180

1) Specified Ψ_{JTOP} is derived under natural convention conditions and provide a correlation between the junction temperature and the temperature on the package top surface. T_A = 85°C. Total power dissipation = 1.5 W

2) Specified R_{thJC} is simulated at natural convention on a cold plate setup (all pins and exposed pad are fixed at ambient temperature). T_A = 85°C. Total power dissipation = 1.5 W

3) Specified R_{thJA1} is generated in accordance with JEDEC JESD51-3 standards at natural convection on FR4 1s0p board. The simulation has been performed on a 76.2 x 114.3 x 1.5 mm board with 70 µm, 300 mm^2 cooling area. Total power dissipation 1.5W distributed statically and homogenously over all power stages

4) Specified R_{thJA2} is generated in accordance with JEDEC JESD51-5,-7 standards at natural convection on FR4 2s2p board. The simulation has been performed on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). A total of six thermal via (∅ = 0.3 mm, plating 25 µm) is placed under the exposed pad contacting the first inner copper layer. Total power dissipation 1.5W distributed statically and homogenously over all power stages

5 Internal supply

This chapter describes the internal supply, its main parameters and functionality.

5.1 Description

As soon as the voltage applied at the supply pin VS is above $V_{SUV(th)}$ and the voltage applied at the EN/DEN pin is above $V_{EN(th)}$, the device is ready to deliver output current from the output stage after the power on reset time t_{POR}. When the supply voltage V_S is below the threshold $V_{SUV(th)}$, the internal Power-ON-Reset (POR) function holds the device in reset state.

The power on reset time t_{POR} has to be taken into account under relevant application conditions, i.e. with PWM control from VS.

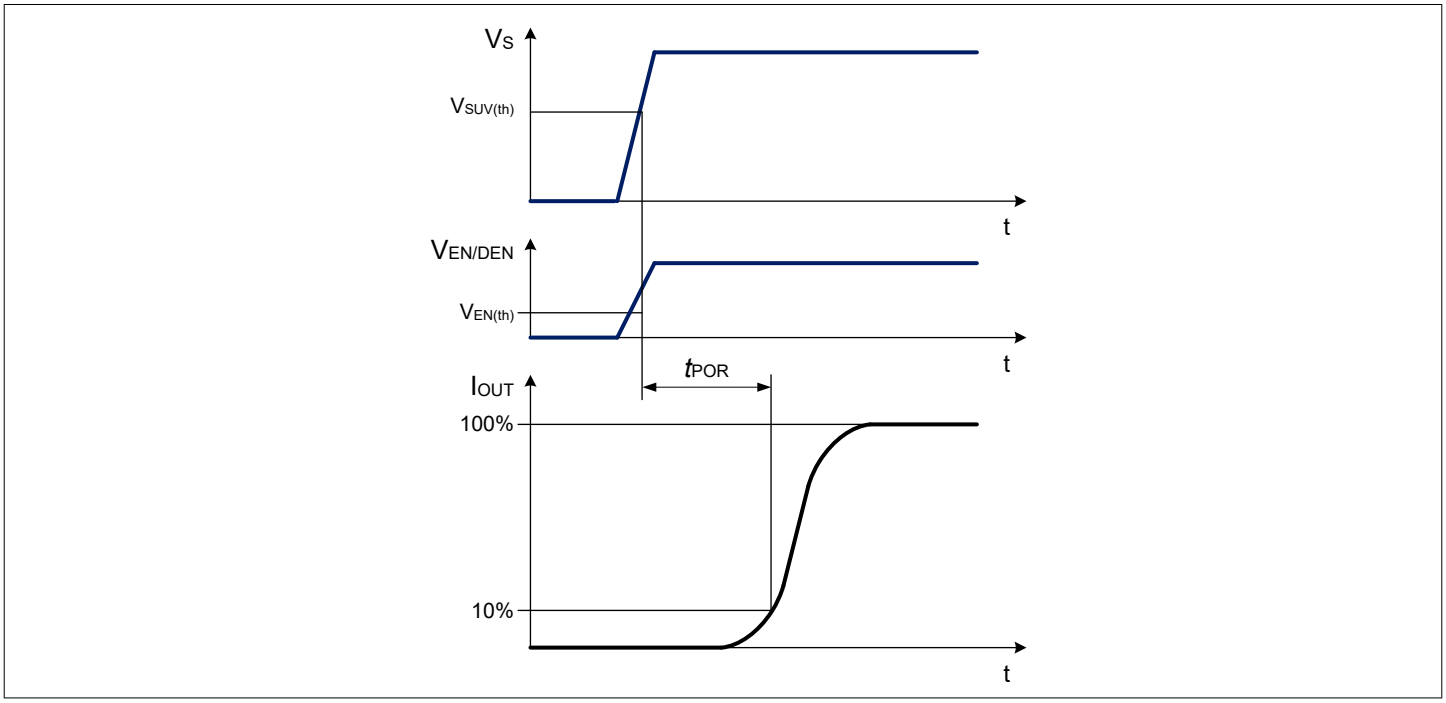


Figure 3 Power on reset timing diagram

If the voltage applied at the EN/DEN pin is below $V_{EN(th)}$ for more than t_{SLEEP} the device enters sleep mode. In this state all internal functions are switched off and the current consumption is reduced to $I_{VS(sleep)}$.

5.2 Electrical characteristics

Table 6 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{VS(sleep)}$	–	–	3	µA	$V_{EN/DEN}$ = 0 V T_J = 150°C	PRQ-85
Current consumption, active mode (no fault)	$I_{VS(active)}$	–	2.5	3.5	mA	$V_{EN/DEN}$ = 5.5 V $V_{ACC/PWMI}$ = 2.4 V IREF pin left open	PRQ-154

(table continues...)

Table 6 (continued) Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption during fault condition (1-fail-all-OFF)	$I_{VS(fault, ERRN)}$	–	–	850	µA	$V_{EN/DEN}$ = 5.5 V V_{ERRN} = 0 V D pin open	PRQ-87
VS undervoltage threshold	$V_{SUV(th)}$	3.5	–	4.5	V	–	PRQ-89
EN/DEN outputs enable threshold	$V_{EN(th)}$	0.6	–	1.8	V	–	PRQ-159
EN/DEN outputs enable hysteresis	$V_{EN(hys)}$	80	120	–	mV	1)	PRQ-160
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	5	µA	$V_{EN/DEN}$ = 3 V	PRQ-161
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	150	µA	$V_{EN/DEN}$ = 18 V	PRQ-371
Power on reset delay time	t_{POR}	–	–	75	µs	V_S rising edge from 0 V to 8 V to 10% of output current $V_{EN/DEN}$ = 5.5 V $V_{ACC/PWMI}$ ≥ 2.4 V	PRQ-164
Sleep mode filter time	t_{SLEEP}	15	–	45	ms	–	PRQ-109

1) Not subject to production test, specified by design

6 Power stage

The power stage sinks from the OUT pin an output current I_{OUT} which is a function of the external sense resistor placed at SENSE pin.

The maximum output current is limited by the power dissipation P_{max} and used cooling areas.

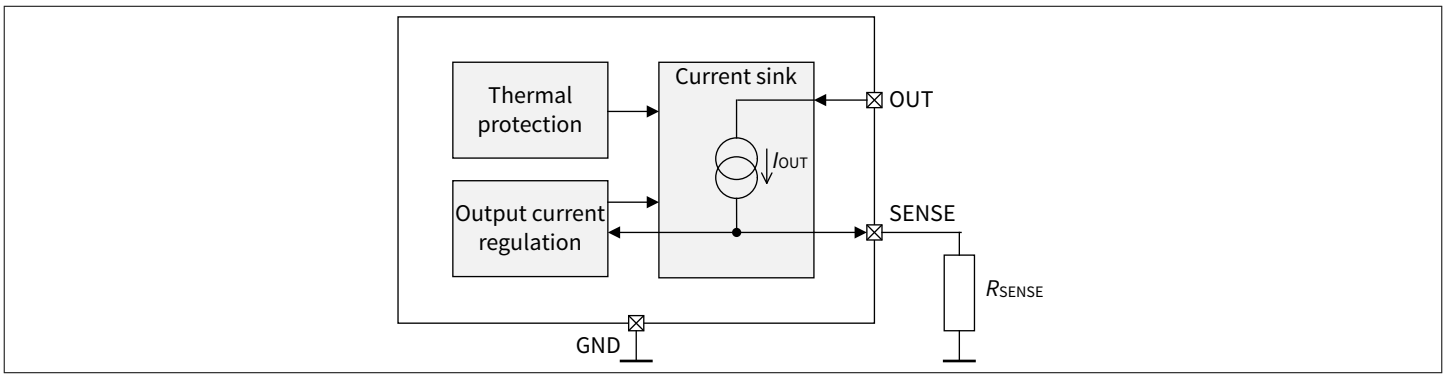


Figure 4 Power stage block diagram

6.1 Output current regulation

The output current regulation block controls the LEDs current by regulating the voltage drop $V_{SENSE(reg)}$ on the external low-side current-sense resistor R_{SENSE} placed between SENSE pin and GND.

When the LEDs current is in regulation, the LEDs current value can be calculated by using the following equation:

$$I_{SENSE} = \frac{V_{SENSE(reg)}}{R_{SENSE}} \quad (1)$$

For an operating output current control loop, the power stage dropout voltage ($V_{DR,CS}$), the $V_{SENSE(reg)}$ voltage, the forward voltage V_{D_RP} of the reverse polarity protection diode (when used) and the minimum supply voltage have to be considered in the LED string design.

To grant a proper control of the output current the following equation has to be satisfied:

$$V_S \geq V_{SENSE(reg)} + V_{DR,CS} + V_{LED\_STRING} + V_{D\_RP} \quad (2)$$

In case the supply voltage drops below the minimum requested, the LEDs current is no longer properly regulated. Consequently, a lower current is delivered and the voltage across the R_{SENSE} resistor is lower than the expected $V_{SENSE(reg)}$.

***Note**: The R_{SENSE} has to be placed as close as possible to the pin VSENSE to avoid current regulation instability.*

6.2 Thermal protection

A thermal protection function is integrated into the device to prevent IC damage under fault conditions described in the datasheet. Fault conditions are considered as "outside" the normal operating range. Protective functions are not designed for continuous operations.

The thermal protection function is achieved by temperature monitoring of the power stage. As soon as the junction temperature exceeds the overtemperature threshold T_{JSD}:

- The output current is disabled by turning off the power stage
- The ERRN/DEN pin is pulled low
- The current consumption is below $I_{VS(fault, ERRN)}$

Once the junction temperature falls below T_{JSD} - $T_{J(hys)}$:

- The power stage recovers to normal operation
- The ERRN/DEN pin is released

6.3 Electrical characteristics

Table 7 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage currents							
Output leakage current	$I_{OUT(leak)}$	–	–	1	µA	1) T_J = 85°C $V_{OUT} \leq$ 16 V $V_{ACC/PWMI}$ = 0 V $V_{EN/DEN}$ = 5.5 V	PRQ-116
Output leakage current	$I_{OUT(leak)}$	–	–	5	µA	T_J = 150°C $V_{OUT} \leq$ 16 V $V_{ACC/PWMI}$ = 0 V $V_{EN/DEN}$ = 5.5 V	PRQ-118
Sense regulation voltage accuracy							
SENSE voltage regulation accuracy	$V_{SENSE(reg)}$	384	400	416	mV	$V_{ACC/PWMI} \geq$ 2.4 V	PRQ-120
SENSE voltage regulation accuracy	$V_{SENSE(reg)}$	95	100	105	mV	$V_{ACC/PWMI}$ = 0.9 V	PRQ-121
SENSE voltage regulation accuracy	$V_{SENSE(reg)}$	14	20	26	mV	$V_{ACC/PWMI}$ = 0.5 V	PRQ-123
Power stage drop out							
Power stage drop out voltage	$V_{DR,CS}$	–	–	0.6	V	I_{OUT} = 400 mA	PRQ-124
Thermal protection thresholds							
Overtemperature shutdown threshold	T_{JSD}	165	175	185	°C	2)	PRQ-131
Overtemperature hysteresis	$T_{J(hys)}$	5	10	15	°C	2)	PRQ-132

1) Not subject to production test, specified by design
2) Not subject to production test, specified by design

7 Power shift

The device manages high power dissipation (higher than allowed by the thermal impedance R_{thJA} of the application) by separating the LED current into two current branches:

- One current sink path through an external drop element (power resistor) and the internal power shift
- One current sink path through the internal power stage

The current flowing into the power shift path and the one flowing into the power stage path are dynamically adjusted in order to obtain that the sum of I_{OUT} and I_{PS} currents is equal to the regulated I_{SENSE} current.

The distribution of the current between the power shift path and the power stage path is defined by the power shift resistor value, the load and the applied battery voltage V_S.

In order to proper dimension the resistor value the following parameters have to be considered:

- Maximum current I_{PS} intended to flow into the power shift path at maximum battery operative voltage $V_{S(PEAK)}$
- Forward voltage V_{LED_STRING} of the output LED load and forward voltage V_{D_RP} of the reverse polarity protection diode
- Voltage drop on the internal power shift element ($V_{PS\_INT} = I_{PS} \times R_{PS\_INT(ON)}$)
- Regulated V_{SENSE} voltage

The resistor can then be calculated using the following formula:

$$R_{PS} = \frac{V_{S(PEAK)} - V_{D\_RP} - V_{LED\_STRING} - V_{PS\_INT} - V_{SENSE}}{I_{PS}} \quad (3)$$

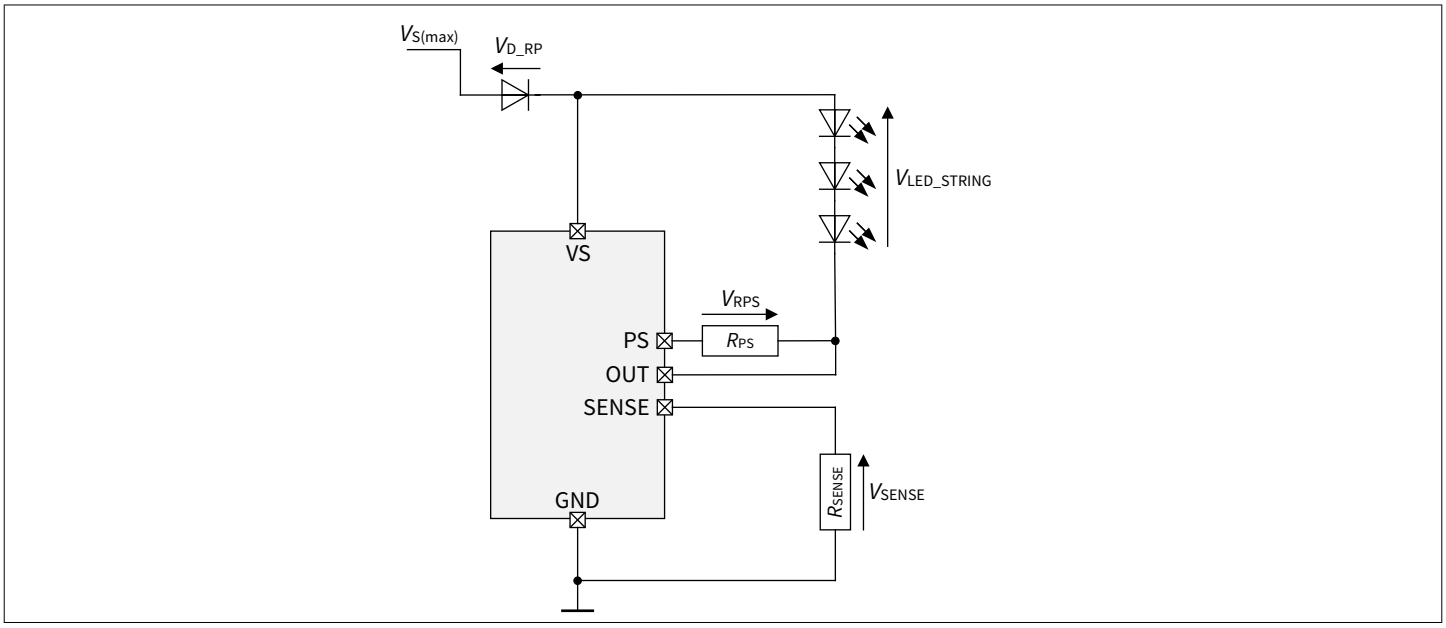


Figure 5 Power shift resistor diagram

***Note**: Please consider that if the R_{PS} is set to 0 Ω all the LED current flows inside the internal power shift path leading to a possible overheating of the device up to the thermal shut-down.*

7.1 Electrical characteristics

Table 8 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power shift ON resistance	$R_{PS\_INT(ON)}$	–	–	3	Ω	1) I_{PS} = 400 mA	PRQ-275
Power shift leakage current	$I_{PS(leak)}$	–	–	1	µA	1) T_J = 85°C $V_{PS} \leq$ 16 V $V_{ACC/PWMI}$ = 0 V $V_{EN/DEN}$ = 5.5 V	PRQ-277
Power shift leakage current	$I_{PS(leak)}$	–	–	3	µA	T_J = 150°C $V_{PS} \leq$ 16 V $V_{ACC/PWMI}$ = 0 V $V_{EN/DEN}$ = 5.5 V	PRQ-287
Power shift ratio	I_{PS}/I_{SENSE}	0.95	–	–	–	V_{PS} - V_{SENSE} > 1.5 V $V_{ACC/PWMI} \geq$ 0.9 V	PRQ-279
SENSE voltage regulation accuracy	$V_{SENSE(reg)}$	384	400	416	mV	$V_{ACC/PWMI} \geq$ 2.4 V	PRQ-408
SENSE voltage regulation accuracy	$V_{SENSE(reg)}$	95	100	105	mV	$V_{ACC/PWMI}$ = 0.9 V I_{SENSE} > 20 mA	PRQ-410
SENSE voltage regulation accuracy	$V_{SENSE(reg)}$	14	20	28	mV	$V_{ACC/PWMI}$ = 0.5 V I_{SENSE} > 20 mA	PRQ-414

1) Not subject to production test, specified by design

8 PWM control

PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

The PWM modulation is performed via the ACC/PWMI pin. The power stage and the power shift are disabled if the voltage applied on the ACC/PWMI pin is lower than $V_{PWM(OFF)}$ while they are enabled if the voltage applied on the PWMI/ACC pin is higher than $V_{PWM(ON)}$.

In Figure 6 two examples of PWM dimming are shown via the ACC/PWMI input pin:

1. In case a resistor is needed on the ACC/PWMI input pin to apply analog current control (i.e. binning or thermal derating) the PWM signal can be applied using an open drain output from the PWM generator
2. In case the analog current control function is not needed a push-pull output from the PWM generator can be used to apply the PWM modulation

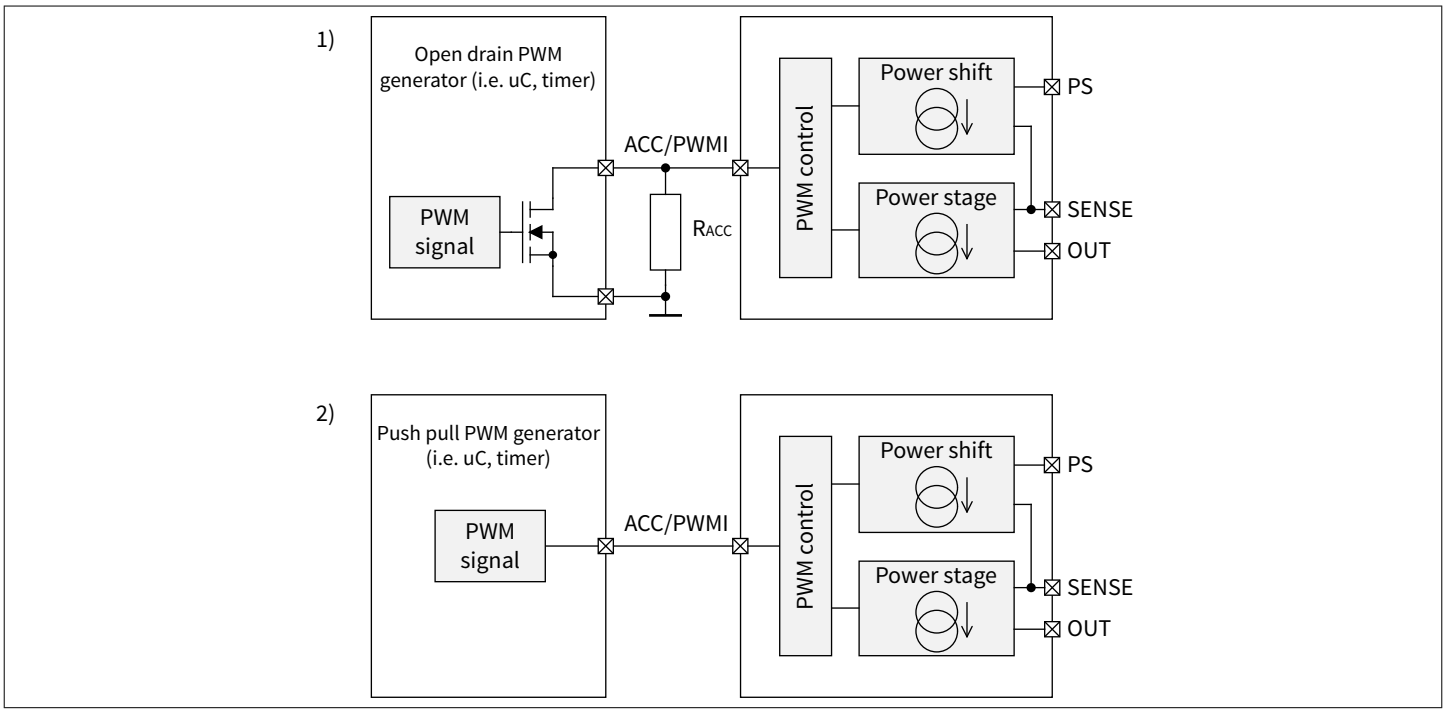


Figure 6 PWM control via ACC/PWMI input pin

The PWM signal can be applied via the EN/DEN pin as well to allow PWM modulation from the battery line. Indeed by applying a proper filtering on the VS pin to avoid to trigger the VS undervoltage threshold, the t_{POR} delay time would be applied only on the first PWM pulse generation after the exit from sleep state, like shown in Figure 9.

When applied on the EN/DEN pin the PWM signal has a frequency range f_{PWM} to avoid to turn-off the channel by triggering the t_{SLEEP} filter time.

The power stage and the power shift of the channel are enabled if the voltage applied on the EN/DEN pin is higher than $V_{EN(th)}$ while they are disabled if the voltage applied on the EN/DENx pin is lower than $V_{EN(th)}$.

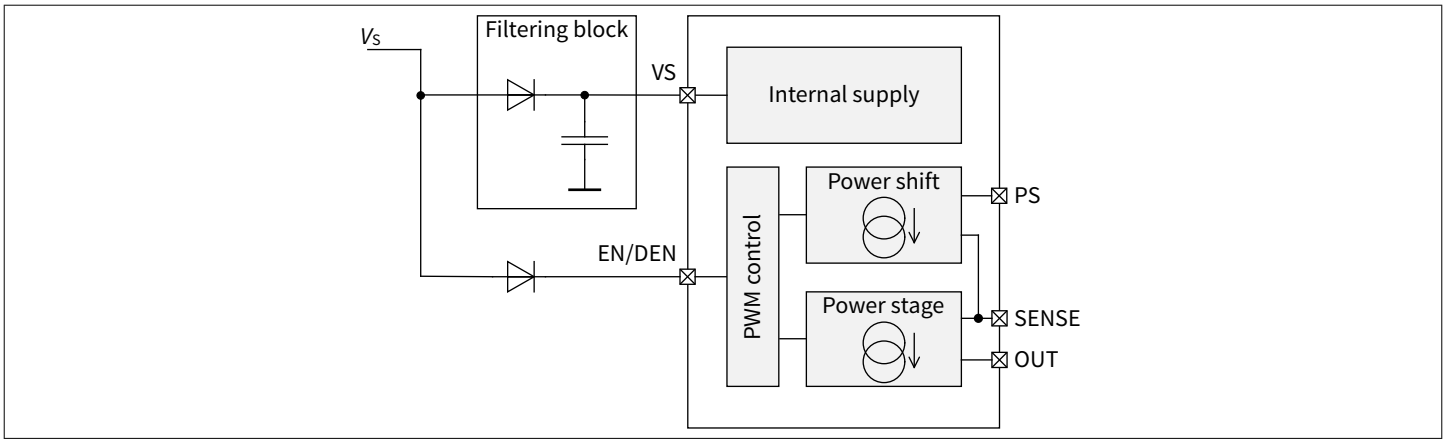


Figure 7 PWM control via EN/DEN input pin

When the voltage applied on the ACC/PWMI pin is below $V_{PWM(OFF)}$, the load diagnostic is disabled unless a fault was previously detected.

As well, when the voltage applied on the EN/DEN pin is below $V_{DEN(th)}$, the load diagnostic is disabled unless a fault was previously detected.

In particular, if a fault is already present when the voltage applied on the ACC/PWMI pin is below $V_{PWM(OFF)}$ or the voltage applied on EN/DEN pin is below $V_{DEN(th)}$ the diagnostic is kept active until the fault condition disappears, after that it is then disabled.

The PWM control block implements a slope control of the V_{SENSE} voltage in order to improve EMC performances. The slew rate timings are defined by dV/dt_{ON} and dV/dt_{OFF} parameters.

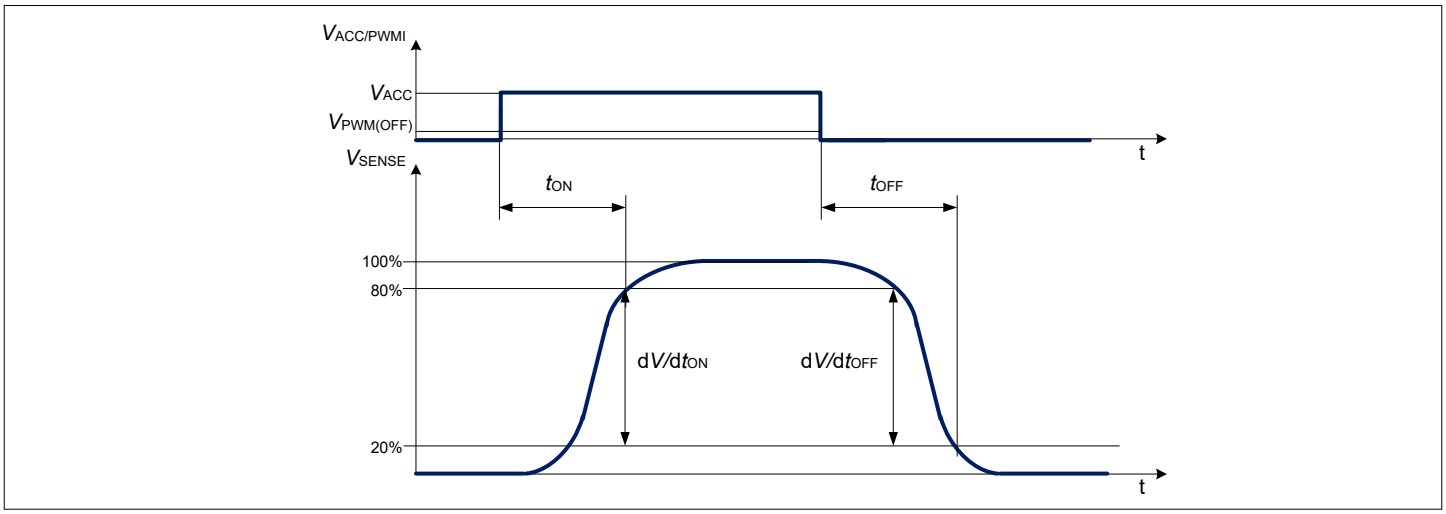


Figure 8 PWMI control timing diagram for $V_{ACC/PWMI} \geq 2.4$ V

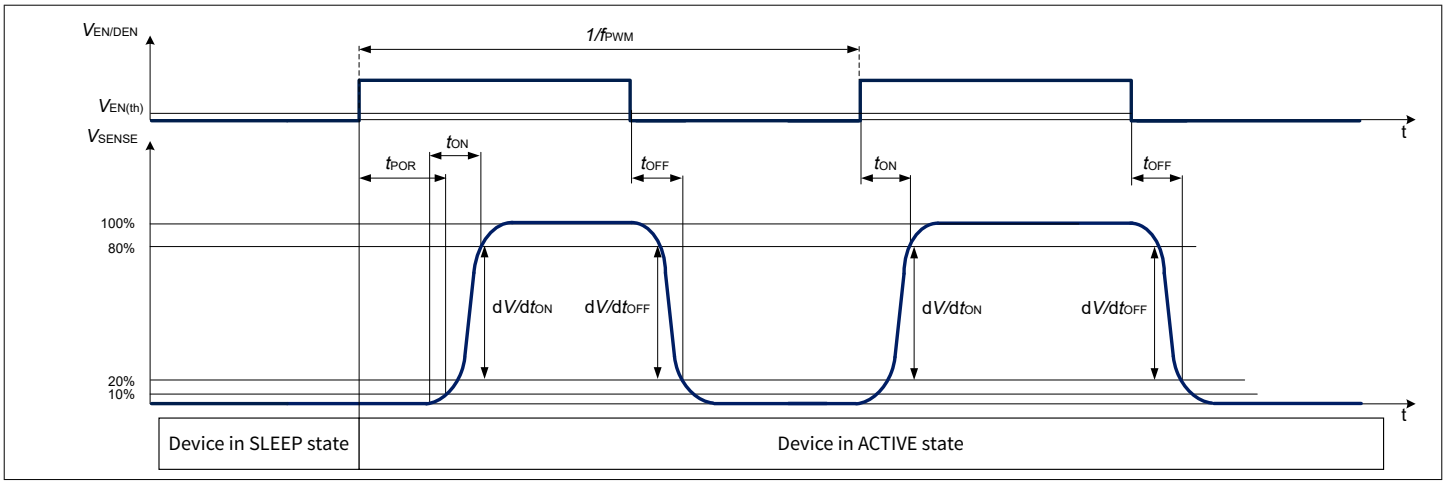


Figure 9 PWM control on EN/DEN timing diagrams for $V_{ACC/PWMI} \geq 2.4$ V

8.1 Electrical characteristics

Table 9 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWM turn off threshold	$V_{PWM(OFF)}$	0.35	0.4	–	V	–	PRQ-145
PWM turn on threshold	$V_{PWM(ON)}$	–	–	0.45	V	–	PRQ-261
PWM frequency range	f_{PWM}	100	–	–	Hz	1)	PRQ-146
PWM turn on time	t_{ON}	–	–	20	µs	1) V_{SENSE} rising to 80% of regulation $V_{ACC/PWMI} \geq 2.4$ V	PRQ-147
PWM turn off time	t_{OFF}	–	–	20	µs	1) V_{SENSE} falling to 20% of regulation $V_{ACC/PWMI}$ falling from ≥ 2.4 V to less than $V_{PWM(OFF)}$	PRQ-148
VSENSE rising slew rate	dV/dt_{ON}	15	35	50	mV/µs	1) V_{SENSE} rising from 20% to 80% of regulation $V_{ACC/PWMI} \geq 2.4$ V	PRQ-149
VSENSE falling slew rate	dV/dt_{OFF}	-50	-35	-15	mV/µs	1) V_{SENSE} falling from 80% to 20% of regulation $V_{ACC/PWMI}$ falling from ≥ 2.4 V to less than $V_{PWM(OFF)}$	PRQ-150

1) Not subject to production test, specified by design

9 Analog output current control

The analog output current control function adjusts the V_{SENSE} voltage by sensing the applied voltage on the ACC/PWMI pin $V_{ACC/PWMI}$.

As described in Chapter 6 the output current provided by the channel is a direct function of the regulated voltage V_{SENSE}. In this way by adjusting the voltage applied on the ACC/PWMI pin it is possible to control the output current.

$$I_{SENSE} = \frac{0.2 \times V_{ACC/PWMI} - 0.08 \quad V}{R_{SENSE}} \tag{4}$$

The relation between the ACC/PWMI voltage $V_{ACC/PWMI}$ and the respective regulated voltage V_{SENSE} is shown in the Figure 10.

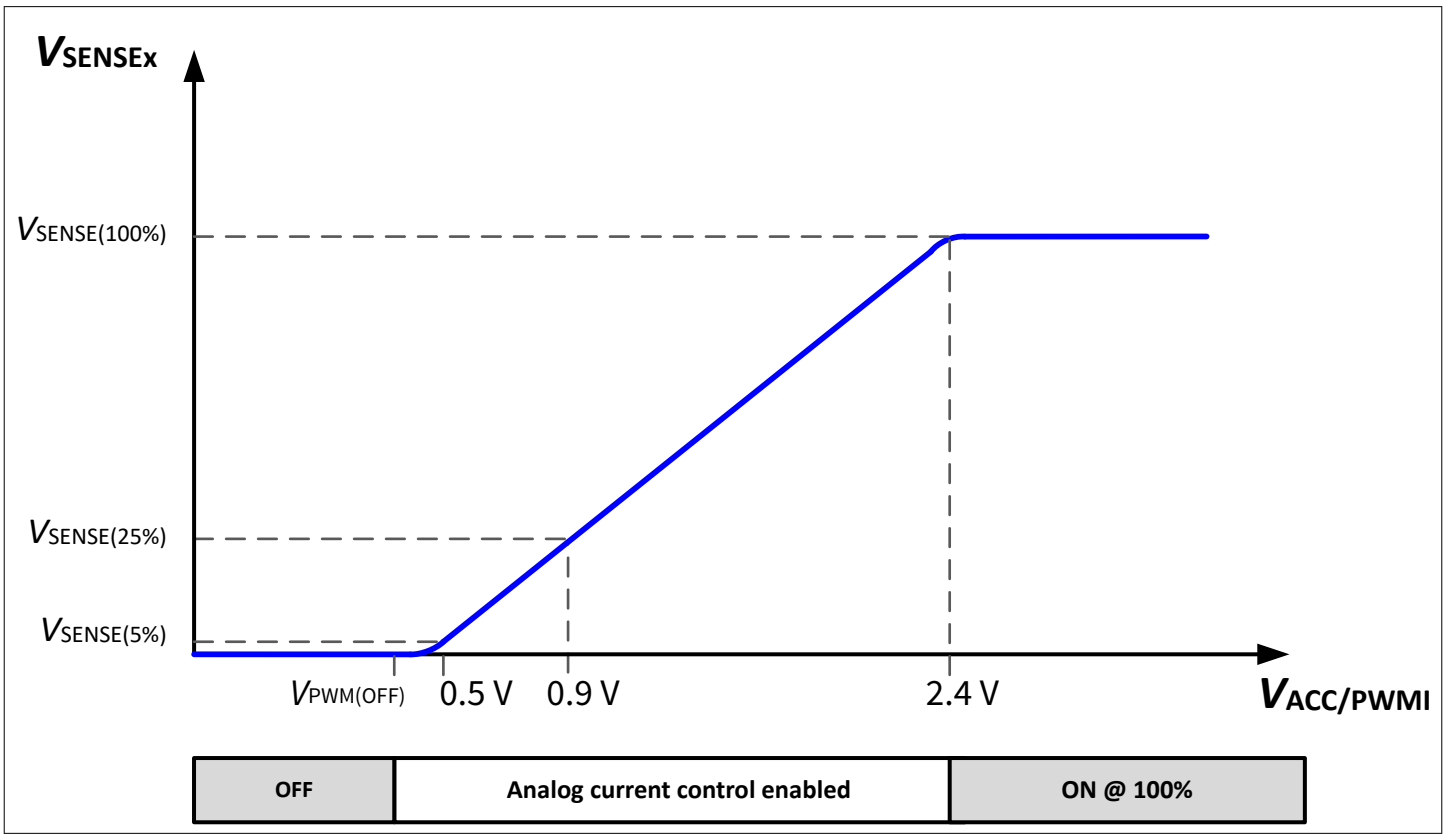


Figure 10 Analog output current control

The voltage on ACC/PWMI can be set by applying an accurate external resistor on the ACC/PWMI pin. In case the resistor is placed in another PCB (i.e. binning resistor) it is recommended to add capacitor of 220 nF close to the ACC/PWMI pin.

The ACC/PWMI pin outputs a constant current based on the IREF output current and the ACC current ratio I_{ACC}/I_{IREF}.

***Note**: In case the analog output current control function is not needed it is recommended to put 100 kΩ pull-down resistor on the IREF pin to proper bias the ACC/PWMI voltage to avoid wrong V_{SENSE} setting.*

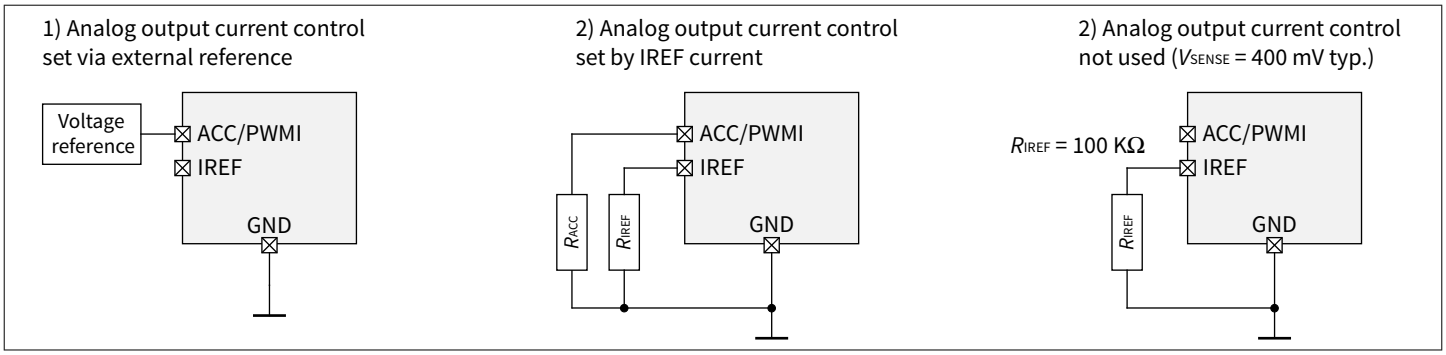


Figure 11 Analog output current control configurations

9.1 Electrical characteristics

Table 10 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ACC current ratio	I_{ACC}/I_{IREF}	4.85	5	5.15	–	20 µA ≤ I_{IREF} ≤ 250 µA	PRQ-253

10 Current reference generation

The current reference generation block, outputs an accurate output reference current with low temperature shift.

The voltage on the IREF pin is regulated in the V_{IREF} range.

It turns out that the reference current can be set by placing an external resistor from IREF pin to GND and can be calculated using the following formula:

$$I_{IREF} = \frac{V_{IREF}}{R_{IREF}} \quad (5)$$

***Note**: The R_{IREF} has to be placed as close as possible to the pin IREF to avoid current regulation instability.*

10.1 Electrical characteristics

Table 11 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
IREF regulated voltage	V_{IREF}	1.164	1.2	1.236	V	–	PRQ-268
IREF current range	I_{IREF}	–	–	250	µA	–	PRQ-269
IREF capacitance	C_{IREF}	–	–	0.22	nF	1)	PRQ-273

1) Not subject to production test, specified by design

11 Load diagnostics

Several diagnosis features are integrated:

- Open load detection (OL)
- Short to supply detection (SC)
- Power shift short to supply detection (SC)
- Overtemperature thermal detection (OT)

The behavior of the device during overload conditions that lead to an excess of internal heating, up to overtemperature condition, is already described in chapter Thermal protection.

An open load condition is detected if the voltage across the power stage $V_{DR} = V_{OUT} - V_{SENSE}$ is below the threshold $V_{DR(OL)}$ for at least a filter time t_{fault}.

A short to supply condition is detected if the output voltage drop over the load $V_S - V_{OUT}$ is below the threshold $V_{OUT(SC)}$ for at least a filter time t_{fault}.

A power shift short to supply condition is detected if the power shift voltage drop $V_S - V_{PS}$ is below the threshold $V_{PS(SC)}$ for at least a filter time t_{fault}.

If an OL condition is detected on the OUT pin or a SC condition is detected on one of the OUT or PS pins, a pull-down current $I_{OUT(fault)}$ flows inside the OUT pin replacing the configured output current.

***Note**: The $I_{OUT(fault)}$ current is limited by the actual load impedance, e.g. it is reduced to zero with an ideal open load.*

11.1 Diagnostics enable

As soon as the voltage applied at the supply pin VS is above $V_{SUV(th)}$ and the voltage applied to the EN/DEN pin is above $V_{DEN(th)}$, the device is ready to detect and report fault conditions via ERRN/DEN pin.

There are several possibilities to program the output enable and diagnosis enable via EN/DEN pin, like a resistor divider from VS to GND, a Zener diode from EN/DEN to VS and also a logic control pin (e.g. from a microcontroller output).

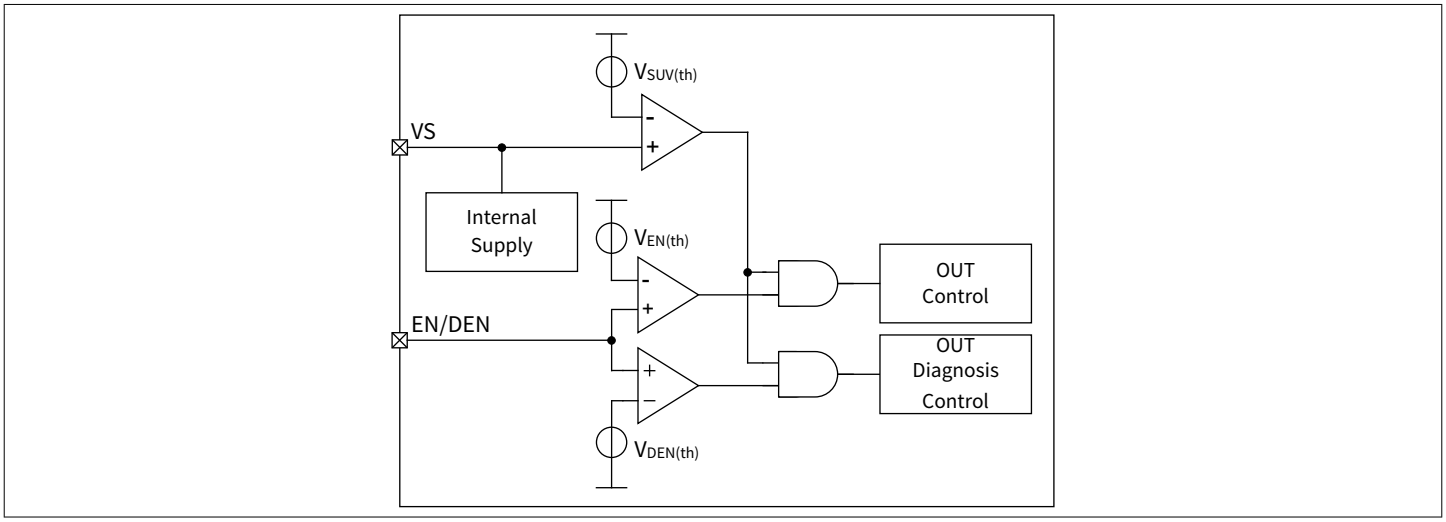


Figure 12 EN/DEN block diagram

11.2 ERRN/DEN pin

The device is able to report a detected failure in its driven load and react to a fault detected by another LED driver in the system if a shared error network is implemented (i.e. driving LED chains of the same light function). This is possible with the usage of an external pull-up resistor, allowing multiple devices to share the open-drain diagnostic output pin ERRN/DEN. All devices sharing a common error network are capable to detect the fault from any of the channels driven by the Basic+ family.

The open-drain ERRN/DEN pin applies a pull-down resistance $R_{ERRN(ON)}$ towards GND when a fault condition is detected for at least a filter time t_{fault}. Therefore, an active low state can be detected at ERRN/DEN pin when $V_{ERRN} < V_{ERRN(fault)}$ and the relative faulty output channel is switched off.

Similarly, when the fault is removed, ERRN/DEN pin is back in high impedance state and the channel reactivation is completed as illustrated in Figure 13.

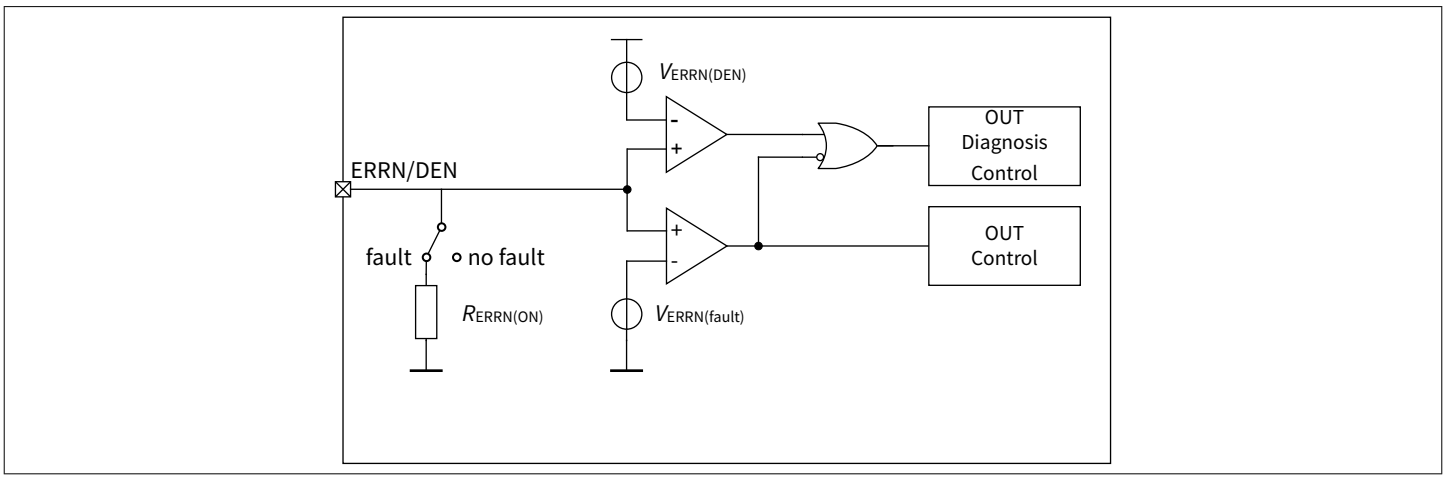


Figure 13 ERRN/DEN pin block diagram

To enable the possibility to decouple the $V_{DEN(th)}$ threshold from the $V_{EN(th)}$ threshold to have the device turning on as soon as needed independently from the diagnostic enable threshold, $V_{DEN(th)}$, the DEN functionality is duplicated on the ERRN/DEN pin.

The diagnostic reporting on ERRN/DEN pin and "open load", "short to supply" and the "power shift short to supply" protections are disabled, unless a fault was previously detected, as soon as one of the following condition is verified:

- The voltage on the ERRN/DEN pin is $V_{ERRN(fault)} < V_{ERRN/DEN} \leq V_{ERRN(DEN)}$
- The voltage on EN/DEN pin is below $V_{DEN(th)}$

When the ERRN/DEN pin applies a pull-down resistor $R_{ERRN(ON)}$ towards GND the $V_{ERRN(DEN)}$ threshold is masked to avoid unwanted toggling of the voltages on the ERRN/DEN pin.

11.3 D pin

The D pin is designed for two main purposes:

- To react to error conditions in LED arrays according to the implementation fault management policy, in systems where multiple LED chains are used for a given function as illustrated in Figure 14
- To extend the channel's deactivation delay time of a value t_D, adding a small signal capacitor from the D-pin to GND. In this way, an unstable or noisy fault condition may be prevented from switching off all the channels of a given light function (i.e. driven by several ICs sharing the same error network)

The functionality of the D-pin is shown in the simplified block diagram illustrated in Figure 15.

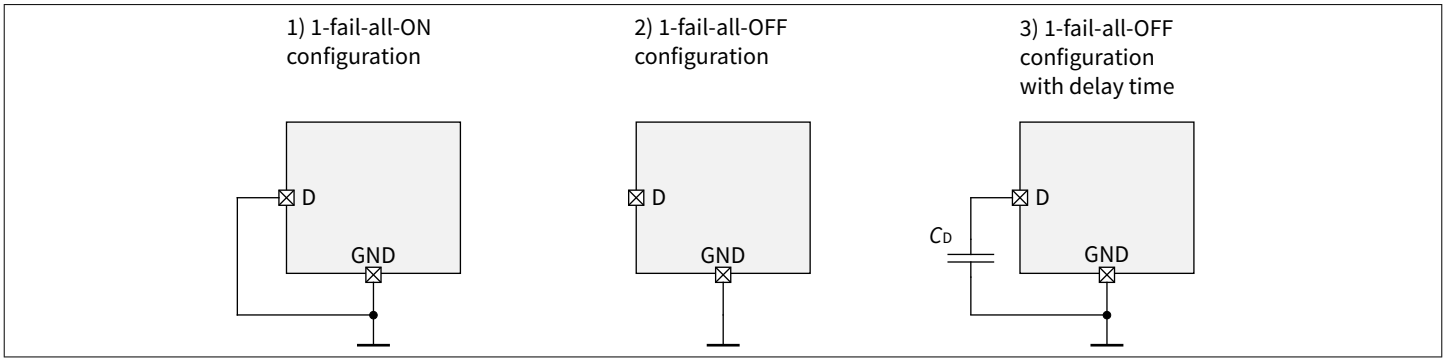


Figure 14 D pin configurations

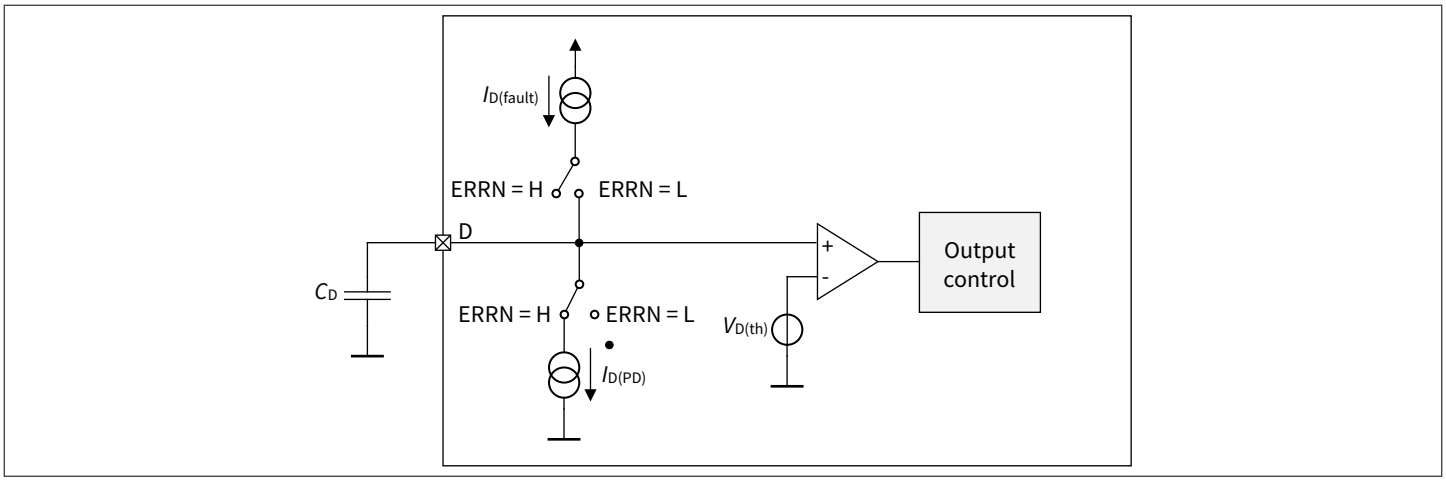


Figure 15 D pin block diagram

In normal operative status (no fault) a pull-down current $I_{D(PD)}$ is sunk from the D-pin to GND.

If there is a fault condition (for at least a filter time t_{fault}) in one of the LED channels driven by the IC or in any of the devices sharing the same ERRN error network line, a pull-up current $I_{D(fault)}$ is instead sourced from the D-pin.

If a capacitive or open load is applied at this pin (1-fail-all-OFF), its voltage starts rising. When $V_{D(th)}$ is reached at D-pin, all the channels driven by the device are switched off and if other devices share the same ERRN/DEN and D-pins nodes, all the devices turn their outputs off.

Alternatively, if the D-pin is tied to GND (1-fail-all-ON), only the channel that has been detected with a fault is safely deactivated.

The capacitor value used at the D-pin, C_D, sets the delay times $t_{D(set/reset)}$ according to the following equations:

$$t_{D(set)} = \frac{C_D \times V_{D(th)}}{I_{D(fault)}} \tag{6}$$

$$t_{D(reset)} = \frac{C_D \times \left(V_{D(CL)} - \left(V_{D(th)} - V_{D(hys)}\right)\right)}{I_{D(PD)}} \tag{7}$$

11.4 Fault management

With D pin open or connected with a capacitor to GND configuration, it is possible to switch off all the channels which share a common error network, without the need of an auxiliary microcontroller. For more details refer also to the timing diagram.

If there is a fault condition at the output or the power shift, the ERRN/DEN pin applies a pull-down resistance $R_{ERRN(ON)}$ towards GND and (with proper dimensioning of the external pull-up resistor) reaches a voltage level below $V_{ERRN(fault)}$. After $t_{D(set)}$, the voltage $V_{D(th)}$ is reached at D pin. The ERRN/DEN low voltage can also be used as input signal for a microcontroller to perform the desired diagnosis policy.

The OL and SC error conditions are not latched: as soon as the fault condition is no longer present, for at least a filter time $t_{fault,}$ ERRN/DEN goes back to high impedance. When its voltage is above $V_{ERRN(fault)}$, the D pin voltage starts decreasing and after $t_{D(reset)}$ goes below ($V_{D(th)}$ - $V_{D(th,hys)}$).

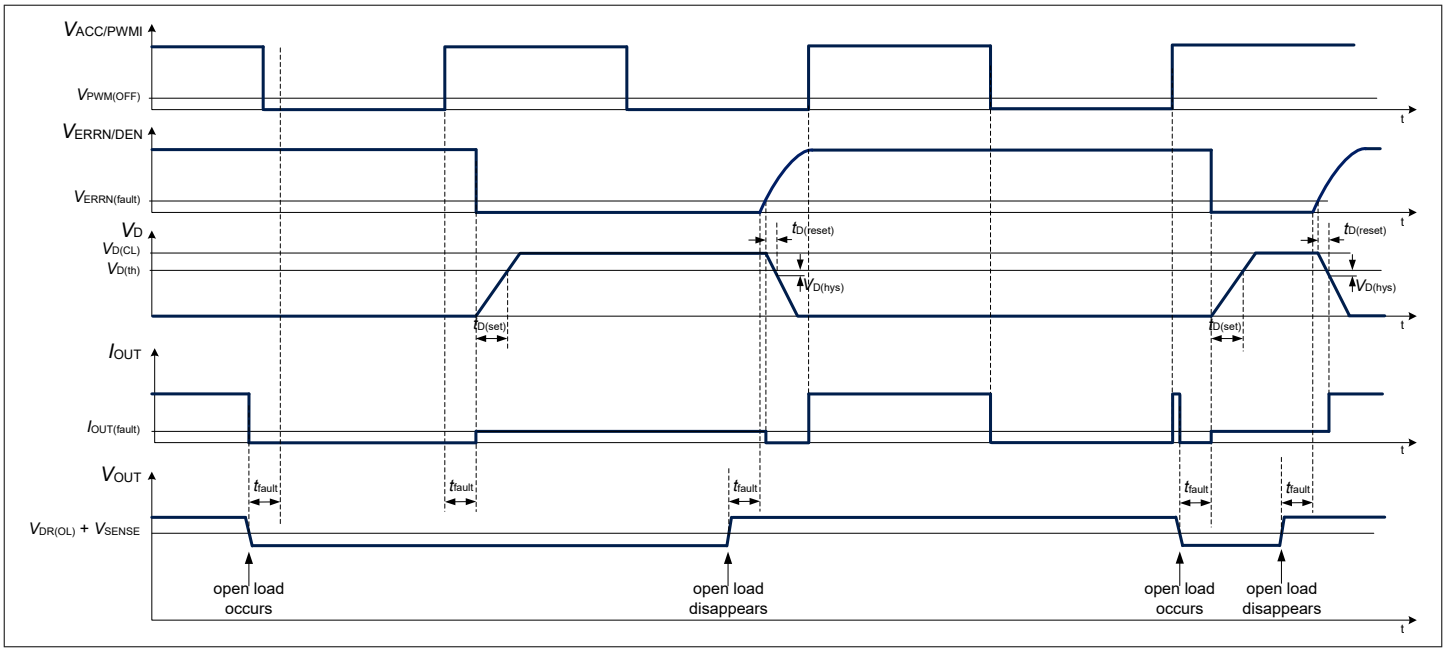


Figure 16 **Open load condition timing diagram example in 1-fail-all-OFF configuration (D pin open or connected to external capacitor)**

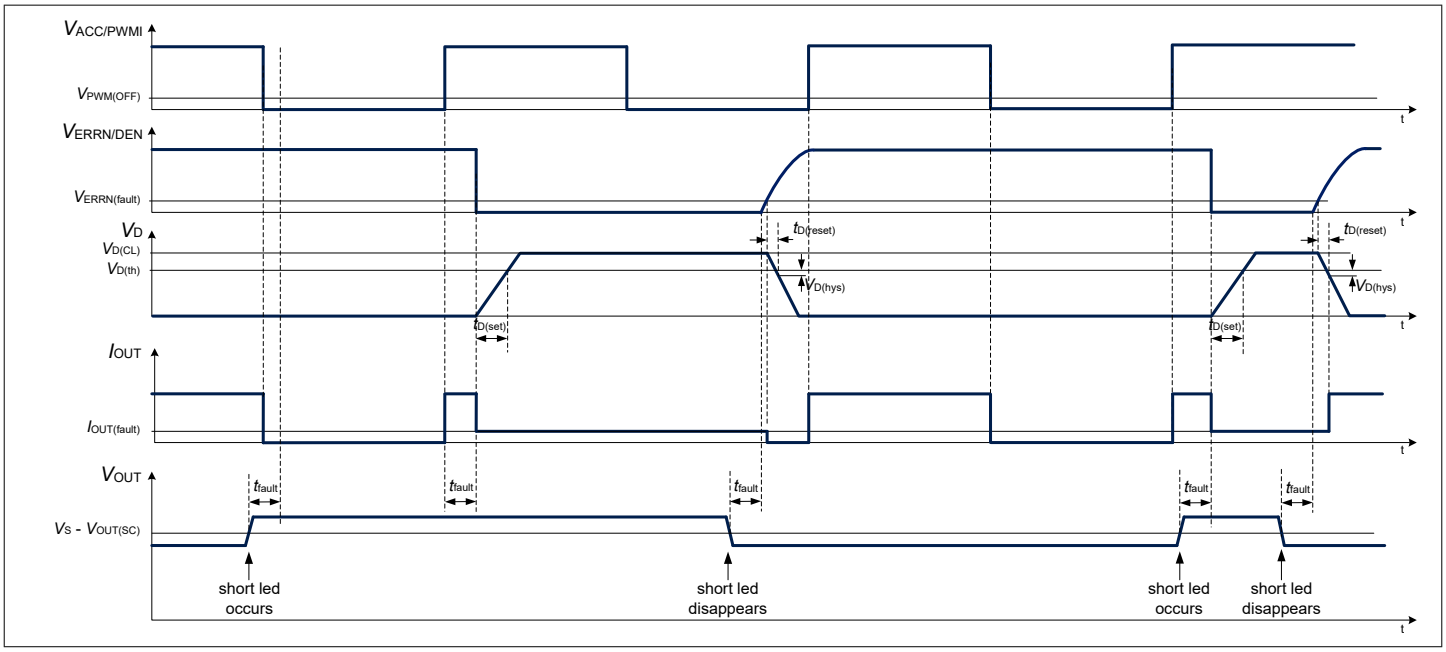


Figure 17 **Output short to supply condition timing diagram example in 1-fail-all-OFF configuration (D pin open or connected to external capacitor)**

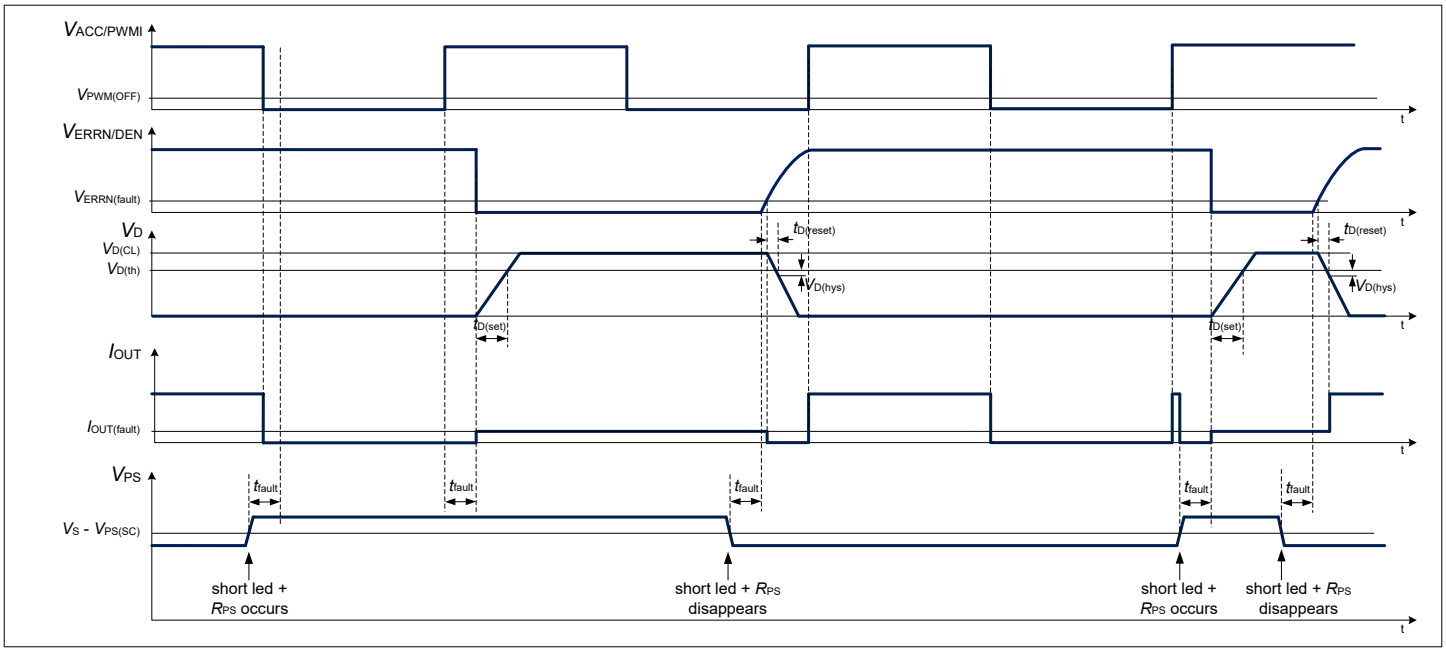


Figure 18 Power shift short to supply condition timing diagram example in 1-fail-all-OFF configuration (D pin open or connected to external capacitor)

With D pin connected to GND, it is possible to deactivate only the channel under fault condition, still sharing ERRN pin in a common error network with other devices of Basic+ family.

If there is a fault condition at the output or the power shift, the ERRN pin applies a pull-down resistance $R_{ERRN(ON)}$ to ground and the voltage level on this pin will drop below $V_{ERRN(fault)}$ if the external pull-up resistor is properly dimensioned. The ERRN low voltage can also be used as input signal for a µC to perform the desired diagnosis policy.

The OL and SC error conditions are not latched: as soon as the fault condition is no longer present (for at least for a filter time t_{fault}) ERRN/DEN goes back to high impedance and the output stage is activated again.

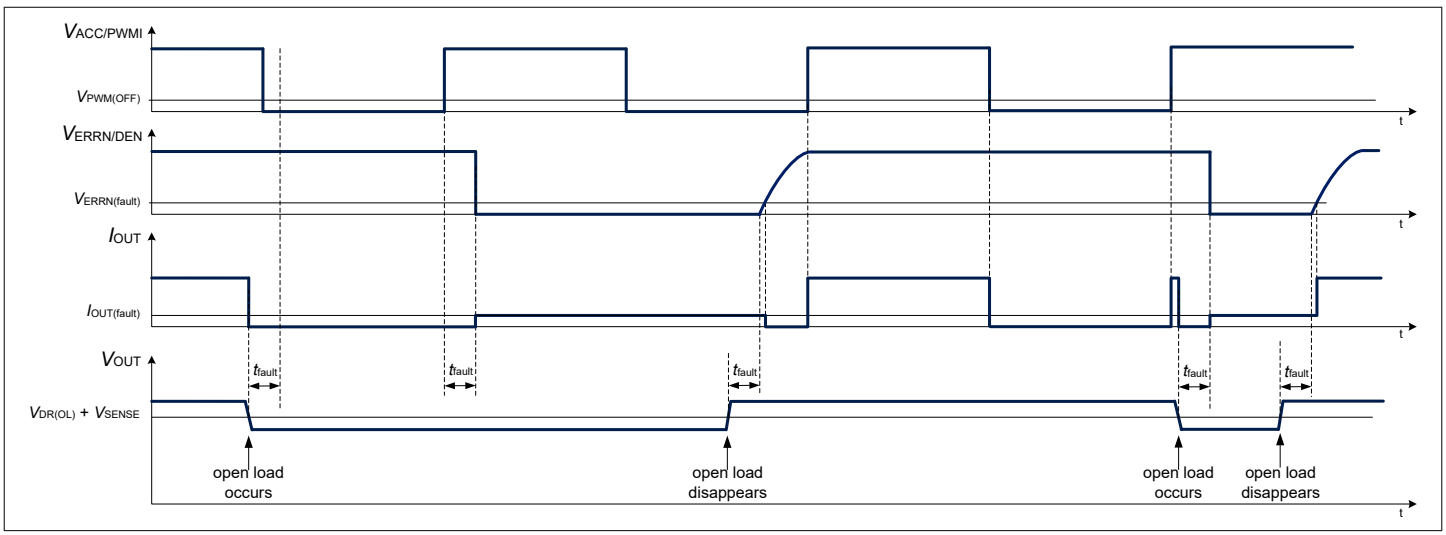


Figure 19 Open load condition timing diagram example in 1-fail-all-ON configuration (D pin shorted to GND)

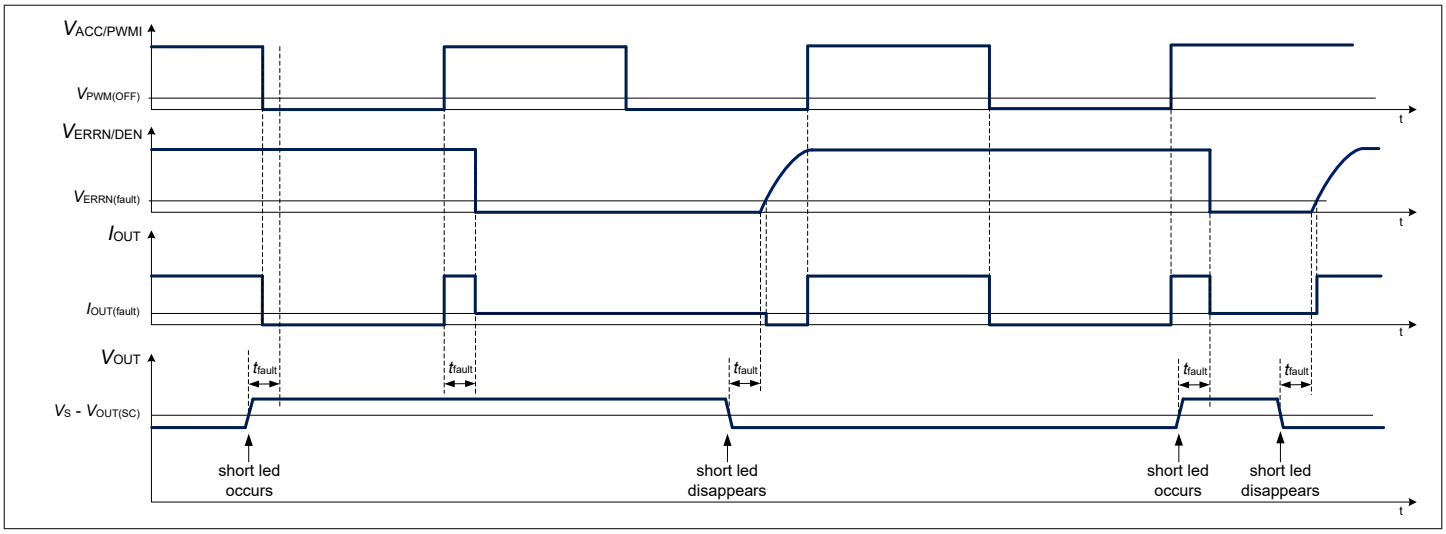


Figure 20 Output short to supply condition timing diagram example in 1-fail-all-ON configuration (D pin shorted to GND)

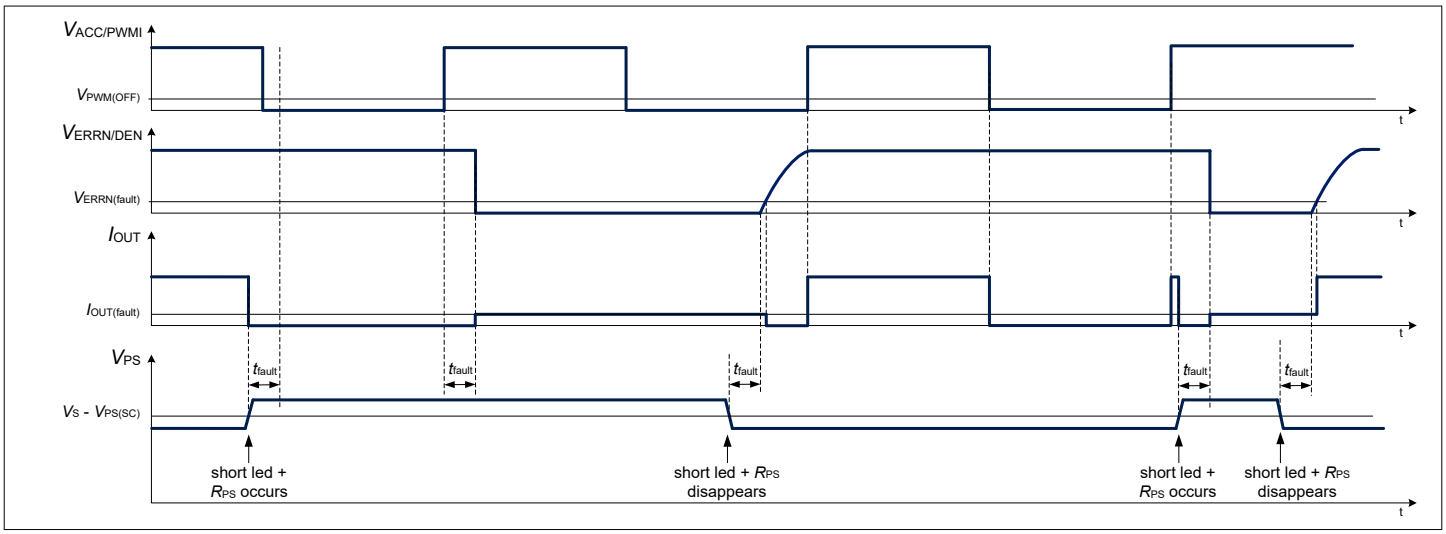


Figure 21 Power shift short to supply condition timing diagram example in 1-fail-all-ON configuration (D pin shorted to GND)

11.5 Electrical characteristics

Table 12 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRN/DEN pin							
ERRN fault threshold	$V_{ERRN(fault)}$	0.7	–	0.9	V	–	PRQ-193

(table continues...)

Table 12 (continued) Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRN ON resistance	$R_{ERRN(ON)}$	–	–	350	Ω	$I_{ERRN/DEN}$ = 2 mA Fault condition $V_{EN/DEN} > V_{DEN(th)}$	PRQ-379
ERRN diagnosis enable threshold	$V_{ERRN(DEN)}$	2.1	–	2.3	V	–	PRQ-255
ERRN pull-down current	I_{ERRN_PD}	–	–	2	µA	No fault condition $V_{EN/DEN} > V_{DEN(th)}$	PRQ-380
Diagnosis enable							
DEN diagnosis enable threshold	$V_{DEN(th)}$	2.3	–	2.7	V	–	PRQ-244
Protections							
OL detection threshold	$V_{DR(OL)}$	0.2	–	0.4	V	$V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-285
OUT SC detection threshold	$V_{OUT(SC)}$	0.8	–	1.35	V	$V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-286
PS SC detection threshold	$V_{PS(SC)}$	0.8	–	1.35	V	$V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-292
Fault detection current	$I_{OUT(fault)}$	–	–	650	µA	OL or SC fault condition $V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} < V_{ERRN(fault)}$	PRQ-294
D pin							
Threshold voltage for function de-activation	$V_{D(th)}$	1.4	1.7	2	V	$V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-299
Threshold hysteresis	$V_{D(hys)}$	70	–	–	mV	$V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$ Not subject to production test, specified by design	PRQ-300
Fault pull-up current	$I_{D(fault)}$	20	35	50	µA	OL or SC fault condition $V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} < V_{ERRN(fault)}$ V_D = 2 V	PRQ-301

(table continues...)

Table 12 (continued) Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Pull-down current	$I_{D(PD)}$	40	60	95	µA	No fault conditions $V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$ V_D = 1.4 V	PRQ-302
Internal clamp voltage	$V_{D(CL)}$	2	–	3	V	OL or SC fault condition $V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} < V_{ERRN(fault)}$ D-pin open	PRQ-303
Timings							
Fault to ERRN delay	t_{fault}	40	–	120	µs	$V_{EN/DEN} > V_{DEN(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-304

12 Application information

***Note**: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

12.1 Application diagram

***Note**: This figure is a simplified example of an application circuit. The function must be verified in the application.*

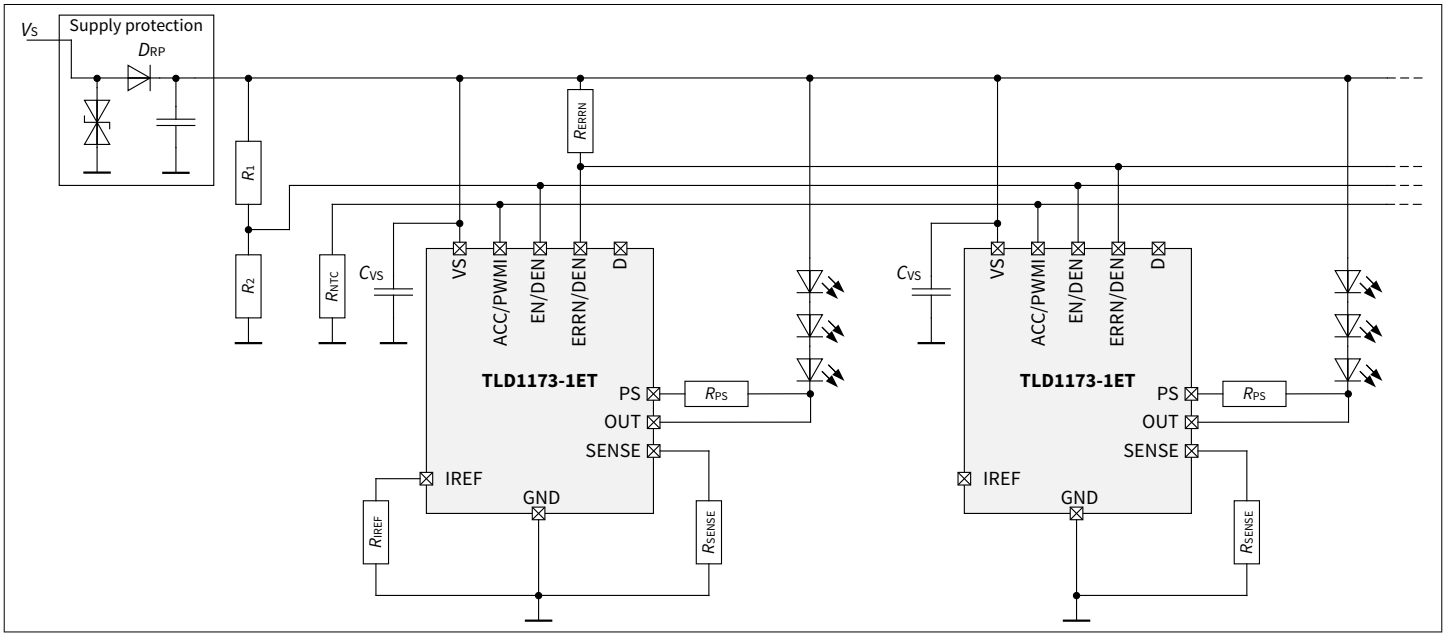
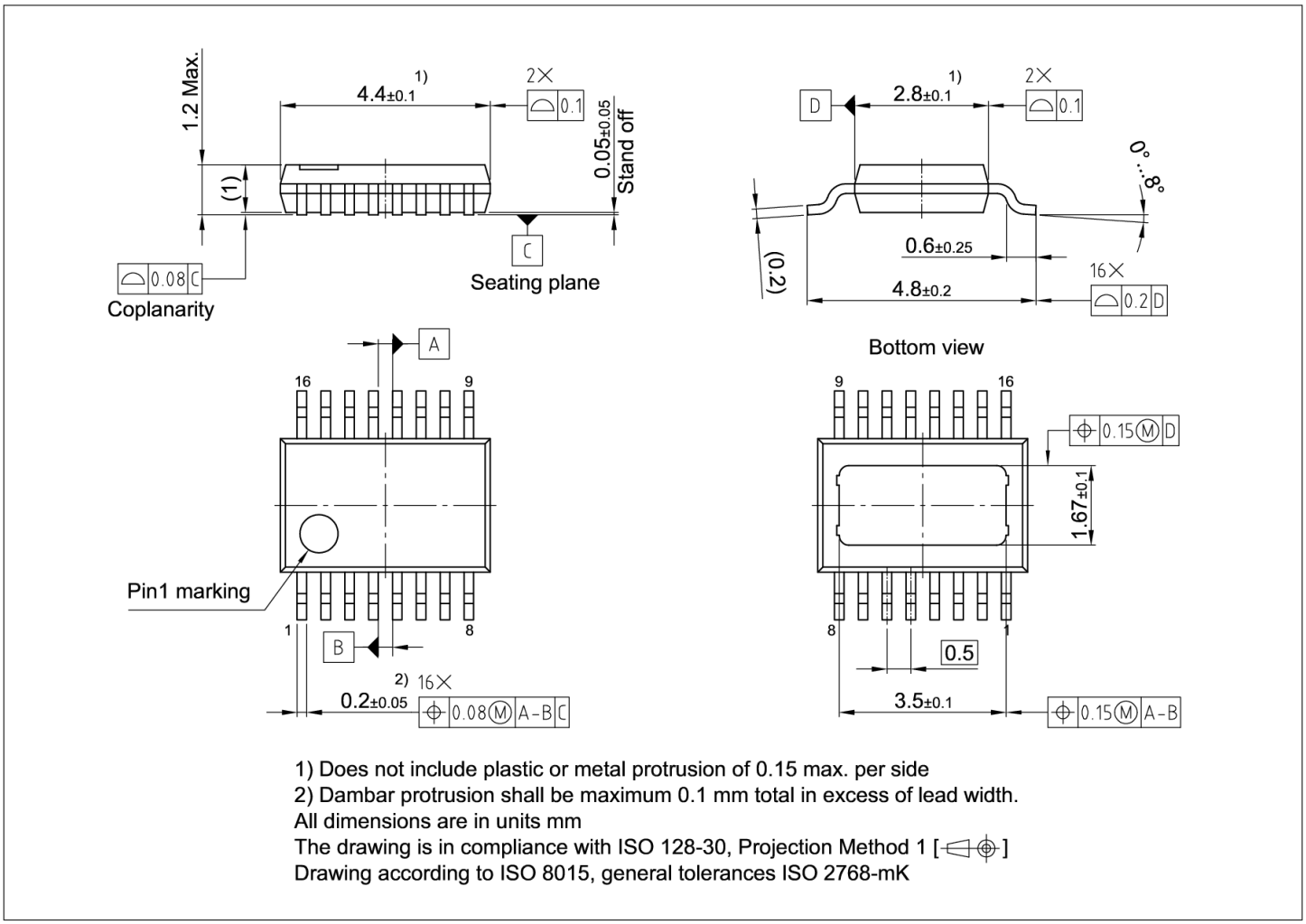


Figure 22 Application diagram example in a shared network with "one fail all off" fault management and central thermal derating

13 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇿]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 23 PG-TFDSO-16 package outline png

Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2024-10-14	• Initial document release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-10-14

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-oqz1652171791319

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.