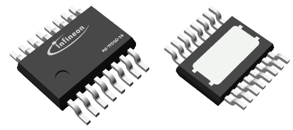
LITIX™ Basic+

Features



- Three-channel device with integrated and protected output stages (current sinks), optimized to drive LEDs
- High output current up to 150 mA per channel
- Possibility to offload power consumption via low cost external resistors to allow maximum current driving capability (Power Shift)
- Independent output current control via enable pins
- Fault management supports 1-fail-all-ON
- Analog output current control input to adjust the output current
- Open load (OL), short to battery (SC) and thermal shutdown protections
- Intelligent fault management: up to 10 devices can share a common error network with only one external resistor
- Thermal derating function via external NTC resistor

RoHS
AEC Qualified

Potential applications

- Cost effective "stop"/"tail" function with shared and separated LEDs per function
- Automotive light functions like turn indicators, position, fog, stop/tail, DRL and side markers
- Animated light functions like sequential indicator and "welcome/goodbye" functions
- Interior lighting functions like ambient lighting, illumination and dash board lighting
- LED indicators for industrial applications and instrumentation

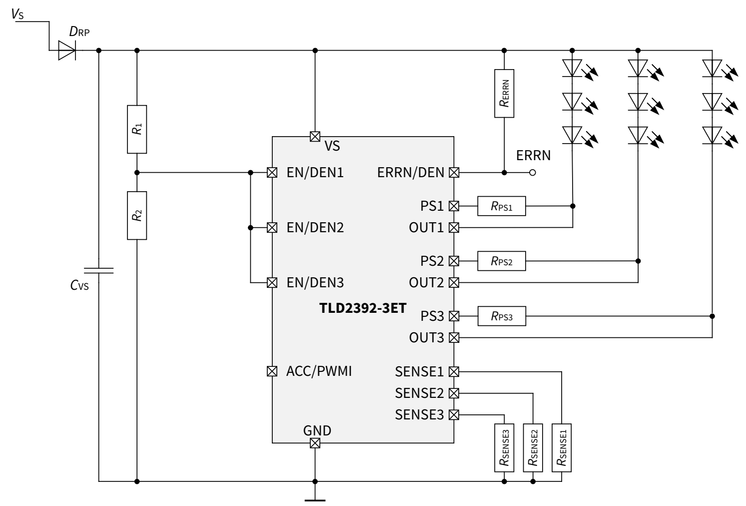
Product validation

Product validation according to AEC-Q100, Grade 1.

Qualified for automotive applications.

Description

The TLD2392-3ET is a three channel low-side driver IC with integrated and protected output stages. It is designed to control LEDs with a current up to 150 mA as linear current sink (LCS). The Power Shift feature allows the device to reach maximum current driving capability by offloading power consumption to external low cost components. The diagnostic features and thermal derating via external NTC resistor provide a reliable solution for high current applications. The fault management, implementing 1 fail-all-ON reaction, allows up to 10 and more devices to share the same error network and to be combined in applications with other LITIX™ LED drivers, such as other LITIX™ Basic+ products and LITIX™ TLD7002-16ES.



Product type	Package	Marking
TLD2392-3ET	TFDSO-16	239

Table of contents

1 Product description

Table 1 Product summary

Parameter	Symbol	Values
Operating voltage	$V_{S(func)}$	5.5 V - 18 V
Extended operating voltage	$V_{S(ext)}$	4.5 V - 36 V
Maximum load current	$I_{SENSE(max)}$	150 mA
Output current accuracy	$V_{SENSE(reg)}$	±4% with V_{SENSE} = 400 mV
Current consumption in sleep mode	$I_{VS(sleep, max)}$	3 µA
Maximum current consumption during fault	$I_{VS(fault, ERRN)}$	850 µA
Maximum dropout voltage	$V_{DR,CS(max)}$	0.6 V

2 Block diagram

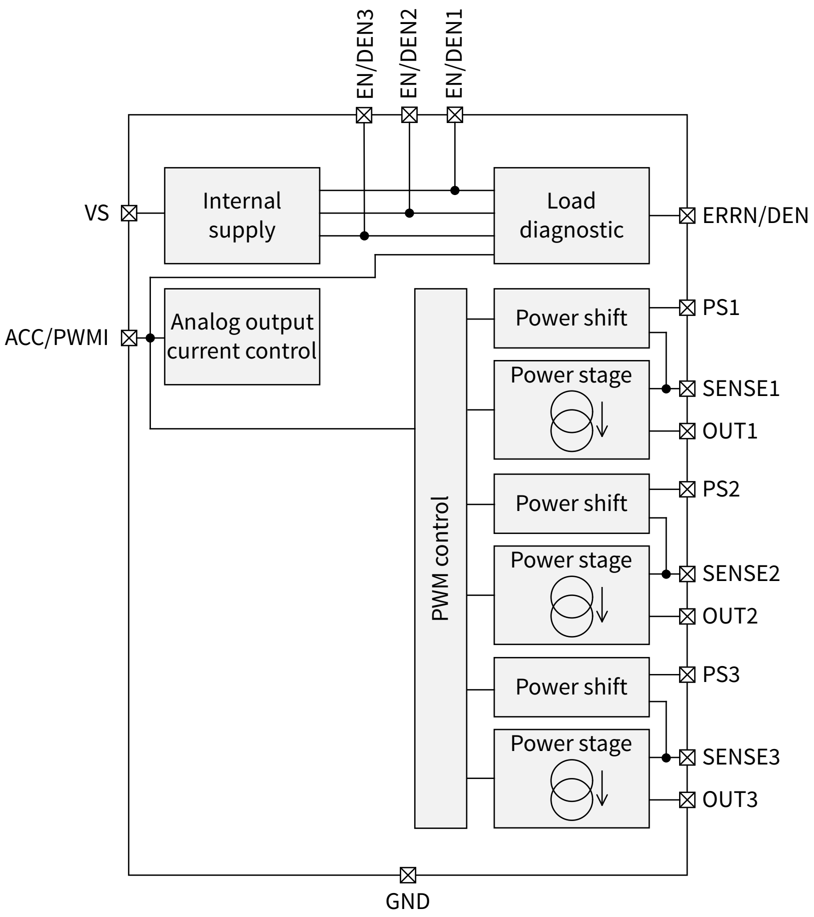


Figure 1 TLD2382-3ET Block diagram

3 Pin configuration

3.1 Pin assignment

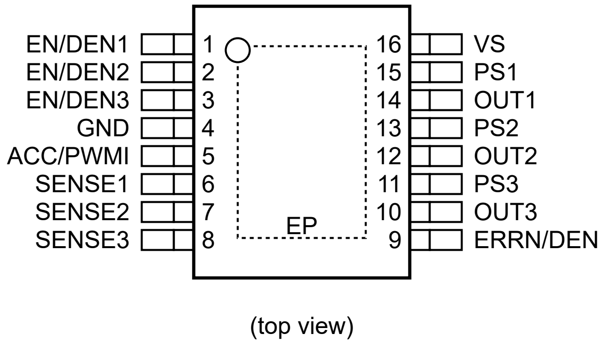


Figure 2 **Pin configuration PG-TFDSO-16**

3.2 Pin definitions and functions

Table 2 **Pin definitions and functions**

Pin	Symbol	Function
16	VS	**Power supply voltage** Battery supply input
4	GND	**Ground** Ground potential. Connect externally close to the chip
1	EN/DEN1	**Output 1 enable and diagnosis control input** Connect to V_S via a resistor divider to enable OUT1 control and diagnosis capability
2	EN/DEN2	**Output 2 enable and diagnosis control input** Connect to V_S via a resistor divider to enable OUT2 control and diagnosis capability
3	EN/DEN3	**Output 3 enable and diagnosis control input** Connect to V_S via a resistor divider to enable OUT3 control and diagnosis capability
9	ERRN/DEN	**ERROR flag I/O and diagnosis control input** Open drain, active low. Connect to V_S via pull-up resistor for ERROR flag capability only otherwise connect to V_S via a resistor divider to enable diagnosis capability
6	SENSE1	**Sense input 1** Connect to low ohmic accurate sense resistor
7	SENSE2	**Sense input 2** Connect to low ohmic accurate sense resistor

(table continues...)

Table 2 (continued) Pin definitions and functions

Pin	Symbol	Function
8	SENSE3	**Sense input 3** Connect to low ohmic accurate sense resistor
14	OUT1	**Channel 1, output pin** Open drain linear current sink. Connect to the target load
15	PS1	**Power shift 1** Connect to external power resistor
12	OUT2	**Channel 2, output pin** Open drain linear current sink. Connect to the target load
13	PS2	**Power shift 2** Connect to external power resistor
10	OUT3	**Channel 3, output pin** Open drain linear current sink. Connect to the target load
11	PS3	**Power shift 3** Connect to external power resistor
5	ACC/PWMI	**Analog current control and PWMI input pin** Connect to external voltage reference to adjust the output current. Connect to external NTC to apply thermal derating. It is possible also to connect to an external open drain PWM controller
Exposed pad	EP	**Exposed pad** Used only for thermal dissipation purpose. Connect externally to GND close to the chip

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

[1] $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	PRQ-32
EN/DENx voltage	$V_{EN/DENx}$	-0.3	–	40	V	–	PRQ-57
Output voltages	V_{OUTx}	-0.3	–	40	V	–	PRQ-58
Power shift voltages	V_{PSx}	-0.3	–	40	V	–	PRQ-60
Sense voltage	V_{SENSEx}	-0.3	–	0.9	V	–	PRQ-62
ERRN/DEN voltage	$V_{ERRN/DEN}$	-0.3	–	40	V	–	PRQ-61
ACC/PWMI voltage	$V_{ACC/PWMI}$	-0.3	–	5.5	V	–	PRQ-64
Temperatures							
Junction temperature	T_{J_ABS}	-40	–	150	°C	–	PRQ-39
Storage temperature	T_{STG}	-55	–	150	–	–	PRQ-40
ESD robustness							
ESD robustness all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	ESD robustness, Human Body Model “HBM” according to AEC Q100-002	PRQ-53
ESD robustness all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	ESD robustness, Charged Device Model “CDM” according to AEC Q100-011 Rev.D	PRQ-41
ESD robustness corner pins (CDM)	$V_{ESD(CDM)\ CR}$	-750	–	750	V	ESD robustness, Charged Device Model “CDM” according to AEC Q100-011 Rev.D	PRQ-54

1) Not subject to production test, specified by design

Note: *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional range

Table 4 Functional range

$T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage for operating range	$V_{S(func)}$	5.5	–	18	V	–	PRQ-33
Extended supply voltage for operating range	$V_{S(ext)}$	4.5	–	36	V	–	PRQ-71
Currents							
Channel output current	$I_{SENSEx(func)}$	5	–	150	mA	–	PRQ-223
Power dissipation							
Max. static and dynamic power dissipation	P_{max}	–	–	1.5	W	T_A = 85°C and R_{thJA} = 40 K/W	PRQ-178
Temperatures							
Junction temperature	$T_{J(func)}$	-40	–	150	°C	–	PRQ-72

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. Within the Extended Operation range, parameters deviations are possible. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

4.3 Thermal resistance

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org*

Table 5 Thermal resistance

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to top	Ψ_{JTOP}	–	7	–	K/W	1)	PRQ-262
Junction to case	R_{thJC}	–	6	–	K/W	2)	PRQ-263
Junction to ambient 1s0p board	R_{thJA1}	–	61	–	K/W	3) T_A = 85°C	PRQ-264
Junction to ambient 2s2p board	R_{thJA2}	–	40	–	K/W	4) T_A = 85°C	PRQ-265

1) Specified Ψ_{JTOP} is derived under natural convention conditions and provide a correlation between the junction temperature and the temperature on the package top surface. T_A = 85°C. Total power dissipation = 1.5 W

2) Specified R_{thJC} is simulated at natural convention on a cold plate setup (all pins and exposed pad are fixed at ambient temperature). T_A = 85°C. Total power dissipation = 1.5 W

3) Specified R_{thJA1} is generated in accordance with JEDEC JESD51-3 standards at natural convection on FR4 1s0p board. The simulation has been performed on a 76.2 x 114.3 x 1.5 mm board with 70 µm, 300 mm^2 cooling area. Total power dissipation 1.5W distributed statically and homogenously over all power stages

4) Specified R_{thJA2} is generated in accordance with JEDEC JESD51-5,-7 standards at natural convection on FR4 2s2p board. The simulation has been performed on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). A total of six thermal via (∅ = 0.3 mm, plating 25 µm) is placed under the exposed pad contacting the first inner copper layer. Total power dissipation 1.5W distributed statically and homogenously over all power stages

5 Internal supply

This chapter describes the internal supply, its main parameters and functionality.

5.1 Description

As soon as the voltage applied at the supply pin VS is above $V_{SUV(th)}$ and the voltage applied at the EN/DENx pins is above $V_{ENx(th)}$, the device is ready to deliver output current from the output stages after the power on reset time t_{POR}. When the supply voltage V_S is below the threshold $V_{SUV(th)}$, the internal Power-ON-Reset (POR) function holds the device in reset state.

The power on reset time t_{POR} has to be taken into account under relevant application conditions, i.e. with PWM control from VS.

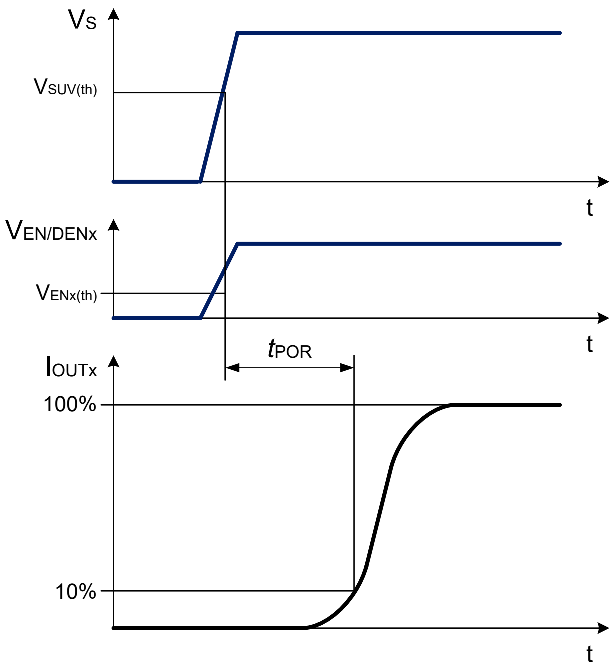


Figure 3 **Power on reset timing diagram**

If the voltage applied at all the EN/DENx pins is below $V_{ENx(th)}$ for more than t_{SLEEP} the device enters sleep mode. In this state all internal functions are switched off and the current consumption is reduced to $I_{VS(sleep)}$.

5.2 Electrical characteristics

Table 6 **Electrical characteristics**

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{VS(sleep)}$	–	–	3	µA	$V_{EN/DENx}$ = 0 V T_J = 150°C	PRQ-84
Current consumption, active mode (no fault)	$I_{VS(active)}$	–	2.5	3.5	mA	$V_{EN/DENx}$ = 5.5 V $V_{ACC/PWMI}$ = 2.4 V	PRQ-306

(table continues...)

Table 6 (continued) Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VS undervoltage threshold	$V_{SUV(th)}$	3.5	–	4.5	V	–	PRQ-89
EN/DENx outputs enable threshold	$V_{ENx(th)}$	0.6	–	1.8	V	–	PRQ-92
EN/DENx outputs enable hysteresis	$V_{ENx(hys)}$	80	120	–	mV	1)	PRQ-93
EN/DENx pull-down current	$I_{EN/DENx(PD)}$	–	–	5	µA	$V_{EN/DENx}$ = 3 V	PRQ-96
EN/DENx pull-down current	$I_{EN/DENx(PD)}$	–	–	150	µA	$V_{EN/DENx}$ = 18 V	PRQ-370
Power on reset delay time	t_{POR}	–	–	75	µs	V_S rising edge from 0 V to 8 V to 10% of output current $V_{EN/DENx}$ = 5.5 V $V_{ACC/PWMI}$ ≥ 2.4 V	PRQ-99
Sleep mode filter time	t_{SLEEP}	15	–	45	ms	–	PRQ-109

1) Not subject to production test, specified by design

6 Power stage

The power stages sinks from the OUTx pins an output current I_{OUTx} which is a function of the external sense resistors placed at SENSEx pins.

The overall maximum output current is limited by the power dissipation and used cooling areas.

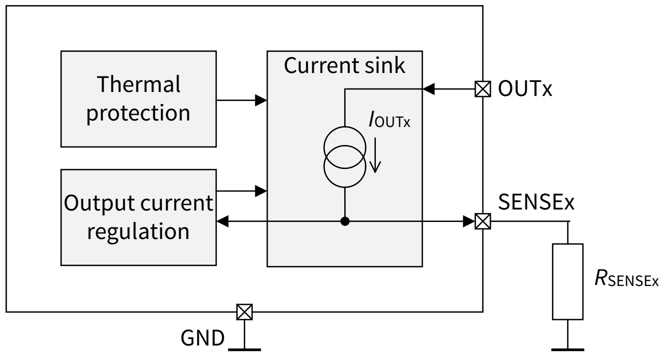


Figure 4 Power stages block diagram

6.1 Output current regulation

The output current regulation block controls the LEDs current by regulating the voltage drop $V_{SENSEx(reg)}$ on the external low-side current-sense resistors R_{SENSEx} placed between SENSEx pin and GND.

When the LEDs current is in regulation, the LEDs current value for each channel can be calculated by using the following equation:

$$I_{SENSEx} = \frac{V_{SENSEx(reg)}}{R_{SENSEx}} \tag{1}$$

For an operating output current control loop, the power stages dropout voltage ($V_{DR,CSx}$), the $V_{SENSEx(reg)}$ voltage, the forward voltage V_{D_RP} of the reverse polarity protection diode (when used) and the minimum supply voltage have to be considered in the LED string design.

To grant a proper control of the output current the following equation has to be satisfied:

$$V_S \geq V_{SENSEx(reg)} + V_{DR,\,CSx} + V_{LED\_STRINGx} + V_{D\_RP} \tag{2}$$

In case the supply voltage drops below the minimum requested by a particular channel, the LEDs current of that channel is no longer properly regulated. Consequently, a lower current is delivered and the voltage across the R_{SENSEx} resistor is lower than the expected $V_{SENSEx(reg)}$.

***Note**: The R_{SENSE} has to be placed as close as possible to the pin VSENSE to avoid current regulation instability.*

6.2 Thermal protection

A thermal protection function is integrated into the device to prevent IC damage under fault conditions described in the datasheet. Fault conditions are considered as "outside" the normal operating range. Protective functions are not designed for continuous operations.

The thermal protection function is achieved by temperature monitoring of the power stages. As soon as the junction temperature exceeds the overtemperature threshold T_{JSD}:

- The output currents are disabled by turning off the power stages
- The ERRN/DEN pin is pulled low
- The current consumption is below $I_{VS(fault,\ ERRN)}$

Once the junction temperature falls below T_{JSD} - $T_{J(hys)}$:

- The power stages recover to normal operation
- The ERRN/DEN pin is released

6.3 Electrical characteristics

Table 7 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Leakage currents							
Output leakage current	$I_{OUTx(leak)}$	–	–	1	µA	[1] $T_J = 85°C$ $V_{OUTx} \leq 16$ V $V_{ACC/PWMI} = 0$ V $V_{EN/DENx} = 5.5$ V	PRQ-115
Output leakage currents	$I_{OUTx(leak)}$	–	–	3	µA	$T_J = 150°C$ $V_{OUTx} \leq 16$ V $V_{ACC/PWMI} = 0$ V $V_{EN/DENx} = 5.5$ V	PRQ-117
Sense regulation voltage accuracy							
SENSEx voltage regulation accuracy	$V_{SENSEx(reg)}$	384	400	416	mV	$V_{ACC/PWMI} \geq 2.4$ V	PRQ-135
SENSEx voltage regulation accuracy	$V_{SENSEx(reg)}$	95	100	105	mV	$V_{ACC/PWMI} = 0.9$ V	PRQ-137
SENSEx voltage regulation accuracy	$V_{SENSEx(reg)}$	14	20	26	mV	$V_{ACC/PWMI} = 0.5$ V	PRQ-139
Power stage drop out							
Power stages drop out voltage	$V_{DR,CSx}$	–	–	0.6	V	$I_{OUTx} = 150$ mA	PRQ-126
Thermal protection thresholds							
Overtemperature shutdown threshold	T_{JSD}	165	175	185	°C	[2]	PRQ-131
Overtemperature hysteresis	$T_{J(hys)}$	5	10	15	°C	[2]	PRQ-132

1) Not subject to production test, specified by design
2) Not subject to production test, specified by design

7 Power shift

The device manages high power dissipation (higher than allowed by the thermal impedance R_{thJA} of the application) by separating the LED current into two current branches:

- One current sink path through an external drop element (power resistor) and the internal power shift
- One current sink path through the internal power stage

The current flowing into the power shift path and the one flowing into the power stage path are dynamically adjusted in order to obtain that the sum of I_{OUTx} and I_{PSx} currents is equal to the regulated I_{SENSEx} current.

The distribution of the current between the power shift path and the power stage path is defined by the power shift resistor value, the load and the applied battery voltage V_S.

In order to proper dimension the resistor value the following parameters have to be considered:

- Maximum current I_{PSx} intended to flow into the power shift path at maximum battery operative voltage $V_{S(PEAK)}$
- Forward voltage $V_{LED\_STRINGx}$ of the output LED load and forward voltage V_{D_RP} of the reverse polarity protection diode
- Voltage drop on the internal power shift element ($V_{PS\_INTx} = I_{PSx} \times R_{PS\_INT(ON)}$)
- Regulated V_{SENSEx} voltage

The resistor can then be calculated using the following formula:

$$R_{PSx} = \frac{V_{S(PEAK)} - V_{D\_RP} - V_{LED\_STRINGx} - V_{PS\_INTx} - V_{SENSEx}}{I_{PSx}} \quad (3)$$

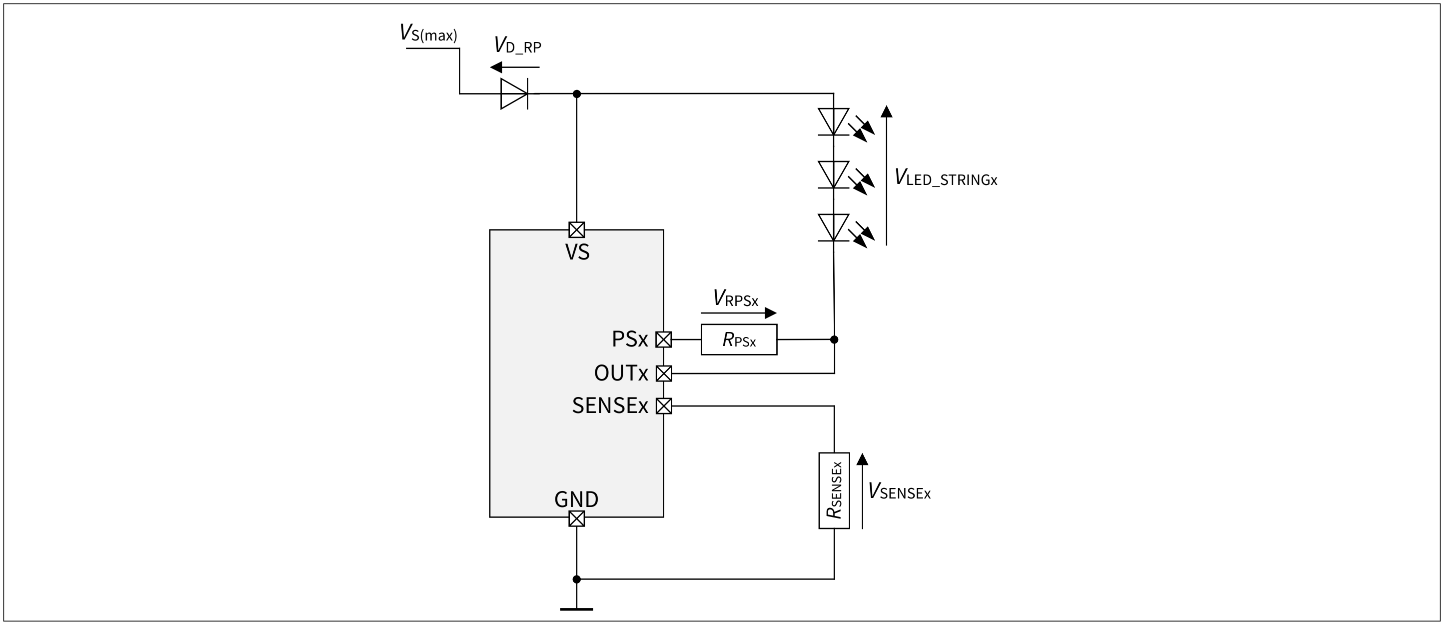


Figure 5 Power shift resistor diagram

***Note**: Please consider that if the R_{PS} is set to 0 Ω all the LED current flows inside the internal power shift path leading to a possible overheating of the device up to the thermal shut-down.*

7.1 Electrical characteristics

Table 8 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power shift ON resistance	$R_{PS\_INT(ON)}$	–	–	7.5	Ω	I_{PSx} = 150 mA	PRQ-276
Power shift leakage current	$I_{PSx(leak)}$	–	–	1	µA	[1] T_J = 85°C $V_{PSx} \leq$ 16 V $V_{ACC/PWMI}$ = 0 V $V_{EN/DENx}$ = 5.5 V	PRQ-278
Power shift leakage current	$I_{PSx(leak)}$	–	–	3	µA	T_J = 150°C $V_{PSx} \leq$ 16 V $V_{ACC/PWMI}$ = 0 V $V_{EN/DENx}$ = 5.5 V	PRQ-288
Power shift ratio	I_{PSx}/I_{SENSEx}	0.95	–	–	–	V_{PSx} - V_{SENSEx} > 1.5 V $V_{ACC/PWMI} \geq$ 0.9 V	PRQ-281
SENSEx voltage regulation accuracy	$V_{SENSEx(reg)}$	384	400	416	mV	$V_{ACC/PWMI} \geq$ 2.4 V	PRQ-409
SENSEx voltage regulation accuracy	$V_{SENSEx(reg)}$	95	100	105	mV	$V_{ACC/PWMI}$ = 0.9 V I_{SENSE} > 20 mA	PRQ-411
SENSEx voltage regulation accuracy	$V_{SENSEx(reg)}$	14	20	28	mV	$V_{ACC/PWMI}$ = 0.5 V I_{SENSE} > 20 mA	PRQ-415

1) Not subject to production test, specified by design

8 PWM control

PWM dimming is adopted to vary LEDs brightness with greatly reduced chromaticity shift. PWM dimming achieves brightness reduction by varying the duty cycle of a constant current in the LED string.

The PWM modulation is performed via the ACC/PWMI pin. The power stages and the power shift blocks are disabled if the voltage applied on the ACC/PWMI pin is lower than $V_{PWM(OFF)}$ while they are enabled if the voltage applied on the ACC/PWMI pin is higher than $V_{PWM(ON)}$.

In Figure 6 two examples of PWM dimming are shown via the ACC/PWMI input pin:

1. In case a resistor is needed on the ACC/PWMI input pin to apply analog current control (i.e. binning or thermal derating) the PWM signal can be applied using an open drain output from the PWM generator
2. In case the analog current control function is not needed a push-pull output from the PWM generator can be used to apply the PWM modulation

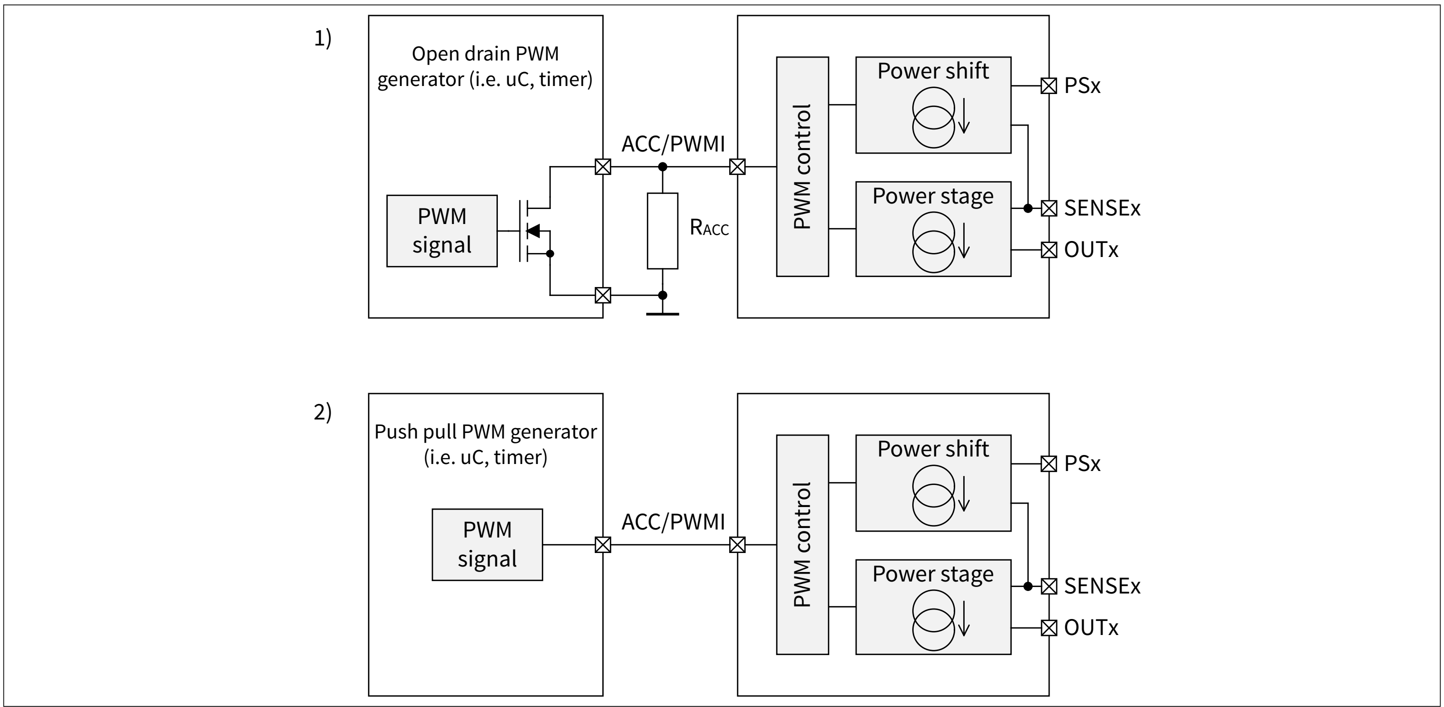


Figure 6 PWM control via ACC/PWMI input pin

The PWM signal can be applied via the EN/DENx pins as well to allow PWM modulation on each channel independently. After the exit from sleep state the t_{POR} delay time has to be considered on the first PWM pulse generation.

When applied on the EN/DENx the PWM signal has a frequency range f_{PWM} to avoid to turn-off any channels by triggering the t_{SLEEP} filter time.

The power stage and the power shift of each channel are enabled if the voltage applied on the EN/DENx pin is higher than $V_{ENx(th)}$ while they are disabled if the voltage applied on the EN/DENx pin is lower than $V_{ENx(th)}$.

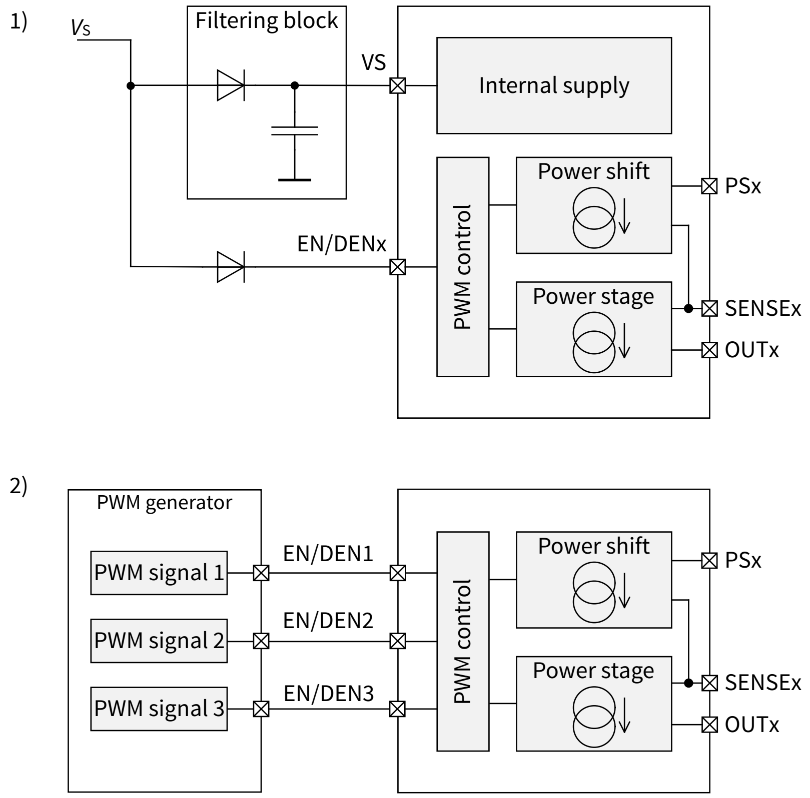


Figure 7 **PWM control via EN/DENx input pins**

When the voltage applied on the EN/DENx pin is below $V_{DENx(th)}$, the load diagnostic of the related channel is disabled unless a fault was previously detected.

While if the voltage applied on the ACC/PWMI pin is below $V_{PWM(OFF)}$, the load diagnostic of all the channels is disabled unless a fault was previously detected.

In particular, if a fault is already present when the voltage applied on the ACC/PWMI pin is below $V_{PWM(OFF)}$ or the voltage applied on EN/DENx pin is below $V_{DENx(th)}$ the diagnostic is kept active until the fault condition disappears, after that it is then disabled.

The PWM control block implements a slope rate control of the V_{SENSEx} voltages in order to improve EMC performances. The slew rate timings are defined by dV/dt_{ON} and dV/dt_{OFF} parameters.

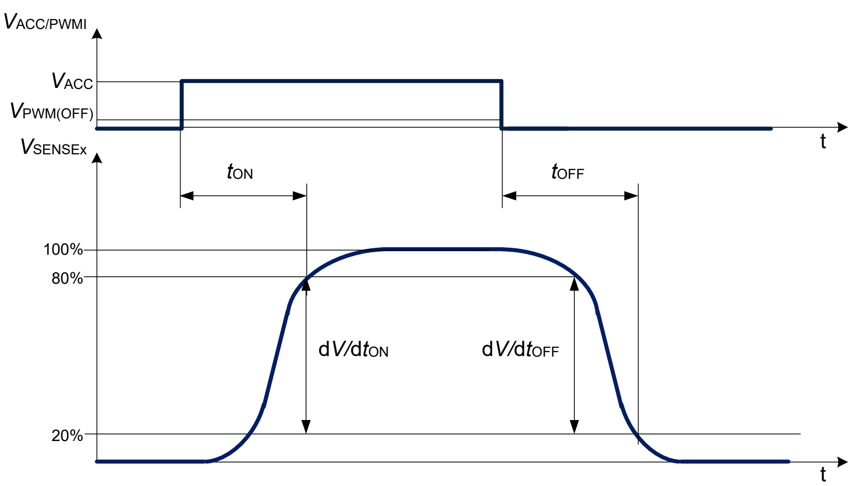


Figure 8 **PWMI control timing diagram for $V_{ACC/PWMI} \geq 2.4$ V**

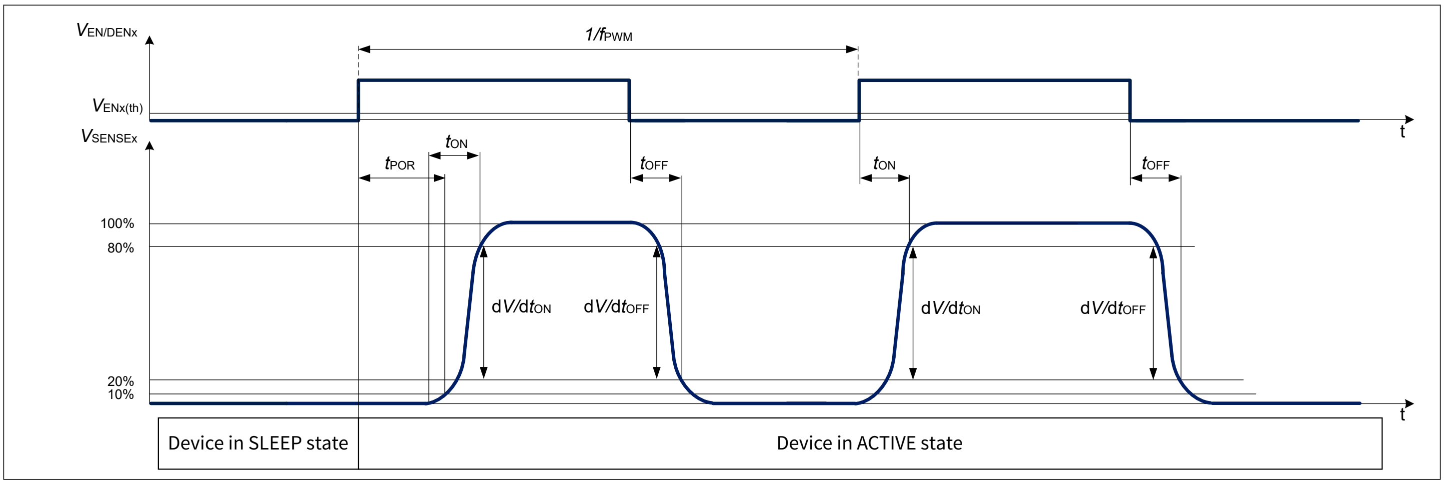


Figure 9 PWM control on EN/DENx timing diagrams for $V_{ACC/PWMI} \geq 2.4$ V

8.1 Electrical characteristics

Table 9 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWM turn off threshold	$V_{PWM(OFF)}$	0.35	0.4	–	V	–	PRQ-145
PWM turn on threshold	$V_{PWM(ON)}$	–	–	0.45	V	–	PRQ-261
PWM frequency range	f_{PWM}	100	–	–	Hz	1)	PRQ-146
PWM turn on time	t_{ON}	–	–	20	µs	1) V_{SENSEx} rising to 80% of regulation $V_{ACC/PWMI} \geq 2.4$ V	PRQ-356
PWM turn off time	t_{OFF}	–	–	20	µs	1) V_{SENSEx} falling to 20% of regulation $V_{ACC/PWMI}$ falling from ≥ 2.4 V to less than $V_{PWM(OFF)}$	PRQ-357
VSENSE rising slew rate	dV/dt_{ON}	15	35	50	mV/µs	1) V_{SENSEx} rising from 20% to 80% of regulation $V_{ACC/PWMI} \geq 2.4$ V	PRQ-358
VSENSE falling slew rate	dV/dt_{OFF}	-50	-35	-15	mV/µs	1) V_{SENSEx} falling from 80% to 20% of regulation $V_{ACC/PWMI}$ falling from ≥ 2.4 V to less than $V_{PWM(OFF)}$	PRQ-359

1) Not subject to production test, specified by design

9 Analog output current control

The analog output current control function adjusts the V_{SENSEx} voltages by sensing the applied voltage on the ACC/PWMI pin $V_{ACC/PWMI}$.

As described in Chapter 6 the output current provided by each channel is a direct function of the regulated voltage V_{SENSEx}. In this way by adjusting the voltage applied on the ACC/PWMI pin it is possible to control the output current of all the channels.

$$I_{SENSEx} = \frac{0.2 \times V_{ACC/PWMI} - 0.08 \quad V}{R_{SENSEx}} \tag{4}$$

The relation between the ACC/PWMI voltage $V_{ACC/PWMI}$ and the respective regulated voltages V_{SENSEx} is shown in the Figure 10.

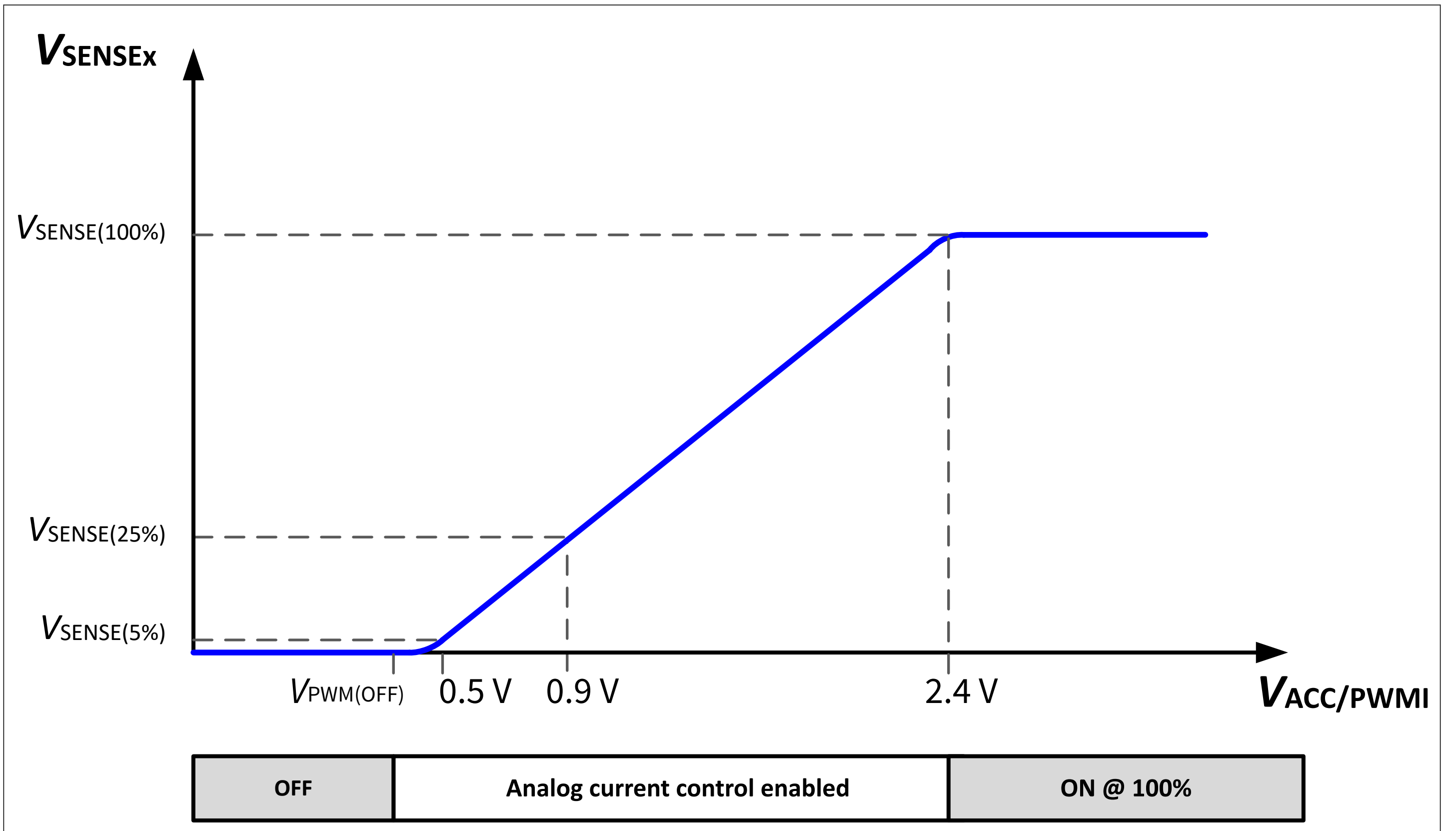


Figure 10 Analog output current control

***Note**: In case the analog output current control function is not needed it is recommended to leave the ACC/PWMI pin open. Indeed the internal pull-up current I_{ACC} can be used to bias the ACC/PWMI voltage to avoid wrong V_{SENSE} setting.*

9.1 Electrical characteristics

Table 10 Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ACC pull-up current	I_{ACC}	8	12.5	17	µA	current flowing outside the pin	PRQ-220

10 Load diagnostics

Several diagnosis features are integrated:

- Open load detection (OL)
- Short to supply detection (SC)
- Power shift short to supply detection (SC)
- Overtemperature thermal detection (OT)

The behavior of the device during overload conditions that lead to an excess of internal heating, up to overtemperature condition, is already described in chapter Thermal protection.

An open load condition is detected if the voltage across the power stage $V_{DRx} = V_{OUTx} - V_{SENSEx}$ is below the threshold $V_{DR(OL)}$ for at least a filter time t_{fault}.

A short to supply condition is detected if the output voltage drop over one of the loads $V_S - V_{OUTx}$ is below the threshold $V_{OUT(SC)}$ for at least a filter time t_{fault}.

A power shift short to supply condition is detected if the power shift voltage drop $V_S - V_{PSx}$ is below the threshold $V_{PS(SC)}$ for at least a filter time t_{fault}.

If an OL condition is detected on the OUT pin or a SC condition is detected on one of the OUT or PS pins, a pull-down current $I_{OUT(fault)}$ flows inside the OUT pin replacing the configured output current.

***Note**: The $I_{OUT(fault)}$ current is limited by the actual load impedance, e.g. it is reduced to zero with an ideal open load.*

10.1 Diagnostics enable

As soon as the voltage applied at the supply pin VS is above $V_{SUV(th)}$ and the voltage applied to the EN/DENx pins is above $V_{DENx(th)}$, the device is ready to detect and report fault conditions via ERRN/DEN pin.

There are several possibilities to program the output enable and diagnosis enable via EN/DENx pins, like a resistor divider from VS to GND, a Zener diode from EN/DENx to VS and also a logic control pin (e.g. from a microcontroller output).

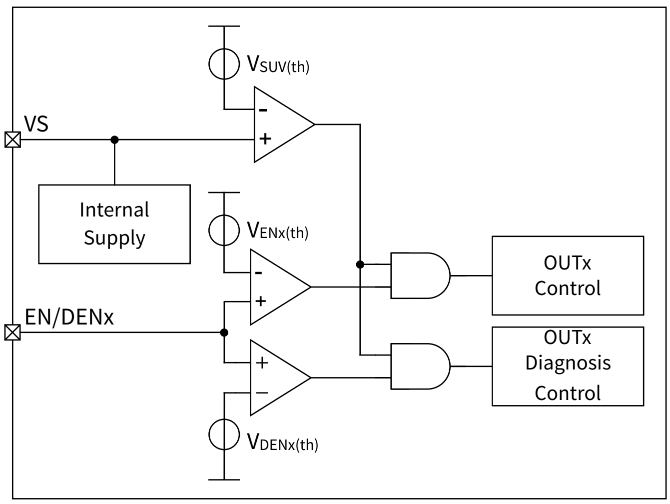


Figure 11 EN/DEN block diagram

10.2 ERRN/DEN pin

The device is able to report a detected failure in one of its driven loads via the ERRN/DEN network.

The open-drain ERRN/DEN pin applies a pull-down resistance $R_{ERRN(ON)}$ towards GND when a fault condition is detected for at least a filter time t_{fault}. Therefore, an active low state can be detected at ERRN/DEN pin when $V_{ERRN} < V_{ERRN(fault)}$ and the relative faulty output channel is switched off.

Similarly, when the fault is removed, ERRN/DEN pin is back in high impedance state and the channel reactivation is completed as illustrated in Figure 12.

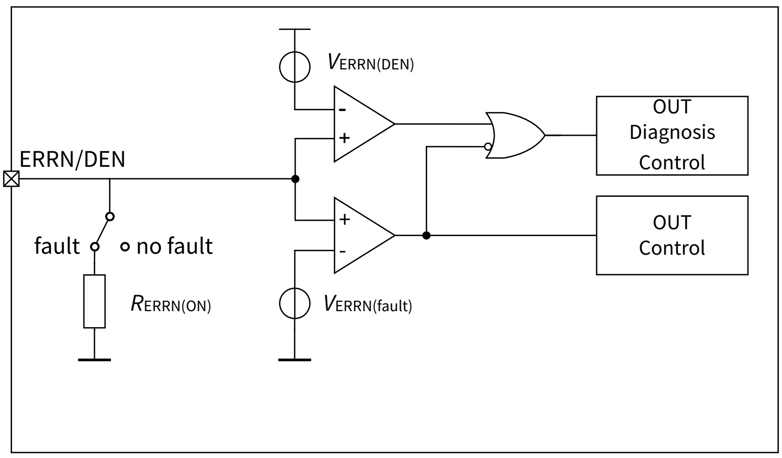


Figure 12 ERRN/DEN pin block diagram

To enable direct connection from a microcontroller to the EN/DENx pins to apply independent PWM signal modulation, the DEN functionality is duplicated on the ERRN/DEN pin. This functionality enables the possibility to decouple the $V_{DENx(th)}$ threshold from the $V_{ENx(th)}$ threshold to have the device turning on as soon as needed independently from the $V_{DENx(th)}$ threshold.

The diagnostic reporting on ERRN/DEN pin and "open load", "short to supply" and the "power shift short to supply" protections are disabled, unless a fault was previously detected, as soon as one of the following condition is verified:

- The voltage on the ERRN/DEN pin is $V_{ERRN(fault)} < V_{ERRN/DEN} \leq V_{ERRN(DEN)}$ the diagnostic is disabled for all the channels
- The voltage on EN/DENx pin is below $V_{DENx(th)}$ the diagnostic is disabled for the relative channel

In addition the "open load" protection is disabled as well in case the voltage on the ERRN/DEN pin is $V_{ERRN/DEN} \leq V_{ERRN(fault)}$ on all the channels that are not already in a fault condition.

When the ERRN/DEN pin applies a pull-down resistor $R_{ERRN(ON)}$ towards GND the $V_{ERRN(DEN)}$ threshold is masked to avoid unwanted toggling of the voltages on the ERRN/DEN pin.

10.3 Fault management

If there is a fault condition on the output or the power shift, the ERRN/DEN pin applies a pull-down resistance $R_{ERRN(ON)}$ towards GND and (with proper dimensioning of the external pull-up resistor) reaches a voltage level below $V_{ERRN(fault)}$. Only the channel under fault condition will be deactivated, still sharing ERRN/DEN pin in a common error network with other devices of Basic+ family, without the need of an auxiliary microcontroller.

The ERRN/DEN low voltage can also be used as input signal for a microcontroller to perform the desired diagnosis policy.

The fault status is not latched: as soon as the fault condition is no longer present (for at least for a filter time t_{fault}), ERRN goes back to high impedance and the output stage which was at fault is activated again.

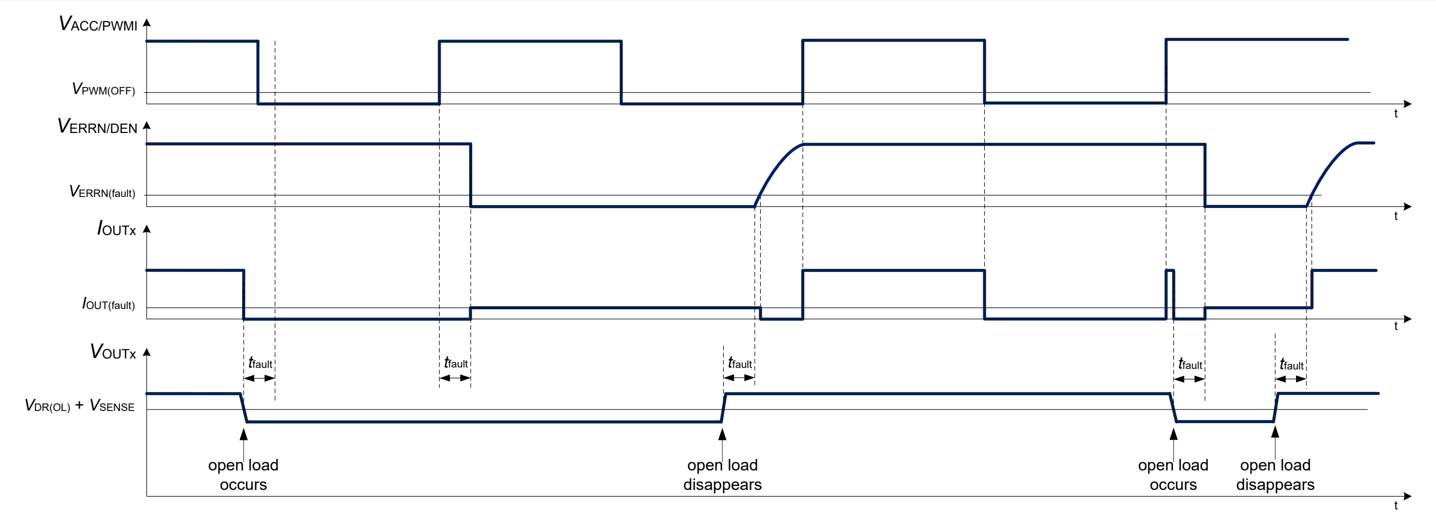


Figure 13 **Open load condition timing diagram example in 1-fail-all-ON configuration**

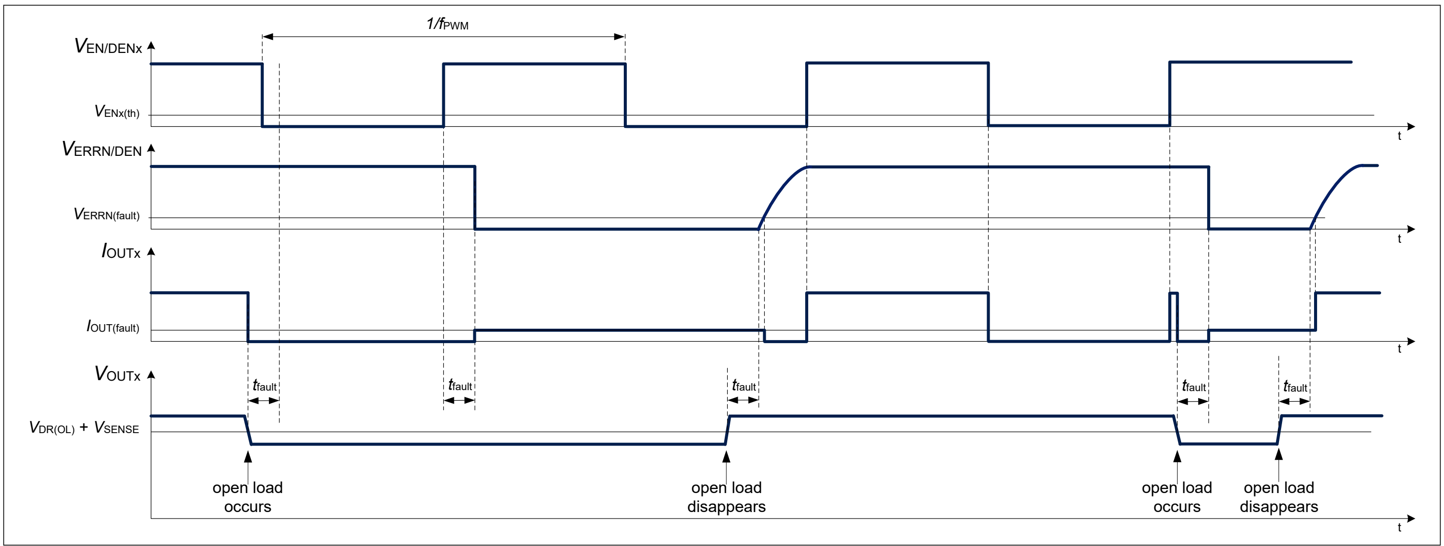


Figure 14 **Open load condition timing diagram example in 1-fail-all-ON configuration with digital dimming applied on EN/DENx pins**

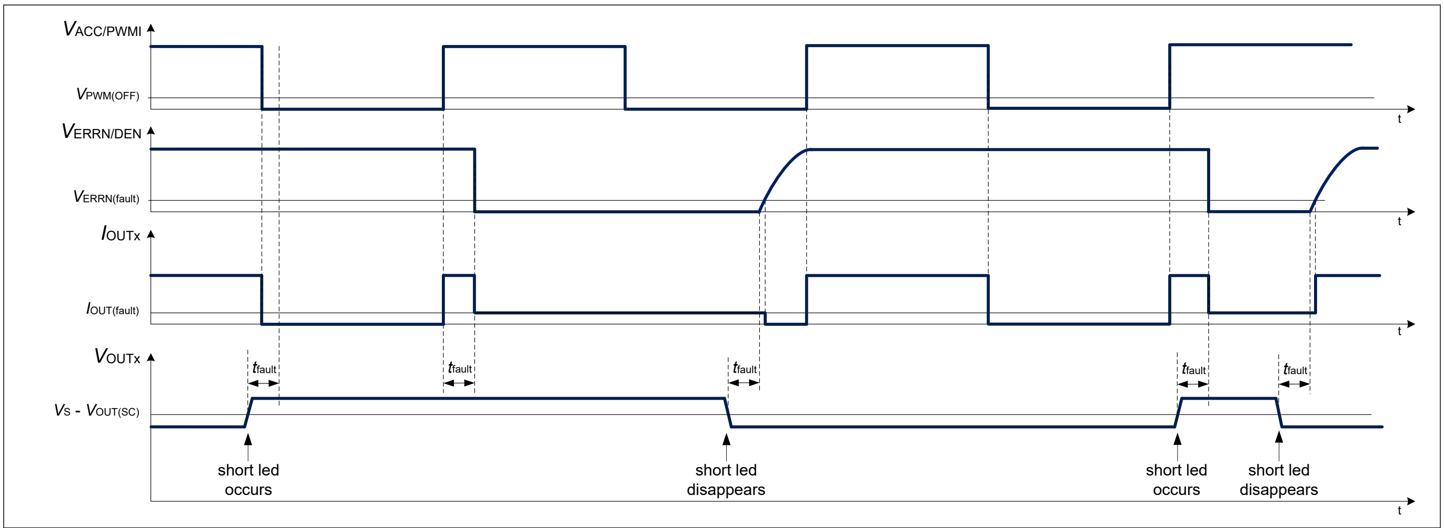


Figure 15 **Output short to supply condition timing diagram example in 1-fail-all-ON configuration**

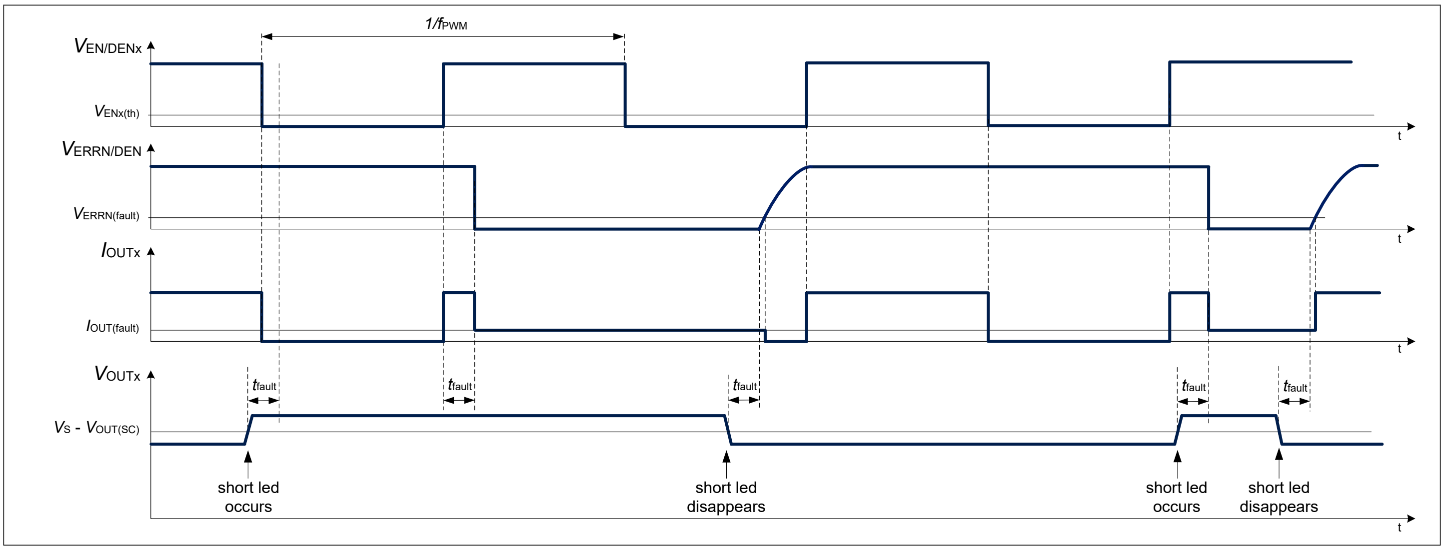


Figure 16 **Output short to supply condition timing diagram example in 1-fail-all-ON configuration with digital dimming applied on EN/DENx pins**

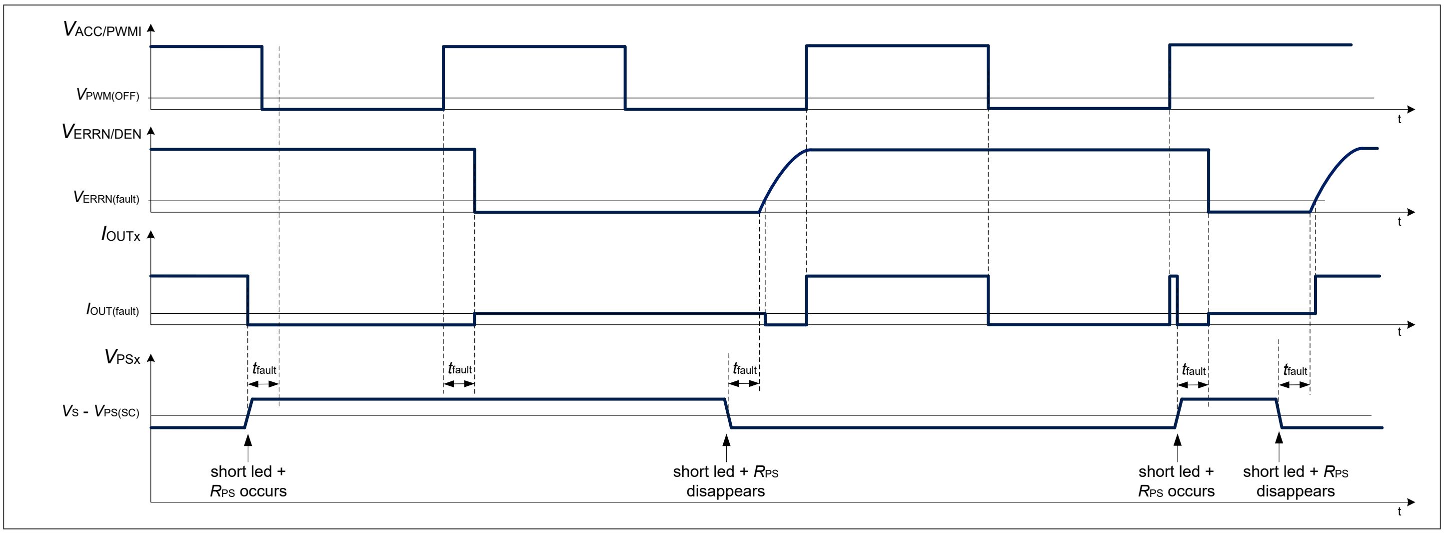


Figure 17 **Power shift short to supply condition timing diagram example in 1-fail-all-ON configuration**

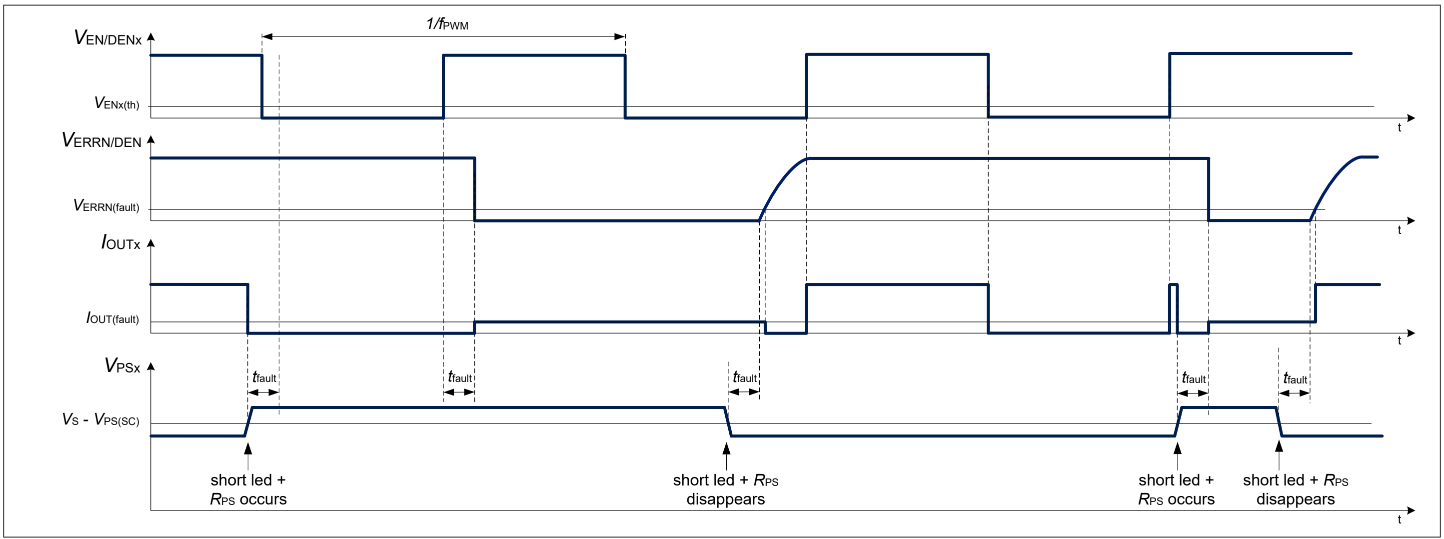


Figure 18 **Power shift short to supply condition timing diagram example in 1-fail-all-ON configuration with digital dimming applied on EN/DENx pins**

10.4 Electrical characteristics

Table 11 **Electrical characteristics**

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ERRN/DEN pin							
ERRN fault threshold	$V_{ERRN(fault)}$	0.7	–	0.9	V	–	PRQ-193
ERRN ON resistance	$R_{ERRN(ON)}$	–	–	350	Ω	$I_{ERRN/DEN}$ = 2 mA Fault condition $V_{EN/DENx} > V_{DENx(th)}$	PRQ-378
ERRN diagnosis enable threshold	$V_{ERRN(DEN)}$	2.1	–	2.3	V	–	PRQ-255
ERRN pull-down current	I_{ERRN_PD}	–	–	2	µA	No fault condition $V_{EN/DEN} > V_{DEN(th)}$	PRQ-380
Diagnosis enable							
DEN diagnosis enable threshold	$V_{DENx(th)}$	2.3	–	2.7	V	–	PRQ-246
Protections							
OL detection threshold	$V_{DR(OL)}$	0.2	–	0.4	V	$V_{EN/DENx} > V_{DENx(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-194
OUT SC detection threshold	$V_{OUT(SC)}$	0.8	–	1.35	V	$V_{EN/DENx} > V_{DENx(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-195

(table continues...)

Table 11 (continued) Electrical characteristics

$V_S = V_{S(func)}$, $T_J = T_{J(func)}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PS SC detection threshold	$V_{PS(SC)}$	0.8	–	1.35	V	$V_{EN/DENx} > V_{DENx(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-293
Fault detection current	$I_{OUT(fault)}$	–	–	650	µA	OL or SC fault condition $V_{EN/DENx} > V_{DENx(th)}$ $V_{ERRN/DEN} < V_{ERRN(fault)}$	PRQ-196
Timings							
Fault to ERRN delay	t_{fault}	40	–	120	µs	$V_{EN/DENx} > V_{DENx(th)}$ $V_{ERRN/DEN} > V_{ERRN(DEN)}$	PRQ-212

11 Application information

***Note**: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

11.1 Application diagram

***Note**: This figure is a simplified example of an application circuit. The function must be verified in the application.*

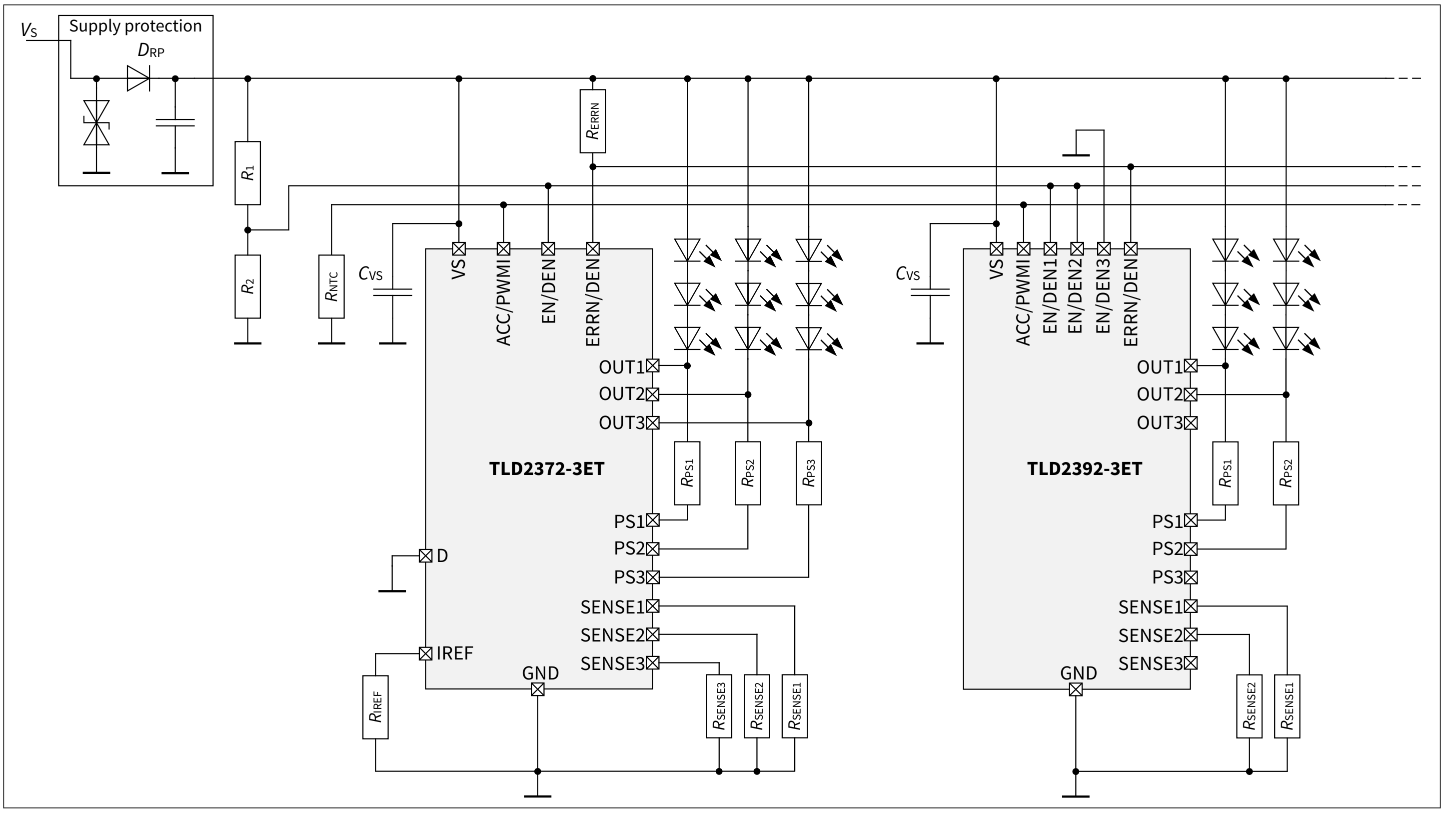


Figure 19 **Application diagram example for a 5 channels light function in a shared network with "one fail all on" fault management and central thermal derating**

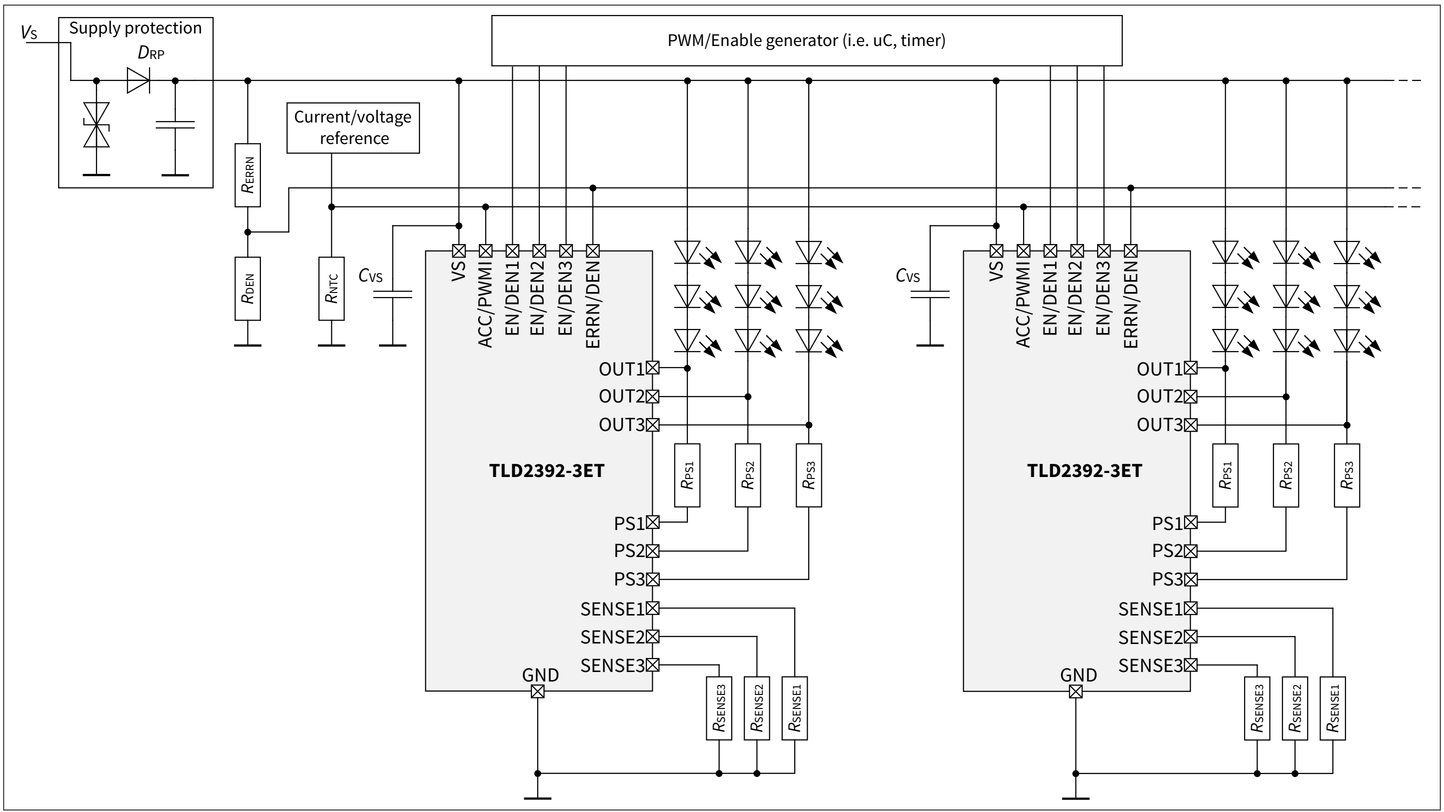
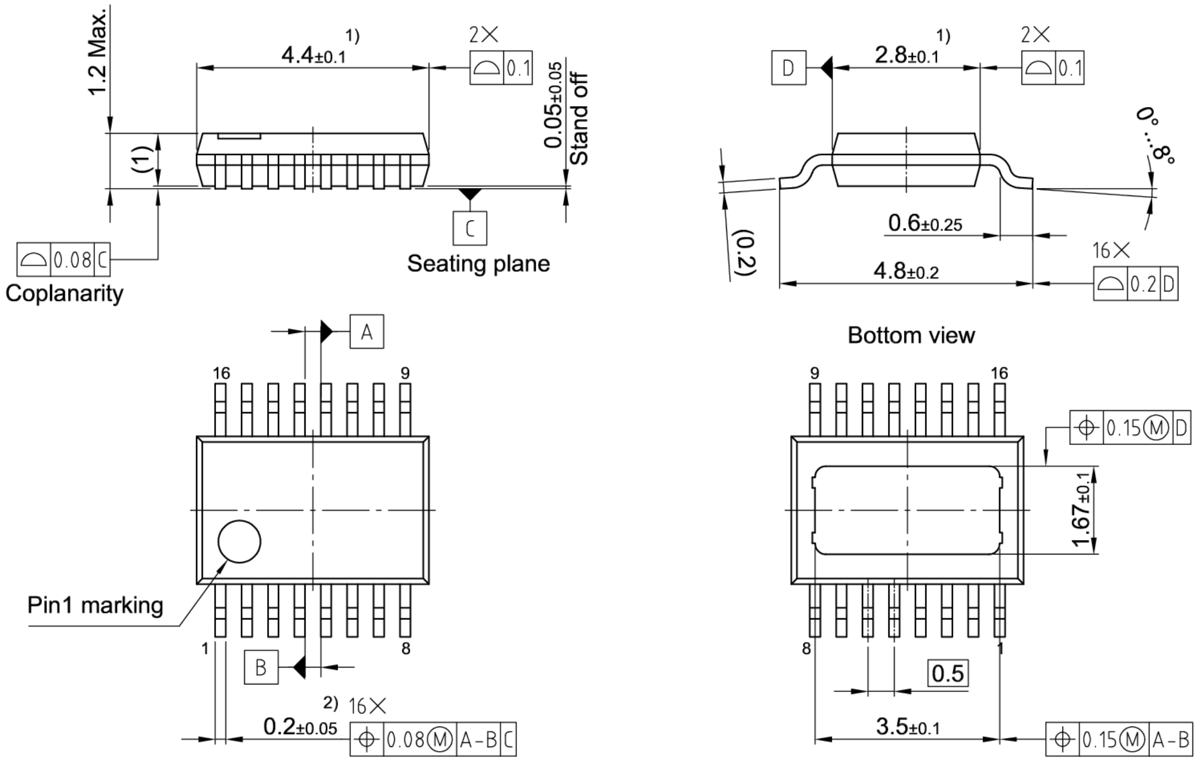


Figure 20 **Application diagram example for animated light function in a shared network with "one fail all on" fault management and central thermal derating**

12 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 21 PG-TFDSO-16 package outline png

Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2024-10-14	• Initial document release

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Edition 2024-10-14

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-pkm1676904717109