

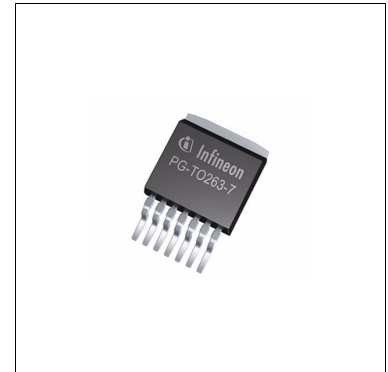
# OPTIREG™ linear TLE4271-2

## 5-V low drop fixed voltage regulator



### Features

- Output voltage tolerance  $\leq \pm 2\%$
- Low-drop voltage
- Integrated overtemperature protection
- Reverse polarity protection
- Input voltage up to 42 V
- Overvoltage protection up to 65 V ( $\leq 400$  ms)
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range
- Adjustable reset and watchdog time
- Green Product (RoHS-compliant)



### Potential applications

General automotive applications.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The OPTIREG™ linear TLE4271-2 is functional and electrical identical to TLE4271.

The device is a 5-V low drop fixed voltage regulator. The maximum input voltage is 42 V (65 V,  $\leq 400$  ms). Up to an input voltage of 26 V and for an output current up to 550 mA it regulates the output voltage within a 2% accuracy. The short circuit protection limits the output current of more than 650 mA. The IC can be switched off via the inhibit input. An integrated watchdog monitors the connected controller. The device incorporates overvoltage protection and temperature protection that disables the circuit at overtemperature.

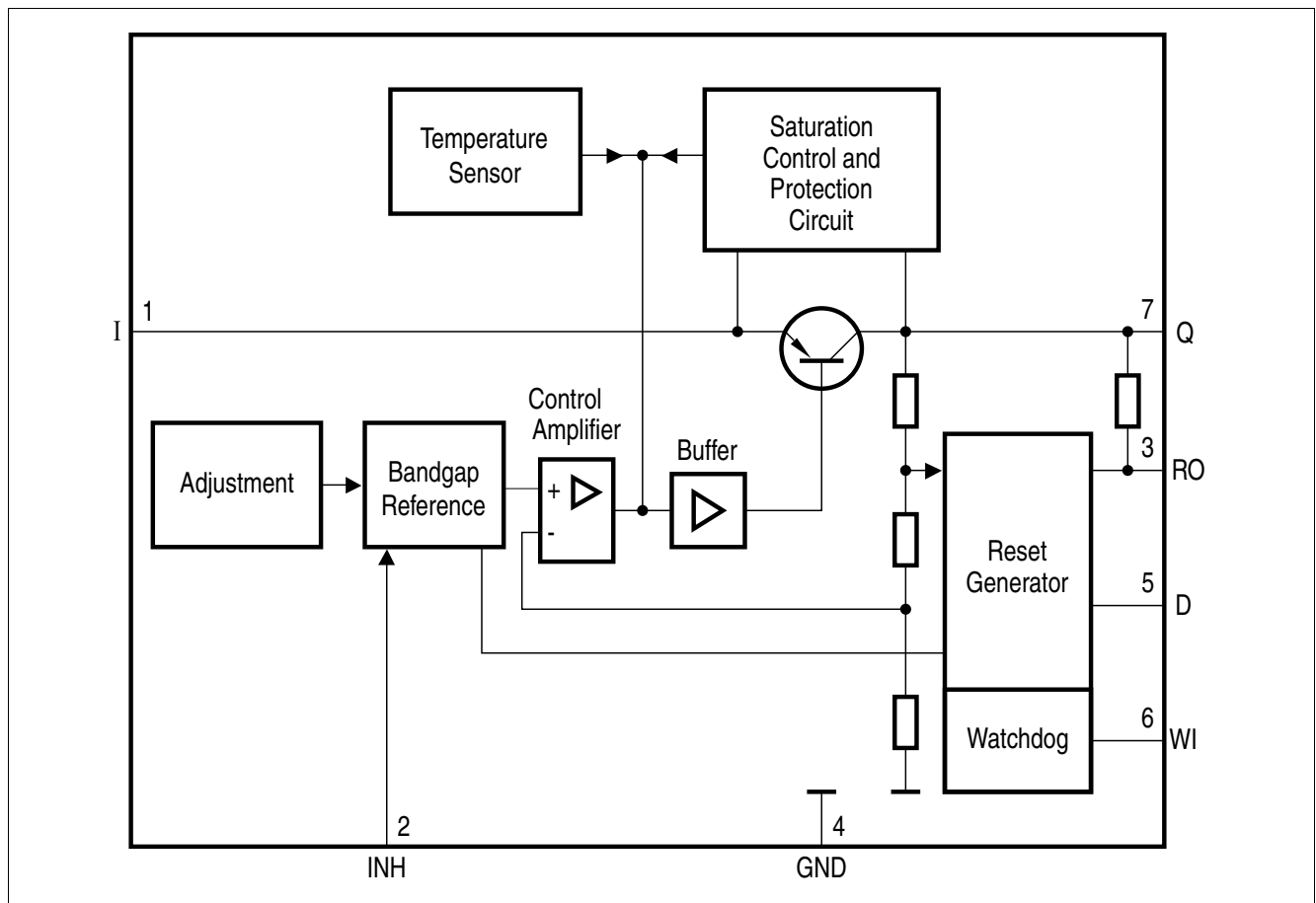
Type	Package	Marking
TLE4271-2G	PG-TO263-7	4271-2

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**Block diagram**

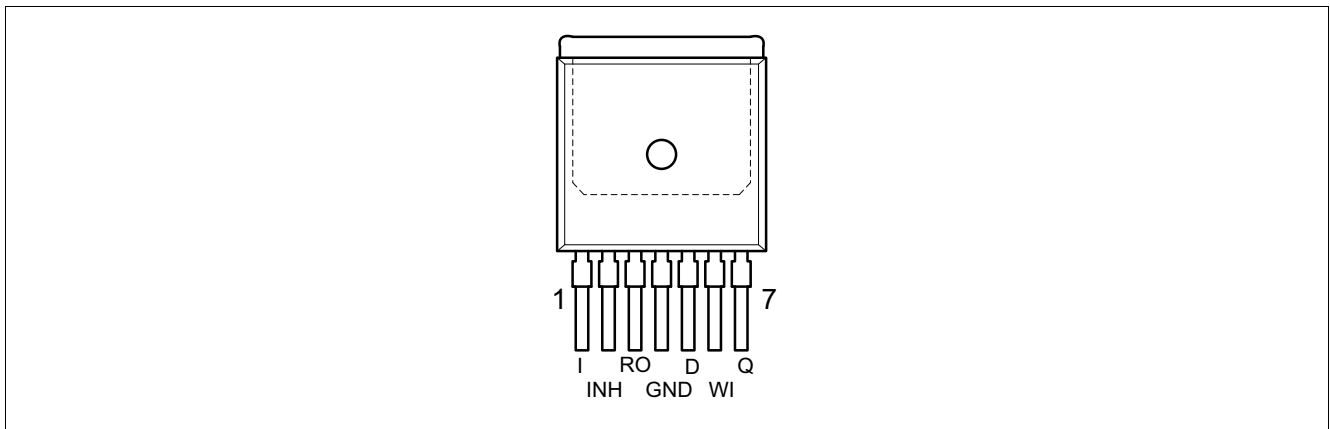
**1 Block diagram**



**Figure 1 Block diagram**

**Pin configuration**

**2 Pin configuration**



**Figure 2 Pin configuration** (top view)

**Table 1 Pin definitions and functions**

Pin	Symbol	Function
1	I	<b>Input</b> Block to ground directly on the IC with ceramic capacitor.
2	INH	<b>Inhibit</b>
3	RO	<b>Reset output</b> The open collector output is connected to the 5 V output via an integrated resistor of 30 kΩ.
4	GND	<b>Ground</b>
5	D	<b>Reset delay</b> Connect a capacitor to ground for delay time adjustment.
6	WI	<b>Watchdog input</b>
7	Q	<b>5-V output</b> Block to ground with 22 μF capacitor, ESR < 3 Ω.

General product characteristics

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>Input</b>						
Voltage	$V_I$	-42	-	42	V	-
Voltage	$V_I$	-	-	65	V	$t \leq 400$ ms
Current	$I_I$	-	-	-	mA	Internally limited
<b>Inhibit</b>						
Voltage	$V_{INH}$	-42	-	42	V	-
Voltage	$V_{INH}$	-	-	65	V	$t \leq 400$ ms
Current	$I_{INH}$	-	-	-	mA	Internally limited
<b>Reset output</b>						
Voltage	$V_{RO}$	-0.3	-	42	V	-
Current	$I_{RO}$	-	-	-	mA	Internally limited
<b>Reset delay</b>						
Voltage	$V_D$	-0.3	-	7	V	-
Current	$I_D$	-5	-	5	mA	-
<b>Watchdog</b>						
Voltage	$V_W$	-0.3	-	7	V	-
Current	$I_W$	-5	-	5	mA	-
<b>Output</b>						
Voltage	$V_Q$	-1.0	-	16	V	-
Current	$I_Q$	-5	-	-	mA	Internally limited
<b>Ground</b>						
Current	$I_{GND}$	-0.5	-	-	A	-
<b>Temperatures</b>						
Junction temperature	$T_j$	-	-	150	$^\circ\text{C}$	-
Storage temperature	$T_{stg}$	-50	-	150	$^\circ\text{C}$	-

**General product characteristics**

**3.2 Operating range**

**Table 3 Operating range**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage	$V_I$	6	–	40	V	–
Junction temperature	$T_j$	-40	–	150	°C	–
<b>Thermal resistance</b>						
Junction ambient	$R_{thja}$	–	–	70	K/W	–
Junction case	$R_{thjc}$	–	–	3	K/W	–
	$Z_{thjc}$	–	–	2	K/W	$t < 1$ ms

**General product characteristics**

**3.3 Characteristics**

**Table 4 Characteristics**

$V_I = 13.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ;  $V_{\text{INH}} > V_{\text{U,INH}}$  (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output voltage	$V_Q$	4.90	5.00	5.10	V	$I_Q = 5\text{ mA}$ to $550\text{ mA}$ ; $V_I = 6\text{ V}$ to $26\text{ V}$
Output voltage	$V_Q$	4.90	5.00	5.10	V	$V_I = 26\text{ V}$ to $36\text{ V}$ ; $I_Q \leq 300\text{ mA}$
Output current limiting	$I_{Q\text{max}}$	650	800	–	mA	$V_Q = 0\text{ V}$
Current consumption $I_q = I_1$	$I_q$	–	–	6	$\mu\text{A}$	$V_{\text{INH}} = 0\text{ V}$ ; $I_Q = 0\text{ mA}$
Current consumption $I_q = I_1$	$I_q$	–	800	–	$\mu\text{A}$	$V_{\text{INH}} = 5\text{ V}$ ; $I_Q = 0\text{ mA}$
Current consumption $I_q = I_1 - I_Q$	$I_q$	–	1	1.5	mA	$I_Q = 5\text{ mA}$
Current consumption $I_q = I_1 - I_Q$	$I_q$	–	55	75	mA	$I_Q = 550\text{ mA}$
Current consumption $I_q = I_1 - I_Q$	$I_q$	–	70	90	mA	$I_Q = 550\text{ mA}$ ; $V_I = 5\text{ V}$
Drop voltage	$V_{\text{dr}}$	–	350	700	mV	$I_Q = 550\text{ mA}^{1)}$
Load regulation	$\Delta V_Q$	–	25	50	mV	$I_Q = 5\text{ mA}$ to $550\text{ mA}$ ; $V_I = 6\text{ V}$
Supply voltage regulation	$\Delta V_Q$	–	12	25	mV	$V_I = 6\text{ V}$ to $26\text{ V}$ ; $I_Q = 5\text{ mA}$
Power supply ripple rejection	$PSRR$	–	54	–	dB	$f_r = 100\text{ Hz}$ ; $V_r = 0.5\text{ Vpp}$

**Reset generator**

Switching threshold	$V_{\text{RT}}$	4.5	4.65	4.8	V	–
Reset high voltage	$V_{\text{ROH}}$	4.5	–	–	V	–
Saturation voltage	$V_{\text{RO,SAT}}$	–	60	–	mV	$R_{\text{intern}} = 30\text{ k}\Omega$ ; $V_Q = 1.0\text{ V}$ to $4.5\text{ V}$
Saturation voltage	$V_{\text{RO,SAT}}$	–	200	400	mV	$I_R = 3\text{ mA}^{2)}$ ; $V_Q = 4.4\text{ V}$
Reset pull-up	$R$	18	30	46	$\text{k}\Omega$	Internally connected to Q
Lower reset timing threshold	$V_{\text{LD}}$	0.2	0.45	0.8	V	$V_Q < V_{\text{RT}}$
Charge current	$I_D$	8	14	25	$\mu\text{A}$	$V_D = 1.0\text{ V}$
Upper timing threshold	$V_{\text{UD}}$	1.4	1.8	2.3	V	–
Delay time	$t_D$	8	13	18	ms	$C_D = 100\text{ nF}$
Reset reaction time	$t_{\text{RR}}$	–	–	3	$\mu\text{s}$	$C_D = 100\text{ nF}$

**General product characteristics**

**Table 4 Characteristics (cont'd)**

$V_I = 13.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ;  $V_{INH} > V_{U,INH}$  (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
<b>Overvoltage protection</b>						
Turn-off voltage	$V_{I,ov}$	40	44	46	V	–
<b>Inhibit</b>						
Turn-on voltage	$V_{U,INH}$	1.0	2.0	3.5	V	$V_Q = \text{high} (> 4.5\text{ V})$
Turn-off voltage	$V_{L,INH}$	0.8	1.3	3.3	V	$V_Q = \text{low} (< 0.8\text{ V})$
Inhibit current	$I_{INH}$	8	12	25	$\mu\text{A}$	$V_{INH} = 5\text{ V}$
<b>Watchdog</b>						
Upper watchdog switching threshold	$V_{UDW}$	1.4	1.8	2.3	V	–
Lower watchdog switching threshold	$V_{LDW}$	0.2	0.45	0.8	V	–
Discharge current	$I_{DWD}$	1.5	2.7	3.5	$\mu\text{A}$	$V_D = 1\text{ V}$
Charge current	$I_{DWC}$	8	14	25	$\mu\text{A}$	$V_D = 1\text{ V}$
Watchdog period	$t_{WD,P}$	40	55	80	ms	$C_D = 100\text{ nF}$
Watchdog trigger time	$t_{WI,tr}$	30	45	66	ms	$C_D = 100\text{ nF}$ see diagram
Watchdog pulse slew rate	$V_{WI}$	5	–	–	V/ $\mu\text{s}$	From 20% to 80% $V_Q$

1) Drop voltage =  $V_I - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input).

2) Test condition not applicable during delay time for power-on reset.



**Circuit description**

**4 Circuit description**

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

The reset output RO is in high-state if the voltage on the delay capacitor  $C_D$  is greater or equal  $V_{UD}$ . The delay capacitor  $C_D$  is charged with the current  $I_D$  for output voltages greater than the reset threshold  $V_{RT}$ . If the output voltage gets lower than  $V_{RT}$  ('reset condition') a fast discharge of the delay capacitor  $C_D$  sets in and as soon as  $V_D$  gets lower than  $V_{LD}$  the reset output RO is set to low-level.

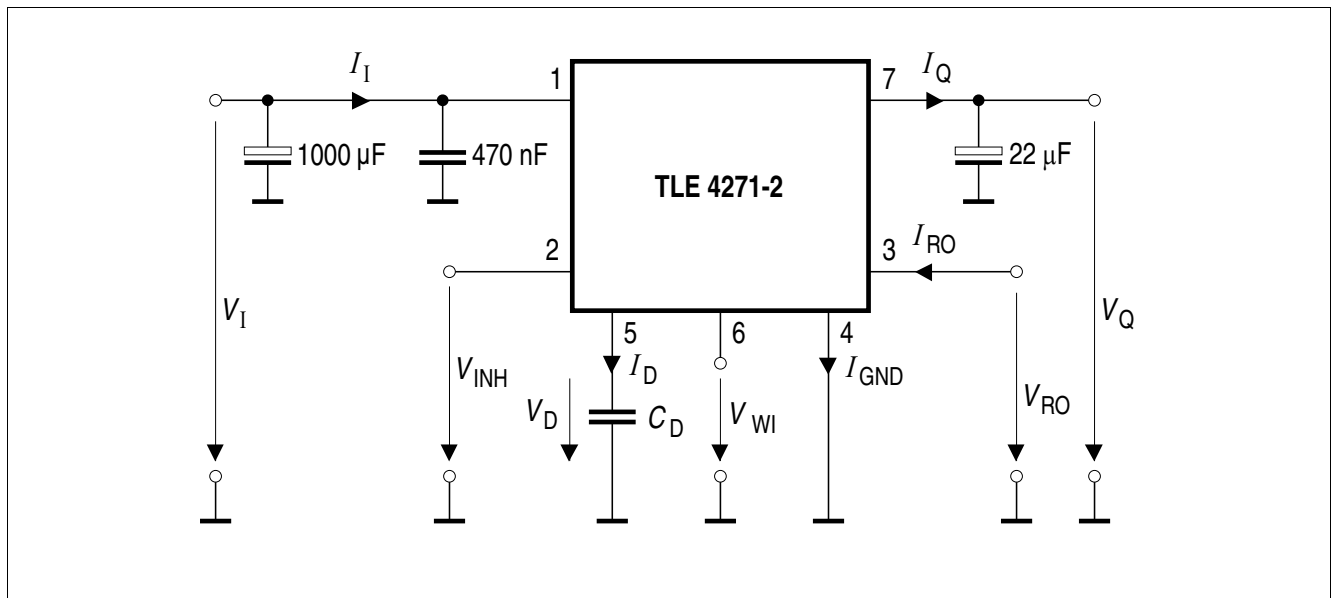
The time for the delay capacitor charge from  $V_{UD}$  to  $V_{LD}$  is the reset delay time  $t_D$ .

When the voltage on the delay capacitor has reached  $V_{UD}$  and reset was set to high, the watchdog circuit is enabled and discharges  $C_D$  with the constant current  $I_{DWD}$ . If there is no rising edge observed at the watchdog input,  $C_D$  will be discharge down to  $V_{LDW}$ , then reset output RO will be set to low and  $C_D$  will be charged again with the current  $I_{DWC}$  until  $V_D$  reaches  $V_{UD}$  and reset will be set high again.

If the watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period  $C_D$  is charged again and the reset output stays high. After  $V_D$  has reached  $V_{UD}$ , the periodical behavior starts again.

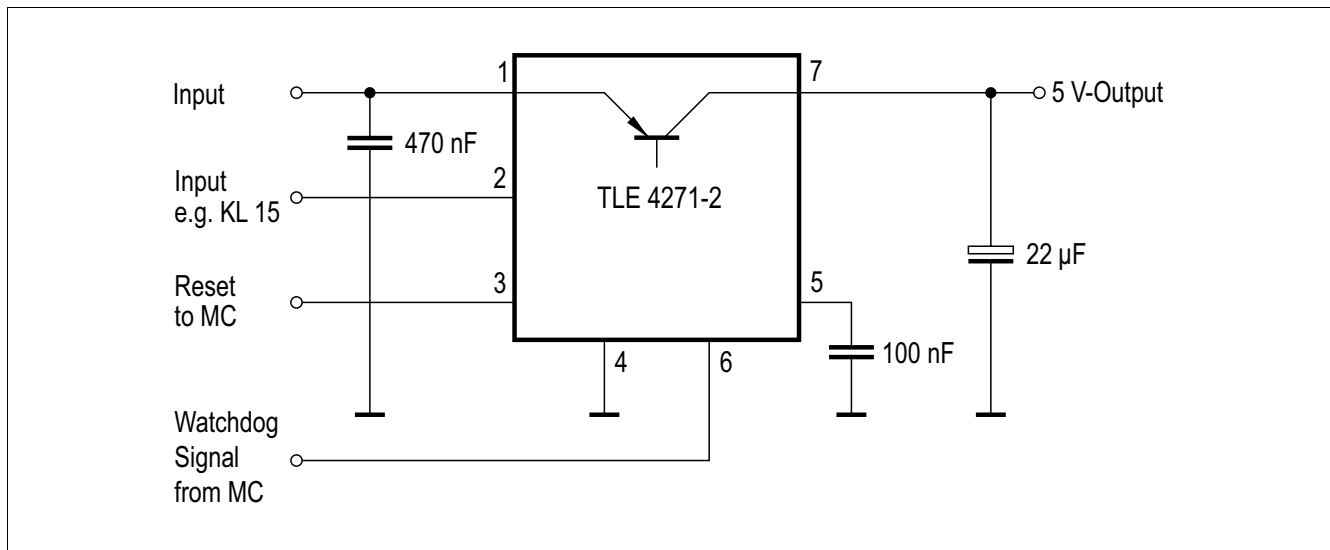
Internal protection circuits protect the IC against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity



**Figure 3 Test circuit**

**Circuit description**



**Figure 4 Circuit**

**Application description**

The IC regulates an input voltage in the range of  $6\text{ V} < V_I < 40\text{ V}$  to  $V_{Qnom} = 5.0\text{ V}$ . Up to 26 V it produces a regulated output current of more than 550 mA. Above 26 V the save-operating-area protection allows operation up to 36 V with a regulated output current of more than 300 mA. Overvoltage protection limits operation at 42 V. The overvoltage protection hysteresis restores operation if the input voltage has dropped below 36 V. The IC can be switched off via the inhibit input, which causes the quiescent current to drop below 10 µA. A reset signal is generated for an output voltage of  $V_O < 4.5\text{ V}$ . The watchdog circuit monitors a connected controller. If there is no positive-going edge at the watchdog input within a fixed time, the reset output is set to low. The delay for power-on reset and the maximum permitted watchdog-pulse period can be set externally with a capacitor.

**Design notes for external components**

An input capacitor  $C_I$  is necessary for compensation of line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with  $C_I$ . An output capacitor  $C_O$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values of  $C_O \geq 22\text{ µF}$  and an ESR of  $< 3\text{ Ω}$ .

**Reset circuitry**

If the output voltage decreases below 4.5 V, an external capacitor  $C_D$  on pin D will be discharged by the reset generator. If the voltage on this capacitor drops below  $V_{DRL}$ , a reset signal is generated on pin RO, i.e. reset output is set low. If the output voltage rises above the reset threshold,  $C_D$  will be charged with constant current. After the power-on-reset time the voltage on the capacitor reaches  $V_{DU}$  and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of  $C_D$ .

**Reset timing**

The power-on reset delay time is defined by the charging time of an external capacitor  $C_d$  which can be calculated as follows:

$$t_D = C_D \times \Delta V / I_D \tag{4.1}$$

Definitions:

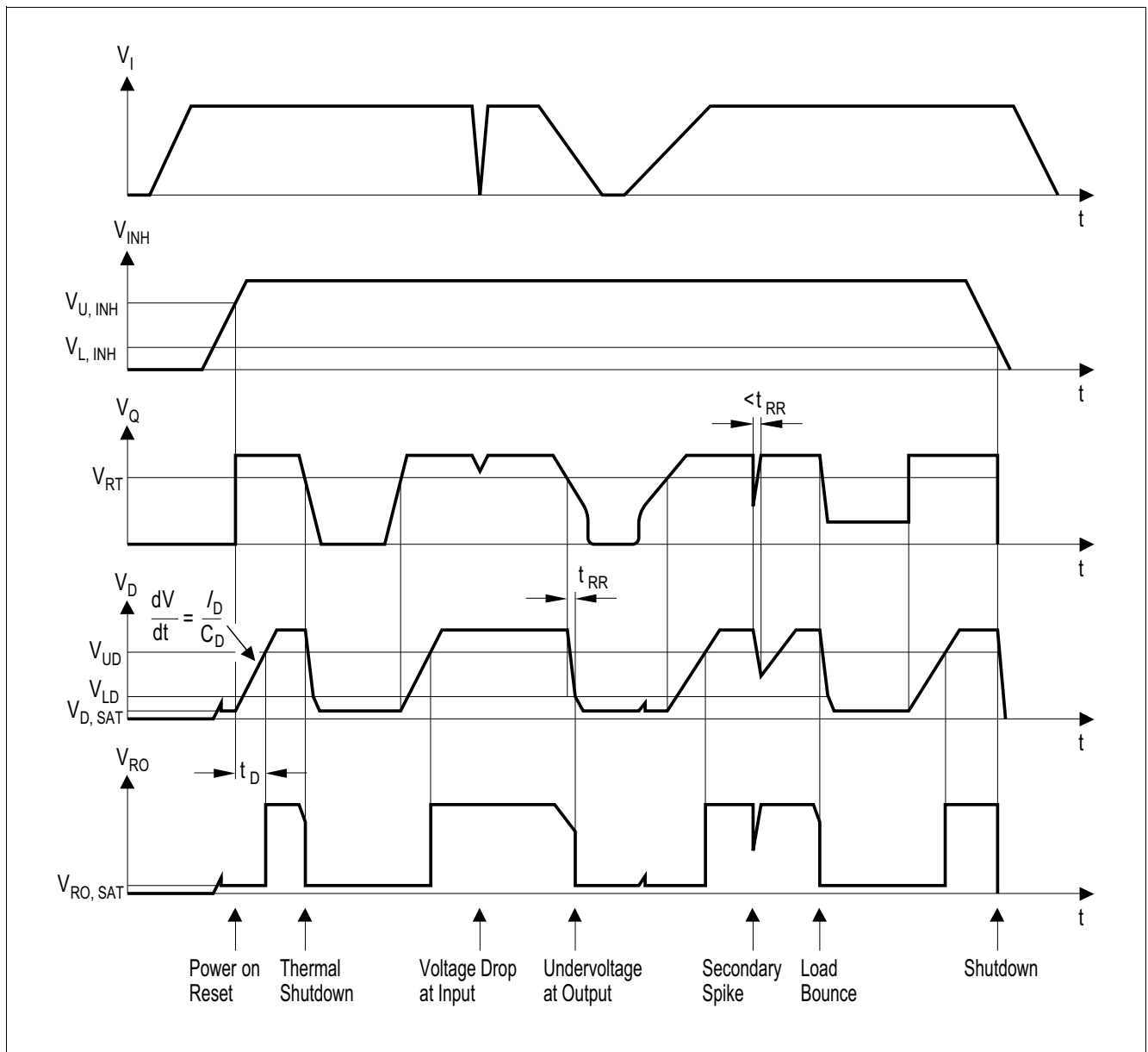
- $C_D$  = delay capacitor

**Circuit description**

- $t_D$  = reset delay time
- $I_D$  = charge current, typical 14  $\mu\text{A}$
- $\Delta V = V_{UD}$ , typical 1.8 V
- $V_{UD}$  = upper delay timing threshold at  $C_D$  for reset delay time

The reset reaction time  $t_{rr}$  is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1  $\mu\text{s}$  for delay capacitor of 47 nF. For other values for  $C_d$  the reaction time can be estimated using the following equation:

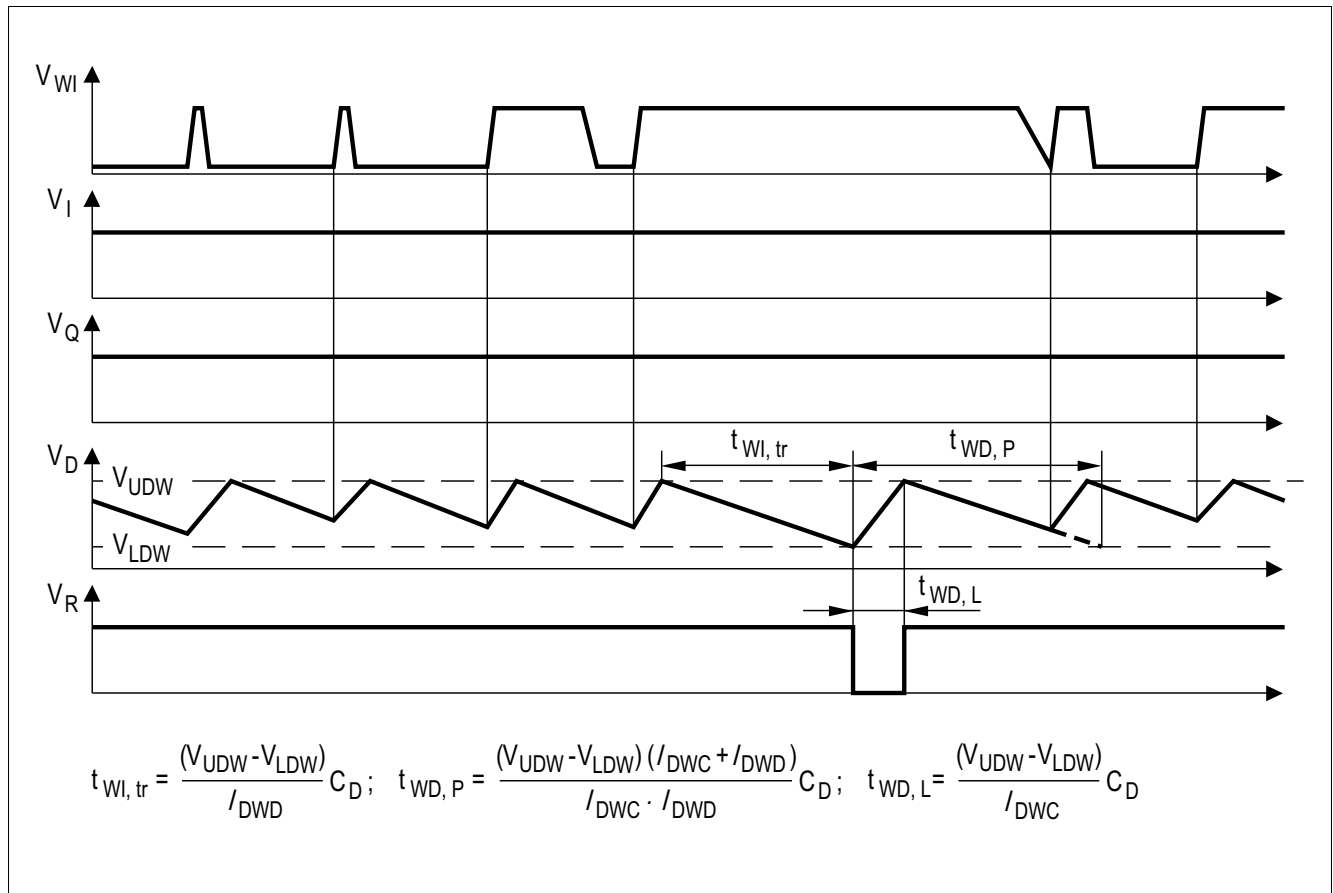
$$t_{RR} \approx 20 \text{ s/F} \times C_d \tag{4.2}$$



**Figure 5 Time response**

**Circuit description**

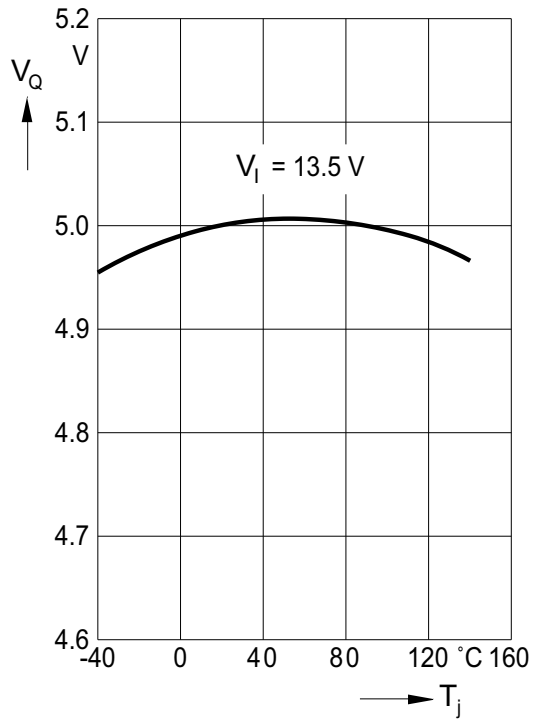
**Watchdog timing**



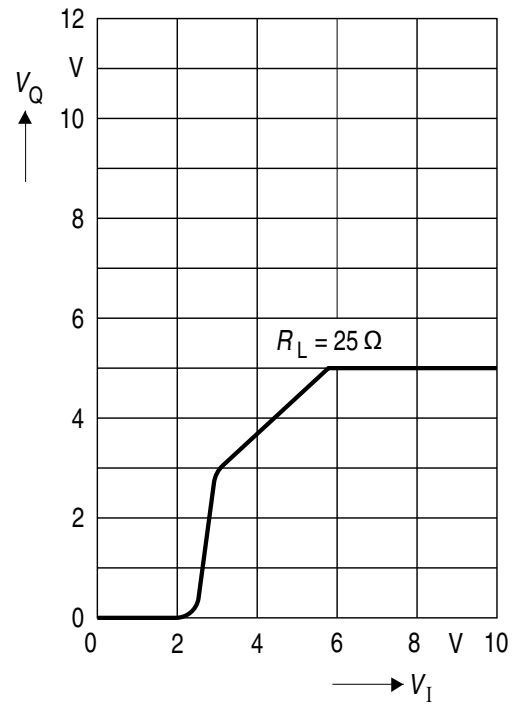
**Figure 6 Time response, watchdog behavior**

## 5 Typical performance characteristics

**Output voltage  $V_Q$  versus junction temperature  $T_j$**

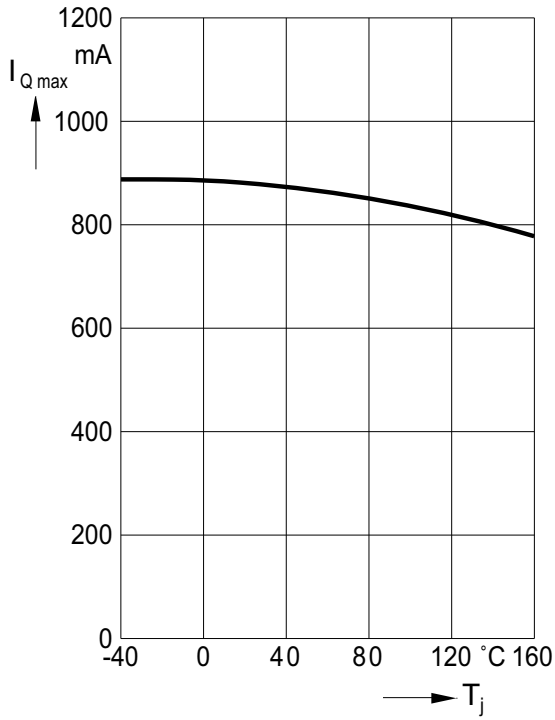


**Output voltage  $V_Q$  versus input voltage  $V_I$  ( $V_{INH} = V_I$ )**

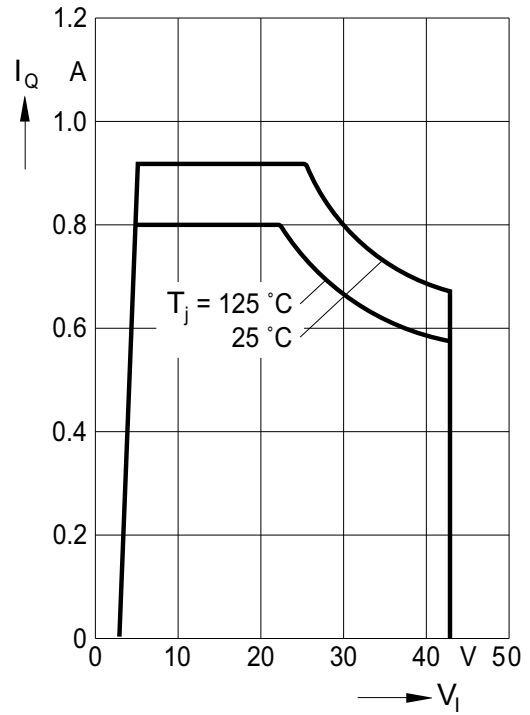


**Typical performance characteristics**

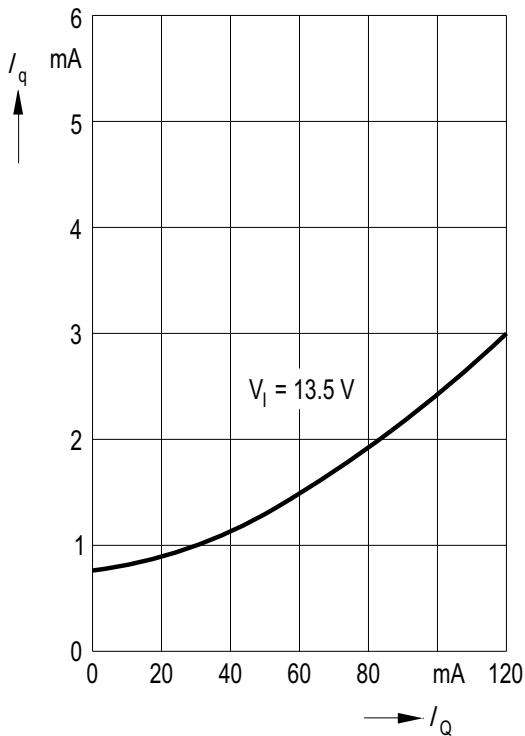
**Output current  $I_Q$  versus junction temperature  $T_j$**



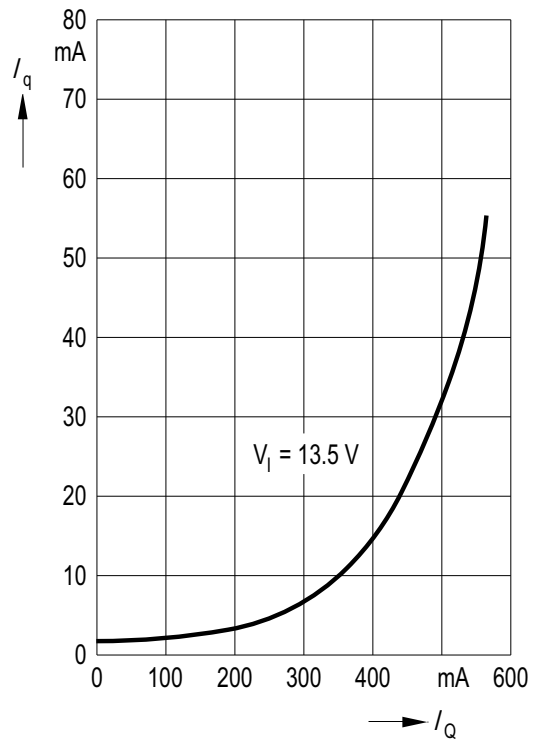
**Output current  $I_Q$  versus input voltage  $V_I$**



**Current consumption  $I_q$  versus output current  $I_Q$**

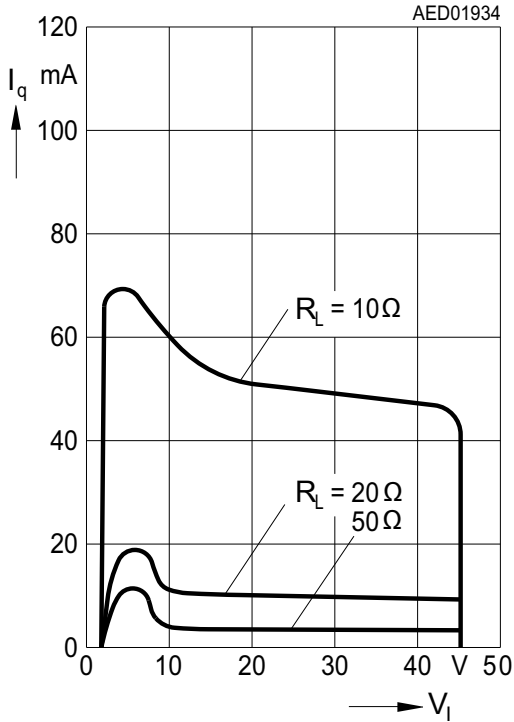


**Current consumption  $I_q$  versus output current  $I_Q$**

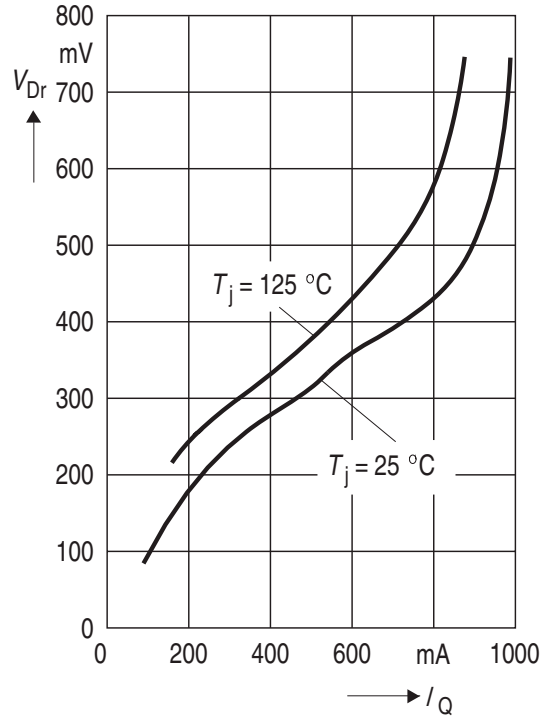


**Typical performance characteristics**

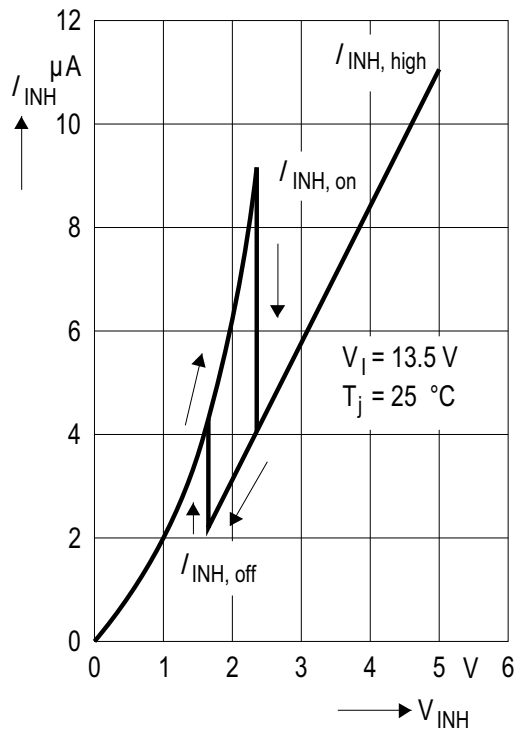
**Current consumption  $I_q$  versus input voltage  $V_I$**



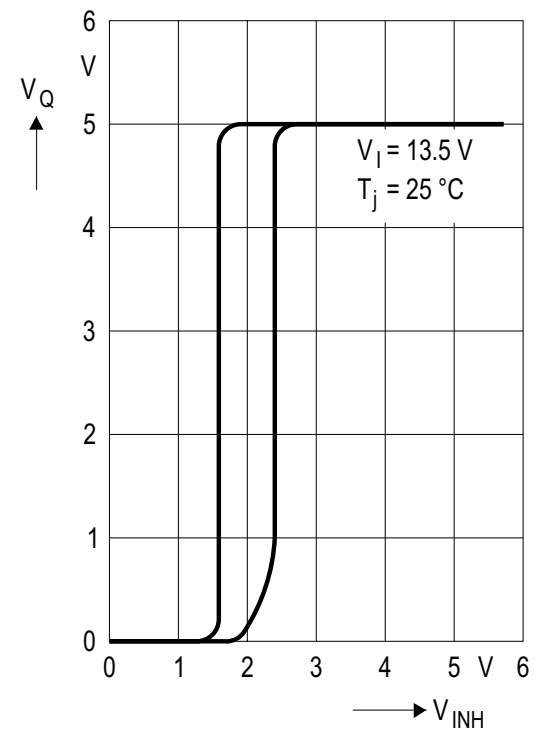
**Drop voltage  $V_{Dr}$  versus output current  $I_Q$**



**Inhibit current  $I_{INH}$  versus inhibit voltage  $V_{INH}$**

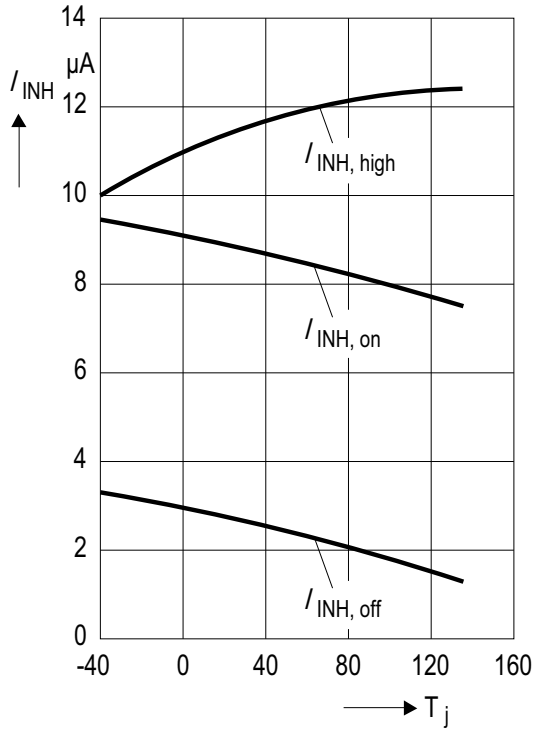


**Output voltage  $V_Q$  versus inhibit voltage  $V_{INH}$**

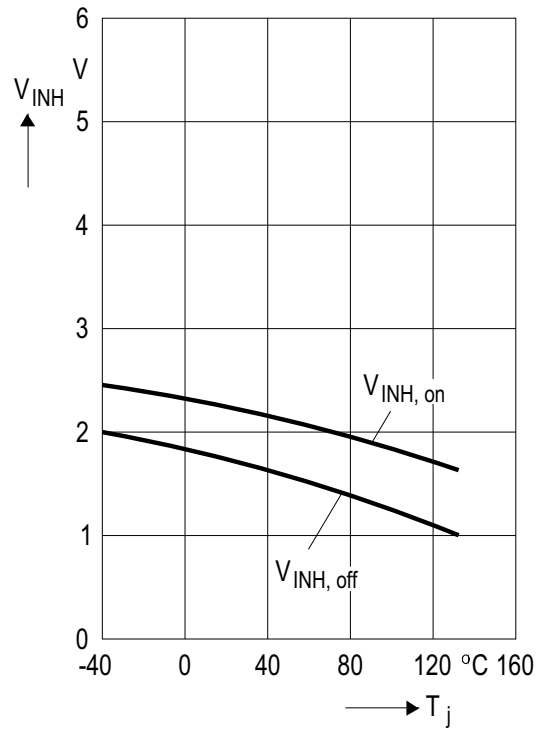


**Typical performance characteristics**

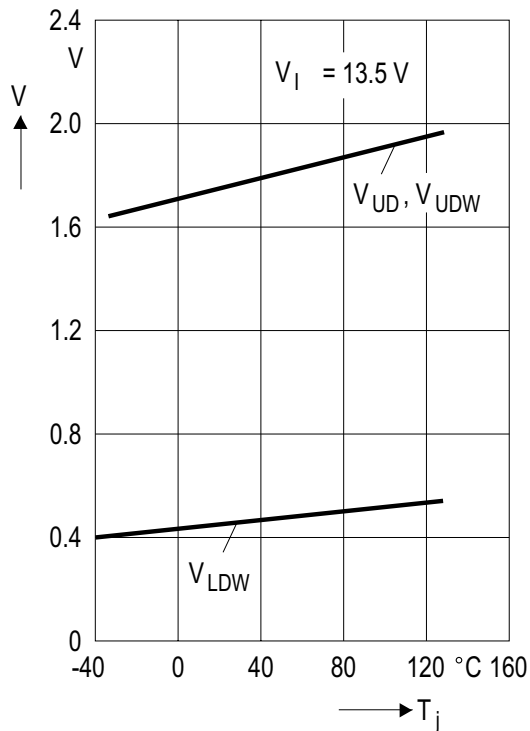
**Inhibit current consumptions  $I_{INH}$  versus temperature  $T_j$**



**Inhibit voltages  $V_{INH}$  versus junction temperature  $T_j$**



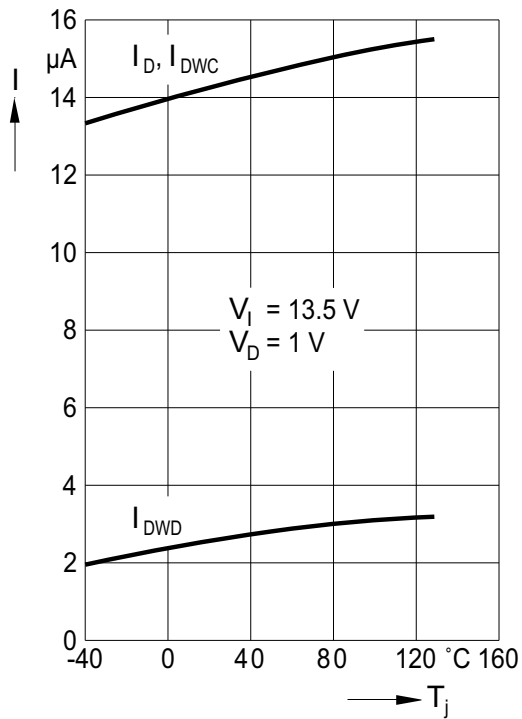
**Switching voltage  $V_{UD}$  and  $V_{LDW}$  versus junction temperature  $T_j$**



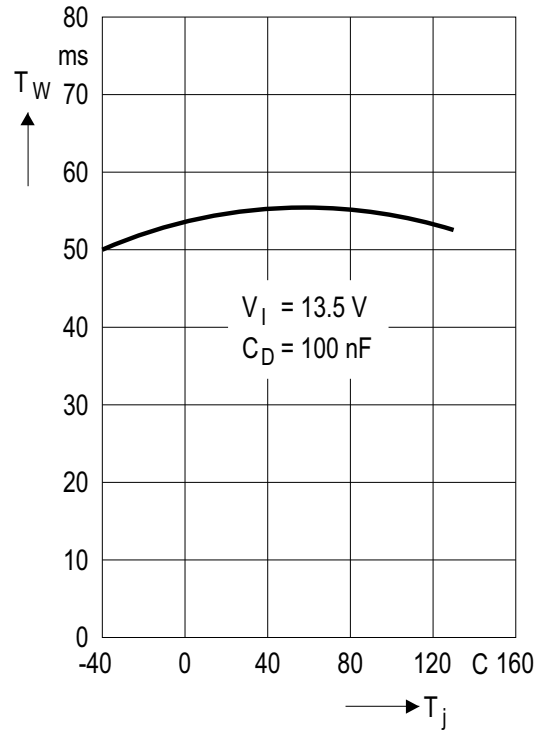


**Typical performance characteristics**

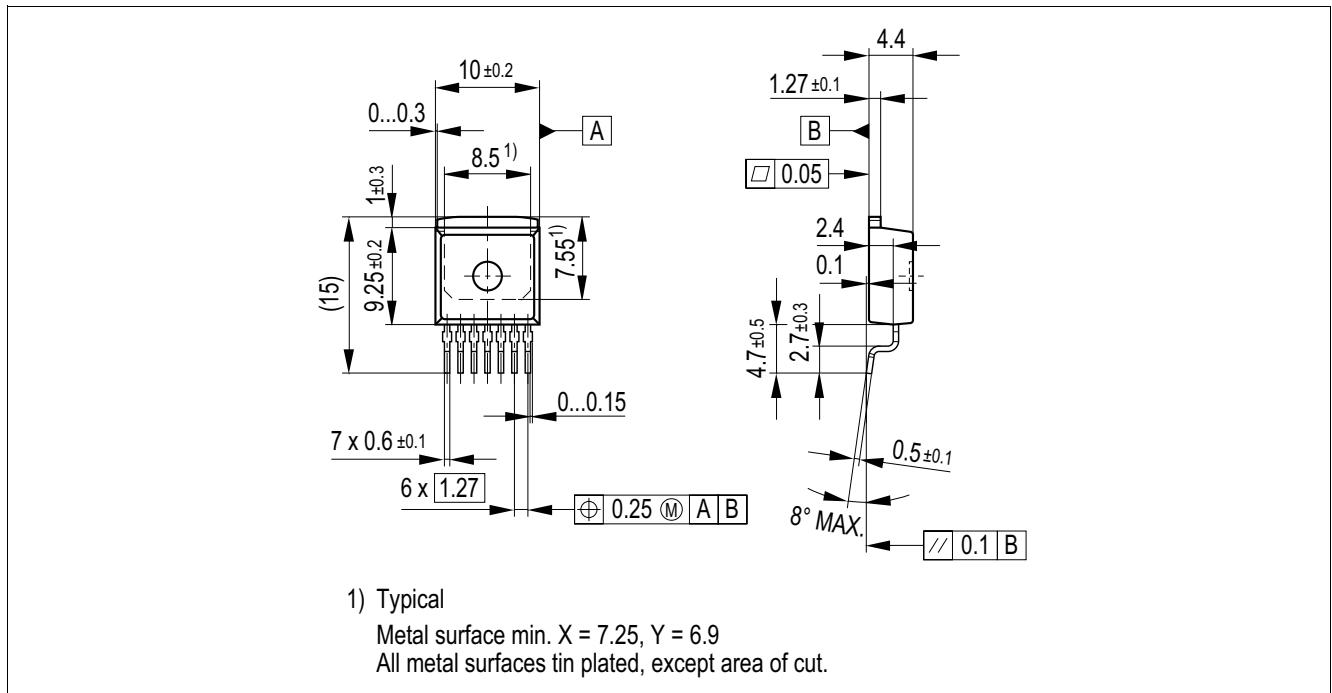
**Charge current  $I_D$ ,  $I_{DWC}$  and discharge current  $I_{DWD}$  versus junction temperature  $T_j$**



**Watchdog pulse time  $T_w$  versus junction temperature  $T_j$**



## 6 Package information



**Figure 7 PG-TO263-7 (Plastic transistor single outline)<sup>1)</sup>**

### Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
2.9	2023-07-05	Chapter 3.2: removed unnecessary comment in junction ambient specification; removed junction ambient specification of 65 K/W for previously discontinued package - PG-TO220-7; Editorial change (marking on page 1)
2.8	2019-07-30	Deleted both packages: PG-TO-220-7 Updated layout and structure frontpage: updated packaged drawings “TLE4271-2” Editorial changes
2.7	2007-03-20	Initial version of RoHS-compliant derivate of TLE4271-2 Page 1: AEC certified statement added Page 1 and Page 18ff: RoHS-compliance statement and Green product feature added Page 1 and Page 18ff: Package changed to RoHS-compliant version Legal Disclaimer updated

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**Document reference**

**Z8F55216529**

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