TLE9012DQU

Improved Li-ion battery monitoring and balancing IC

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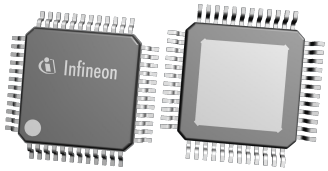
AEC Qualified | RoHS | ISO 26262 compliant

Features



- Voltage monitoring of up to 12 battery cells connected in series
- Hot plugging support
- Dedicated 16-bit high precision delta-sigma ADC for each cell with selectable measurement mode
- High-accuracy measurement with typical ±0.2 mV initial accuracy at ambient temperature with a typical lifetime adder of 1 LSB after 10 years of usage
- Integrated stress sensor with digital compensation algorithm and temperature-compensated measurements
- Secondary ADC with identical averaging filter characteristics as advanced end-to-end safety mechanism
- Five temperature measurement channels for external NTC elements
- Two internal temperature sensors
- Integrated balancing switch allows up to 200 mA balancing current
- Differential robust serial 2 Mbit/s communication interface with up to 38 devices
- Additional four GPIO pins to e.g. connect an external EEPROM and PWM driver
- Internal round robin cycle routine triggers majority of diagnostics mechanisms
  - Automatic balancing overcurrent and undercurrent detection
  - Automatic open load and open wire detection
  - Automatic NTC measurement unit monitoring
- End-to-end CRC secured iso UART/UART communication
- Wake from bus capability (EMM)
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL D
- Green Product (RoHS compliant)

Potential applications

Multi-cell battery monitoring and balancing system IC designed for Li-ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in 12 V/48 V Li-ion batteries and energy storage systems (ESS).

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The device is a IC for lithium-ion battery cell management. The main function is to measure all cell voltages in parallel with high precision and accuracy as well as temperatures. Additionally, the device is able to individually and parallelly balance all cell voltages. The device offers a UART interface and an isolated daisy chain interface called iso UART for communication with the host controller. The small package design and robust technology enables a lean design and a ultra low bill of materials.

Type	Package	Marking
TLE9012DQU	PG-TQFP-48	TLE9012DQU

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1 Block diagram

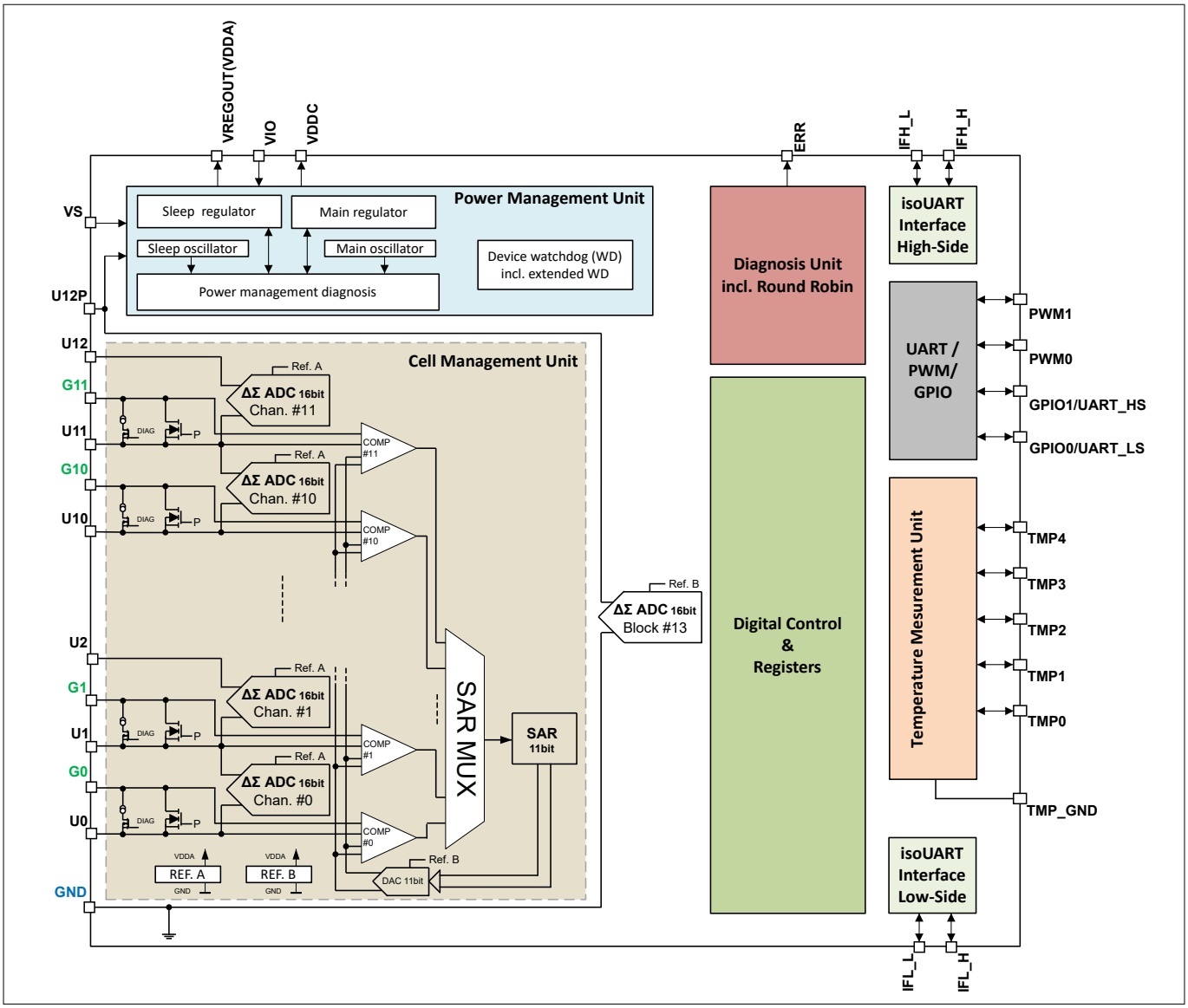

Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

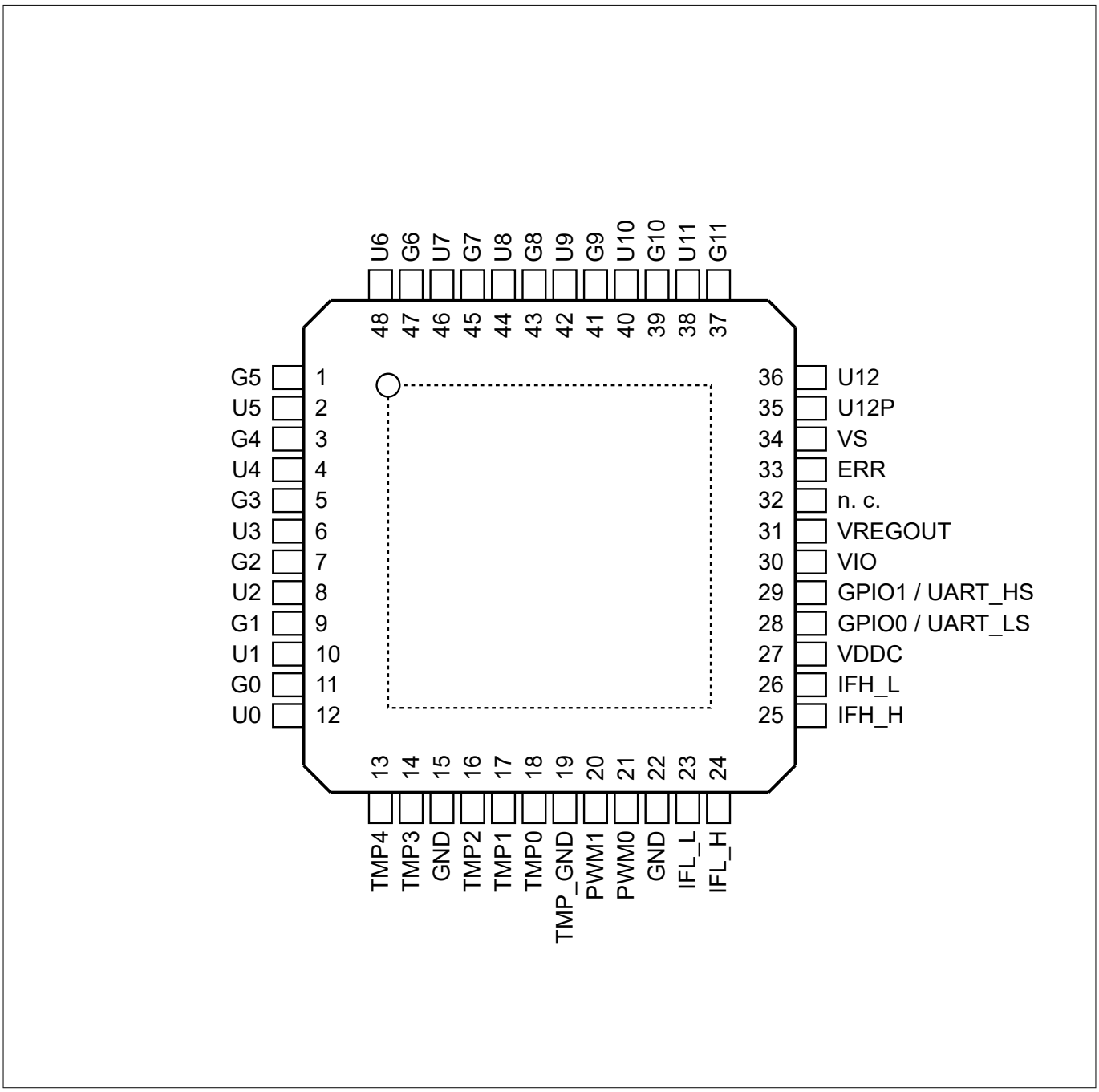

Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

Pin	Symbol	Pin type	Function
1	G5	A_I / O	Cell-balancing channel 5.
2	U5	A_I	Cell voltage measurement channel 5, negative terminal (positive terminal of cell 4).

2 Pin configuration

Pin	Symbol	Pin type	Function
3	G4	A_I / O	Cell-balancing channel 4.
4	U4	A_I	Cell voltage measurement channel 4, negative terminal (positive terminal of cell 3).
5	G3	A_I / O	Cell-balancing channel 3.
6	U3	A_I	Cell voltage measurement channel 3, negative terminal (positive terminal of cell 2).
7	G2	A_I / O	Cell-balancing channel 2.
8	U2	A_I	Cell voltage measurement channel 2, negative terminal (positive terminal of cell 1).
9	G1	A_I / O	Cell-balancing channel 1.
10	U1	A_I	Cell voltage measurement channel 1, negative terminal (positive terminal of cell 0).
11	G0	A_I / O	Cell-balancing channel 0.
12	U0	A_I	Cell voltage measurement channel 0, negative terminal (same potential as local GND).
13	TMP4	IO	Temperature sensor 4. If not used connect pin to GND via a pull-down resistor > 10 kΩ. If TMP4 is disabled, the pin can be used as 0 to 2 V auxiliary ADC miscellaneous pin.
14	TMP3	IO	Temperature sensor 3. If not used connect pin to GND via a pull-down resistor > 10 kΩ. If TMP3 is disabled, the pin can be used as 0 to 2 V auxiliary ADC miscellaneous pin.
15	GND	GND	Local GND of CSC (cell supervision circuit) device
16	TMP2	IO	Temperature sensor 2. If not used connect pin to GND via a pull-down resistor > 10 kΩ. If TMP2 is disabled, the pin can be used as 0 to 2 V auxiliary ADC miscellaneous pin.
17	TMP1	IO	Temperature sensor 1. If not used connect pin to GND via a pull-down resistor > 10 kΩ. If TMP1 is disabled, the pin can be used as 0 to 2 V auxiliary ADC miscellaneous pin.
18	TMP0	IO	Temperature sensor 0. If not used connect pin to GND via a pull-down resistor > 10 kΩ. If TMP0 is disabled, the pin can be used as 0 to 2 V auxiliary ADC miscellaneous pin.
19	TMP_GND	IO	Temperature sensor reference. This pin can be connected to local GND.
20	PWM1	IO	PWM output channel 1. This pin also has a general purpose input/output function. If not used connect pin to GND via a pull-down resistor > 10 kΩ.
21	PWM0	IO	PWM output channel 0. This pin also has a general purpose input/output function. If not used connect pin to GND via a pull-down resistor > 10 kΩ.
22	GND	GND	Local GND of CSC device (cell supervision circuit).
23	IFL_L	D_I / O	Lower isolated UART (iso UART) L pin.
24	IFL_H	D_I / O	Lower isolated UART (iso UART) H pin.
25	IFH_H	D_I / O	Upper isolated UART (iso UART) H pin.
26	IFH_L	D_I / O	Upper isolated UART (iso UART) L pin.
27	VDDC	Supply	Buffer capacitor pin for internal iso UART supply.

2 Pin configuration

Pin	Symbol	Pin type	Function
28	GPIO0 / UART_LS	D_I / O	General-purpose input/output channel 0. This pin also has the function of UART_LS. If not used connect pin to GND.
29	GPIO1 / UART_HS	D_I / O	General-purpose input/output channel 1. This pin also has the function of UART_HS. If not used connect pin to GND.
30	VIO	S	Supply for GPIO interface.
31	VREGOUT	S	Output pin for the internal regulator.
32	n.c.	n.c.	Not connected. Connect to GND in application.
33	ERR	HV_D_O	Error output to microcontroller; open drain PMOS connected to VS. If not used, leave unconnected.
34	VS	S	Supply pin of internal regulator $V_{VREGOUT}$.
35	U12P	S	Positive supply pin. Connect to positive terminal of topmost cell in block. Input for the sleep regulator.
36	U12	A_I	Cell voltage measurement channel 11, positive terminal (most upper cell in the block).
37	G11	A_I / O	Cell-balancing channel 11.
38	U11	A_I	Cell voltage measurement channel 11, negative terminal (positive terminal of cell 10).
39	G10	A_I / O	Cell-balancing channel 10.
40	U10	A_I	Cell voltage measurement channel 10, negative terminal (positive terminal of cell 9).
41	G9	A_I / O	Cell-balancing channel 9.
42	U9	A_I	Cell voltage measurement channel 9, negative terminal (positive terminal of cell 8).
43	G8	A_I / O	Cell-balancing channel 8.
44	U8	A_I	Cell voltage measurement channel 8, negative terminal (positive terminal of cell 7).
45	G7	A_I / O	Cell-balancing channel 7.
46	U7	A_I	Cell voltage measurement channel 7, negative terminal (positive terminal of cell 6).
47	G6	A_I / O	Cell-balancing channel 6.
48	U6	A_I	Cell voltage measurement channel 6 negative terminal (positive terminal of cell 5).
–	Exposed Pad	GNDA	Cooling tab. Connect to GND in the application.

Pin types: A = analog, D = digital, HV = high-voltage, I = input, O = output, I/O = bidirectional, P = power, S = supply

3 General product characteristics

Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS	V_{VS_max}	-0.3	–	75	V	–	PRQ-486
Supply voltage VS relative	$V_{VS\_rel\_max}$	$V_{VREGOUT}$ - 0.3	–	–	V	–	PRQ-489
Transient high voltage	$V_{transient\_high\_max}$	75	–	90	V	Maximum transient duration 60 sec. Valid for following pins vs. GND: VS, U12P, U12, Gn, Un (0 ≤ n ≤ 11)	PRQ-521
Supply voltage U12P	V_{U12P_max}	-0.3	–	75	V	–	PRQ-487
Supply voltage VIO	V_{VIO_max}	-0.3	–	5.5	V	–	PRQ-488
Regulator output VREGOUT	$V_{VREGOUT\_max}$	-0.3	–	3.6	V	–	PRQ-490
Regulator output VDDC	V_{VDDC_max}	-0.3	–	3.6	V	Assuming I_{VDDC} ≤ 1 mA continuous current	PRQ-491
Cell sense input voltage absolute Un	V_{Un_max}	-0.3	–	75	V	0 ≤ n ≤ 12	PRQ-494
Cell sense input voltages relative Un	$V_{Un\_rel\_max}$	V_{Un-1} - x	–	V_{Un-1} + 9	V	**1.** 1 ≤ n ≤ 12 **2.** x = -0.0016 × T_j + 0.54 **3.** Typical clamping voltage **4.** Maximum allowed current into/out of the pin: 40 mA **5.** For 7.5 V < V_{Un} < 9 V: Current flowing into the pin is below 10 mA	PRQ-495

(table continues...)

Table 1 (continued) Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell balancing pin absolute Gn	V_{Gn_max}	-0.3	–	75	V	0 ≤ n ≤ 11	PRQ-496
Cell balancing pins relative Gn	$V_{Gn\_rel\_max}$	V_{Un} - 0.3	–	V_{Un+1} + 0.3	V	0 ≤ n ≤ 11	PRQ-497
General purpose I/O voltages absolute GPIOq	V_{GPIOq_max}	-0.3	–	5.5	V	0 ≤ q ≤ 1	PRQ-505
General purpose I/O voltages relative GPIOq	$V_{GPIOq\_rel\_max}$	-0.3	–	V_{VIO} + 0.3	V	0 ≤ q ≤ 1	PRQ-506
Open drain output pin absolute ERR	V_{ERR_max}	-0.3	–	75	V	–	PRQ-510
Open drain output pin relative ERR	$V_{ERR\_rel\_max}$	-0.3	–	V_{VS} + 0.3	V	–	PRQ-509
iso UART interface IFL_x	$V_{IFL\_L\_max}$ $V_{IFL\_H\_max}$	-4.1	–	6.6	V	1) BCI test maximum 300 mA injected via twisted pair cable onto iso UART interface (maximum pin current 150 mA)	PRQ-493
iso UART interface IFH_x	$V_{IFH\_L\_max}$ $V_{IFH\_H\_max}$	-4.1	–	6.6	V	1) BCI test maximum 300 mA injected via twisted pair cable onto iso UART interface (maximum pin current 150 mA)	PRQ-492
Temperature sensor input voltages absolute TMPz	V_{TMPz_max}	-0.3	–	3.63	V	0 ≤ z ≤ 4	PRQ-863

(table continues...)

Table 1 (continued) Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Temperature sensor input voltages relative TMPz	$V_{TMPz\_rel\_max}$	-0.3	–	$V_{VREGOUT}$ + 0.3	V	0 ≤ z ≤ 4	PRQ-864
Temperature sensor input voltage absolute TMP_GND	$V_{TMP\_GND\_max}$	-0.3	–	2.75	V	–	PRQ-503
Temperature sensor input voltages relative TMP_GND	$V_{TMP\_GND\_rel\_max}$	-0.3	–	$V_{VREGOUT}$ + 0.3	V	–	PRQ-504
Pulse width modulation I/O voltages absolute PWMp	V_{PWMp_max}	-0.3	–	5.5	V	0 ≤ p ≤ 1	PRQ-865
Pulse width modulation I/O voltages relative PWMp	$V_{PWMp\_rel\_max}$	-0.3	–	V_{VIO} + 0.3	V	0 ≤ p ≤ 1	PRQ-866
Ground pin GND	V_{GND}	0	–	0	V	Absolute GND	PRQ-511
ESD robustness							
ESD robustness 2 kV	$V_{ESD\_2kV\_max}$	-2	–	2	kV	2) HBM; all pins	PRQ-514
ESD robustness 4 kV	$V_{ESD\_4kV\_max}$	-4	–	4	kV	2) HBM; robustness versus GND for pins: VS, U12P, Un, Gn, TMPz, TMP_GND, IFH_x, IFL_x	PRQ-515
ESD robustness CDM 500 V	$V_{ESD\_cdm\_all\_max}$	-500	–	500	V	3) CDM; all pins	PRQ-516

(table continues...)

Table 1 (continued) Absolute maximum ratings

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
ESD robustness CDM 750 V	$V_{ESD\_Corner\_max}$	-750	–	750	V	3) CDM; corner pins	PRQ-517
Temperatures							
Junction temperature	T_{j_max}	-40	–	150	°C	–	PRQ-512
Storage temperature	T_{stg_max}	-55	–	150	°C	–	PRQ-513

1) Positive and negative transients with a maximum duration of 100 ns allowed between ± 8 V; This should simulate ESD events; however, during normal and steady-state condition voltage on these pins must stay inside the maximum ratings specified.
2) ESD robustness, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
3) ESD robustness, Charged Device Model JESD22-C101.

Notes:

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 2 Functional range

T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage VS	$V_{VS\_functional}$	4.75	–	60	V	–	PRQ-518
Supply voltage U12P	$V_{U12P\_functional}$	4.75	–	60	V	–	PRQ-519
Supply voltage VIO	$V_{VIO\_functional}$	3	–	5.5	V	–	PRQ-520
Cell sense input voltage Un	$V_{Un\_functional}$	V_{Un-1} - x	–	V_{Un-1} + 7	V	**1.** $1 \le n \le 12$ **2.** $x = -0.0016 \times T_j + 0.54$	PRQ-1358

3.3 Thermal resistance

Table 3 Thermal resistance

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	6	–	K/W	1)	PRQ-522
Junction to ambient	R_{thJA}	–	30	–	K/W	1) 2)	PRQ-523

1) Not subject to production test, specified by design.
2) Specified *R*thJA value is according to JEDEC JESD51-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). The thermal via array under the exposed pad consists of 16 vias with a diameter of 0.3 mm and a plating thickness of 25 µm.

4 Monitoring of internal oscillators

The IC includes monitoring of two internal oscillators:

1. Main oscillator operating at f_{main_osc}
2. Sleep oscillator operating at f_{sleep_osc} → in sleep mode only the sleep mode oscillator is active

In normal mode both oscillators are active. The oscillators monitor each other for drift and stuck-at errors. As soon as the IC detects an error, it enters sleep mode. The oscillator error prevents reliable writing to any register and hence the IC does not set any error bit before entering sleep mode.

4.1 Electrical characteristics monitoring of internal oscillators

Table 4 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Oscillator							
Main unit oscillator frequency	f_{main_osc}	13.44	14	14.56	MHz	–	PRQ-564
Sleep unit oscillator frequency	f_{sleep_osc}	90	100	110	kHz	–	PRQ-565

5 Power Management Unit (PMU)

5.1 Functional description

The IC has an internal power supply unit connected to the pins VS, U12P and GND. It consumes energy from the monitored battery cells and generates the internal supply voltages for the IC as well as the output voltages V_{VDDC} and $V_{VREGOUT}$.

Note: The output pins VDDC and VREGOUT require a capacitance to ground as stated in the Application information/External components.

Note: No supply currents are drawn from Un pins.

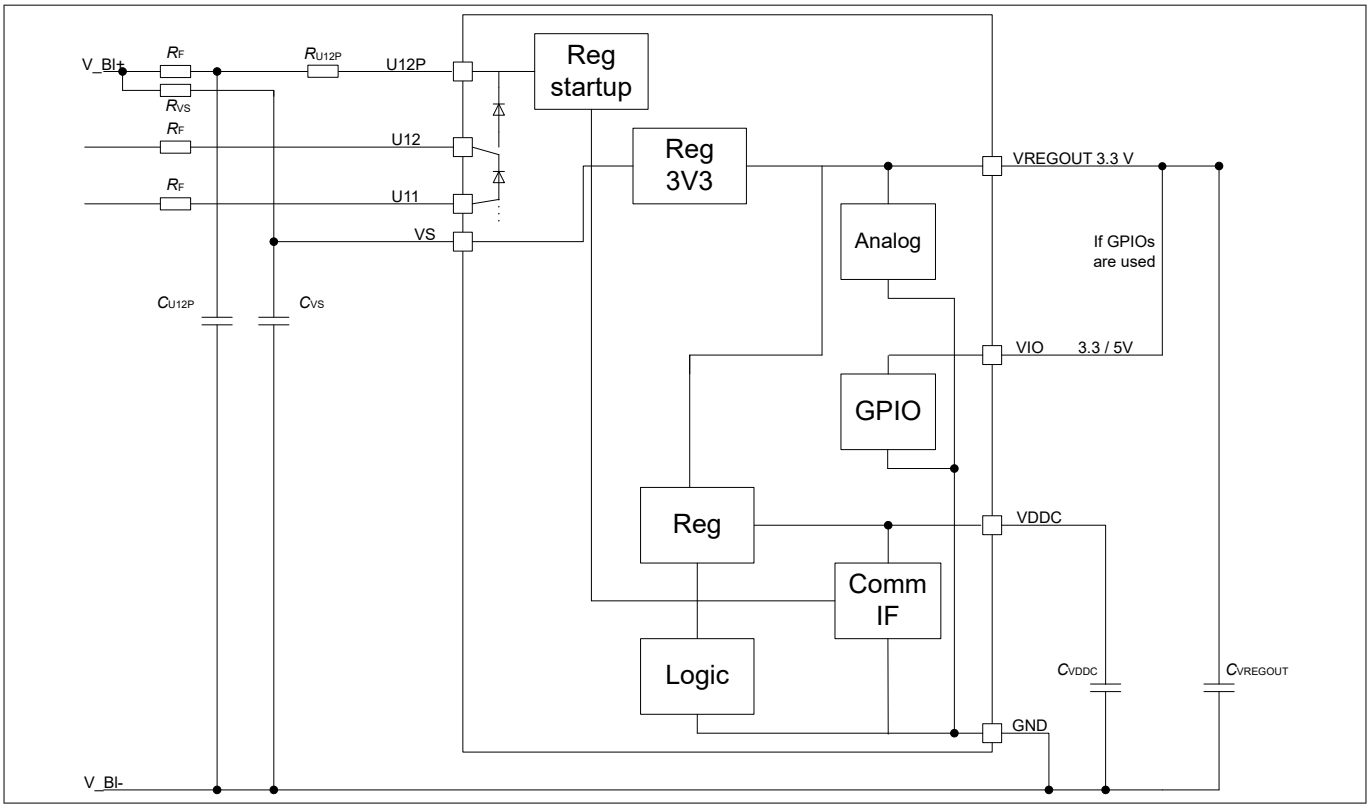

Figure 3 Typical power supply configuration using the internal voltage regulator

The IC has a sleep mode with reduced current consumption supplied via U12P and GND.

The IC can be put into sleep mode by setting the sleep mode bit. The sleep mode features a reduced current consumption, I_{U12P_sleep}, supplied via U12P and GND.

To supply the communication interface, the device provides a regulated output voltage V_{VDDC} on pin VDDC.

If the voltage V_{VDDC} falls below the undervoltage threshold $V_{VDDC\_th\_UV}$ for a longer time than $t_{PS\_ERR\_deg}$, then the IC enters sleep mode. The power supply error sleep bit in the general diagnostics register indicate a fault, which can be read after waking the IC.

The device provides a regulated output voltage $V_{VREGOUT}$ with an output current $I_{VREGOUT}$ on pin VREGOUT which can supply the GPIOs of the device or other loads.

The multi purpose supply incorporates an overcurrent protection. If the current $I_{VREGOUT}$ exceeds $I_{VREGOUT\_th\_OC}$ for a longer time than $t_{PS\_ERR\_deg}$, then it switches off the output voltage supply. The IC enters sleep mode after the deglitching time $t_{PS\_ERR\_deg}$. The power supply error sleep bit in the general diagnostics register indicates a fault, which can be read after waking up the IC.

The voltage at the VIO pin sets the logic levels and supplies the GPIOs. The pin can be connected directly to the VREGOUT pin or to another desired voltage level using an external regulator.

If the voltage V_{VIO} falls below the undervoltage threshold $V_{VIO\_th\_UV\_fall}$ for a longer time than $t_{PS\_ERR\_deg}$, then the IC sets the VIO undervoltage error bit in the general purpose input/output register. After V_{VIO} has exceeded the $V_{VIO\_th\_UV\_rise}$ threshold for longer than $t_{PS\_ERR\_deg}$, the UV_VIO bit can be cleared with a write command.

Note: If the GPIO.VIO_UV bit is 0, the GPIO functionality is enabled and wake-up via GPIO is possible.

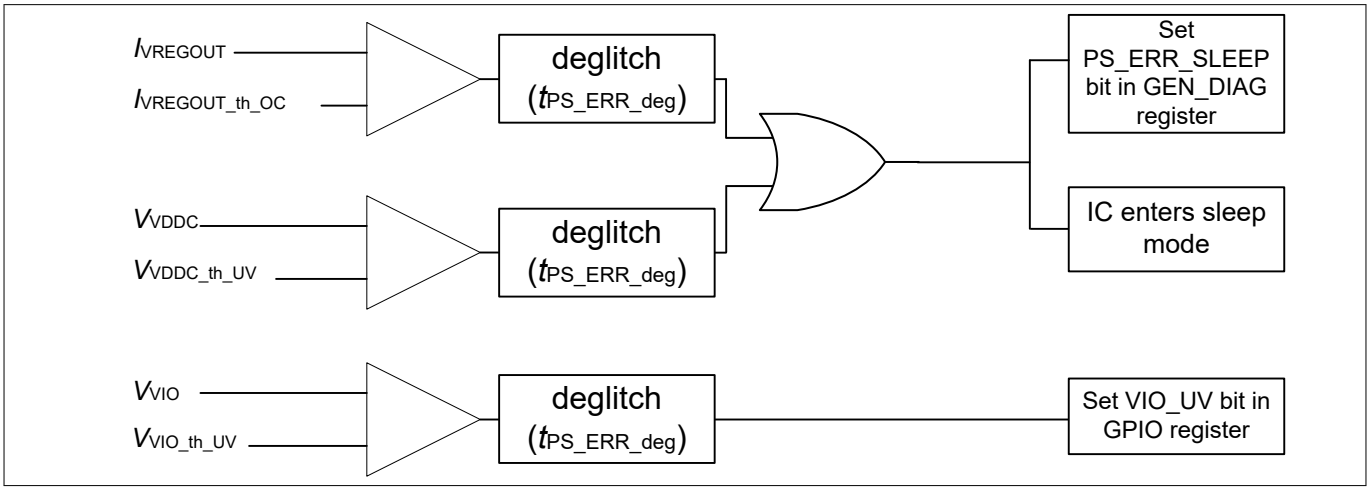

Figure 4 Power supply monitoring

The IC ensures wake-up and operation even if any single wire connected to a cell is open in case of failure (assumption: U12P and VS connected on PCB level). If an absolute maximum rating is violated due to an open wire, then performance degradation may occur.

5.2 Electrical characteristics power management unit (PMU)

Table 5 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal regulators							
VREGOUT internal regulator output voltage	$V_{VREGOUT}$	3.3	3.45	3.6	V	–	PRQ-544
VDDC output voltage	V_{VDDC}	2.42	2.5	2.63	V	–	PRQ-549

(table continues...)

Table 5 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply currents							
Current consumption in 100 ms period - RT	$I_{VS\_100ms\_cyc\_RT}$	5.4	5.6	5.8	mA	**1.** T_j = 25°C **2.** Assumed cycle 100 ms period and 16-Bit mode (EN_ALL_ADC = 1) • 5% cell Voltage Measurement • 40% NTC current source activated • 5% diagnostics (Temperature and RR) • 7% communication • 43% idle **3.** Current to charge-up external interface components not included (see $I_{VS\_comm\_ext}$)	PRQ-563
U12P sleep mode current	I_{U12P_sleep}	–	2.5	9.9	µA	**1.** Typical value at T_j = 25°C **2.** -40°C ≤ T_j ≤ 85°C; **3.** Round robin in sleep mode deactivated	PRQ-553
U12P sleep mode current - room temperature	$I_{U12P\_sleep\_RT}$	–	2.5	3.5	µA	T_j = 25°C	PRQ-554
U12P idle current	I_{U12P_idle}	–	2.5	10	µA	IC in idle mode	PRQ-556
VS sleep mode leakage current	I_{VS_sleep}	-1	–	1	µA	-40°C < T_j < 85°C	PRQ-555
VS idle current	I_{VS_idle}	–	4.9	6.5	mA	IC in idle mode	PRQ-557
VREGOUT current consumption multi purpose supply	$I_{VREGOUT}$	–	–	5	mA	No load on VIO	PRQ-1373

(table continues...)

Table 5 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VIO current consumption during GPIO communication	I_{VIO_comm}	–	–	5	mA	No load on VREGOUT	PRQ-558
VS current consumption during PCVM, SCVM and BVM measurement	I_{VS_meas}	–	22.5	24	mA	**1.** PCVM (EN_ALL_ADC = 1) **2.** SCVM **3.** BVM **4.** VIO connected to VREGOUT **5.** Including idle consumption I_{VS_idle}	PRQ-559
VS current consumption during round robin scheme running	I_{VS_RR}	–	9.0	11	mA	**1.** Average current consumption during round robin **2.** VIO connected to VREGOUT **3.** Including idle consumption I_{VS_idle} **4.** NR_TEMP_SENSE ≥ 2, EN_ALL_ADC = 1, CVM_DEL = 0x01	PRQ-560
VS current consumption during communication	I_{VS_comm}	–	$I_{VS\_idle\_typ}$ + 0.9	$I_{VS\_idle\_max}$ + 1.2	mA	[1] **1.** GPIO communication. **2.** Current to charge external interface components not included.	PRQ-561
VS current consumption during iso UART communication including external interface components	$I_{VS\_comm\_isoU}$	–	–	I_{VS_comm} + 7.6	mA	[1] **1.** C_{ser} = 1 nF **2.** BR_{iso_U} = 2 Mbit/s **3.** R_{ser} = 39 Ω **4.** $C_{isoUART\_F}$ = 220 pF **5.** Valid for one iso UART interface in TX mode	PRQ-562
Protection and Detection							
VREGOUT overcurrent threshold	$I_{VREGOUT\_th\_OC}$	31	40	60	mA	Tested during idle mode	PRQ-545
VIO undervoltage threshold falling	$V_{VIO\_th\_UV\_fall}$	2.2	–	2.76	V	–	PRQ-546

(table continues...)

Table 5 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VIO undervoltage threshold rising	$V_{VIO\_th\_UV\_rise}$	2.24	–	2.9	V	–	PRQ-547
VIO undervoltage threshold hysteresis	$V_{VIO\_th\_UV\_hys}$	40	100	160	mV	–	PRQ-548
VDDC undervoltage threshold	$V_{VDDC\_th\_UV}$	2.15	–	2.42	V	–	PRQ-550
VDDC undervoltage threshold hysteresis	$V_{VDDC\_th\_UV\_hys}$	80	100	140	mV	–	PRQ-551
Power supply error detection deglitch time	$t_{PS\_ERR\_deg}$	8	15	24	µs	1)	PRQ-552

1) Not subject to production test; verified by design or characterization.

6 Watchdog and wake-up function (WD)

6.1 Functional description

The following events trigger a wake-up:

1. A wake-up pattern received via the iso UART or UART interfaces. The signal alternates with the frequency f_{WAKEUP}. After n_{WAKE_det} signal periods received by the IC, it performs a wake-up. The IC completes the wake-up process within t_{wake}. After that the IC forwards the same wake-up signal for n_{WAKEUP} periods. The IC forwards a wake-up signal received via UART to the iso UART interface, a wake-up signal received via iso UART to the adjacent iso UART interface.
2. A round robin sleep timeout.
3. An EMM signal recognized as wake-up signal.

The IC generates the wake-up pattern on:

- IFL, if the IC received a valid wake-up pattern on interface IFH.
  - (1) indicates the source of wake-up, (2) indicates the propagation on IFL_x
- IFH, if the IC received a valid wake-up pattern on interface IFL.
  - (3) indicates the source of wake-up, (4) indicates the propagation on IFH_x
- IFL, if the IC received a valid wake-up pattern on interface GPIO1/UART_HS.
  - (5) indicates the source of wake-up, (6) indicates the propagation on IFL_x
- IFH, if the IC received a valid wake-up pattern on interface GPIO0/UART_LS.
  - (7) indicates the source of wake-up, (8) indicates the propagation on IFH_x

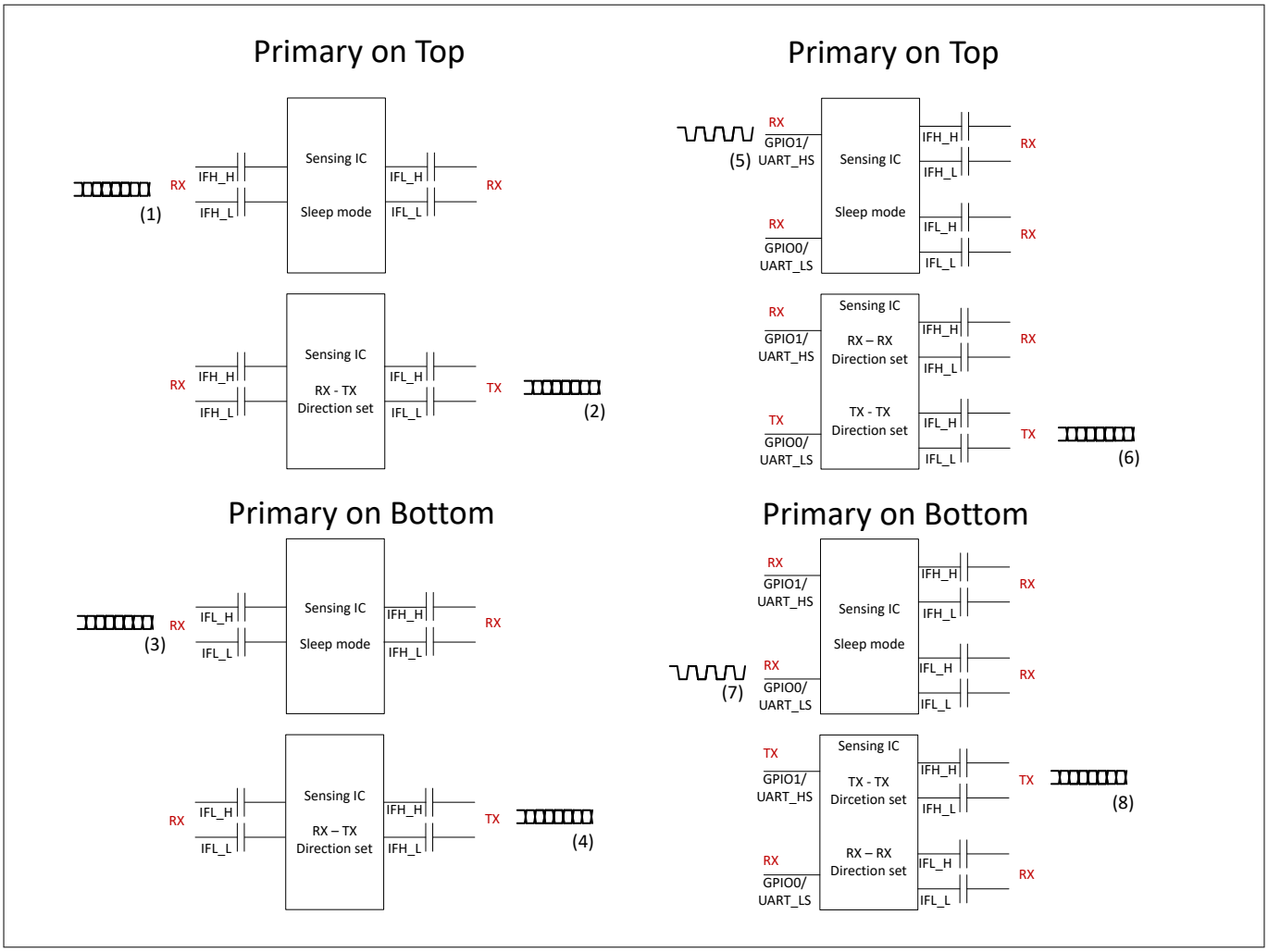

Figure 5 Wake-up signal propagation

The device configures the communication interface automatically after wake-up.

The device configures the iso UART interface of the wake-up signal received as RX during idle mode (no communication) until the next wake-up. The device configures the other iso UART interface as TX in idle mode until the next wake-up.

The IC has a 7-bit watchdog counter which is counting downwards. The watchdog counter must be serviced via an UART or iso UART command before it reaches 0. Otherwise the device enters sleep mode. The watchdog counter can be set to maximum t_{WD_max} with a resolution of t_{WD_LSB}, via the watchdog counter register.

Note: After the IC wake-up, the watchdog counter is set to its maximum value t_{WD_max}

If a longer counter interval is needed, the IC can be put into an extended watchdog mode by setting the operation mode register. In this mode the maximum time until the watchdog counter expires is defined by $t_{WD\_EXT\_max}$ with a resolution of $t_{WD\_EXT\_LSB}$. When the counter expires, the device enters sleep mode.

The device provides a free-running 9-bit main counter which is counting upwards and can be checked via the communication interface reading the watchdog counter register.

The maximum length is t_{Count_max} with a resolution of t_{Count_LSB}. The precisely timed reading of the main counter gives an indication of the main oscillator speed.

If bitfield RR_CONFIG.RR_SYNC is set, then a WDOG_CNT write command resets the main counter. This prepares for a broadcast read of all main counters.

After the device wakes up on a standard wake-up signal the device's node ID is set to 0 by default. In this state, the device does not forward any communication. A node ID other than 0 must be set in the address (ID) bits of configuration register before the watchdog timer expires. Only then the device forwards communication.

Note: If an EMM signal is received, the device forwards it even though the device is not enumerated.

6.2 Electrical characteristics watchdog and wake-up function (WD)

Table 6 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Wake-up function							
WD wake-up signal frequency	f_{WAKEUP}	48	50	1040	kHz	–	PRQ-572
WD device wake-up time	t_{WAKE}	200	370	500	µs	48 kHz wake-up frequency. From the first falling edge of the input pattern to the first edge of the propagated wake-up sequence.	PRQ-573
WD wake-up - number of detected periods	n_{WAKE_det}	4	–	8	periods	–	PRQ-574
WD wake-up propagation - length in periods	n_{WAKE}	8	–	8	periods	–	PRQ-575
Watchdog counter							
WD interval step	t_{WD_LSB}	14.5	16	17.8	ms	1) EXT_WD = 0	PRQ-576
WD maximum interval	t_{WD_max}	1.8	2.03	2.3	s	1) EXT_WD = 0	PRQ-578
WD interval step - extended	$t_{WD\_EXT\_LSB}$	13.5	15.07	17	min	1) EXT_WD = 1	PRQ-577
WD maximum interval - extended	$t_{WD\_EXT\_max}$	28.9	31.9	35.5	h	1) EXT_WD = 1	PRQ-579
Main counter							
WD main counter interval step	t_{Count_LSB}	281	292.57	305	µs	1)	PRQ-580
WD main counter maximum interval	t_{Count_max}	144.03	149.8	156.03	ms	1)	PRQ-581

1) Not subject to production test; verified by design or characterization.

7 Measurement control (MC)

7.1 Functional description

The various voltage measuring modules on the IC follow these rules:

- All voltage measurements (PCVM, SCVM, BVM, BAVM, AVM) can be manually triggered by a communication command.
- A triggered measurement sets a lock bit which inhibits a measurement triggered by a cyclical task. The device clears the lock bit after completion of the measurement.
- BVM, PCVM and SCVM can be triggered simultaneously.
- Bipolar auxiliary voltage measurement (BAVM), PCVM and SCVM can be triggered simultaneously.

The IC provides two independent reference voltages which are used with the SD-ADC blocks.

1. PCVM uses reference A.
2. BVM, AVM, and SCVM use reference B.

The resolution of the various voltage measurements is V_{x_LSB} and is defined by the LSB of the digital conversion.
x=PCVM; SCVM; AVM; BVM

The measurement time t_{VM} of the PCVM, SCVM and BVM is configurable in the measurement control register.
PCVM/SCVM uses the cell voltage measurement mode bits, while BVM uses the block/auxiliary bits.

Table 7 Voltage measurement modes

CVM_Mode/ BVM_Mode [2:0]	PCVM/BVM resolution [bit]	SCVM resolution [bit]	t_{VM} [ms]
111	14	11	t_{VM_LR}
110	16	11	4.68
101	15	11	2.34
100	14	11	1.17
011	13	11	0.59
010	12	11	0.29
001	11	11	0.15
000	10	11	0.07

Note: The resolution of AVM is 10 bit. The resolution of SCVM is 11 bit. t_{vm} of SCVM is adjusted to CVM_MODE configuration.

Setting the start bit of a measurement in the measurement control register initiates a voltage measurement. The result of the measurement is the average of the cell voltage over the measurement time and is available in the RESULT register.

The resolution of the measured value (in bit) can be configured using the measurement control register.

On completion of a measurement the device clears the corresponding start bit. For manually triggered measurements (PCVM, SCVM, BVM), the result registers are set to 0 during measurement time t_{VM} and measurement delay time t_{VM_DEL}, except in long-running mode.

In long-running mode, the result register is updated after the end of the measurement.

The result registers of the voltage measurement keep the results irrespective of internal cyclic diagnostics checks.

The configurable delay time t_{VM_del} delays the start of the cell voltage, block voltage and bipolar auxiliary voltage measurements (PCVM, SCVM, BVM and BAVM) with a resolution of $t_{VM\_del\_LSB}$.

The maximum delay time is defined by $t_{VM\_del\_max}$.

If the long-running mode is selected for PCVM and/or BVM by writing the corresponding bits in the measurement control register, the IC measures eight times in a row using the 14-bit measurement mode. If the long-running mode is selected for SCVM by writing the corresponding bits in the measurement control register, the IC performs eight times several 11-bit measurements while the measurement time t_{VM} of a 14-bit measurement. After the long running measurements are finished the PCVM result register contains the average of all 14-bit measurements while the SCVM result register contains the average value of all 11-bit measurements.

Each of those measurements starts automatically after the time $t_{restart}$, for a total measurement time t_{VM_LR} equals $t_{VM\_LR} = 8 * t_{restart}$.

The time $t_{restart}$ is defined by the configurable 6-bitfield of the operation mode register with a resolution of $t_{restart\_LSB}$ within the range of $t_{restart\_range}$.

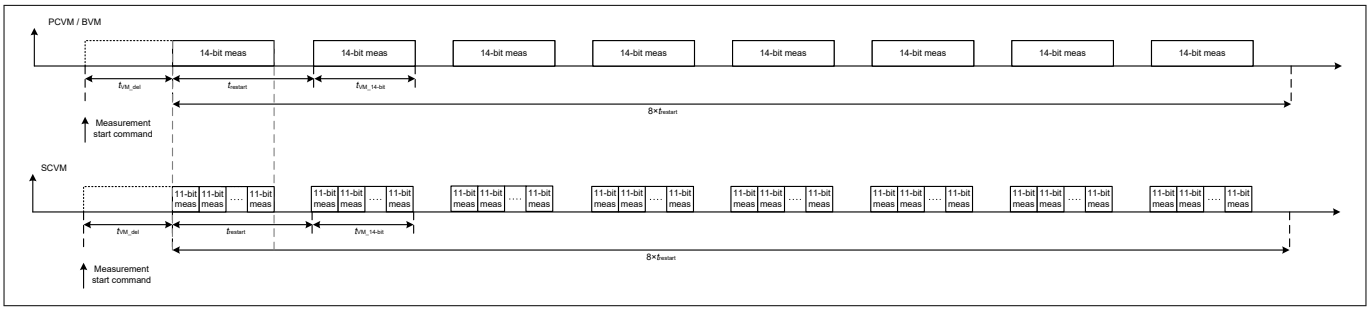

Figure 6 Voltage measurement long-running mode

7.2 Electrical characteristics measurement control (MC)

Table 8 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
MC PCVM, BAVM, AVM and BVM ADC sampling frequency	f_{s_ADC}	13.44	14	14.56	MHz	1)	PRQ-600
MC PCVM, SCVM, BAVM and BVM propagation delay within IC	t_{VM_prop}	2.75 µs - 1/BR_{GPIO}	–	3.5 µs - 1/BR_{GPIO}	s	1) Time between completion of a received measurement start command and the actual start of the measurement delay time t_{VM_del}.	PRQ-592
MC PCVM, SCVM, BAVM and BVM start delay timer resolution	$t_{VM\_del\_LSB}$	35.1	36.6	38.1	µs	1)	PRQ-593

(table continues...)

Table 8 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
MC PCVM, SCVM, BAVM and BVM start delay timer maximum interval	$t_{VM\_del\_max}$	1.09	1.13	1.18	ms	1)	PRQ-594
MC Voltage measurement time	t_{VM}	–	$2^m / f_{s\_ADC}$	–	s	1) **1.** m bits: 10 ≤ m ≤ 16 **2.** Mode: CVM_MODE; BVM_MODE **3.** Except for long-running mode	PRQ-602
Long-running mode							
MC long-running mode restart time - 1	$t_{restart\_1}$	1.13	1.17	1.22	ms	For LR_TIME = 00_H	PRQ-1919
MC long-running mode restart time - 2	$t_{restart\_2}$	1.20	1.25	1.3	ms	For LR_TIME = 01_H	PRQ-1920
MC long-running mode restart resolution	$t_{restart\_LSB}$	100.1	104.1	108.5	µs	For LR_TIME > 01_H	PRQ-1297
MC long-running restart range	$t_{restart\_range}$	1.13	–	8.03	ms	–	PRQ-1312
Full scale ranges							
MC PCVM, SCVM and comparator full-scale range	FSR_{PCVM} FSR_{SCVM} FSR_{Comp}	0	–	5	V	1)	PRQ-623
MC BVM full-scale range	FSR_{BVM}	4.75	–	60	V	1) Measured at V_{U12P} - V_{GND}	PRQ-666
MC BAVM full-scale range	FSR_{BAVM}	-2	–	2	V	–	PRQ-1387

(table continues...)

Table 8 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
MC AVM and TMP full-scale range	FSR_{AVM} FSR_{TMP}	0	–	2	V	1)	PRQ-792
Measurement resolution							
MC PCVM resolution	V_{PCVM_LSB}	–	$FSR_{PCVM}/2^m$	–	V	1) m bits: 10 ≤ m ≤ 16	PRQ-599
MC SCVM resolution	V_{SCVM_LSB}	–	$FSR_{SCVM}/2^{11}$	–	V	1)	PRQ-624
MC BVM resolution	V_{BVM_LSB}	–	$FSR_{BVM}/2^m$	–	V	1) m bits: 10 ≤ m ≤ 16	PRQ-667
MC BAVM resolution	V_{BAVM_LSB}	–	$FSR_{BAVM}/2^m$	–	V	1) m bits: 10 ≤ m ≤ 16	PRQ-1388
MC AVM resolution	V_{AVM_LSB}	–	$FSR_{AVM}/2^{10}$	–	V	1)	PRQ-682

1) Not subject to production test; verified by design or characterization.

8 Primary cell voltage measurement (PCVM)

8.1 Functional description

The primary cell voltage measurement (PCVM) unit of the IC can measure each cell voltage individually and simultaneously using the Un pins. The measured voltage is defined as V_{PCVM} = (V_{Un+1} - V_{Un}) (0 ≤ n ≤ 11) and is measured with the defined accuracy $PCVM_{ERR}$ and a relative accuracy of $PCVM_{ERR\_rel}$.

The primary cell voltage measurement is initiated by setting the PCVM_START bitfield in the MEAS_CTRL register. The primary cell voltage is calculated using: V_{PCVM} [V] = (FSR_{PCVM} / 2^{16}) × RESULT[LSB16]

The measurement is triggered by a host controller command synchronously for all cells connected to the IC. These conditions apply:

- The maximum start measurement propagation delay is t_{VM_prop}.
- The maximum PCVM time deviation between channels within one IC is Dev_{PCVM_IC}.
- The maximum PCVM time deviation across all ICs in a chain is Dev_{PCVM_chain}.
- The start of the measurement is delayed by the configurable time t_{VM_del}.
- The maximum iso UART propagation delay is $t_{isoU\_prop\_del}$.

The number of activated cells can be configured in the PART_CONFIG register. With the register minimum value 0000_H no cell is activated and with maximum value $0FFF_H$ all 12 cells are activated.

8.2 Electrical characteristics primary cell voltage measurement (PCVM)

Table 9 Electrical characteristics

V_{VS} = $V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell sense inputs							
PCVM differential input current Un	I_{Un_PCVM}	18	25	32	µA	**1.** During PCVM **2.** V_{PCVM} = 5 V **3.** This differential current flows into Un+1 and has the opposite direction on Un for the channels (0 ≤ n ≤ 12) **4.** The typical average value I_{Un_PCVM} = V_{PCVM} / 200 kΩ	PRQ-590
Input leakage current Un	I_{Un_leak}	-0.6	–	0.6	µA	**1.** 0 ≤ n ≤ 12 **2.** In sleep mode and idle mode **3.** V_{Un} ≤ 5.5 V	PRQ-591

(table continues...)

Table 9 (continued) Electrical characteristics

V_{VS} = $V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Synchronization timing							
Maximum PCVM time deviation between channels within IC	Dev_{PCVM_IC}	-0.5	–	+0.5	%	1) Deviation between t_{VM}.	PRQ-596
Maximum PCVM time deviation across ICs	Dev_{PCVM_chain}	-4	–	4	%	1)	PRQ-597
Primary cell voltage measurement							
PCVM relative accuracy initial - RT	$PCVM_{ERR\_init}$	-0.8	–	0.8	mV	2) 3) Relative accuracy over all devices against each other within the given conditions: **1.** 16-bit mode **2.** (V_{Un+1} - V_{Un}) = 4.3 V **3.** T_j = 25°C	PRQ-603
PCVM relative accuracy	$PCVM_{ERR\_rel}$	-1	–	1	mV	Relative accuracy over all devices against each other within the given conditions: **1.** 16-bit mode **2.** $\Delta(V_{Un+1} - V_{Un})$ = 600 mV within 2.5 V ≤ (V_{Un+1} - V_{Un}) ≤ 4.3 V **3.** ΔT_j = 10 K within -40°C ≤ T_j ≤ 70°C **4.** Over a period of t_0 and t_{0+x} (x ≤ 12 hours) 4)	PRQ-1848
PCVM accuracy EoL - 1	$PCVM_{ERR\_EOL\_1}$	-1.1	–	1.1	mV	5) 6) 3) **1.** 16-bit mode **2.** 2.5 V ≤ (V_{Un+1} - V_{Un}) ≤ 3.6 V **3.** T_j = 25°C	PRQ-605
PCVM accuracy EoL - 2	$PCVM_{ERR\_EOL\_2}$	-1.2	–	1.2	mV	5) 6) 3) **1.** 16-bit mode **2.** 3.6 V < (V_{Un+1} - V_{Un}) ≤ 4.3 V **3.** T_j = 25°C	PRQ-606

(table continues...)

Table 9 (continued) Electrical characteristics

V_{VS} = $V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PCVM accuracy EoL - 3	$PCVM_{ERR\_EOL\_3}$	-2.0	–	2.0	mV	5) 6) 3) **1.** 16-bit mode **2.** 1 V ≤ (V_{Un+1} - V_{Un}) ≤ 3.6 V **3.** -40°C ≤ T_j ≤ 50°C	PRQ-1360
PCVM accuracy EoL - 4	$PCVM_{ERR\_EOL\_4}$	-2.1	–	2.1	mV	5) 6) 3) **1.** 16-bit mode **2.** 3.6 V < (V_{Un+1} - V_{Un}) ≤ 4.3 V **3.** -40°C ≤ T_j ≤ 50°C	PRQ-1361
PCVM accuracy EoL - 5	$PCVM_{ERR\_EOL\_5}$	-2.6	–	2.6	mV	5) 6) 3) **1.** 16-bit mode **2.** 1 V ≤ (V_{Un+1} - V_{Un}) ≤ 3.6 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-607
PCVM accuracy EoL - 6	$PCVM_{ERR\_EOL\_6}$	-2.8	–	2.8	mV	5) 6) 3) **1.** 16-bit mode **2.** 3.6 V < (V_{Un+1} - V_{Un}) ≤ 4.3 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-608
PCVM accuracy EoL - 7	$PCVM_{ERR\_EOL\_7}$	-2.6	–	2.6	mV	5) 6) 3) **1.** 16-bit mode **2.** 0.05 V ≤ (V_{Un+1} - V_{Un}) ≤ 1 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-609
PCVM accuracy EoL - 8	$PCVM_{ERR\_EOL\_8}$	-3.5	–	3.5	mV	5) 6) 3) **1.** 16-bit mode **2.** 4.3 V < (V_{Un+1} - V_{Un}) ≤ 4.8 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-611
PCVM accuracy EoL - 9	$PCVM_{ERR\_EOL\_9}$	-2.6	–	2.6	mV	5) 6) 3) **1.** 16-bit mode **2.** 1 V < (V_{Un+1} - V_{Un}) ≤ 3.6 V **3.** -40°C ≤ T_j ≤ 70°C	PRQ-1852
PCVM accuracy EoL - 10	$PCVM_{ERR\_EOL\_10}$	-2.8	–	2.8	mV	5) 6) 3) **1.** 16-bit mode **2.** 3.6 V < (V_{Un+1} - V_{Un}) ≤ 4.3 V **3.** -40°C ≤ T_j ≤ 70°C	PRQ-1853
PCVM accuracy EoL - 10-bit	$PCVM_{ERR\_EOL\_10bit}$	-15	–	15	mV	6) 3) **1.** 10-bit mode **2.** 0.05 V ≤ (V_{Un+1} - V_{Un}) ≤ 4.8 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-612

8 Primary cell voltage measurement (PCVM)

1) Not subject to production test; verified by design or characterization.
2) Initial accuracy verified by Infineon backend.
3) With 12 cells attached and activated
4) Test condition: The IC is pre assembled on a PCB. A PCVM is started at any time t_0 within the device lifetime. The IC is in sleep mode between t_0 and t_{0+x} and RR_ERR_CNT.RR_SLEEP_CNT bitfield is 000_H.
5) Lower resolution has additional quantization error e.g. additional $PCVM_{ERR\_EOL}$ ± 2 LSB[m]; m bits: 14 ≤ m ≤ 15
Please contact Infineon for more details for other ADC resolutions.
6) End-of-Life (EoL) accuracy; according to AEC-Q100 Grade 1 Rev. H automotive qualification

9 Secondary cell voltage measurement (SCVM)

9.1 Functional description

The device includes a secondary cell voltage measurement (SCVM) unit. The measured voltage V_{SCVM} = (V_{Gn} - V_{Un}) (0 ≤ n ≤ 11) is measured with the accuracy $SCVM_{ERR\_EOL}$ and a resolution of V_{SCVM_LSB}.

The secondary cell voltage measurement is initiated by setting the SCVM_START bitfield in the MEAS_CTRL register. The secondary cell voltage is calculated using: V_{SCVM} [V] = (FSR_{SCVM} / 2^{11}) × RESULT[LSB11]

The SCVM unit can measure the voltage of at least one cell simultaneously with the primary cell voltage measurement within t_{VM_prop}. At least one cell must be enabled in the SCVM configuration register. The corresponding cells for SCVM must also be activated in the PART_CONFIG register.

Note: A binary search algorithm follows the highest and the lowest cell voltage of all cells enabled in the SCVM_CONFIG register for each sample. Within the sampling time 1/$f_{s\_SCVM\_ADC}$ both voltages are sampled once. The SCVM averages all samples of the lowest and all samples of the highest voltage over the entire measurement time.

A 2-bit update counter in each SCVM register, SCVM lowest cell voltage and SCVM highest cell voltage, indicates the availability of a new secondary cell voltage measurement.

After the measurement time, the SCVM needs additional time t_{SCVM_ave} to calculate the average results. After t_{SCVM_ave}, the value of the highest voltage measured by the SCVM is stored in the SCVM highest cell voltage register. The lowest voltage is stored in SCVM lowest cell voltage register, respectively.

Note: If a single cell is measured, then calculate the average of the two results registers to improve filtering.

9.2 Electrical characteristics secondary cell voltage measurement (SCVM)

Table 10 Electrical characteristics

V_{VS} = $V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell sensing inputs							
SCVM differential input current Gn	I_{Gn_SCVM}	–	7	10	µA	1) **1.** Average during SCVM **2.** V_{SCVM} = 5 V **3.** This differential current flows into Gn and has the opposite direction on Un for channels 0 ≤ n ≤ 11	PRQ-621
Input leakage current Gn	I_{Gn_leak}	-1.0	–	1.0	µA	**1.** 0 ≤ n ≤ 11 **2.** In sleep mode and idle mode **3.** V_{Gn} ≤ 5.5 V	PRQ-642
Synchronization timing							
SCVM to PCVM time deviation	Dev_{SCVM_PCVM}	-0.5	–	+0.5	%	Within one IC, the maximum deviation between SCVM (11-bit) time and PCVM (11-bit) time.	PRQ-622

(table continues...)

Table 10 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SCVM data averaging time	t_{SCVM_ave}	286	298	311	µs		PRQ-1390
Secondary cell voltage measurement							
SCVM ADC sampling frequency	$f_{s\_SCVM\_ADC}$	–	f_{s_ADC} / 64	–	MHz	2)	PRQ-625
SCVM accuracy EoL - limited range	$SCVM_{ERR\_EOL\_1}$	-19	–	19	mV	3) **1.** 2.7 V ≤ (V_{Gn} - V_{Un}) ≤ 4.3 V **2.** -40°C ≤ T_j ≤ 50°C	PRQ-626
SCVM accuracy EoL	$SCVM_{ERR\_EOL\_2}$	-28	–	28	mV	3) **1.** 1 V ≤ (V_{Gn} - V_{Un}) ≤ 4.8 V **2.** -40°C ≤ T_j ≤ 150°C	PRQ-627
Maximum deviation between PCVM and SCVM	$\Delta_{PCVM\_vs\_SCVM}$	-25	–	25	mV	1 V ≤ (V_{Un+1} - V_{Un}) ≤ 4.8 V	PRQ-1305
Analog undervoltage and overvoltage comparators							
Comparator resolution	$FSRV_{Comp\_LSB}$	–	FSR_{Comp} / 2^{10}	–	V	2)	PRQ-629
Comparator accuracy - limited range	$COMP_{ERR\_1}$	-30	–	30	mV	**1.** (V_{Gn} - V_{Un}) = 3.6 V **2.** -40°C ≤ T_j ≤ 25°C	PRQ-1300
Comparator accuracy	$COMP_{ERR\_2}$	-50	–	50	mV	**1.** 1 V < (V_{Gn} - V_{Un}) < 4.7 V **2.** -40°C < T_j < 150°C	PRQ-630
Comparator sampling frequency	f_{COMP}	1	–	–	MHz	2)	PRQ-632
Comparator checking time	t_{comp}	–	2^{10} / f_{s_ADC}	–	µs	2)	PRQ-635

1) Not subject to production test; verified by design or characterization.
2) Not subject to production test; verified by design or characterization.
3) End-of-Life accuracy; according to AEC-Q100 Grade 1 Rev. H automotive qualification

10 Block voltage measurement (BVM)

10.1 Functional description

The IC can measure the sum total voltage of all the cells connected to the device using separate pins, called block voltage. The block voltage $V_{BVM} = (V_{U12P} - V_{GND})$ is measured with the accuracy BVM_{ERR_EOL} and a configurable resolution of V_{BVM_LSB}.

The block voltage measurement is initiated by setting the BVM_START bitfield in the MEAS_CTRL register. The block voltage is calculated: V_{BVM} [V] = (FSR_{BVM} / 2^{16}) × RESULT_BVM [LSB16]

10.2 Electrical characteristics block voltage measurement (BVM)

Table 11 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cell sense inputs							
BVM input current U12P	I_{U12P_BVM}	–	280	400	µA	1) During BVM	PRQ-664
Block voltage measurement							
Maximum BVM to PCVM time deviation within IC	$Dev_{BVM\_PCVM\_IC}$	-0.5	–	+0.5	%	2) Deviation between BVM t_{VM} and PCVM t_{VM} with the same resolution setting.	PRQ-670
Maximum BVM time deviation across ICs	Dev_{BVM_chain}	-4	–	4	%	2) Deviation between BVM t_{VM} over all ICs with the same resolution setting.	PRQ-671
BVM accuracy EoL - 1	$BVM_{ERR\_EOL\_1}$	-50	–	50	mV	3) **1.** 14-bit to 16-bit mode **2.** 4.75 V ≤ V_{BVM} ≤ 51.6 V **3.** -40°C ≤ T_j ≤ 70°C	PRQ-1850
BVM accuracy EoL - 2	$BVM_{ERR\_EOL\_2}$	-55	–	55	mV	3) **1.** 14-bit to 16-bit mode **2.** 4.75 V ≤ V_{BVM} ≤ 60 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-672
BVM accuracy EoL - 10 Bit	BVM_{ERR_10Bit}	-250	–	110	mV	1) 3) **1.** 10-bit mode **2.** 4.75 V ≤ V_{BVM} ≤ 60 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-673

(table continues...)

Table 11 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
BVM versus sum of PCVM relative accuracy EoL	$BVM_{ERR\_vs\_PCVM}$	$\frac{BVM_{ERR\_EOL\_2\_min}+1}{2} \times PCVM_{ERR\_EOL\_6\_min}$	–	$\frac{BVM_{ERR\_EOL\_2\_max}+1}{2} \times PCVM_{ERR\_EOL\_6\_max}$	mV	14-bit to 16-bit mode	PRQ-676
Relative ADC error margin - sum of PCVM versus BVM EoL	$ERR_{PCVM\_BVM\_10bit}$	-78	–	78	mV	**1.** 10-bit mode **2.** -40°C ≤ T_j ≤ 150°C **3.** 1 V ≤ (V_{Un+1} - V_{Un}) ≤ 4.8 V **4.** Plausibility check as part of the round robin scheme	PRQ-1851

1) Not subject to production test; verified by design or characterization.
2) Not subject to production test; verified by design or characterization.
3) End-of-Life accuracy; according to AEC-Q100 Grade 1 Rev. H automotive qualification

11 Auxiliary voltage measurement (AVM)

11.1 Functional description

The IC also provides the possibility to measure other voltages, called auxiliary voltage measurement. The auxiliary voltage $V_{AVMz} = (V_{TMPz} - V_{TMP\_GND})$, $(0 \le z \le 4)$ is measured with the accuracy AVM_{ERR_EOL} and a resolution of V_{AVM_LSB}.

The auxiliary voltage measurement is initiated by setting the AVM_START bitfield in the MEAS_CTRL register. The auxiliary voltage is calculated using: V_{AVMz} [V] = (FSR_{AVM} / 2^{10}) × RESULT [LSB10]

Additional to the unipolar AVM the device can be configured to measure a bipolar voltage applied on the TMP3 and TMP4 pins instead. The voltage $V_{BAVM} = (V_{TMP4} - V_{TMP3})$ is measured with the accuracy $BAVM_{ERR\_EOL}$ and a configurable resolution of V_{BAVM_LSB}.

The BAVM measurement is enabled by setting the AVM_CONFIG.AUX_BIPOLAR bitfield, the resolution is set by the MEAS_CTRL.BVM_MODE and the measurement is triggered by the MEAS_CTRL.BVM_START bit. The BAVM measurement result is stored in the BVM result register.

The bipolar voltage is calculated using: V_{BAVM} = (BVM.RESULT[signed LSB15] × 2 V) / 2^{15}[LSB15]

Note: Either BVM or BAVM can be performed synchronized to the PCVM/SCVM.

All external temperature measurement channels can be selected to be measured by the AVM function:

To measure an auxiliary voltage using a TMP channel, the temperature measurement function must be disabled in the temperature measurement configuration register. Since only one auxiliary voltage can be measured at a time, the configured auxiliary channels are measured sequentially.

11.2 Electrical characteristics auxiliary voltage measurement (AVM)

Table 12 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
AVM accuracy EoL	AVM_{ERR_EOL}	-10	–	10	mV	1) **1.** 10-bit mode **2.** 0.1 V ≤ V_{AVMy} ≤ 1.95 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-684
BAVM accuracy EoL	$BAVM_{ERR\_EOL}$	-3.3	–	3.3	mV	1) **1.** 14-bit to 16-bit mode **2.** -2 V ≤ VTMP3/4 ≤ 2 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-1389
BAVM accuracy EoL - long-running mode	$BAVM_{ERR\_EOL\_LR}$	$BAVM_{ERR\_EOL}$ - 14.7	–	$BAVM_{ERR\_EOL}$ + 14.7	mV	**1.** Long-running mode **2.** -2 V ≤ $V_{TMP3/4}$ ≤ 2 V **3.** -40°C ≤ T_j ≤ 150°C	PRQ-1829

1) End-of-Life accuracy; according to AEC-Q100 Grade 1 Rev. H automotive qualification

12 Temperature measurement unit (TMP)

12.1 Functional description

The temperature measurement unit provides the possibility to measure up to five external temperature NTCs as well as two internal temperature sensors and provides the results in the corresponding temperature registers.

A valid bit, which is cleared after readout, indicates a new measurement result in both cases.

The NTCs are measured with an accuracy of NTC_{ERR} whilst the internal sensor accuracy is defined by $T_{ERR\_int\_abs}$.

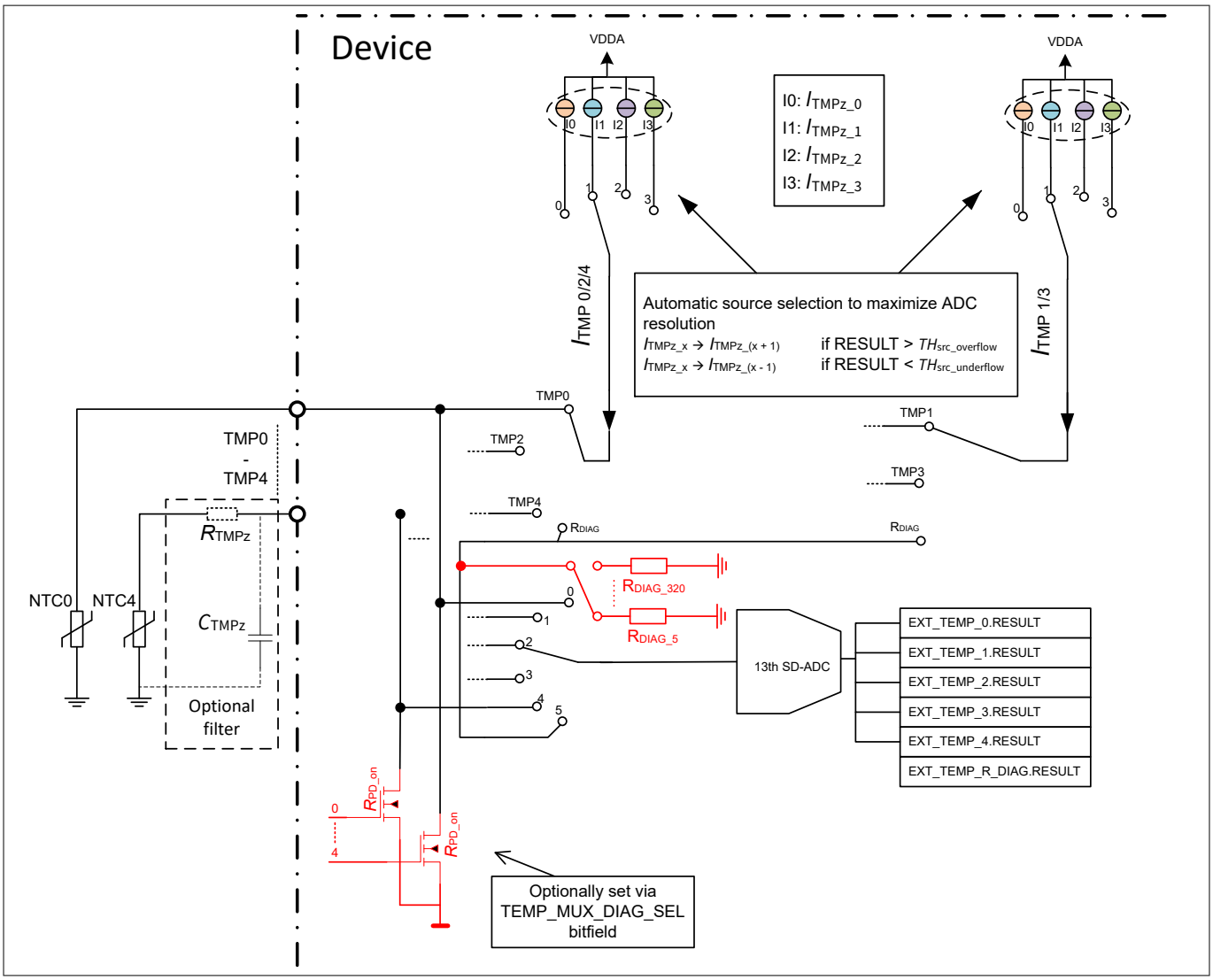

Figure 7 External temperature measurement

If not all provided measurement channels are needed, unused channels must be deactivated in the temperature configuration register.

Note: The TMP channels must be connected in consecutive order starting with TMP0. Deactivated channels can be used as AVM inputs.

The internal temperature measurement as well as the measurement of the selected NTC channels are triggered via the internal round robin. Within three round robin cycles all NTCs are updated.

Note: The first round robin after wake-up does not measure any NTC.

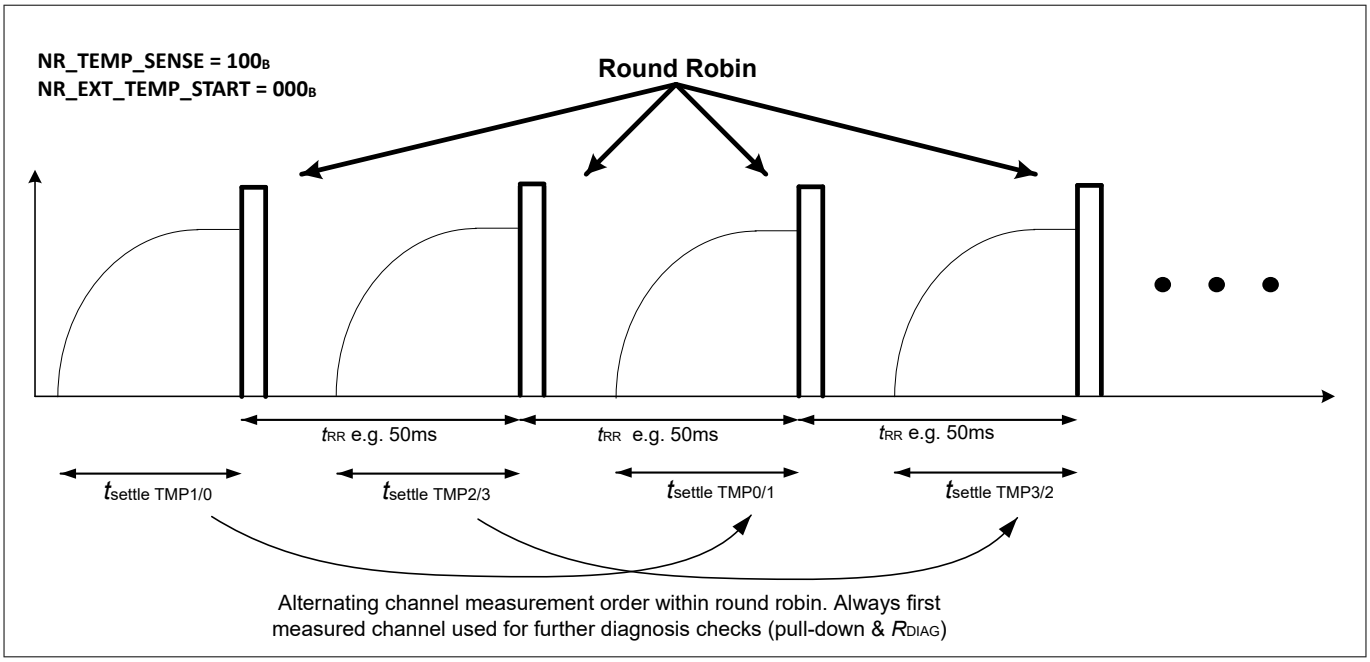

Figure 8 TMP triggering

To measure an external NTC, the device provides four selectable internal current sources I_{TMPz_x} ($0 \le z \le 4$, $0 \le x \le 3$). The device automatically identifies which one of the four sources is the best one to use in the next round robin for each NTC channel individually by using the overflow and underflow thresholds $TH_{Src\_overflow}$ and $TH_{Src\_underflow}$.

Current source I_{TMPz_1} is selected first. If, for example, an overflow is detected, the next lower source is selected. A valid result is available (or NTC short/open is detected) after maximum three round robin cycles per activated NTC channel.

Note: The source is activated prior to the measurement. The time is defined by t_{settle}.

For every TMP channel, a result register is available. The results register contains the following information:

- The result of the measurement.
- The used current source.
- The valid bit is set to indicate a new measurement. Reading the result clears the valid bit.
- Whether the pull-down of this channel was activated.
- Whether a pull-down error occurred.

The NTC resistor value is calculated by using the voltage measurement result and the selected current source.

R_{NTC} [Ω] = (EXT_TEMP_z.RESULT [LSB10] × FSR_{TMP} [V] × $4^{EXT\_TEMP\_z.INTC}$) / (2^{10} × 320 µA) - R_{TMP}; INTC = 0 to 3 (used current source).

To check if the temperature measurement unit works correctly the IC performs internal diagnostics checks as part of the round robin:

1. It measures an internal diagnostics resistor R_{DIAG} with the current source I_{TMPz_x} ($0 \le x \le 3$, $0 \le z \le 4$) used for TMPz.
2. It activates the pull down switch of the selected TMP channel after the measurement and it measures the channel again. The measured value is then compared with the expected value R_{PD_ON}. An open wire or increased resistance value can be detected and is indicated by setting the GEN_DIAG.EXT_T_ERR (external temperature error).

Note: Only one TMP channel is checked per RR cycle (channel that was measured first during RR). The pull down resistor can be activated by setting the corresponding bits in the auxiliary voltage measurement configuration register

The device checks whether an overtemperature condition at the NTC exists by comparing the voltage measurement result against the external overtemperature threshold.

The 10-bit overtemperature threshold is configurable with a resolution of V_{TMP_LSB} using the external overtemperature threshold bits of the temperature measurement configuration register TEMP_CONF.EXT_OT_THR.

Note: In order to ensure the detection of an external overtemperature, the overtemperature threshold must be defined within the range of 250 to 800 (LSB10).

The device additionally checks if an overtemperature condition on at least one of the internal temperature sensors exists by comparing the measurement result against internal overtemperature threshold which is valid for both sensors.

The 10-bit overtemperature threshold is configurable with a resolution of T_{int_LSB} using the internal overtemperature threshold bits of the internal temperature measurement configuration register INT_OT_WARN_CONF.INT_OT_THR (recommended value: T_j = 150°C).

If the overtemperature threshold is reached, the device disables the balancing function and sets the internal overtemperature warning flag.

The junction temperature T_j can be calculated using the formula: Temperature [°C] = -T_{int_LSB} × INT_TEMP_x.RESULT + 547.3, (1 ≤ x ≤ 2)

12.2 Electrical characteristics temperature measurement (TMP)

Table 13 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Internal temperature sensor							
TMP internal temperature resolution	T_{int_LSB}	–	0.6624	–	K	1)	PRQ-787
TMP internal temperature accuracy EoL absolute	$T_{ERR\_int\_abs}$	-10	–	10	°C	–	PRQ-788
External temperature sensors							
TMP measurement resolution	V_{TMP_LSB}	–	$FSR_{TMP}/2^{10}$	–	V	–	PRQ-1303
TMP measurement accuracy - 1	TMP_{ERR_1}	-2	–	2	%	Accuracy of measured NTC resistance value in the range of 1.22 kΩ to 390 kΩ	PRQ-789
TMP measurement accuracy - 2	TMP_{ERR_2}	-4.2	–	4.2	%	Accuracy of measured NTC resistance value in the range of 610 Ω to 1.22 kΩ	PRQ-790
TMP measurement accuracy - 3	TMP_{ERR_3}	-6.2	–	6.2	%	Accuracy of measured NTC resistance value in the range of 400 Ω to 610 Ω	PRQ-791

(table continues...)

Table 13 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TMP pull-down switch on-state resistance	R_{PD_on}	–	–	400	Ω	–	PRQ-797
TMP source selection overflow threshold	$TH_{src\_overflow}$	–	1000	–	LSB10	1)	PRQ-803
TMP source selection underflow threshold	$TH_{src\_underflow}$	–	200	–	LSB10	1)	PRQ-804
TMP current source activation before RR starts	t_{settle}	38.4	40	41.8 + t_{vm}	ms	1) $t_{RR} > t_{settle}$	PRQ-777
TMP measurement current source 3	I_{TMPz_3}	4.5	5	5.5	µA	**1.** 0 ≤ z ≤ 4 **2.** Within FSR_{TMP}	PRQ-868
TMP measurement current source 2	I_{TMPz_2}	19.0	20	21.1	µA	**1.** 0 ≤ z ≤ 4 **2.** Within FSR_{TMP}	PRQ-869
TMP measurement current source 1	I_{TMPz_1}	75.9	80	84.1	µA	**1.** 0 ≤ z ≤ 4 **2.** Within FSR_{TMP}	PRQ-870
TMP measurement current source 0	I_{TMPz_0}	304.0	320	336.0	µA	**1.** 0 ≤ z ≤ 4 **2.** Within FSR_{TMP}	PRQ-871
TMP internal diagnostics resistor source 0_320uA	R_{DIAG_320}	3.825	5.1	6.375	kΩ	–	PRQ-799

(table continues...)

Table 13 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
TMP internal diagnostics resistor source 1_80uA	R_{DIAG_80}	8.4	11.2	14	kΩ	–	PRQ-800
TMP internal diagnostics resistor source 2_20uA	R_{DIAG_20}	19.875	26.5	33.125	kΩ	–	PRQ-801
TMP internal diagnostics resistor source 3_5uA	R_{DIAG_5}	46.5	62	77.5	kΩ	–	PRQ-802

1) Not subject to production test; verified by design or characterization.

13 Cell balancing (CB)

13.1 Functional description

The IC supports balancing of each cell in the cell stack individually in any combination including all channels in parallel with a balancing current per cell of I_{BAL}.

Overview of balancing current for one cell:

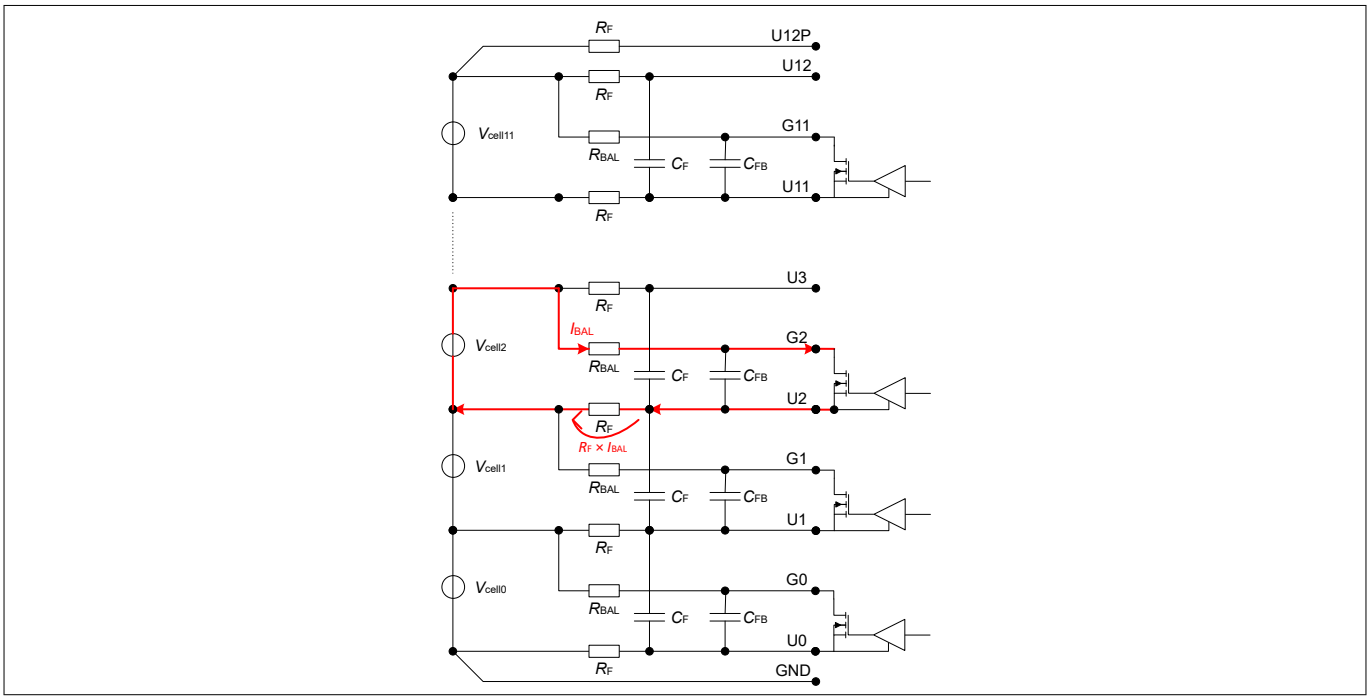

Figure 9 Passive balancing

To activate cell balancing, the respective bit in the balancing settings register can bet set for each cell individually.

If the PBOFF bit in the measurement control register is set, then the IC pauses balancing automatically. The balancing is paused for the duration of a PCVM/SCVM/BVM measurement ($t_{VM} + t_{VM\_del}$) so that the cell voltage measurement is not corrupted by any ongoing balancing.

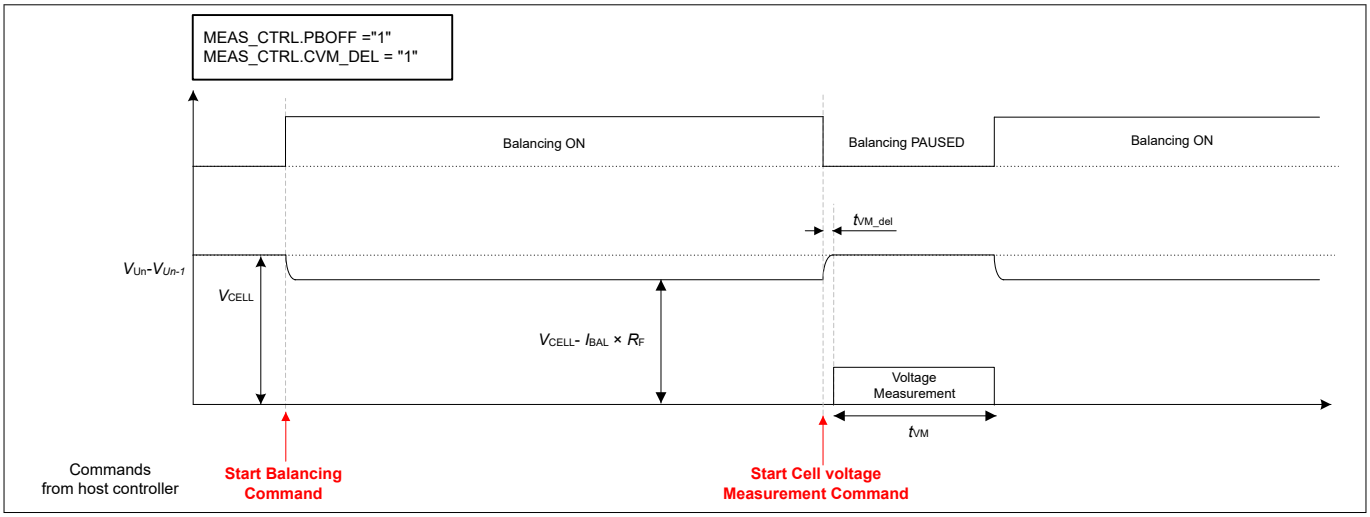

Figure 10 Balancing and cell voltage measurement

The IC can balance each cell for an individual period of time, without necessary periodic WDOG communication.

The individual time t_{BAL} is compared to the balancing counter. t_{BAL} is defined by $t_{BAL\_OFFn\_LSB}$ with a maximum interval defined by $t_{BAL\_OFFn\_max}$. The balancing of each cell is active until the balancing counter reaches the cell individual threshold.

If the extended watchdog function is enabled and a write command to the communication watchdog register is performed, then the balancing timer counter starts. The device deactivates time goal balancing as soon as the counter reaches the individual threshold t_{BAL}.

The IC supports a PWM balancing function with the period of t_{RR} and a PWM step size of $t_{BAL\_PWM\_LSB}$. The function can be configured via the communication interfaces by the host controller. If balancing for one or more cells is activated, then the device activates the balancing switch during the on-time of the PWM and deactivates it during the off-time of the PWM. Other functions such as the voltage measurement and round robin task can overrule the PWM balancing function.

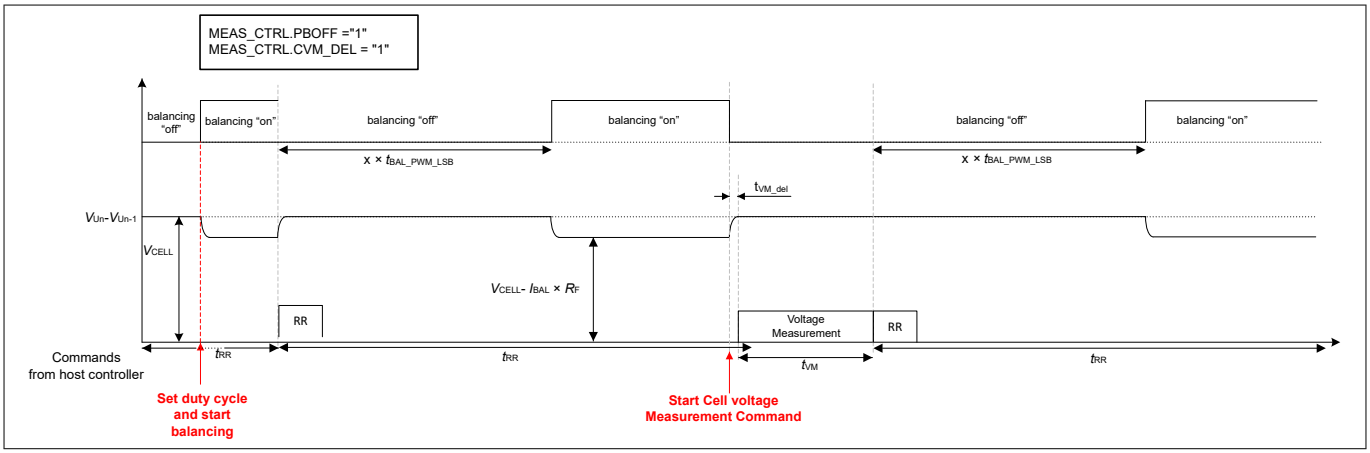

Figure 11 PWM balancing function

Balancing is available in PCVM/SCVM long-running mode. If the PBOFF bit is set, then the device pauses cell balancing during the delay time of the measurement and during the measurement itself.

Note: Only if $t_{vm\_del} + t_{vm\_14bit} < t_{restart}$.

In addition to the internal passive balancing function, the IC also supports the use of an external passive balancing device. It is recommended to connect a PMOS logic level type device to the corresponding Gn pin as an external balancing device.

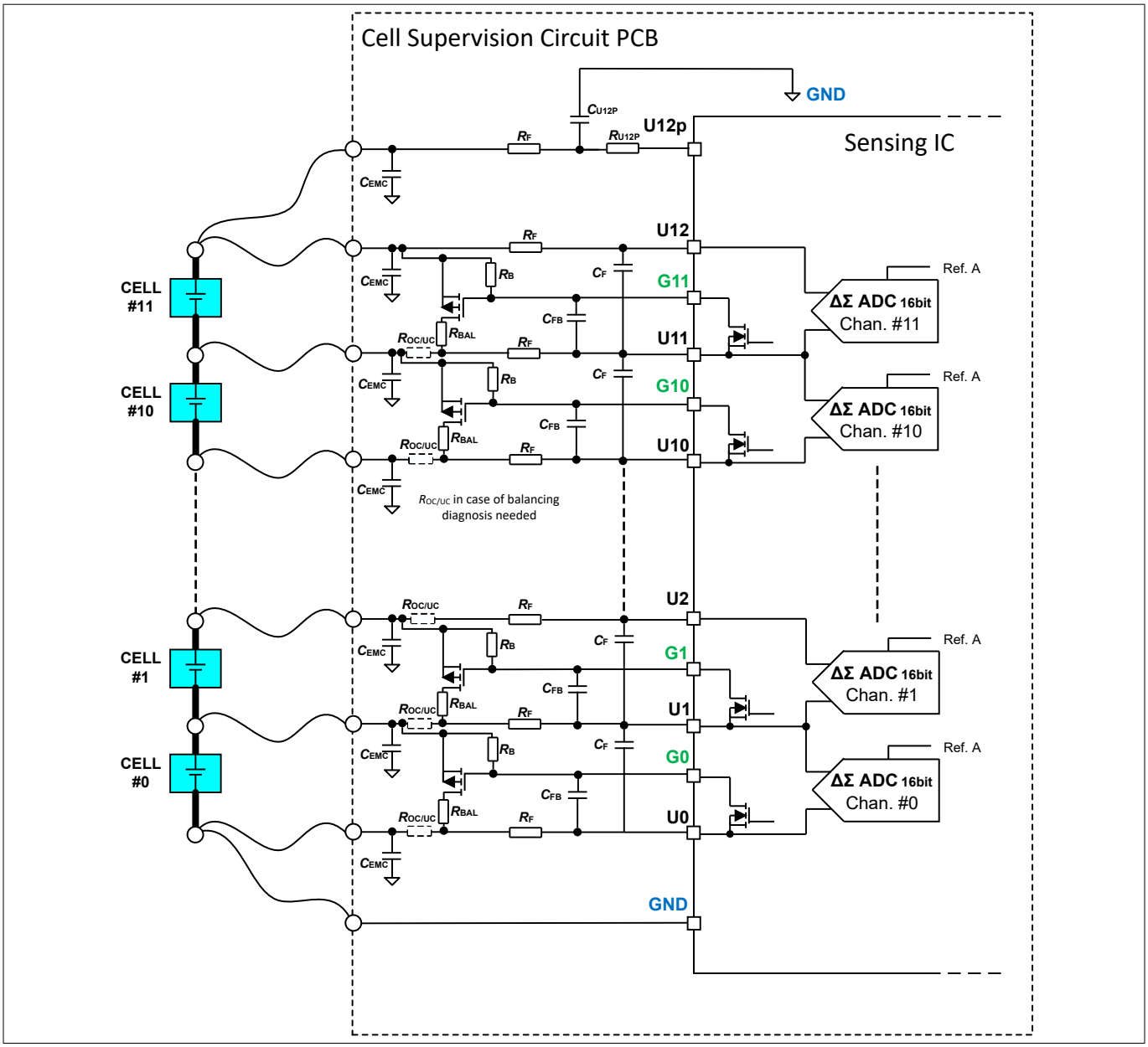

Figure 12 External balancing device

The IC supports overcurrent and undercurrent diagnostics for the external balancing device, using an additional resistor $R_{OC/UC}$.

Note: For the calculation of the overcurrent and undercurrent thresholds the voltage drop $I_{BAL} \times R_{OC/UC}$ is used.

13.2 Electrical characteristics cell balancing (CB)

Table 14 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CB balancing switch on-state resistance - 1	$R_{BAL\_on\_1}$	1.5	2.6	5.0	Ω	**1.** 1 V ≤ (V_{Un+1} - V_{Un}) ≤ 5 V **2.** I_{BAL} ≤ 150 mA	PRQ-643
CB balancing switch on-state resistance - 2	$R_{BAL\_on\_2}$	1.6	2.8	5.6	Ω	**1.** 1 V ≤ (V_{Un+1} - V_{Un}) ≤ 5 V **2.** 150 mA < I_{BAL} ≤ 200 mA	PRQ-1849
CB balancing current	I_{BAL}	–	–	200	mA	1 V ≤ (V_{Un+1} - V_{Un}) ≤ 5 V	PRQ-645
Passive balancing timer							
CB Individual balancing time interval step	$t_{BAL\_OFFn\_LSB}$	7.24	7.54	7.85	min	**1.** 1 ≤ n ≤ 12 **2.** EXT_WD = 1	PRQ-647
CB Individual balancing timer maximum interval	$t_{BAL\_OFFn\_max}$	3.74	3.9	4.06	h	**1.** 1 ≤ n ≤ 12 **2.** EXT_WD = 1, no WDOG timeout **3.** 5-bit counter	PRQ-648
PWM balancing							
CB balancing PWM step size	$t_{BAL\_PWM\_LSB}$	–	t_{RR} / 8	–	ms	1)	PRQ-1363

1) Not subject to production test; verified by design or characterization.

14 Cell diagnostics (CD)

14.1 Functional description

The IC provides automatic open wire and open load detection for each wire connected to a cell. The device performs the detection by a voltage measurement while sinking the current I_{OL_DIAG} into the balancing pin during a round robin cycle. It checks the odd channels in the first cycle and the even channels in the subsequent cycle.

If the delta voltage ((V_{Un+1} - V_{Un}) before OL compared to (V_{Un+1} - V_{Un}) during OL) is not between the minimum and maximum open load threshold, then a failure is detected. The open wire and open load-detection threshold can be configured with a resolution of OL_{thr_LSB} until the maximum threshold of OL_{thr_max} is reached using the cell voltage thresholds register.

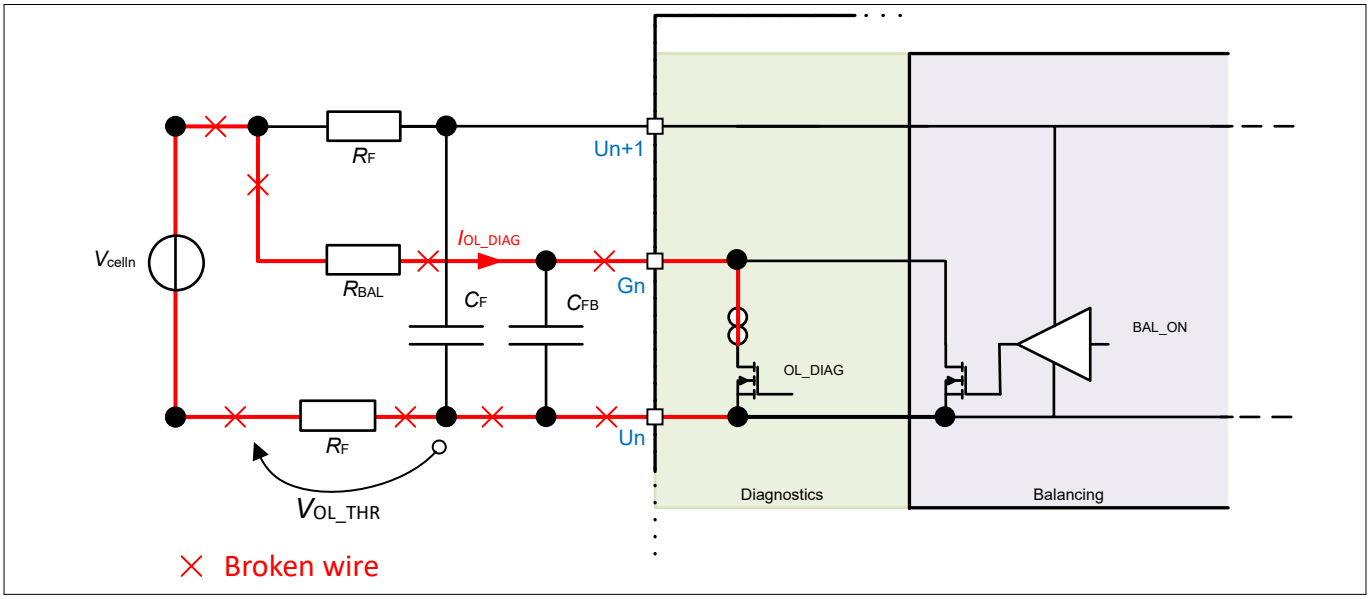

Figure 13 Open wire and open load diagnostics detection schematic

If the device detects an open wire or open load, then it indicates it in the corresponding bitfield of the diagnostics open load register as well as in the open load error bit of the general diagnostic register.

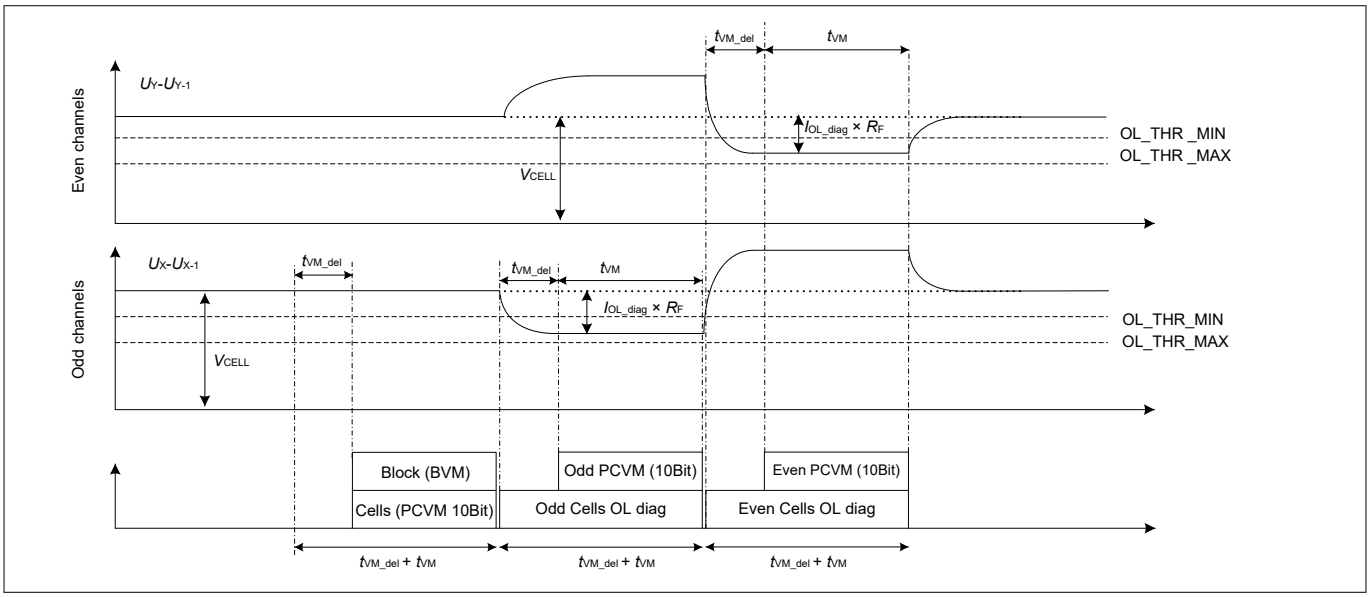

Figure 14 Open wire and open load diagnostics detection process

For OL_THR_MIN=0, no OL error is detected if the cell voltage is not decreased during activated OL current.

For OL_THR_MAX=0, no OL error is detected if the cell voltage is decreased more than the value in the OL_THR_MAX register.

As part of the round robin the device performs a balancing overcurrent and an undercurrent check for each cell for which the balancing function is active. The overcurrent threshold OC_{thr} and the undercurrent threshold UC_{thr} is configurable with a resolution of CD_{thr_LSB} until the maximum threshold of OC_{thr_max} or UC_{thr_max} respectively is reached using the balancing current threshold register.

If the device detects an balancing overcurrent or balancing undercurrent error, then it deactivates balancing. It reports error details in the BAL_DIAG_OC/BAL_DIAG_UC result register and summarized in the GEN_DIAG.BAL_ERR_OC/BAL_ERR_UC bitfields.

By setting the configuration bit OP_MODE.I_DIAG_EN, the device discharges all configured channels with the diagnostics current I_{OL_DIAG} regardless of the BAL_SETTINGS register and independent of round robin.

14.2 Electrical characteristics cell diagnostics (CD)

Table 15 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Open load							
CD sink current for open load detection	I_{OL_DIAG}	10	15	18.3	mA	0.75 V < (V_{Gn} - V_{Un}) < 5 V	PRQ-650
CD open load threshold resolution	OL_{thr_LSB}	–	19.5	–	mV	1)	PRQ-652
CD open load threshold maximum value	OL_{thr_max}	–	1.23	–	V	1)	PRQ-651
Overcurrent & undercurrent							
CD balancing overcurrent or undercurrent error threshold resolution	CD_{thr_LSB}	–	19.5	–	mV	1)	PRQ-655
CD maximum balancing overcurrent error threshold	OC_{thr_max}	–	4.98	–	V	1) 1. OC_thr = overcurrent threshold 2. I_{OC_thr} = OC_THR [V] / R_F	PRQ-653

(table continues...)

Table 15 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CD maximum balancing undercurrent error threshold	UC_{thr_max}	–	4.98	–	V	1) **1.** UC_thr = undercurrent threshold **2.** I_{UC_thr} = UC_THR [V] / R_F	PRQ-654
CD balancing overcurrent detection time	$t_{BAL\_OC\_DET}$	–	–	t_{RR_max}	ms	1) Equivalent to maximum round robin cycle time if the error counter is disabled (which is the default value, M_NR_ERR_BAL_OC = 1)	PRQ-646

1) Not subject to production test; verified by design or characterization.

15 General-purpose input/output (GPIO/PWM)

15.1 Functional description

The device provides individual GPIOq/PWMp (0 ≤ q ≤ 1, 0 ≤ p ≤ 1) pins which can be used for digital input or digital output.

After receiving a wake-up signal via iso UART, GPIOq can be used as GPIOs. A wake-up signal via UART sets the GPIOq pins to act as interface pins.

PWMp can be used as GPIO or be configured to act as PWM unit.

PWMp can be configured to act as PWM outputs using the GPIO register.

The period T_{PWM} and the duty cycle D_{PWM} can be configured with their respective resolution T_{PWM_LSB} and D_{PWM_LSB}.

15.2 Electrical characteristics general-purpose input/output (GPIO/PWM)

Table 16 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GPIO/PWM period resolution	T_{PWM_LSB}	–	2	–	µs	Bitfield with 5 bits.	PRQ-1338
GPIO/PWM duty cycle resolution	D_{PWM_LSB}	–	3.57	–	%	**1.** Bitfield with 5 bits. **2.** 100% DC = 11100_B	PRQ-1339
GPIO/PWM input "low" level	V_{GPIOq_low} V_{PWMp_low}	0	–	V_{VIO} × 0.3	V	**1.** 0 ≤ q ≤ 1 **2.** 0 ≤ p ≤ 1	PRQ-1393
GPIO/PWM input "high" level	V_{GPIOq_high} V_{PWMp_high}	V_{VIO} × 0.7	–	V_{VIO}	V	**1.** 0 ≤ q ≤ 1 **2.** 0 ≤ p ≤ 1	PRQ-825
GPIO/PWM output "low" level	V_{GPIOq_low} V_{PWMp_low}	0	–	0.45	V	**1.** I_{GPIO} ≤ 5 mA **2.** 0 ≤ q ≤ 1 **3.** 0 ≤ p ≤ 1	PRQ-826
GPIO/PWM output high level	V_{GPIOq_high} V_{PWMp_high}	V_{VIO} - 0.45	–	V_{VIO}	V	**1.** I_{GPIO} ≥ -5 mA **2.** 0 ≤ q ≤ 1 **3.** 0 ≤ p ≤ 1	PRQ-827
GPIO/PWM output current	I_{GPIOq} I_{PWMp}	-5	–	5	mA	**1.** Current capability of GPIO/PWM output **2.** 0 ≤ q ≤ 1 **3.** 0 ≤ p ≤ 1	PRQ-829

(table continues...)

Table 16 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
External capacitance on GPIOq/ PWMp	C_{GPIOq} C_{PWMp}	–	–	30	pF	1) **1.** $0 \le q \le 1$ **2.** $0 \le p \le 1$	PRQ-830

1) Not subject to production test; verified by design or characterization.

16 Communication

16.1 Functional description

The device supports the following communication interfaces.

1. UART
2. iso UART

iso UART communications allows to stack multiple devices.

The device can be used in different configurations:

- Direct connection via UART, for low voltage applications
- Primary on bottom (PoB) communication with EMM function
- Primary on top (PoT) communication with EMM function
- Ring communication with EMM function

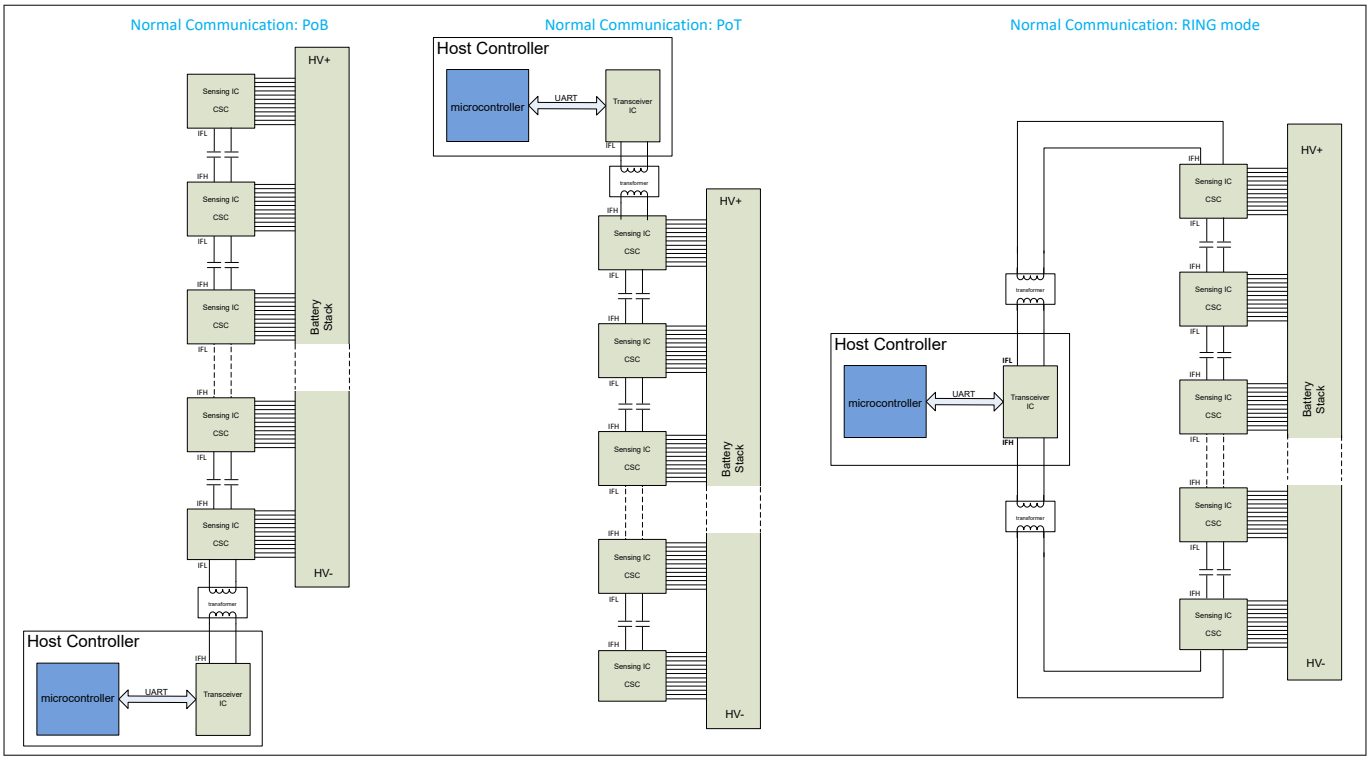

Figure 15 Communication configurations

The IC communication direction is determined during a wake-up cycle. The device configures the iso UART interface or the UART interface, which receives the wake-up pattern, as RX. The device configures the other interface as TX. To change the direction and consequently the pins, the device must be put to sleep and woken up again.

There is a reply delay t_{reply_delay}, which determines the time between the last stop bit of the read/write command (incoming command from the primary) and the first falling edge of the reply frame from the secondary.

The device forwards a received message to the next device in the system. The time between receiving and forwarding the message depends upon the receiving interface:

- Receiving on UART and forwarding on iso UART: $t_{UART\_isoU\_del}$
- Receiving on iso UART and forwarding on iso UART: $t_{isoU\_prop\_del}$
- Receiving on iso UART and forwarding on UART: $t_{UART\_isoU\_del}$

16 Communication

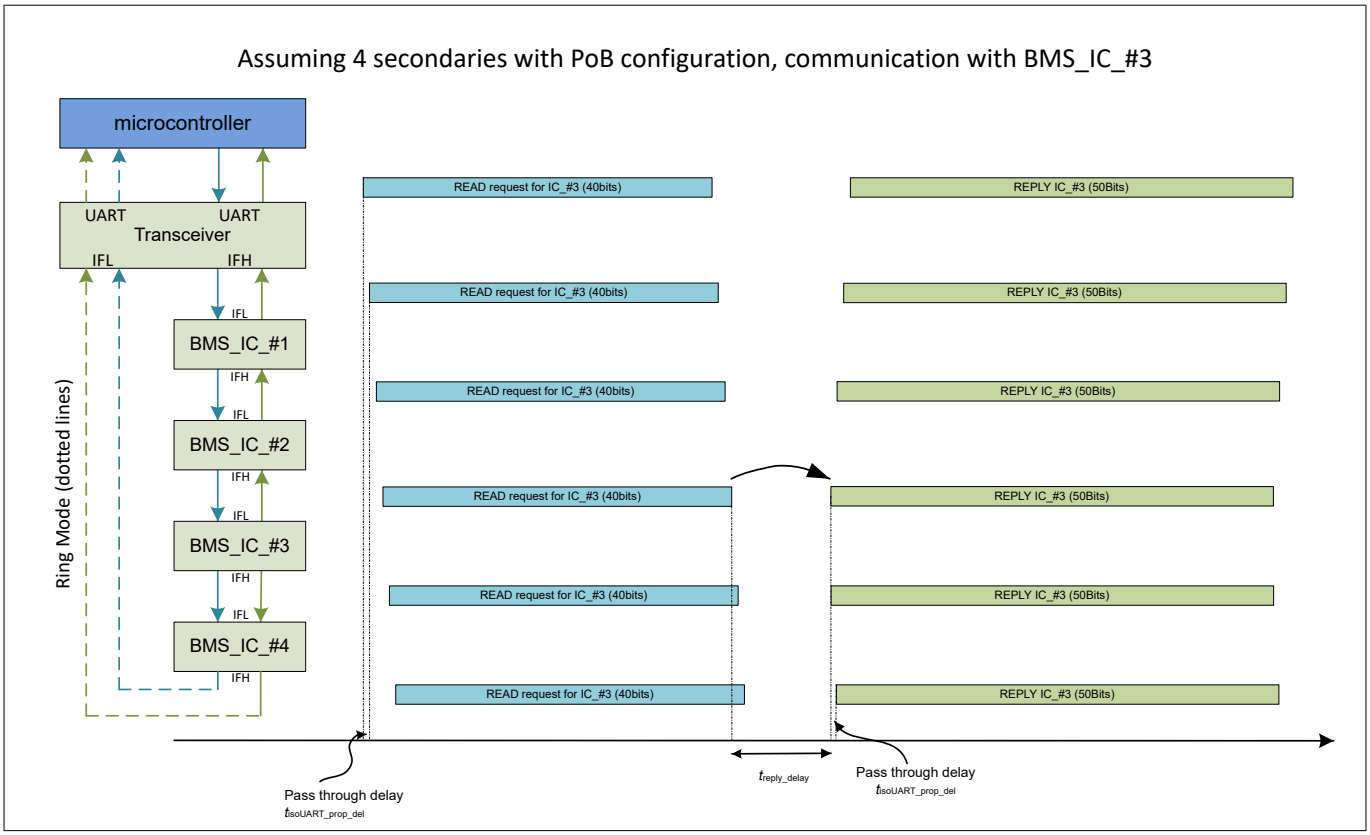

Figure 16 Communication propagation delays

iso UART waveform specification

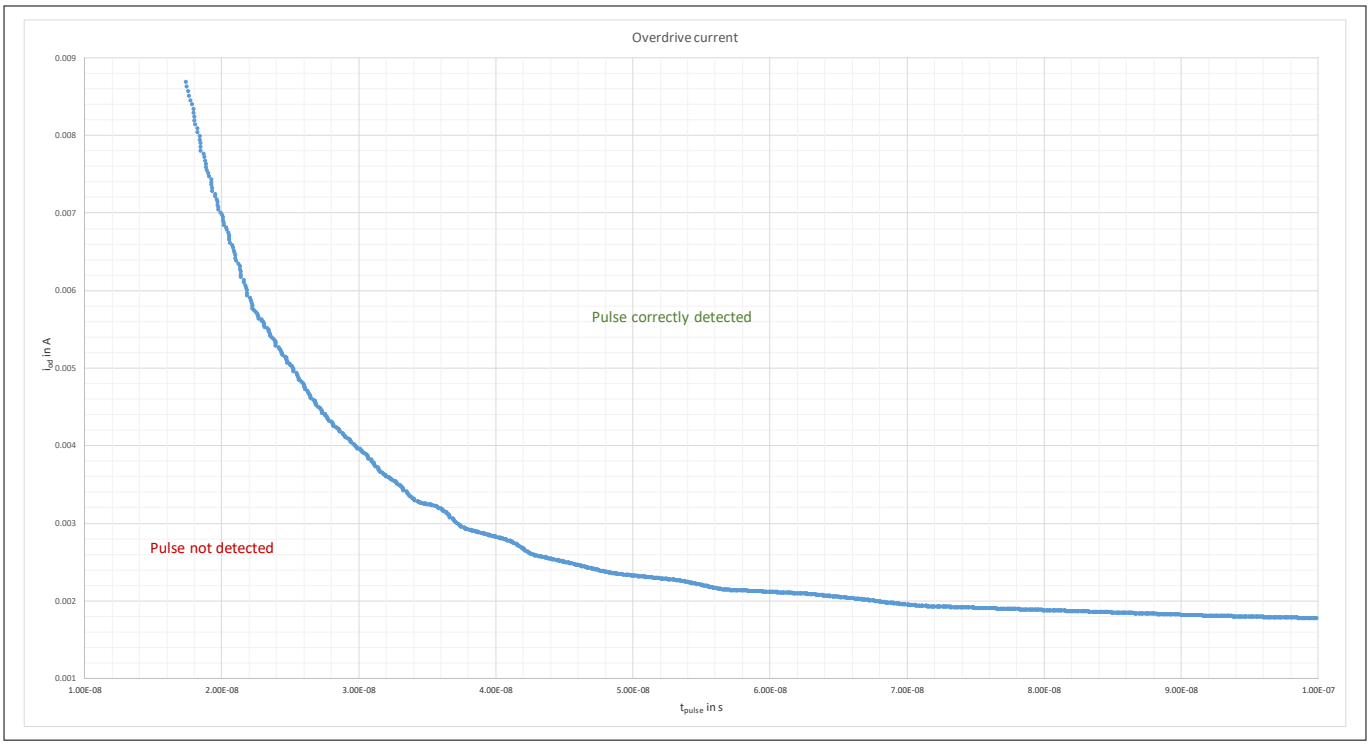

Figure 17 iso UART waveform specification

16.1.1 Register write modes

There are the following approaches for writing content into the device:

- Direct write: Writes a single register in a single device.
- Broadcast write: Writes a single register in all devices in the same stack with one write command.

With broadcast write, each device of the chain first writes data. On successful write it switches its RX and TX units to allow the reply frame to be transferred. The last device in the chain (final node) initiates the reply frame and the device switch their RX and TX units back to their initial state.

16.1.2 Communication frames

UART and iso UART communication consists of sending or retrieving sets of frames. A frame consists of 8 bits preceded by a start bit and followed by a stop bit.

The following frames are available:

- Synchronization frame
- ID frame
- Address frame
- Data frames
- CRC frame
- Reply frame

Note: Frames start with the most significant bit (MSB).

Synchronization frame

The communication is always initiated by sending a fixed synchronization frame.

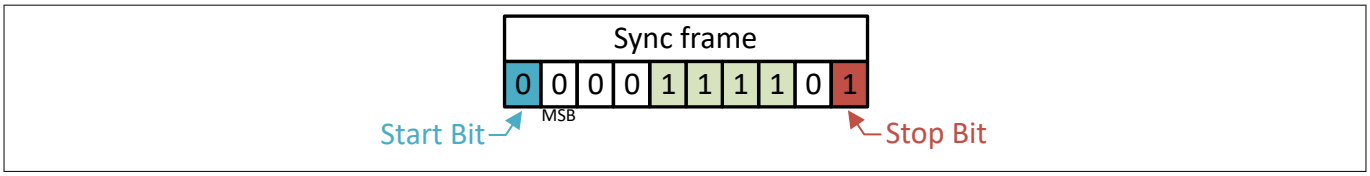

Figure 18 Synchronization frame

ID frame

The ID frame defines, which device receives the message. It also determines the type of command.

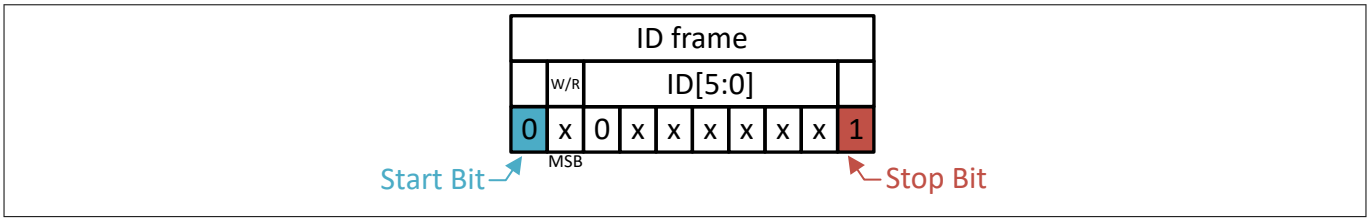

Figure 19 ID frame

Table 17 Bit assignment ID frame

ID frame bits	Function
W/R[7]	1: Write command 0: Read command
ID[5:0]	000000: Default x: ID 111111: Broadcast command

Note: The ID 00_H is only available after reset, before enumeration. The ID $3F_H$ is exclusively used for broadcast commands.

Address frame

The address frame determines which register is affected by the read or write command.

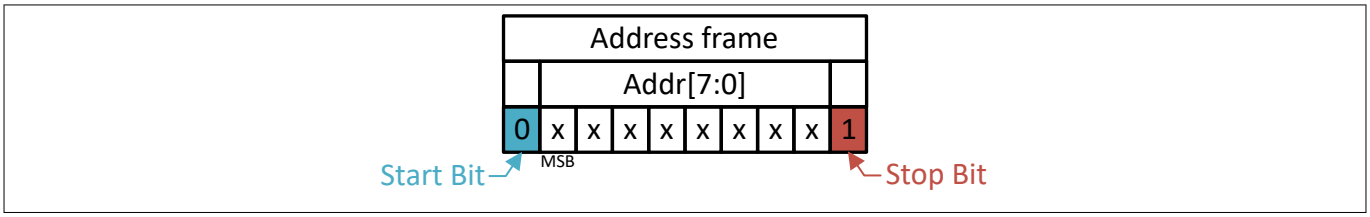

Figure 20 Address frame

Data frame

The data frame contains the sent or retrieved data.

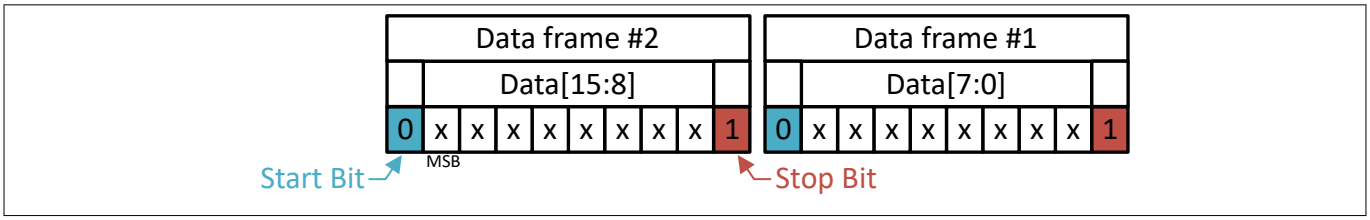

Figure 21 Data frames

CRC frame

For read and write commands, an 8-bit CRC protection conforming to SAE J1850 for the entire message including the synchronization frame is calculated and appended to the frames.

8-bit polynomial: $G(z) = z^8 + z^4 + z^3 + z^2 + 1$ (initial value = FF_H; XOR value = FF_H)

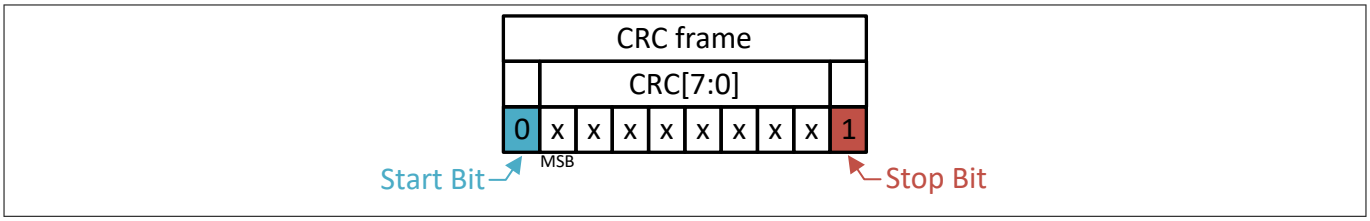

Figure 22 CRC frame

Note: If the device encounters an invalid CRC, it neither accepts the message nor replies to it.

Reply frame

The device acknowledges a received write command with a reply frame. In case of a broadcast write command only the last device in the chain generates the reply frame.

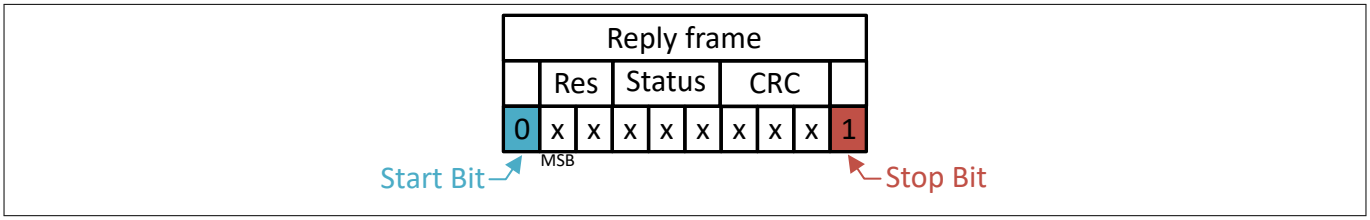

Figure 23 Reply frame

The message reply frame is protected by a 3-bit CRC calculated as: $G(z) = z^3 + z + 1$.

Table 18 Bit assignment reply frame

Reply-Frame	Function	
bit[7:6]	Res [1:0]	Reserved
bit[5]	Status [2]	0: Write command successfully transmitted 1: CRC checked register error
bit[4]	Status [1]	0: Register address for write command valid 1: Register address for write command invalid
bit[3]	Status [0]	0: No fault in general diagnostics register 1: Fault in general diagnostics register
bit[2:0]	CRC [2:0]	3-bit reply CRC

16.1.3 Register read modes

There are the following approaches for reading content from the device:

- Direct read: Read a single register from a single IC.
- Broadcast read: Read a single register from all ICs in the same stack with one read command.
- Multi read: Read multiple registers from a single IC. The read command for multiple registers is configurable in the multi read register MULTI_READ_CFG and can read the following measurement results with one read command of the MULTI_READ register:
  - PCVM
  - BVM
  - SCVM
  - External temperature measurement
  - Internal temperature measurement
  - R_{DIAG} measurement

16.2 Electrical characteristics communication

Table 19 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
GPIO/PWM physical layer							
UART to iso UART propagation delay	$t_{UART\_isoU\_del}$	–	25	60	ns	Propagation delay from UART to iso UART	PRQ-828
GPIO bit rate	BR_{GPIO}	0.97	2	2.1	Mbit/s	–	PRQ-831
UART broadcast read bus release time	$t_{UART\_rel\_BR}$	–	–	15 × 1/ BR_{GPIO}	s	Time to wait before sending a new command after end of broadcast read reply	PRQ-1909

(table continues...)

Table 19 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
UART read, write, broadcast write, multiread release time	t_{UART_rel}	–	–	3 × 1/ BR_{GPIO}	s	Time to wait before sending a new command after end of read/write/ broadcast write/multiread reply	PRQ-1910
iso UART physical layer							
iso UART current threshold "high"	$I_{isoU\_th\_high}$	2.25	4.5	6.5	mA	$(I_{IFx\_H} - I_{IFx\_L}) / 2$ I_{IFx_H}: Current in the iso UART high pin I_{IFx_L}: Current in the iso UART low pin	PRQ-832
iso UART current threshold "low"	$I_{isoU\_th\_low}$	-6.5	-4.5	-2.25	mA	$(I_{IFx\_H} - I_{IFx\_L}) / 2$ I_{IFx_H}: Current in the iso UART high pin I_{IFx_L}: Current in the iso UART low pin	PRQ-833
iso UART propagation delay	$t_{isoU\_prop\_del}$	–	25	70	ns	*1)* Propagation delay from IFH to IFL and IFL to IFH	PRQ-834
iso UART overdrive current	I_{od}	3	–	–	mA	*2)* with t_{pulse} = 38 ns	PRQ-1370
Reply delay time	t_{reply_delay}	0	1.7	3	µs	*2)* internal reply delay time of one IC	PRQ-837
iso UART bit rate	BR_{isoU}	0.97	2	2.1	Mbit/s	–	PRQ-838
Series resistor value	R_{ser}	37.05	39	40.95	Ω	*2) 3)*	PRQ-836
Series capacitor value	C_{ser}	0.95	1	1.05	nF	*2) 3)*	PRQ-835
Transceiver Ron @100mA	R_{ON}	19	22	27	Ω	–	PRQ-1845

1) Tested with standard external circuit (C_{ser}, R_{ser}).
2) Not subject to production test; verified by design or characterization.
3) External RC network needs to be adjusted depending on the application constraints, for example cable length.

17 Round robin (RR)

17.1 Functional description

The device automatically performs a round robin (RR) scheme, which triggers several measurements as well as internal diagnostics to check for possible faults independently of any communication commands.

The setting of the partition configuration register determines, which cells are measured and diagnosed.

Note: To manually start a round robin cycle, use the RR_CONFIG.RR_SYNC bitfield and then perform a write command to WD_CNT.

The automatic round robin diagnostic cycle is performed periodically every t_{RR}. The period is configurable from t_{RR_min} to t_{RR_max} with a resolution of t_{RR_LSB}.

The duration of the actual diagnostic checks is defined by $t_{RR\_duration}$. *Note: The first round robin cycle is performed immediately after each IC wake-up. If the WD_CNT command is missing or delayed for > t_{RR}, then in RR_SYNC mode the RR is performed automatically after t_{RR}.*

The IC wakes up periodically from sleep mode to perform one RR cycle on a programmable periodical basis with an interval t_{RR_sleep} from $t_{RR\_sleep\_min}$ to $t_{RR\_sleep\_max}$ with a resolution of $t_{RR\_sleep\_LSB}$. If the number of NTCs is > 0, then two RR schemes are executed after wake-up before the IC returns to sleep mode.

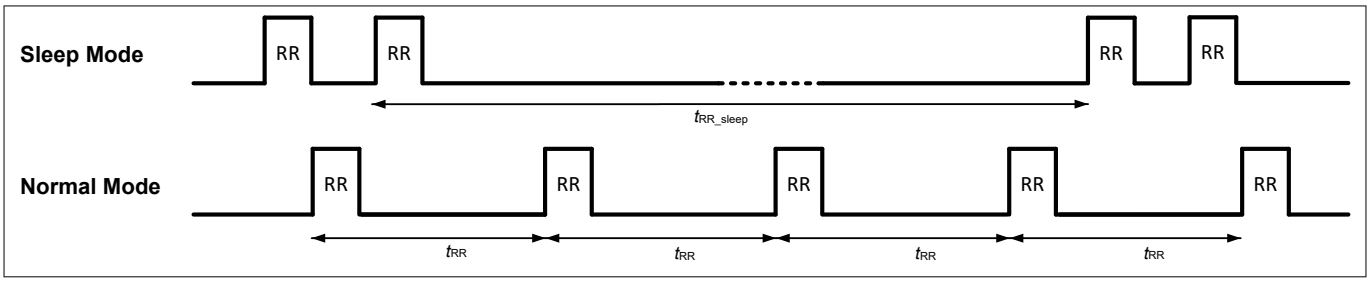

Figure 24 Round robin diagnostics timing during sleep mode

The following measurements are performed once during one round robin cycle in the following sequence:

1. Temperature measurements of both internal temperature sensors
2. ADC stress sensor compensation measurements and calculation
3. PCVM (10-bit) for all activated cells
4. BVM (10-bit)
5. NTC resistance measurement
6. NTC diagnostic measurements

Note: To measure all connected NTCs up to three cycles might be needed. The result registers of PCVM and BVM are not updated.

During a round robin the following checks are performed subsequent to the corresponding measurements, if set active.

1. Internal overtemperature check
2. The sum of all PCVMs is compared to the block voltage for a plausibility check
3. Cell voltage overvoltage and undervoltage check. If the voltage of a cell violates the programmed threshold (identified either by the digital or the analog comparator)
4. Open load diagnostic for all voltage sensing and balancing pins
5. Balancing overcurrent and undercurrent check for each cell where the balancing function is active
6. NTC overtemperature check
7. NTC diagnostics checks

Each fault detected in a RR check increases the respective error counter by 1.

17 Round robin (RR)

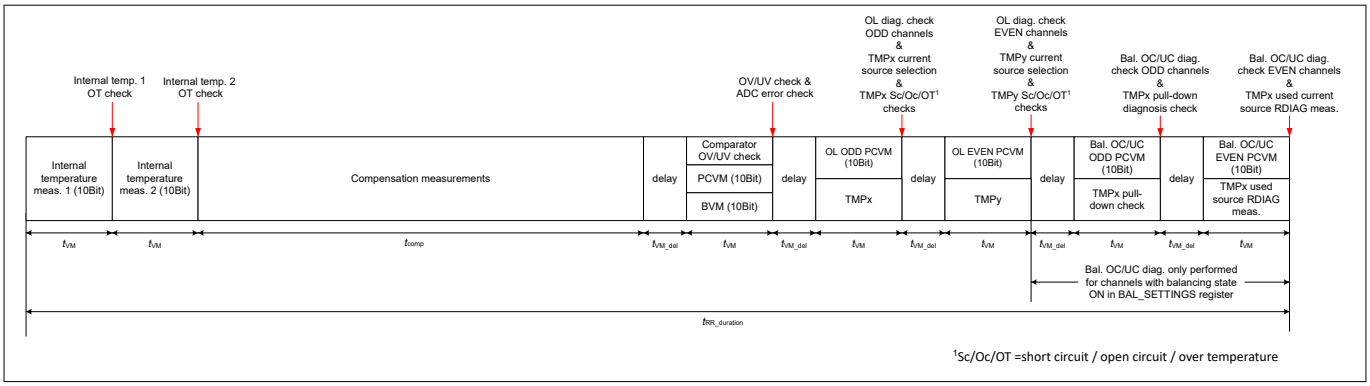

Figure 25 RR task timing diagram

During a round robin cycle, the connections on the activated TMPz channels are checked for open or short conditions. If it detects an open or short failure, then the corresponding fault bit in the external overtemperature warning register is set. Additionally, the external temperature error bit of the general diagnostics register is set. If the measured NTC value violates the corresponding thresholds, then an error flag is set.

$NTC\_open_{thr} \leq$ EXT_TEMP_z.RESULT $\leq NTC\_short_{thr}$

Clearing the external temperature error bit of the general diagnostics register resets the external overtemperature warning register.

Note: RR_ERR_CNT.NR_EXT_TEMP_START bitfields setting and the current source range selection impacts the number of RRs needed to detect a failure condition.

If the device detects an error during a round robin cycle, the individual error counter is increased by one. If the error counter is greater than n_{ERROR}, the respective error bit is set. The counter limit n_{ERROR} (3-bit) is configurable and valid for all counters. It is possible to deactivate a specific error counter by setting a mask bit.

Note: Setting n_{ERROR} to 0, sets the error flag with the first detection of the failure condition.

The status of the diagnostics registers which have been updated during a round robin cycle can be read via a command. If a fault was detected, the information is latched and can be cleared via a clear command.

Note: The following diagnostics registers are available:

- *General diagnosis GEN_DIAG*
- *Cell voltage supervision warning flag CELL_UV*
- *Cell voltage supervision warning flag CELL_OV*
- *External overtemperature warning flags EXT_TEMP_DIAG*
- *Diagnosis OPENLOAD DIAG_OL*
- *Cell voltage supervision warning flags CELL_UV_DAC_COMP*
- *Cell voltage supervision warning flags CELL_OV_DAC_COMP*
- *Passive balancing diagnosis OVERCURRENT BAL_DIAG_OC (only if balancing function is active)*
- *Passive balancing diagnosis UNDERCURRENT BAL_DIAG_UC (only if balancing function is active)*

The IC keeps the diagnostic results (except for BAL_DIAG_OC and BAL_DIAG_UC) in sleep mode, as long as the sleep mode supply is available on U12P pin. In sleep mode, the IC resets the passive balancing diagnostic registers for overcurrent BAL_DIAG_OC and undercurrent BAL_DIAG_UC.

After the 10-bit cell voltage measurement task in the round robin cycle, the measurement results are compared to configurable undervoltage and overvoltage thresholds. To configure the thresholds, the corresponding bits in the cell voltage thresholds registers can be set with a resolution of V_{Comp_LSB}.

The undervoltage detection is disabled in case of UV_THR = 000_H.

The overvoltage detection is disabled in case of OV_THR = $3FF_H$.

The IC has an automatic overvoltage and undervoltage detection. The comparator monitors the V_{Gn} - V_{Un} voltage and sets the OV/UV bits in the registers CELL_UV_DAC_COMP and CELL_OV_DAC_COMP.

The delta sigma ADC monitors the (V_{Un+1} - V_{Un}) voltage and sets the OV/UV bits in the registers.

17 Round robin (RR)

In a round robin cycle, the balancing function is paused during overvoltage and undervoltage check.

If the RR_SYNC bit is set, then the IC synchronizes the start of the round robin cycle to the watchdog command.

If this bit is set, then the next round robin cycle is triggered every time the watchdog WD_CNT is served. Additionally, the round robin counter is reset.

Note: Autonomous RR is active if t_{RR} expires before WD_CNT command arrives. This mechanism can synchronize all devices in the chain as well as the round robin to other tasks.

After triggering a PCVM, SCVM, BVM, or AVM, the IC performs that measurement and terminates the round robin (case 3). The GEN_DIAG.LOCK_MEAS bit is set to 1 in this case and it is not possible to start a second manual measurement since RR cannot be skipped a second time, see cases 2, 3 and 4 in Figure. After the measurement is finished, the round robin task is restarted.

The round robin cycle has a lower priority than the triggered measurement.

Note: This is also true for a long running mode measurement.

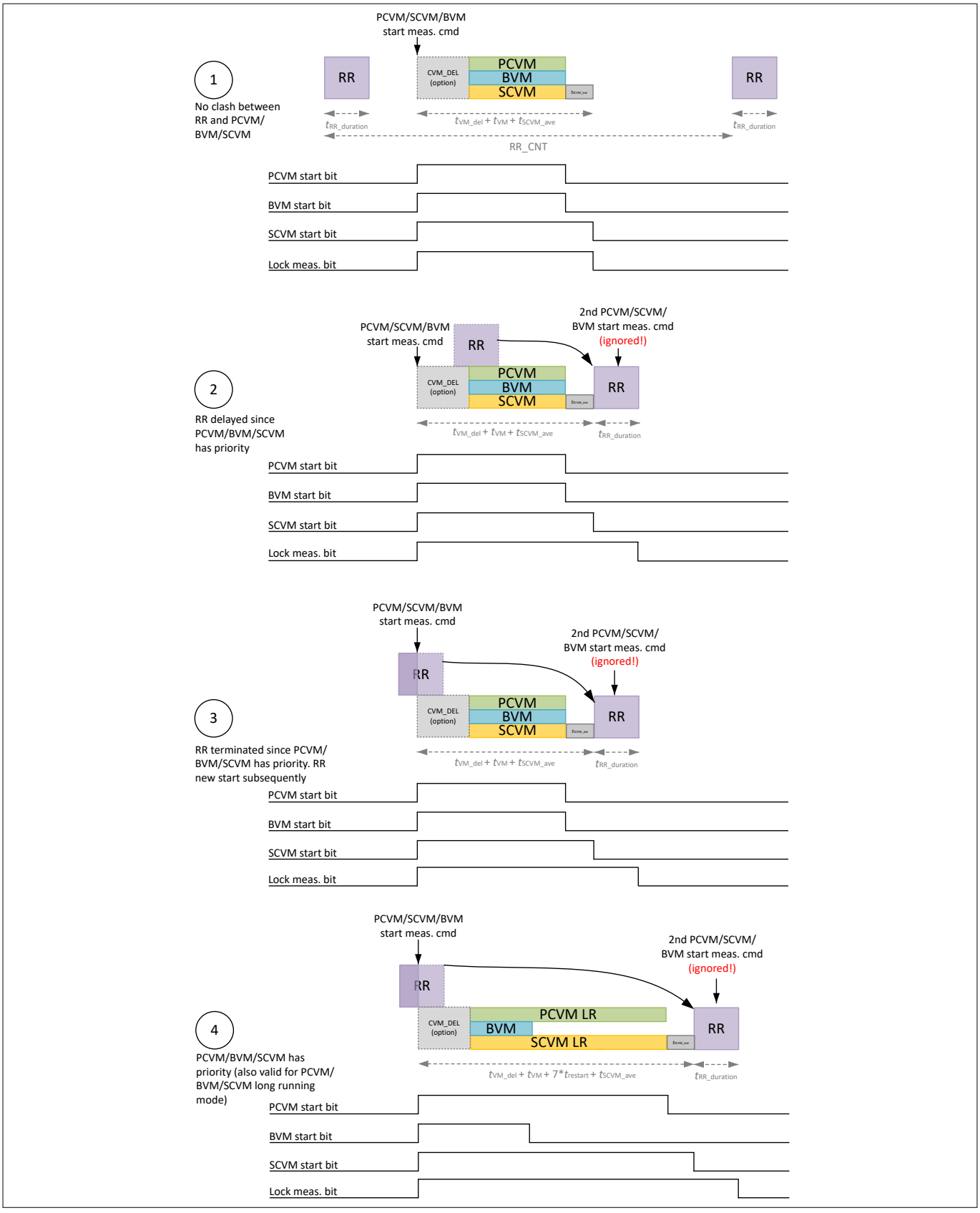

Figure 26 Prioritizing PCVM, SCVM, BVM, and AVM versus round robin

If a round robin is delayed by a manually triggered measurement, then the device synchronizes the subsequent RR scheme to start at the end of the measurement time t_{vm}.

Internal IC data, such as ADC trimming values is ECC protected and a register CRC check as well as an internal data check is executed with a fixed hardware cycle time t_{CRC_check} independent of the round robin scheme interval time t_{RR}. The registers with the following addresses are CRC protected: 01_H, 02_H, 03_H, 04_H, 05_H, 08_H, 09_H, $0A_H$, 14_H, 15_H, 17_H, 36_H, 38_H, $3A_H$, $3E_H$.

Note: The register CRC error as well as the internal IC error do not have an error counter.

17.2 Electrical characteristics round robin (RR)

Table 20 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overvoltage and undervoltage detection							
OV/UV threshold resolution	V_{OVUV_LSB}	–	$FSR_{PCVM}/2^{10}$	–	mV	1)	PRQ-766
OV/UV threshold maximum value	V_{OVUV_max}	0	–	FSR_{PCVM}	V	1)	PRQ-767
Round robin counter							
RR scheme duration	$t_{RR\_duration}$	–	–	1.2	ms	1) Only valid if the measurement delay time t_{VM_del} is not higher than $t_{VM\_del\_LSB}$.	PRQ-774
RR interval step	t_{RR_LSB}	1.12	1.17	1.22	ms	1)	PRQ-770
RR minimum interval	t_{RR_min}	6.7	7.1	7.4	ms	1)	PRQ-768
RR maximum interval time	t_{RR_max}	149	155.7	163	ms	1) 7-bit counter	PRQ-769
RR sleep interval step	$t_{RR\_sleep\_LSB}$	13.64	15	16.67	sec	1)	PRQ-773
RR sleep maximum interval time	$t_{RR\_sleep\_max}$	3.88	4.26	4.74	h	1) 10-bit counter	PRQ-771
Error counter	n_{ERROR}	0	–	7	-	1) 3-bit counter	PRQ-776
CRC check cyclic interval	t_{CRC_check}	47	49.15	52	ms	1)	PRQ-775

(table continues...)

Table 20 (continued) Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
RR compensation measurement and calculation	t_{comp}	385	405	425	µs	1)	PRQ-1392
ADC ERROR result (ΣPCVM versus BVM) comparison error threshold	ADC_ERR_{th}	–	256	–	mV	–	PRQ-1304
NTC Open / short diagnostics							
NTC short threshold	NTC_short_{thr}	–	64	–	LSB10	Using I_{TMPz_0} with 0 ≤ z ≤ 4	PRQ-1306
NTC open threshold	NTC_open_{thr}	–	1023	–	LSB10	Using I_{TMPz_3} with 0 ≤ z ≤ 4	PRQ-1307

1) Not subject to production test; verified by design or characterization.

18 Emergency mode (EMM) and ERR pin (ERR)

18.1 Functional description

One of the following reactions of the IC to an error can be configured in the ERR pin/EMM mask register:

- Indicate the issue via a "high" level on the ERR pin.
- Send an emergency signal (EMM) via iso UART to each adjacent device in the chain.

The ERR pin is protected against short to GND.

The emergency signal is an alternating signal with the frequency f_{EMM}. The EMM is received and sent via the iso UART communication interfaces.

The IC can detect and forward an EMM signal in sleep mode. The EMM signal is used for the IC wake-up. On detecting an EMM signal, the IC reproduces and forwards it to the opposite iso UART interface.

After the transmit process the IC returns to sleep mode.

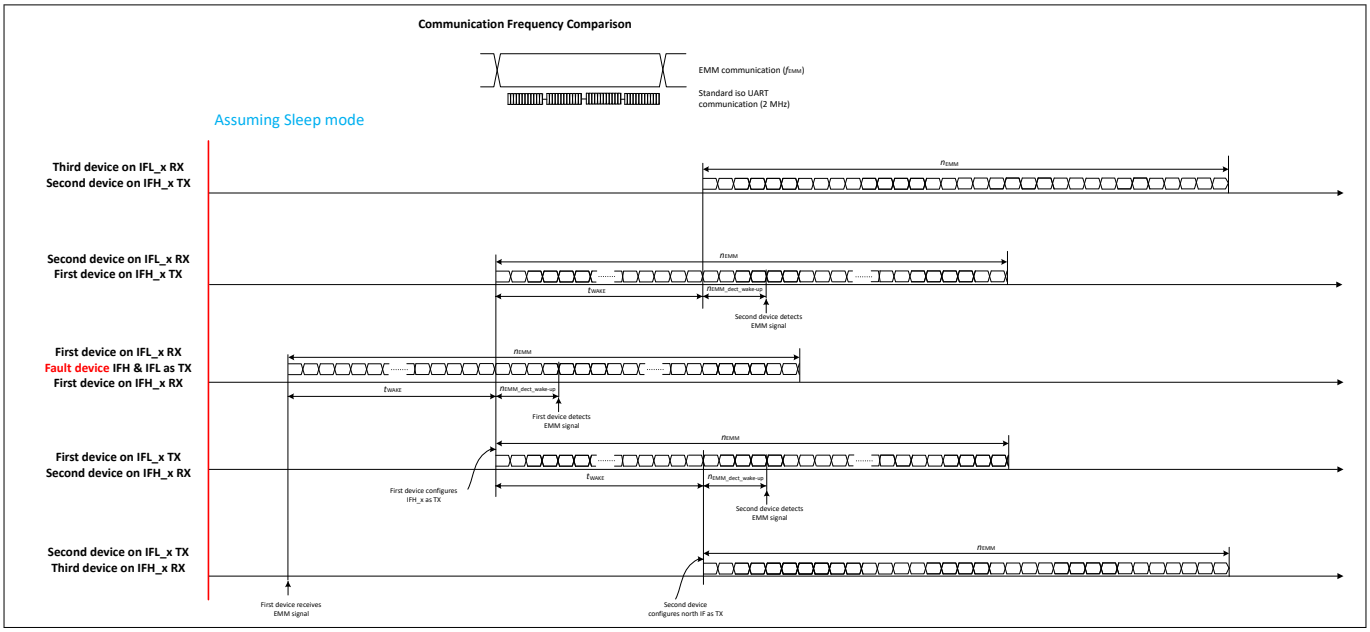

Figure 27 EMM in sleep mode process

With a chain in sleep mode, the EMM signal reaches the transceiver from both sides.

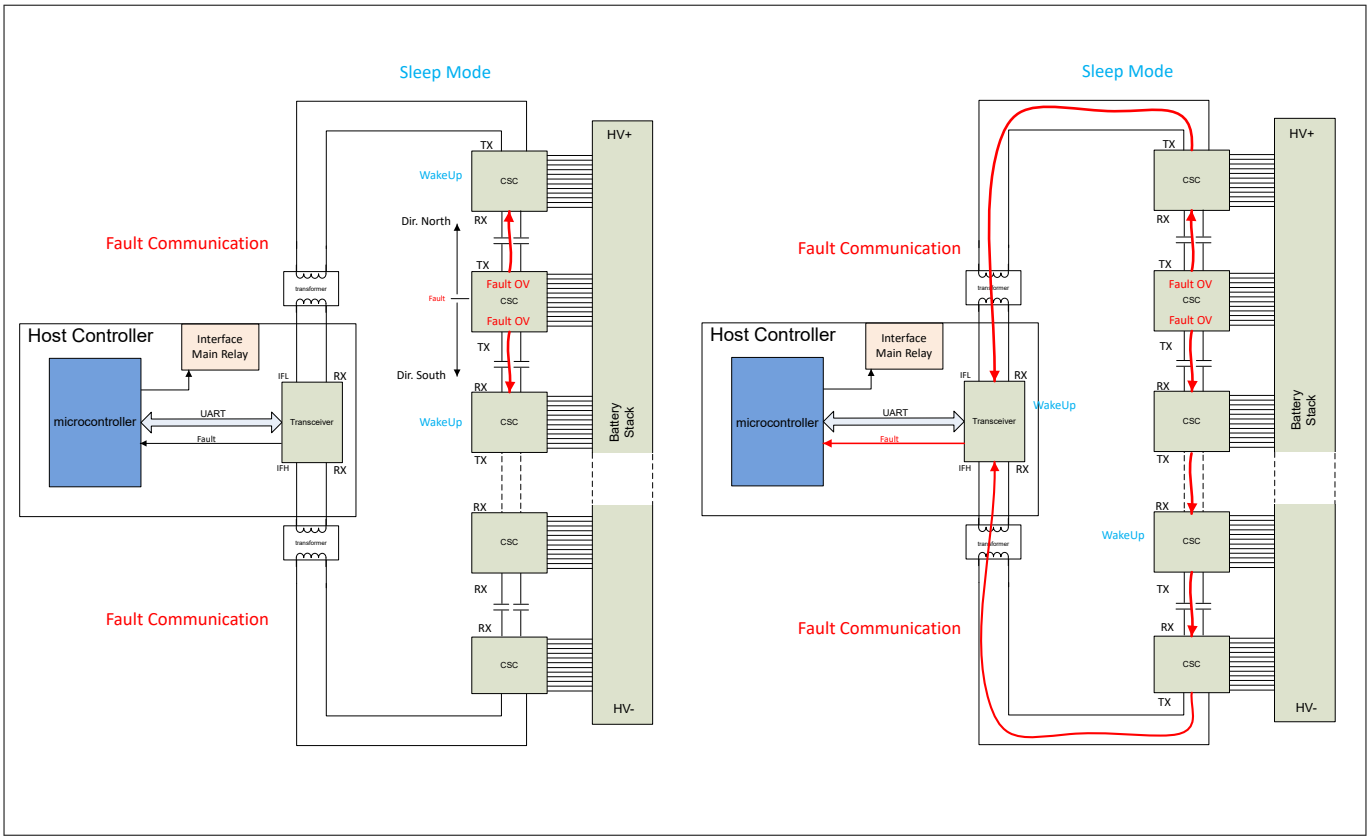

Figure 28 EMM in sleep mode path

In normal operation the communication mode (PoT or PoB) is already defined and the adjacent device shows either a TX or RX interface. In case of EMM, the contiguous device showing a TX interface will not forward the EMM signal. Therefore, the EMM signal follows the path that shows the RX interface back to the microcontroller.

18 Emergency mode (EMM) and ERR pin (ERR)

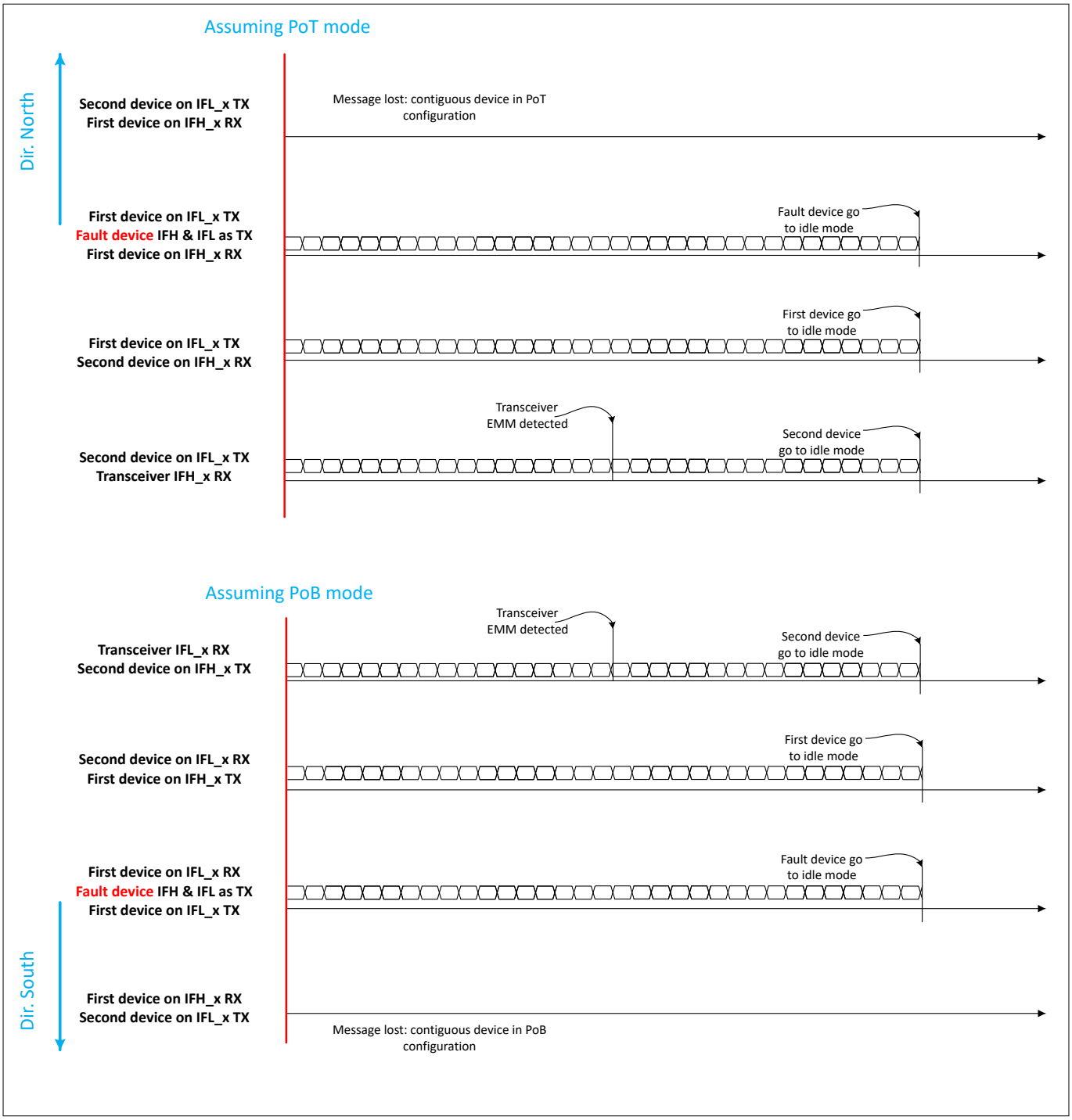

Figure 29 EMM in normal mode process

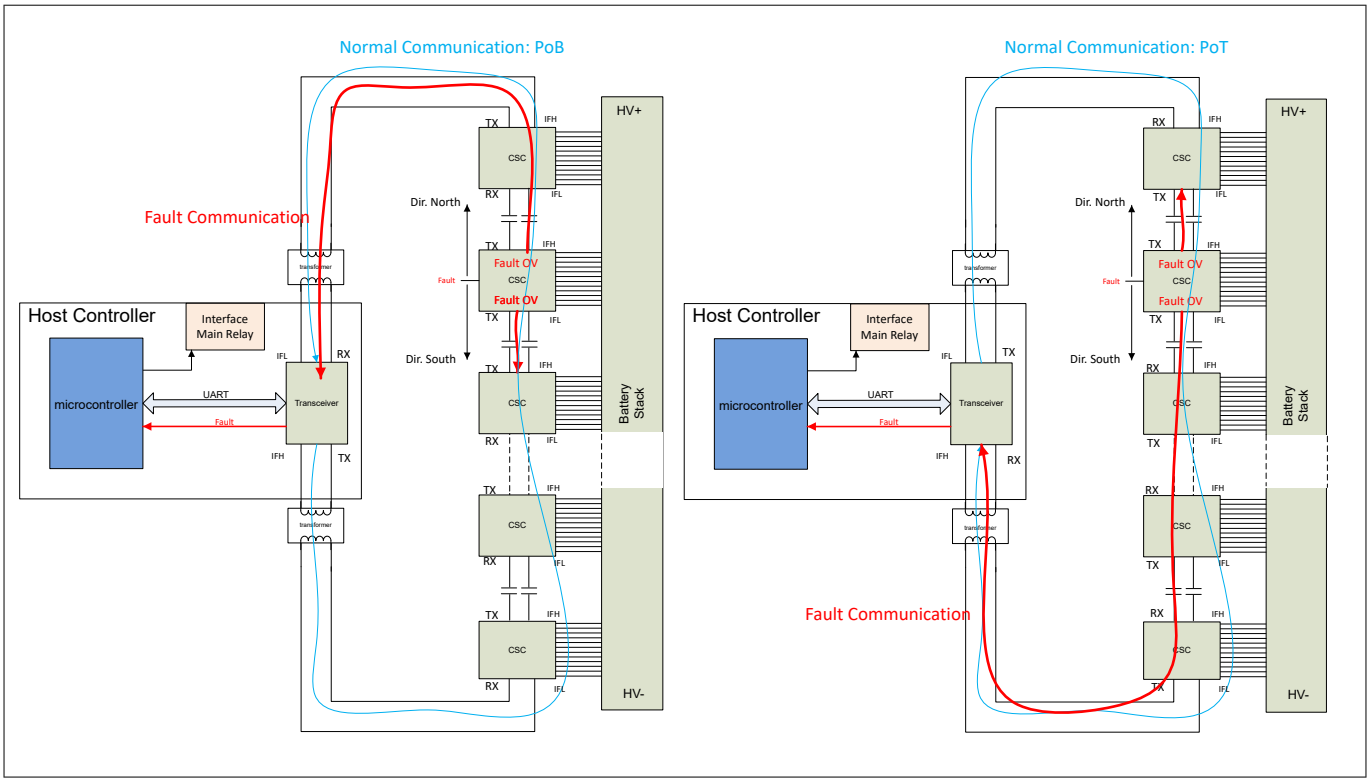

Figure 30 EMM in normal mode path

A device which sends the EMM signal transmits it for n_{EMM} periods. The number of periods the IC needs to detect and forward an EMM signal depends on the operation mode:

1. Idle mode: n_{EMM_dect}
2. Straight after wake-up caused by EMM: $n_{EMM\_dect\_wake-up}$

The IC's ERR pin default state is low and is pulled down using the external pull-down resistor R_{ERR_PD}. If the device detects an error, then it switches the ERR pin to VS until the following actions are performed:

- The microcontroller clears the fault, which triggered the ERR signal.
- The IC enters sleep mode.

If a fault that activates the ERR pin is detected in round robin sleep, then the IC remains in normal mode until t_{WD_max} elapses.

The following faults can trigger the EMM mode or the ERR pin, depending on the configuration in the ERR pin / EMM mask register:

- Overvoltage or undervoltage of a cell
- External NTC resistance measurement fault
- Open load diagnostics error for any voltage sensing and balancing pin
- Balancing overcurrent and undercurrent error
- ADC cross-check error
- Internal overtemperature detected
- Register CRC check fault detected
- Internal IC error

Setting the corresponding bits in the ERR pin and EMM mask register prevents faults from leading to an emergency signal (EMM) emission or to an ERR pin reaction.

18.2 Electrical characteristics emergency mode (EMM) and ERR pin (ERR)

Table 21 Electrical characteristics

$V_{VS} = V_{VS\_functional}$, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Emergency mode EMM							
EMM signal frequency	f_{EMM}	48	50	52	kHz	1)	PRQ-737
EMM number of periods to detect EMM signal - straight after wake-up	$n_{EMM\_dect\_wake-up}$	4	–	4	periods	1) **1.** Wake-up due to the EMM signal **2.** During forwarding of the wake-up signal	PRQ-738
EMM number of periods to detect EMM signal - idle mode	n_{EMM_dect}	16	–	16	periods	1) IC is in idle mode and not enumerated (ID = 0)	PRQ-740
Transmitted EMM signal periods	n_{EMM}	32	–	32	periods	1)	PRQ-742
ERR pin function							
ERR fault indication voltage	V_{ERR}	V_{VS} - 0.25 V	–	V_{VS}	V	$I_{ERR} \leq I_{ERR\_max}$	PRQ-743
ERR input current	I_{ERR}	-1	–	–	mA	Current capability of pin additionally to R_{ERR_PD} (= 100 kΩ) current	PRQ-744
ERR pull-down resistor	R_{ERR_PD}	75	100	–	kΩ	External pull down resistance	PRQ-745

1) Not subject to production test; verified by design or characterization.

19 Application information

19.1 External circuitry and components

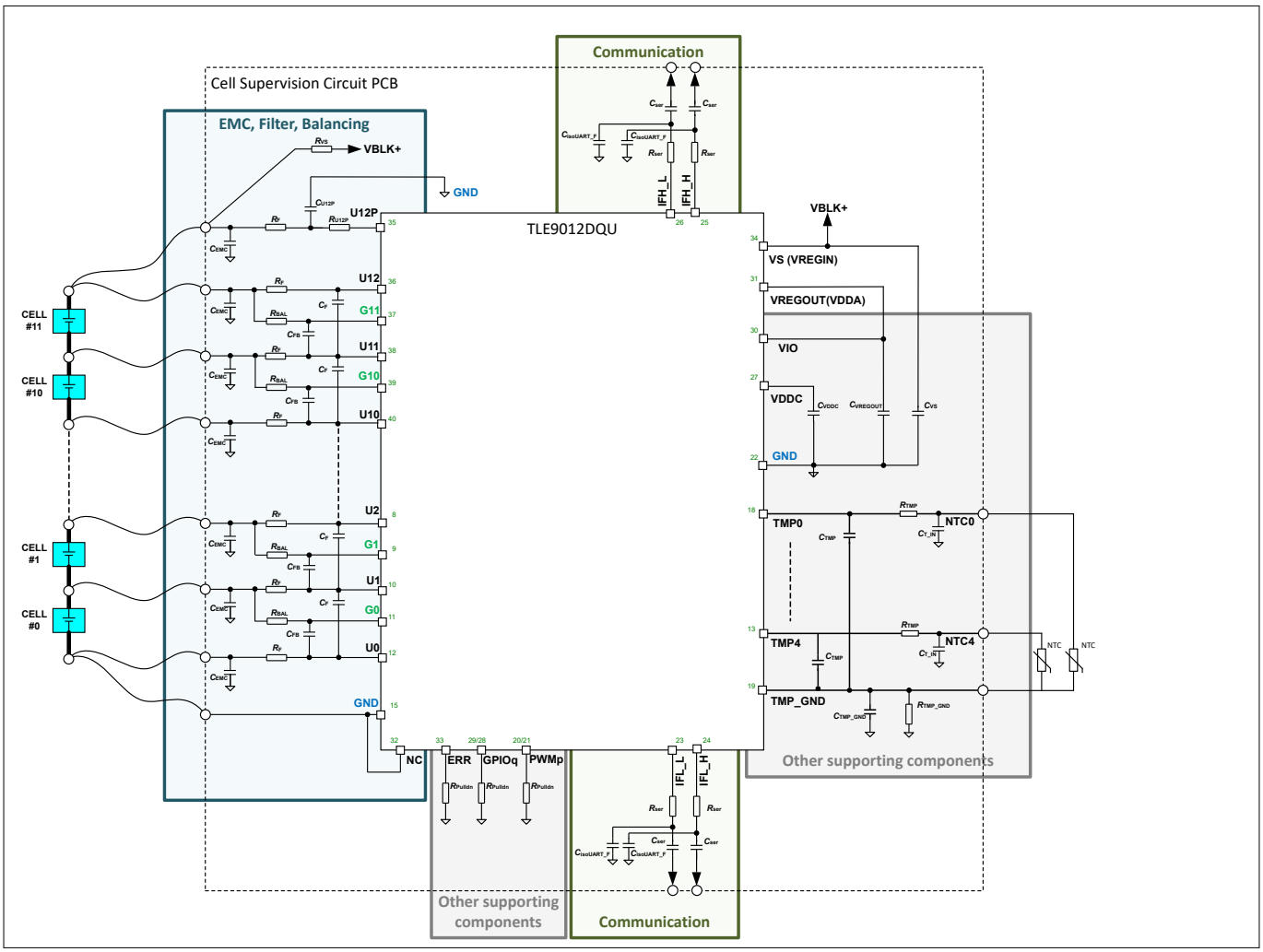

Figure 31 External circuitry TLE9012DQU

Table 22 External components

Name	Symbol	Typ.	Unit	Condition
External filter resistor RF	R_F	10	Ω	Valid for pin U0 - U12
External filter resistor RU12P	R_{U12P}	5.1	Ω	
External balancing resistor RBAL	R_{BAL}	41	Ω	
External filter capacitor CF	C_F	330	nF	
EMC network capacitor CEMC	C_{EMC}	1	nF	
Filter capacitor (Gn/Un) CFB	C_{FB}	100	nF	
Buffer capacitor CVS	C_{VS}	100	nF	
Filtering resistor RVS	R_{VS}	5.1	Ω	

(table continues...)

Table 22 (continued) External components

Name	Symbol	Typ.	Unit	Condition
Buffer capacitor on U12P	C_{U12P}	100	nF	
Buffer capacitor on VREGOUT	$C_{VREGOUT}$	100	nF	
Buffer capacitor on VIO	C_{VIO}	100	nF	If VIO is connected to VREGOUT, then C_{VIO} is omitted.
Buffer capacitor on VDDC	C_{VDDC}	330	nF	
Bypass capacitor on iso UART	$C_{isoUART\_F}$	220	pF	
Input capacitor on TMP	C_{TMP}	10	nF	
NTC filter resistor RTMP	R_{TMP}	100	Ω	
NTC filter capacitor CT_IN	C_{T_IN}	4.7	nF	
External wiring resistance	R_{WH_ch}	0.2	Ω	

19.2 Typical application diagram

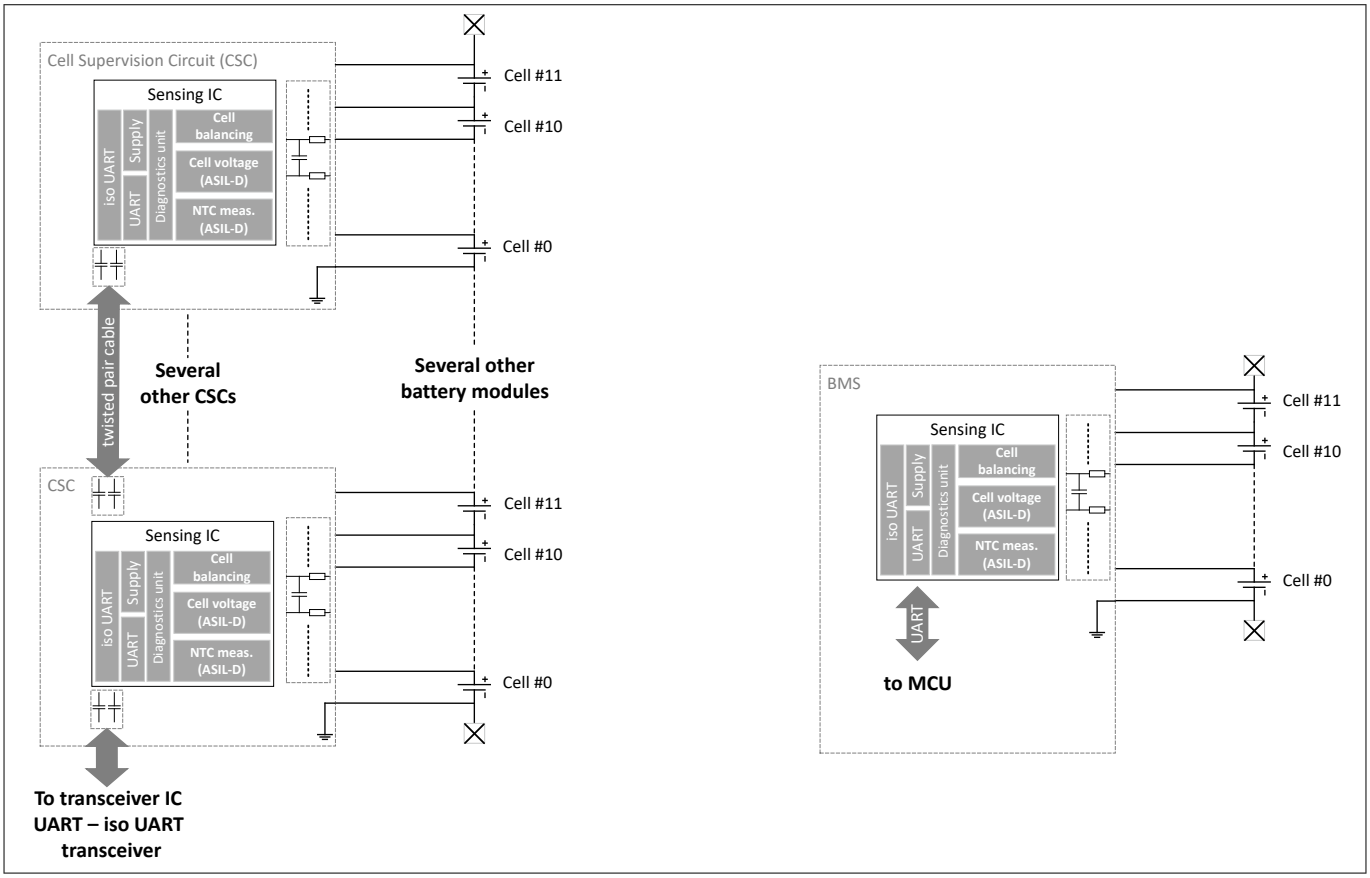

Figure 32 Typical application diagram

20 Package information

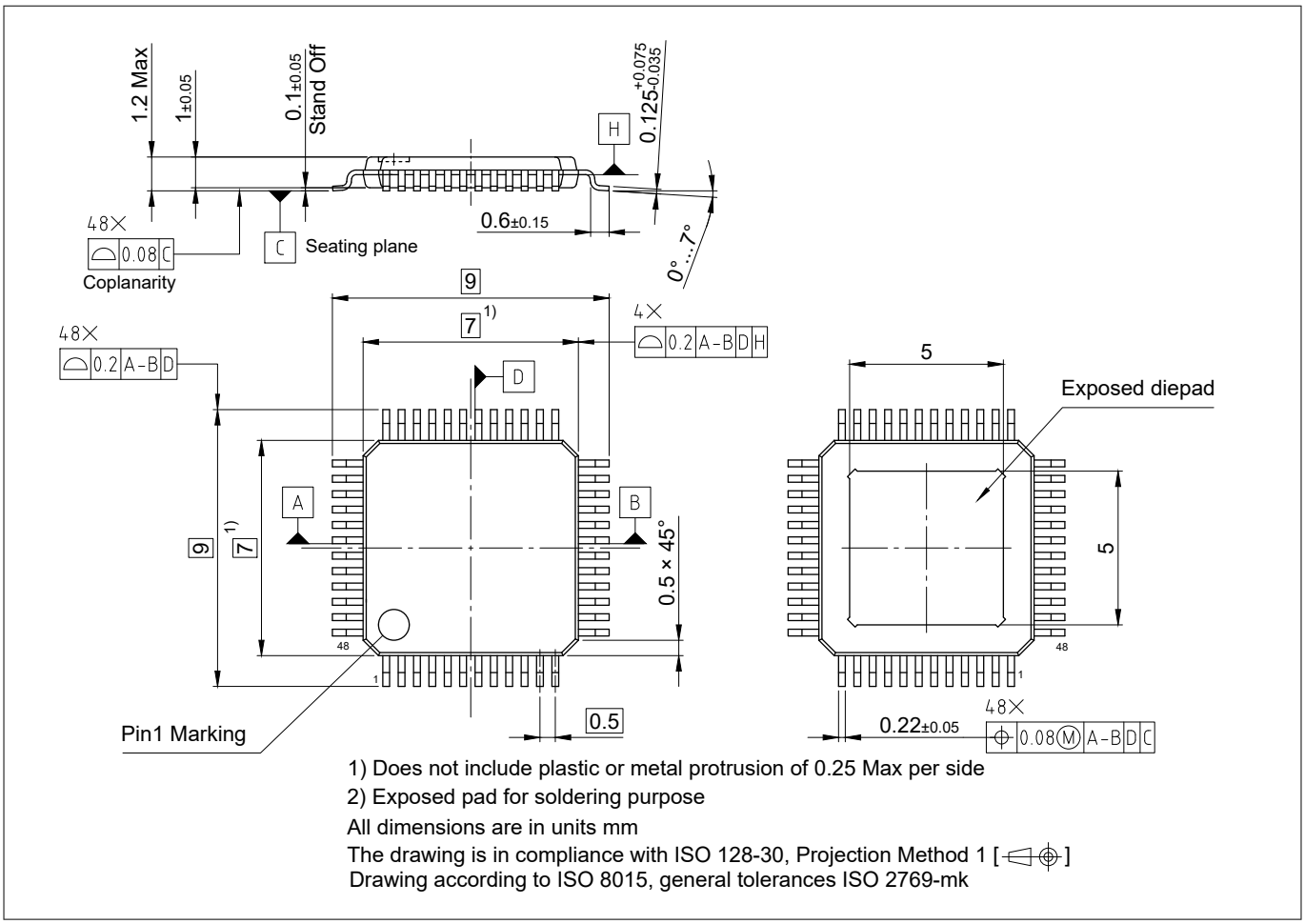

Figure 33 PG-TQFP-48

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

21 Revision history

Revision	Date	Changes
2.0	2023-11-02	Improved accuracy specification, editorial updates and corrections
1.0	2022-01-24	Initial release of datasheet

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