

# OPTIREG™ PMIC TLF11251EP

## 2.5 A half bridge with integrated driver and level shifter



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Family overview



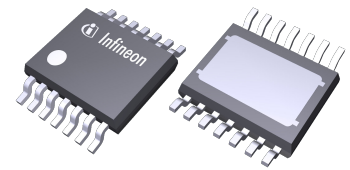
Support



RoHS

## Features

- AEC-Q100 Grade 0 for high temperature mission profiles
- Integrated PMOS and NMOS complementary output bridge with 2.5 A current capability
- Integrated gate drivers
- Single control input with an integrated dead time logic for optimized control and high efficiency
- Output current sensing
- Output current limitation
- Overtemperature protection
- Low quiescent current
- No external dead time adjustment required
- Infineon automotive quality
- Green Product (RoHS compliant)



## Potential applications

Companion for the OPTIREG™ PMIC TLF3558xxxx for core voltage regulation of AURIX™ TC3xx microcontroller in:

- Car powertrain and transmission applications
- Electric power steering
- Battery management
- Inverter applications
- Engine management
- Domain control

## Product validation

Qualified for automotive applications with higher temperature requirements. Product validation according to AEC-Q100, Grade 0.

## Description

The OPTIREG™ PMIC TLF11251EP is a 2.5 A half bridge with integrated driver and level shifter. It also contains a high side P-channel MOSFET and a low side N-channel MOSFET in a single package. The integrated level shifting stage allows for conversion of the input logic signals to the supply voltage level of the gate drivers. The input signal levels are CMOS compatible. The level shifter and the gate driver provide a dead time generation to simplify the interface with the embedded core voltage regulator of the AURIX™ TC3xx microcontroller. The low propagation delay allows for use in closed loop control applications with limited requirements for timing. The

# OPTIREG™ PMIC TLF11251EP

## 2.5 A half bridge with integrated driver and level shifter

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### Description

output stage allows for a high switching frequency. The TLF11251EP integrates protection features against overcurrent at the high side MOSFET and at the low side MOSFET as well as against overtemperature events. Internal power-on reset releases the digital logic and ensures its operation for the supply voltage within the specified range.

Type	Package	Marking
TLF11251EP	PG-TSDSO-14	TLF11251

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1 Block diagram

1 Block diagram

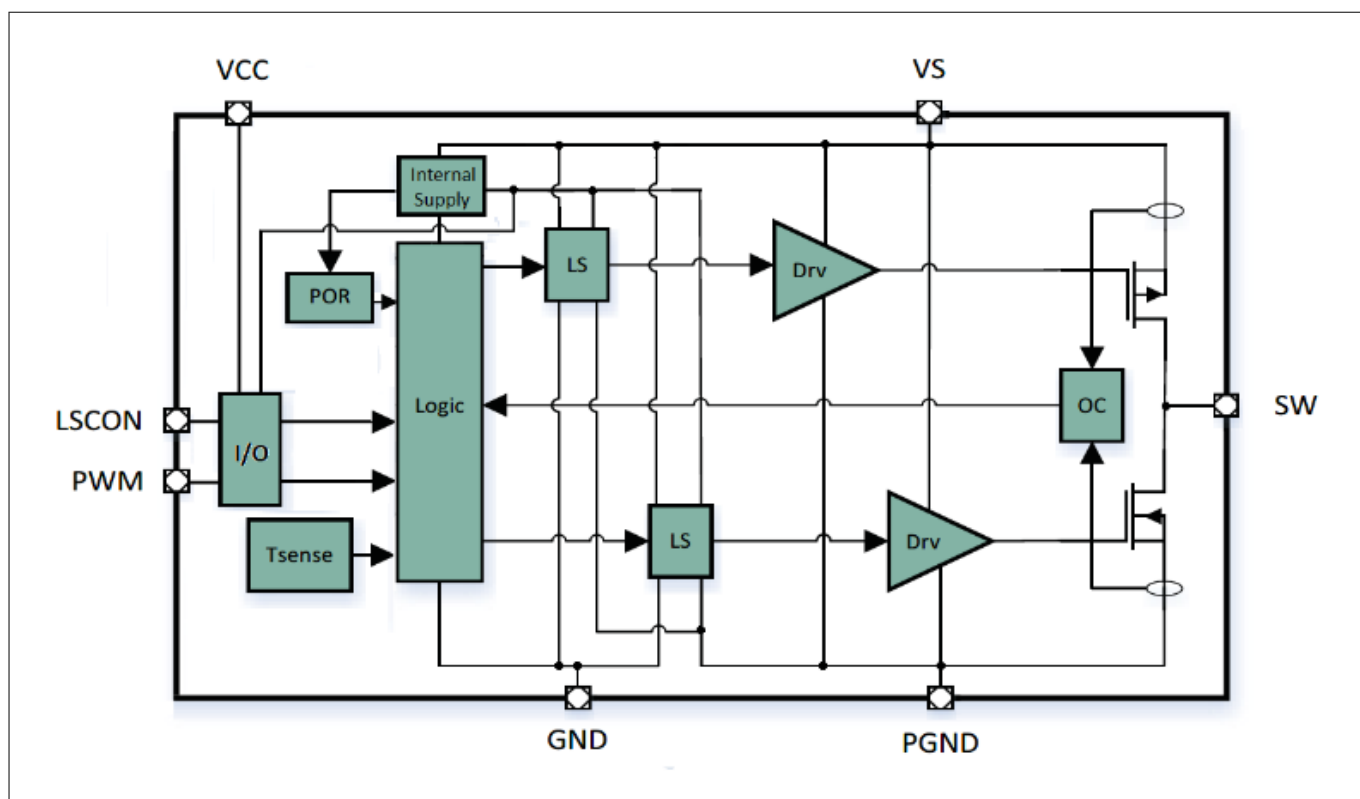
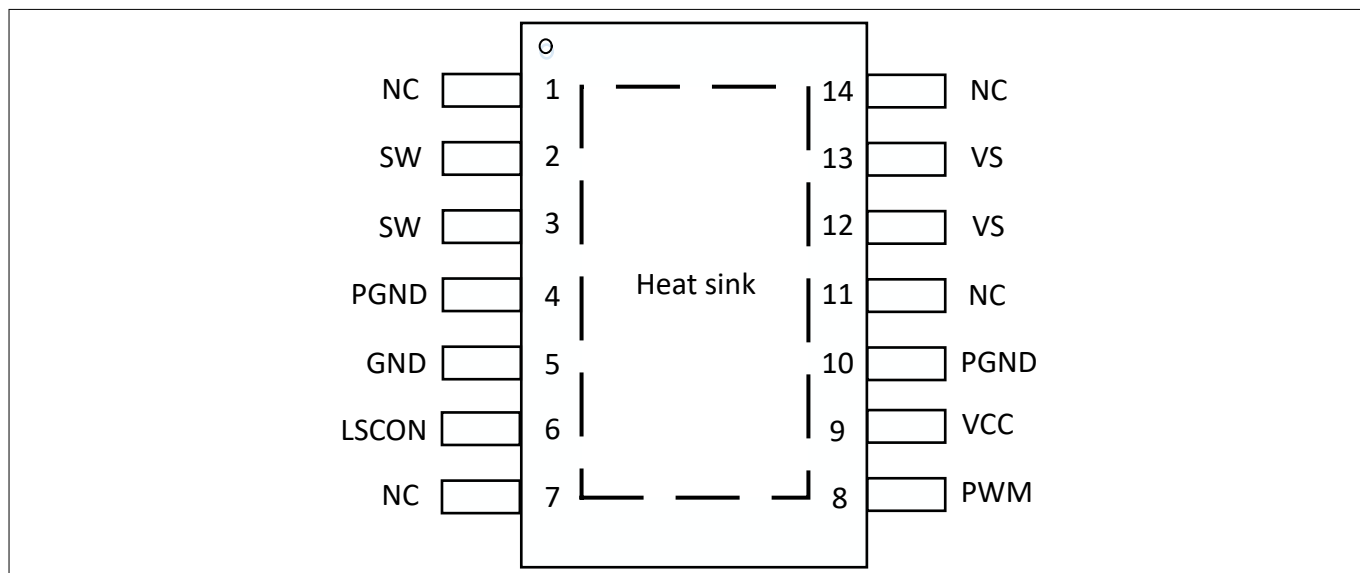


Figure 1 Block diagram

**2 Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment**



**Figure 2 Pin configuration**

## 2 Pin configuration

### 2.2 Pin definitions and functions

Pin	Symbol	Function
1	NC	Not connected. This pin is not connected internally; leave it open.
2, 3	SW	Switch node: Half bridge drains; typically connected to the input of the LC filter in buck circuits
4, 10	PGND	Power ground: Half bridge low side source
5	GND	Ground: Logical ground
6	LSCON	Bridge control scheme: Defines the low side state during PWM input "high". Switch to "high" enables synchronous control of high side and low side, based on PWM input state. Switch to "low" disables low side control.
7	NC	Not connected: This pin is not connected internally; leave it open.
8	PWM	Control input: Input for the logical signal that controls the state of the half bridge transistors. Switch to "high" opens the high side switch and closes the low side switch. Switch to "low" closes the high side switch and opens the low side switch.
9	VCC	Supply voltage input: Supply voltage for the PWM and LSCON inputs; typically the same as the supply of microcontroller output pins.
11	NC	Not connected: This pin is not connected internally; leave it open.
12, 13	VS	Supply voltage input: Supply to gate drivers, connected to half bridge high side source
14	NC	Not connected: This pin is not connected internally; leave it open
–	Heat sink	Connect to heat sink area. Connect to GND and PGND.

**3 General product characteristics**

**3 General product characteristics**

**3.1 Absolute maximum ratings**

**Table 1 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Supply voltage VS	$V_S$	-0.3	–	7.0	V	–	P_3.1.1
Supply voltage VCC	$V_{CC}$	-0.3	–	7.0	V	–	P_3.1.2
Switch node SW	$V_{SW}$	-0.3	–	7.0	V	–	P_3.1.3
Input PWM	$V_{PWM}$	-0.3	–	7.0	V	–	P_3.1.4
Input LSCON	$V_{LSCON}$	-0.3	–	7.0	V	–	P_3.1.5
<b>Currents</b>							
Continuous drain current high side	$I_{DHS}$	-2.5	–	–	A	PWM = off	P_3.1.6
Continuous drain current low side	$I_{DLS}$	–	–	2.5	A	PWM = on	P_3.1.7
Pulsed drain current high side	$I_{DHS}$	-4.4	–	–	A	Valid during active overcurrent protection	P_3.1.8
Pulsed drain current low side	$I_{DLS}$	–	–	4.4	A	Valid during active overcurrent protection	P_3.1.9
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	–	150	°C	–	P_3.1.10
Storage temperature	$T_{stg}$	-55	–	150	°C	–	P_3.1.11
<b>ESD susceptibility</b>							
ESD susceptibility all pins	$V_{ESD}$	-2	–	2	kV	<sup>2)</sup> HBM	P_3.1.12
ESD susceptibility all pins	$V_{ESD}$	-500	–	500	V	<sup>3)</sup> CDM	P_3.1.13
ESD susceptibility (corner pins)	$V_{ESD}$	-750	–	750	V	<sup>3)</sup> CDM	P_3.1.14

1) Not subject to production test, specified by design.

2) Human body model (HBM) robustness according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

3) Charged device model (CDM) robustness according to JEDEC JESD22-C101.

**Notes:**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.



**3 General product characteristics**

**3.2 Functional range**

**Table 2 Functional range**

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Supply voltage range VS	$V_{S,nom}$	3.5	–	7.0	V	–	P_3.2.1
Supply voltage range VCC	$V_{CC,nom}$	2.35	–	7.0	V	–	P_3.2.2
Supply voltage VS transient slew rate	$dV_S/dt$	-120	–	120	V/ms	<sup>1)</sup>	P_3.2.3
Supply voltage VCC transient slew rate	$dV_{CC}/dt$	-120	–	120	V/ms	<sup>1)</sup>	P_3.2.4
Junction temperature	$T_j$	-40	–	175	°C	–	P_3.2.6
Supply current total, normal operation	$I_{C,norm}$	–	–	35	mA	PWM input @ 1.8 MHz	P_3.2.9
Supply current total, no switching	$I_{C,ns}$	–	200	–	μA	$V_S < 5.8\text{ V};$ $V_{CC} < 5.1\text{ V};$ $T_j < 85^\circ\text{C}$	P_3.2.10

<sup>1)</sup> Not subject to production test, specified by design.

**Note:** *Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

**3 General product characteristics**

**3.3 Thermal resistance**

**Table 3 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Junction to case top, high side	$R_{thJCT(HS)}$	30.9	–	34.1	K/W	–	P_3.3.6
Junction to case top, low side	$R_{thJCT(LS)}$	39.5	–	43.7	K/W	–	P_3.3.7
Junction to case bottom, high side	$R_{thJCB(HS)}$	9.6	–	10.6	K/W	–	P_3.3.8
Junction to case bottom, low side	$R_{thJCB(LS)}$	13.4	–	14.8	K/W	–	P_3.3.9
Junction to ambient	$R_{thJA}$	–	43.3	–	K/W	<sup>2)</sup>	P_3.3.10

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a  $76.2 \times 114.3 \times 1.5 \text{ mm}^3$  board with two inner copper layers ( $2 \times 70 \text{ } \mu\text{m Cu}$ ,  $2 \times 35 \text{ } \mu\text{m Cu}$ ). Where applicable, a thermal via array next to the package contacted the first inner copper layer.

**Note:** This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit [www.jedec.org](http://www.jedec.org).

## 4 Block description and electrical characteristics

### 4 Block description and electrical characteristics

The device simplifies the interface of microcontroller control outputs to the half bridge.

#### 4.1 Logical inputs

A single PWM input controls the state of the half bridge MOSFETs. The inverted logical scheme translates the PWM input state to the gate signal shifted to the output supply level, thus the device switches the high side MOSFET off during PWM logical on-state, and it switches them on during PWM logical off state. The built-in dead time control circuitry prevents a shoot-through condition over the MOSFET bridge and improves system efficiency while used in buck power conversion circuits. No external dead time adjustment is required.

In addition to the PWM input, the LSCON input determines the low side MOSFET control scheme and allows for both synchronous as well as asynchronous operation in buck converter applications. Logical off state at the LSCON input switches off the low side MOSFET independently of the PWM input signal, so that the device only controls the high side MOSFET.

A permanent logical on state at the LSCON input allows both high side and low side operation according to PWM input state with the internal dead time generation. If such operation is required, then the LSCON input can be pulled-up or connected directly to the VCC supply rail.

The device interprets a toggling input signal at LSCON as a control request for synchronous low side and high side MOSFET switching. In this case the device generates dead time internally in accordance with the PWM input timing. Frequency detection at LSCON inputs detect toggling input signals within the acceptable range referred to as  $t_{det}$ .

**Table 4 Switching states**

LSCON	PWM	High side MOSFET	Low side MOSFET
On	<sup>1)</sup> On	Off	On
On	<sup>2)</sup> Off	On	Off
Off	On	Off	Off
Off	Off	On	Off
Toggling between on and off <sup>3)</sup>	On	Off	On
	Off	On	Off
Toggling between on and off stopped <sup>4)</sup> ( $< t_{fil}$ )	On	Off	On
	Off	On	Off
Toggling between on and off stopped ( $> t_{fil}$ ); LSCON: on	On	Off	On
Toggling between on and off stopped ( $> t_{fil}$ ); LSCON: on	Off	On	Off
Toggling between on and off stopped ( $> t_{fil}$ ); LSCON: off	On	Off	Off
Toggling between on and off stopped ( $> t_{fil}$ ); LSCON: off	Off	On	Off

**4 Block description and electrical characteristics**

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- 1) On: "high"
  - 2) Off: "low"
  - 3) Toggling between on and off: The device detects switching on and off at a frequency corresponding to the detection range  $t_{det}$  at the LSCON input.
  - 4) Toggling between on and off stopped: After the toggling between on and off, the device detects a permanent on or off state.
- 

The switching states in [Table 4](#) are only valid for device input supplies within the operational range and if no protection feature is active.

If the PWM pin is not connected, then the integrated weak pull-up ensures a defined level.

If an AURIX™ TC3xx microcontroller controls the device, then place an additional pull-down resistor at the LSCON input to keep the low side MOSFET switched off during power-down, see [Application information](#).

**4 Block description and electrical characteristics**

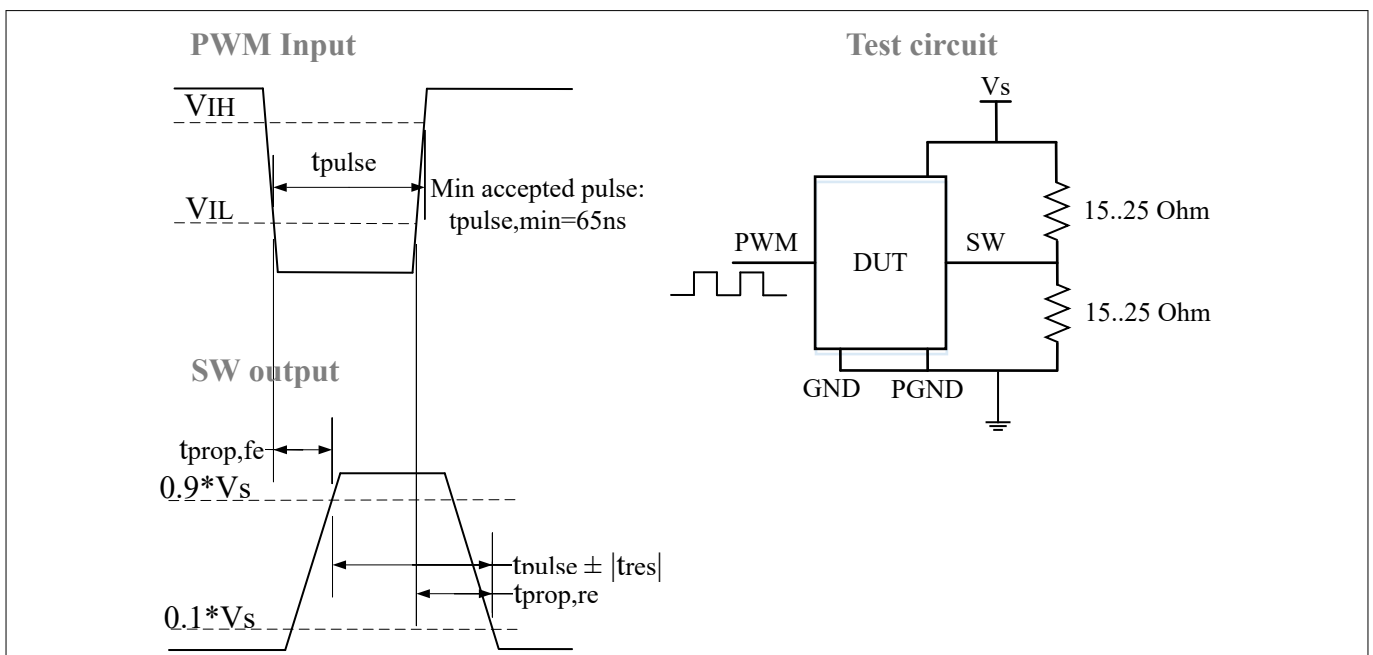
**4.2 Control parameters**

**4.2.1 Functional description control parameters**

The device provides a high frequency switching capability with a low propagation delay. The input stage and the drivers can react to fast changing PWM signals and provide a  $t_{res}$  resolution to the on-time of the input signal with a pulse duration longer than  $t_{pulse}$ . The "low" state pulse duration is limited to  $t_{pulse, min}$ .

The total propagation time  $t_{prop}$  is the time from the "low" to "high" edge transition or from the "high" to "low" edge transition at the PWM input to the SW output level transitions to 10% or 90% of  $V_S$  supply level accordingly. The internal dead time generation provides optimal efficiency during switching phases and performs the state change of the switching node SW within the specified propagation delay.

The device is optimized for a switching frequency in a buck converter application from 0.3 MHz to 2 MHz.



**Figure 3 Control timing diagram**

**4 Block description and electrical characteristics**

**4.2.2 Electrical characteristics control parameters**

**Table 5 Electrical characteristics control parameters**

$V_S = 3.5\text{ V to }7\text{ V}$ ;  $V_{CC} = 2.35\text{ V to }7\text{ V}$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Propagation time, PWM falling edge	$t_{prop,fe}$	–	–	60	ns	High side drain connected to resistive load; $V_{CC} > 3.0\text{ V}$ ; $V_S > 4.5\text{ V}$	P_4.2.1
Propagation time, PWM rising edge	$t_{prop,re}$	–	–	60	ns	Low side drain connected to resistive load; $V_{CC} > 3.0\text{ V}$ ; $V_S > 4.5\text{ V}$	P_4.2.2
Minimum pulse width input	$t_{pulse,min}$	65	–	–	ns	<sup>1)</sup>	P_4.2.3
Pulse resolution time	$t_{res}$	–	–	3	ns	<sup>1)</sup>	P_4.2.4
Dead time "high" to "low"	$t_{dead,hl}$	–	15	–	ns	<sup>1)</sup>	P_4.2.5
Dead time "low" to "high"	$t_{dead,lh}$	–	18	–	ns	<sup>1)</sup>	P_4.2.6
LSCON frequency detector frequency range	$f_{det,lscn}$	0.72	–	–	MHz	–	P_4.2.7
LSCON frequency detector filter time	$t_{fil,lscn}$	3	–	–	$\mu\text{s}$	<sup>1)</sup>	P_4.2.8

**Logic inputs**

Input voltage "high"	$V_{IH}$	$0.67 \times V_{CC}$	–	–	V	CMOS function	P_4.2.9
Input voltage "low"	$V_{IL}$	–	–	$0.33 \times V_{CC}$	V	CMOS function	P_4.2.10
Input voltage hysteresis	$V_{IHYS}$	0.05	–	–	V	–	P_4.2.11
Input capacitance	$C_{IN}$	–	10	–	pF	<sup>1)</sup>	P_4.2.12

<sup>1)</sup> Not subject to production test, specified by design.

**4 Block description and electrical characteristics**

**4.3 Output stage**

**4.3.1 Functional description output stage**

The P-N-channel output half bridge of the device can operate at a switching frequency up to 2 MHz nominal range, providing very low power dissipation in synchronous buck converter topology. The P-channel MOSFET used as high side switch eliminates the need for a charge pump circuitry and improves the EMI performance. The output stage delivers a minimum output current of 2.5 A within the specified voltage and temperature range.

**4.3.2 Electrical characteristics output stage**

**Table 6 Electrical characteristics output stage**

$V_S = 3.5\text{ V to }7\text{ V}$ ;  $V_{CC} = 2.35\text{ V to }7\text{ V}$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin (unless otherwise specified).

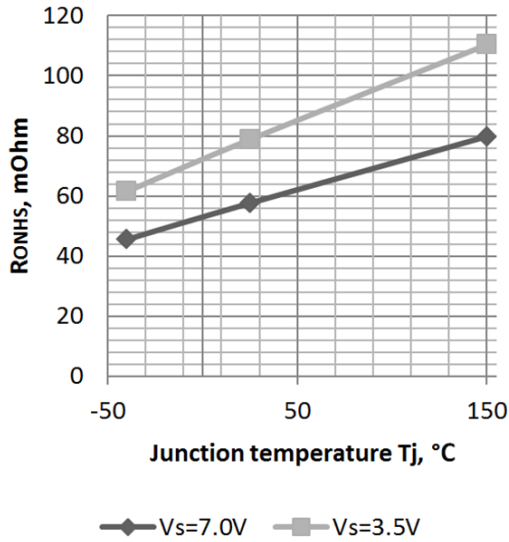
Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
On-state resistance high side	$R_{ONHS}$	-	-	100	mΩ	$T_j \leq 150^\circ\text{C}$ ; $I_d = -2\text{ A}$ ; $V_s = 5.8\text{ V}$	P_4.3.1
		-	-	70	mΩ	<sup>1)</sup> $T_j \leq 85^\circ\text{C}$ ; $I_d = -2\text{ A}$ ; $V_s = 5.8\text{ V}$	P_4.3.2
On-state resistance low side	$R_{ONLS}$	-	-	105	mΩ	$T_j \leq 150^\circ\text{C}$ ; $I_d = 2\text{ A}$ ; $V_s = 5.8\text{ V}$	P_4.3.3
		-	-	75	mΩ	<sup>1)</sup> $T_j \leq 85^\circ\text{C}$ ; $I_d = 2\text{ A}$ ; $V_s = 5.8\text{ V}$	P_4.3.4
Body diode forward voltage high side	$V_{DFHS}$	-	0.67	0.95	V	$I_{fw} = 2\text{ A}$	P_4.3.5
Body diode forward voltage low side	$V_{DFLS}$	-	0.72	0.91	V	$I_{fw} = 2\text{ A}$	P_4.3.6

<sup>1)</sup> Not subject to production test, specified by design.

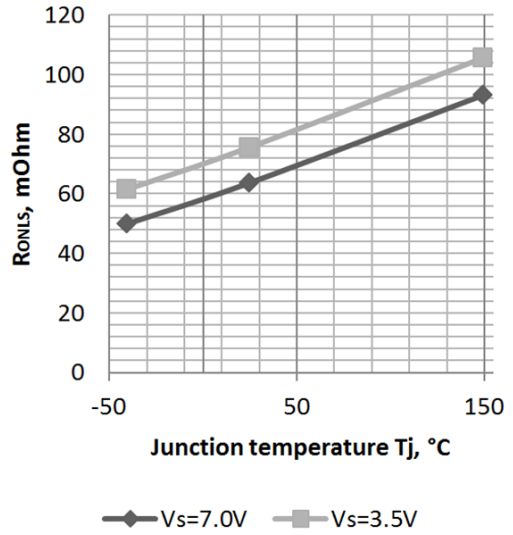
**4 Block description and electrical characteristics**

**4.3.3 Typical performance characteristics output stage**

Maximum on-state resistance high side  $R_{ONHS}$   
(PWM = "low") versus  $T_j = -40^\circ\text{C}, 25^\circ\text{C}, 150^\circ\text{C}$



Maximum on-state resistance low side  $R_{ONLS}$   
(PWM = "high") versus  $T_j = -40^\circ\text{C}, 25^\circ\text{C}, 150^\circ\text{C}$





## 4 Block description and electrical characteristics

### 4.4 Protection functions

The following integrated protection functions prevent the device and the output circuitry from destruction as well as from operation under unspecified conditions:

- High side and low side overcurrent detection and limitation
- Undervoltage shutdown
- Overtemperature protection

The device reacts within the time specified for each protection feature. This is related to the state change of the half bridge MOSFETs independent from the PWM input signal. The device performs the input logic reset release at  $V_S$  voltage exceeding the minimum functional limit of 3.5 V, where protection functions are also operational. For the  $V_{CC}$  voltage below  $V_{CCUV}$ , the output half bridge MOSFETs remain in the off-state and the output switch node SW is floating.

#### 4.4.1 Undervoltage shutdown

##### 4.4.1.1 Functional description undervoltage shutdown

The device monitors the input supply  $V_{CC}$  for undervoltage conditions. If the output voltage drops below the  $V_{CCUV}$  limit, then the device switches off the high side MOSFET and the low side MOSFET, so that the device is only operational within the specified supply limits. The voltage hysteresis circuitry  $V_{CCUVH}$  protects from noise conditions.

##### 4.4.1.2 Electrical characteristics undervoltage shutdown

**Table 7** Electrical characteristics undervoltage shutdown

$V_S = 3.5\text{ V to }7\text{ V}$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Undervoltage limit at $V_{CC}$ supply	$V_{CCUV}$	1.95	–	2.28	V	$V_{CC}$ falling	P_4.4.2.1
Undervoltage detector hysteresis	$V_{CCUVH}$	0.05	–	0.1	V	–	P_4.4.2.2
Undervoltage detector reaction time	$V_{UVR}$	–	–	3	$\mu\text{s}$	1)	P_4.4.2.3

1) Not subject to production test, specified by design.

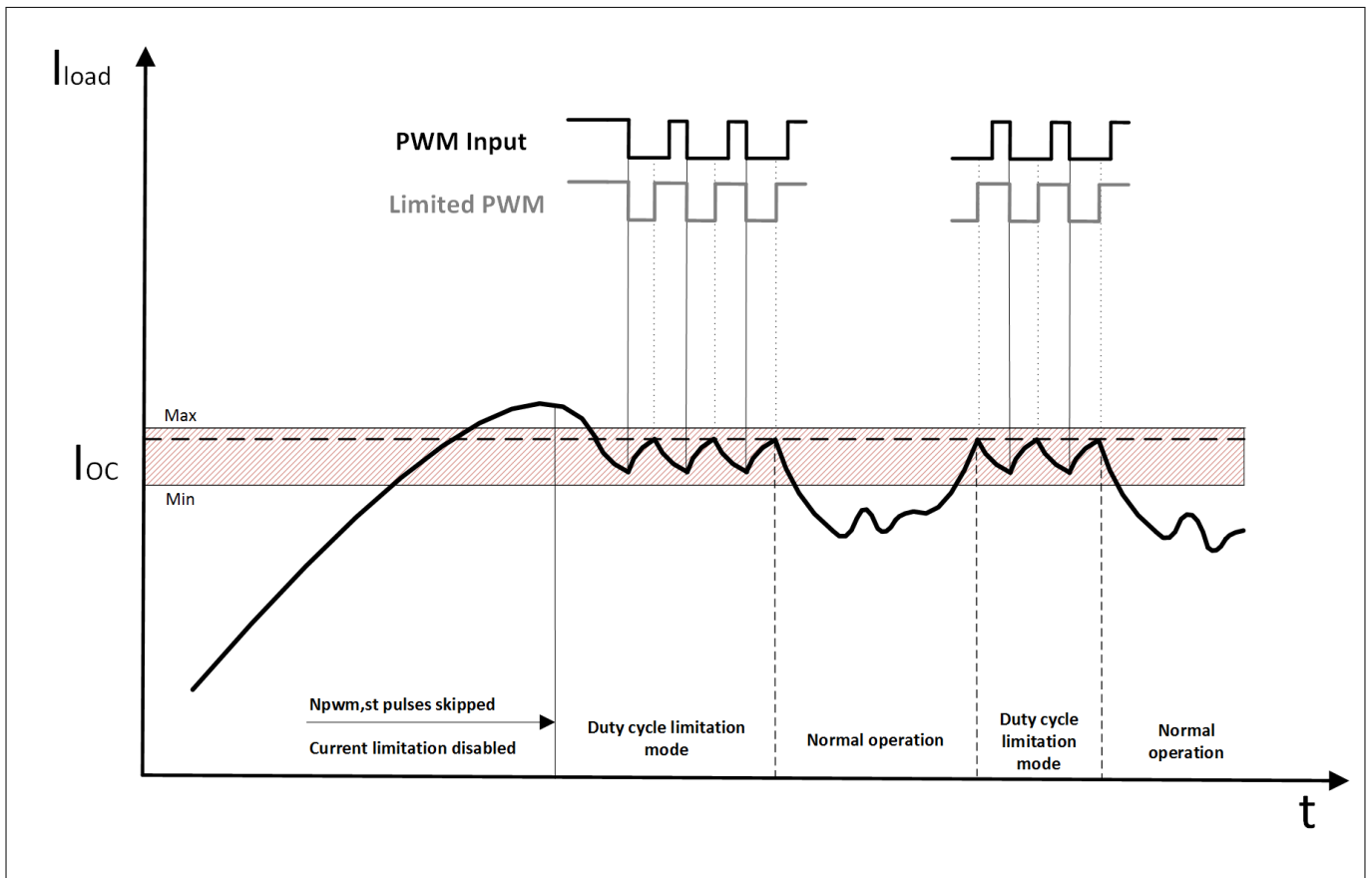
**4 Block description and electrical characteristics**

**4.4.2 Overcurrent protection**

**4.4.2.1 Functional description overcurrent protection**

The overcurrent protection works in a cycle-by-cycle limitation mode. If the sensed input drain current exceeds the peak current limit  $I_{oc,lim}$  during a switching cycle, then the device switches off the high side MOSFET and the switch node SW current decreases. If the overcurrent protection circuitry is active, then the device limits the PWM input duty cycle for each cycle.

During startup or with  $V_{CC}$  supply power cycle after the logic reset is released, the overcurrent protection remains inactive for the number of PWM pulses  $n_{pwm,st}$  to avoid accidental activation due to startup current overshoot.



**Figure 4 Overcurrent protection example**

**4 Block description and electrical characteristics**

**4.4.2.2 Electrical characteristics overcurrent protection**

**Table 8 Electrical characteristics overcurrent protection**

$V_S = 3.5\text{ V to }7\text{ V}$ ;  $V_{CC} = 2.35\text{ V to }7\text{ V}$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Overcurrent sensing limit	$I_{oc,lim}$	-4.4	–	-2.6	A	–	P_4.4.3.1
Startup protection inactive, number of PWM pulses	$n_{pwm,st}$	–	–	5500	–	$V_{CC}$ rising above $V_{CC,min}$	P_4.4.3.2

**4 Block description and electrical characteristics**

**4.4.3 Overtemperature protection**

**4.4.3.1 Functional description overtemperature protection**

If an overtemperature condition  $T_{jOT}$  occurs, then the integrated temperature sensor disables the device by switching off the high side and low side MOSFETs. Only if both the temperature decreases by the hysteresis temperature  $dT_j$  and the temperature falls below  $T_{jSO}$ , then the MOSFETs resume operation.

**4.4.3.2 Electrical characteristics overtemperature protection**

**Table 9 Electrical characteristics overtemperature protection<sup>1)</sup>**

$V_S = 3.5\text{ V to }7\text{ V}$ ;  $V_{CC} = 2.35\text{ V to }7\text{ V}$ ;  $T_j = -40^\circ\text{C to }150^\circ\text{C}$ ; all voltages with respect to ground; positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Overtemperature shutdown	$T_{jOT}$	175	–	200	°C	–	P_4.4.4.1
Switch-on temperature	$T_{jSO}$	–	–	165	°C	–	P_4.4.4.2
Overtemperature switch-on hysteresis	$dT_j$	–	15	–	°C	–	P_4.4.4.3

1) Not subject to production test, specified by design.

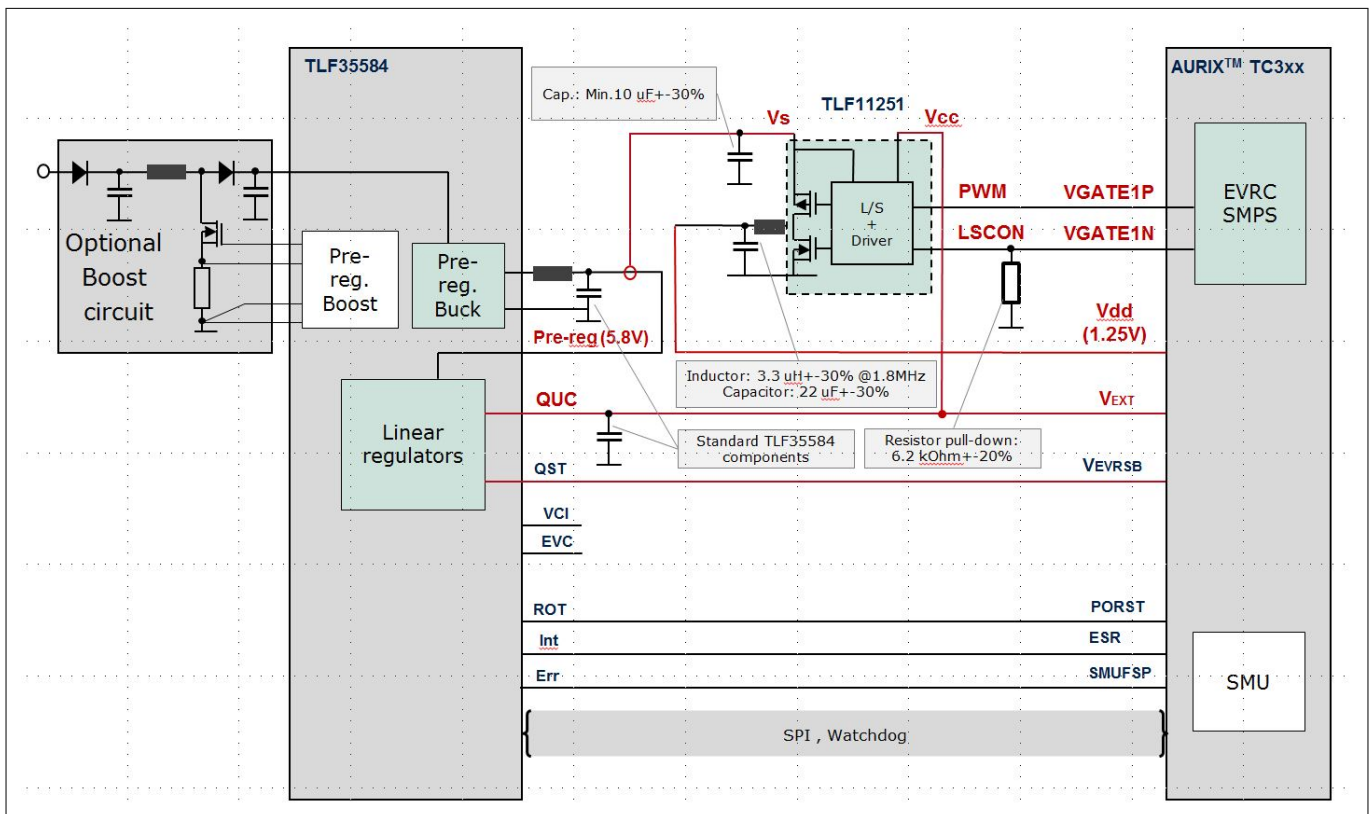
**5 Application information**

**5 Application information**

**Note:** *The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**5.1 Application diagram**

In the target application scenario the device is the counterpart for an AURIX™ TC3xx microcontroller for core voltage generation with the system power supply TLF35584. The device configuration allows connectivity with the half bridge control output of the microcontroller’s embedded voltage regulator core (EVRC) converter, which generates the core voltage  $V_{dd}$ . The device only supports power supply topologies that use different sources for the microcontroller supply domain  $V_{ext}$  and the EVRC input  $V_S$ , expecting different voltage levels.  $V_S$  must exceed  $V_{CC}$  during startup, in normal operation and during power-down.



**Figure 5 Application diagram**

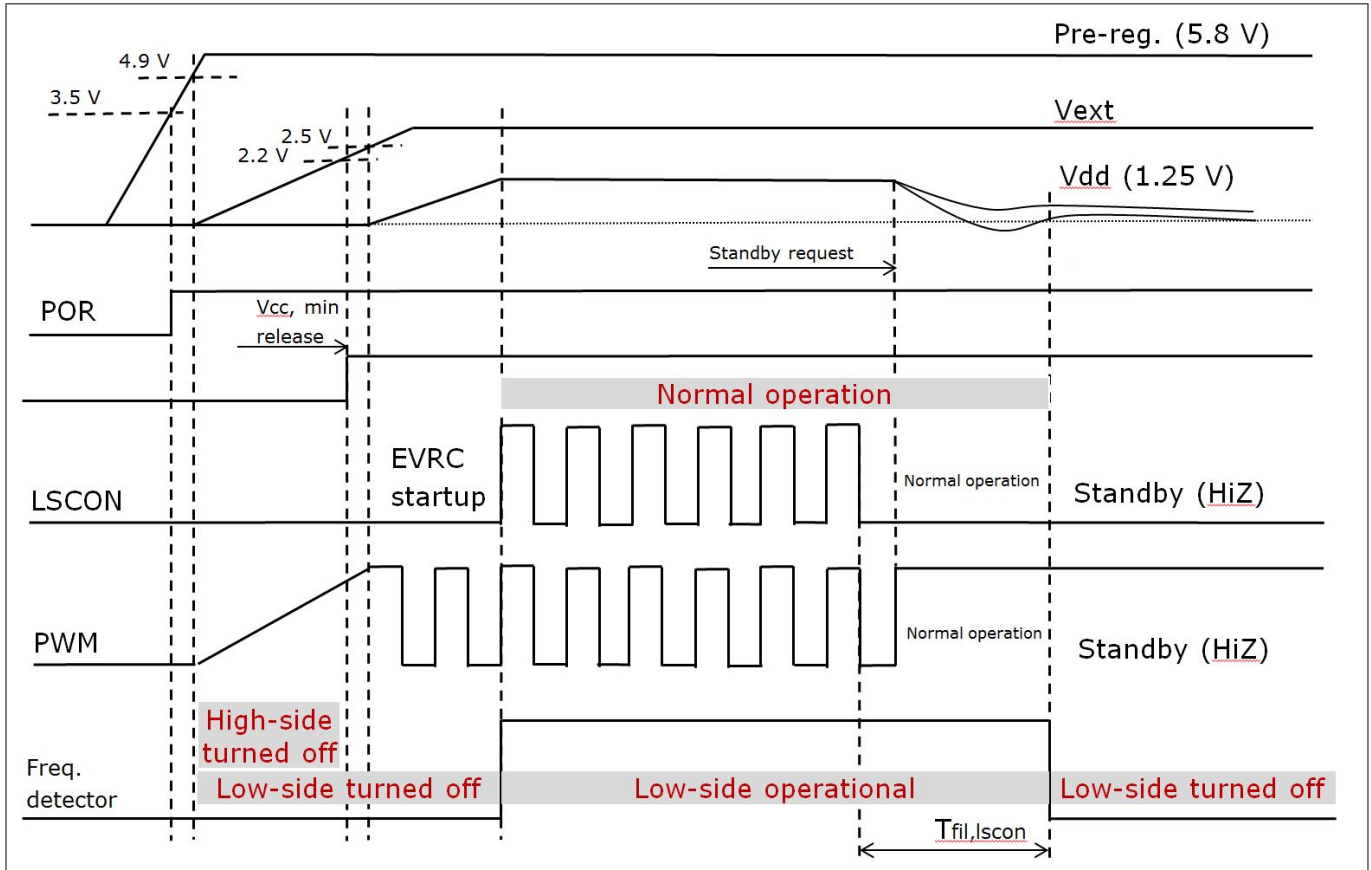
**Note:** *This figure is a simplified example of an application circuit. The function must be verified in the application.*

As soon as  $V_S$  voltage reaches 3.5 V during power-up, the device releases the internal logic reset. During this phase the central function logic is operational. Only if  $V_{CC}$  is within the specified range, then the device reacts to the input signals LSCON and PWM as specified. However, the operational  $V_{CC}$  voltage minimum is specified at 2.35 V, which allows for early device readiness, even if the microcontroller is not yet operational.

The VGATEP output of the microcontroller controls the PWM signal, while the VGATEN output is connected to LSCON. The microcontroller typically starts in an open loop mode, controlling only VGATEP and allowing for fast  $V_{dd}$  voltage ramp-up and startup. After ramp-up time, the EVRC starts to control the high side and low side MOSFETs of the half bridge. The LSCON input detects this phase with the frequency detector. If the microcontroller is switched into power-down mode and if the high side and low side control signals are off,

**5 Application information**

then the frequency detector recognizes it as a request to set the SW output floating. Therefore add a pull-down resistor for the LSCON signal in order to limit its possible variation during the power-down phase after the supply voltage reaches the hard reset limit of the microcontroller.



**Figure 6 Start-up and ramp-down example**

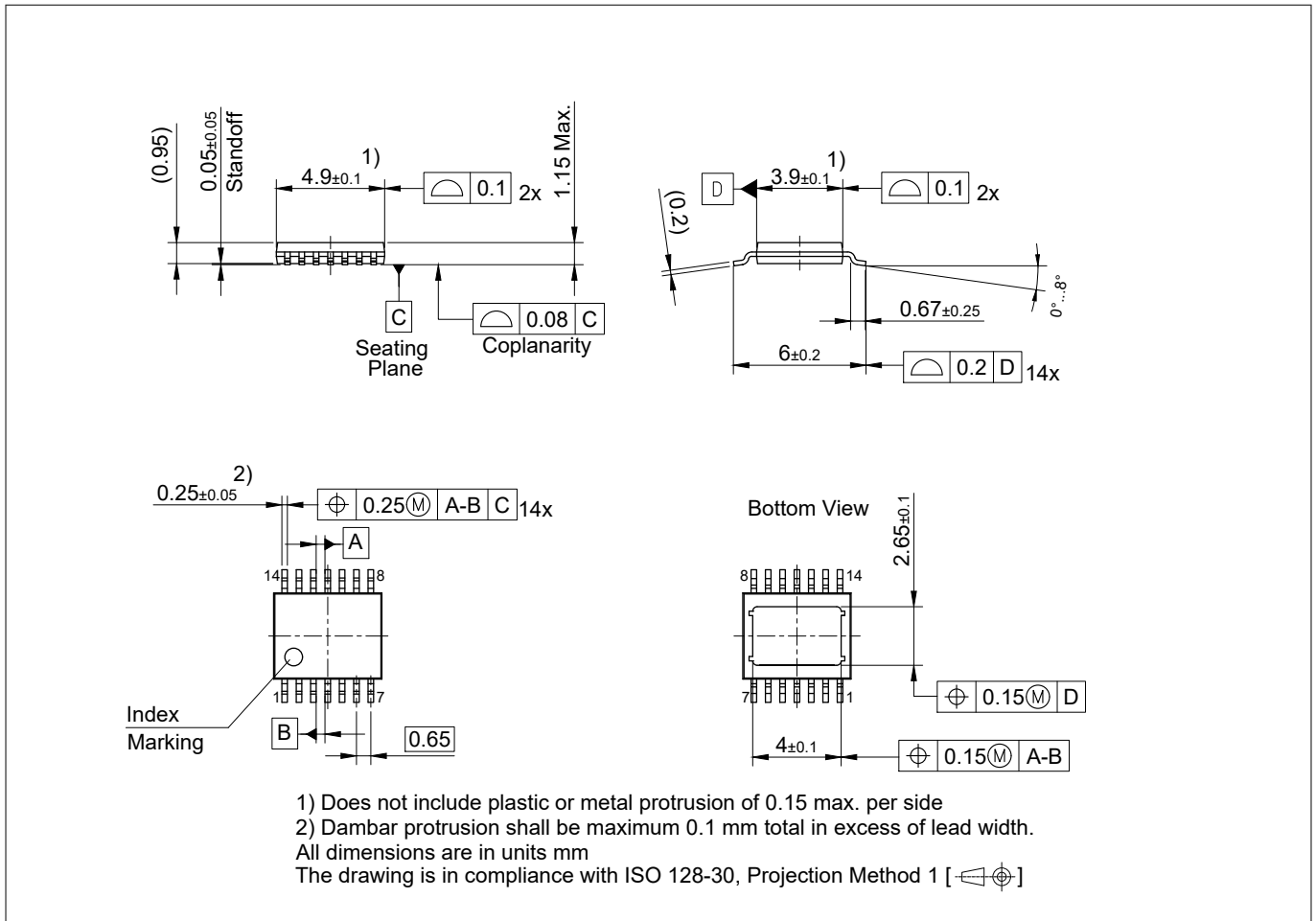
Table 10 shows the required nominal values of the discrete components for proper operation.

**Table 10 Nominal values of discrete components**

Component name	Nominal value	Acceptable variation	Note
$C_{VS}$	10 $\mu$ F	$\pm 30\%$	Input capacitor
$C_{VDD}$	22 $\mu$ F	$\pm 30\%$	Output capacitor
$L_{VDD}$	3.3 $\mu$ H	$\pm 30\%$ (@ 1.8 MHz)	Output inductor
$R_{LSCON}$	6.2 k $\Omega$	$\pm 20\%$	LSCON input pull-down

**6 Package information**

**6 Package information**



**Figure 7 PG-TSDSO-14**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Information on alternative packages**

Please visit [www.infineon.com/packages](http://www.infineon.com/packages).

**Revision history**

**Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.04	2024-10-02	Package information: dimension
1.03	2022-11-25	Editorial changes
1.02	2021-02-05	Editorial changes
1.01	2021-01-14	Editorial changes
1.0	2020-01-23	Datasheet created



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**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

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