

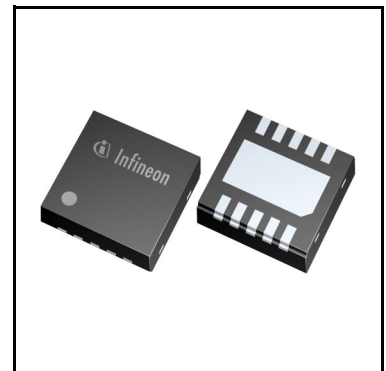
OPTIREG™ linear TLF4277-2LD

Low dropout linear voltage regulator with integrated current monitor



Features

- Integrated current monitor
- Overvoltage, overtemperature, and overcurrent detection
- Adjustable output voltage
- Output current up to 300 mA
- Adjustable output current limitation
- Stable with ceramic output capacitor of 1 μ F
- Wide input voltage range up to 40 V
- Reverse-polarity protection
- Short-circuit protected
- Overtemperature shutdown
- Automotive temperature range $-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$
- Green Product (RoHS- and WEEE-compliant)



Potential applications

- Automotive sensor, camera, and peripheral supply
- Active antenna supply
- Automotive applications that are permanently connected to the battery

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLF4277-2LD is the ideal companion IC to supply active antennas for car infotainment and telematics applications. The adjustable current limitation, adjustable output voltage, and the diagnostic features make the TLF4277-2LD capable of supplying the majority of standard active antennas, such as GPS, GNSS, FM/AM, DAB, XM, and SIRIUS.

The TLF4277-2LD is a monolithic integrated low dropout voltage regulator capable of supplying loads up to 300 mA. For an input voltage up to 40 V, the TLF4277-2LD provides an adjustable output voltage in a range from 5 V up to 12 V. The integrated current monitor function is a unique feature that provides diagnosis and system-protection functionality. Fault conditions such as overtemperature and output overvoltage are

OPTIREG™ linear TLF4277-2LD
Low dropout linear voltage regulator with integrated current monitor



monitored and indicated at the current-sense output. The maximum output current-limit of the device is adjustable to provide additional protection to the connected load.

Via the enable function, the IC can be disabled to lower the power consumption.

Type	Package	Marking
TLF4277-2LD	PG-TSON-10	4277-2

Table of contents

	Features	1
	Potential applications	1
	Product validation	1
	Description	1
	Table of contents	3
1	Block diagram	4
2	Pin configuration	5
2.1	Pin assignment	5
2.2	Pin definitions and functions	5
3	General product characteristics	6
3.1	Absolute maximum ratings	6
3.2	Functional range	7
3.3	Thermal resistance	8
4	Voltage regulator	9
4.1	Description of the voltage regulator	9
4.2	Electrical characteristics of the voltage regulator	10
4.3	Application information for setting the variable output voltage	11
4.4	Typical performance characteristics voltage regulator	12
5	Current consumption	13
5.1	Electrical characteristics of the current consumption	13
5.2	Typical performance graphs current consumption	14
6	Current and protection monitor functions	15
6.1	Description current and protections monitor	15
6.1.1	Linear current monitor	16
6.1.2	Adjustable output-current limitation	17
6.1.3	Overvoltage detection	17
6.1.4	Thermal shutdown detection	17
6.1.5	Status output signal	17
6.2	Electrical characteristics current monitor function	18
6.3	Typical performance graphs current monitor function	19
7	Enable function	20
7.1	Description of the enable function	20
7.2	Electrical characteristics enable function	20
8	Application information	21
8.1	Application diagram	21
8.2	Selection of external components	22
8.2.1	Input pin	22
8.2.2	Output pin	22
8.3	Thermal considerations	23
8.4	Reverse polarity protection	24
8.5	Further application information	24
9	Package information	25
10	Revision history	26

Pin configuration

2 Pin configuration

2.1 Pin assignment

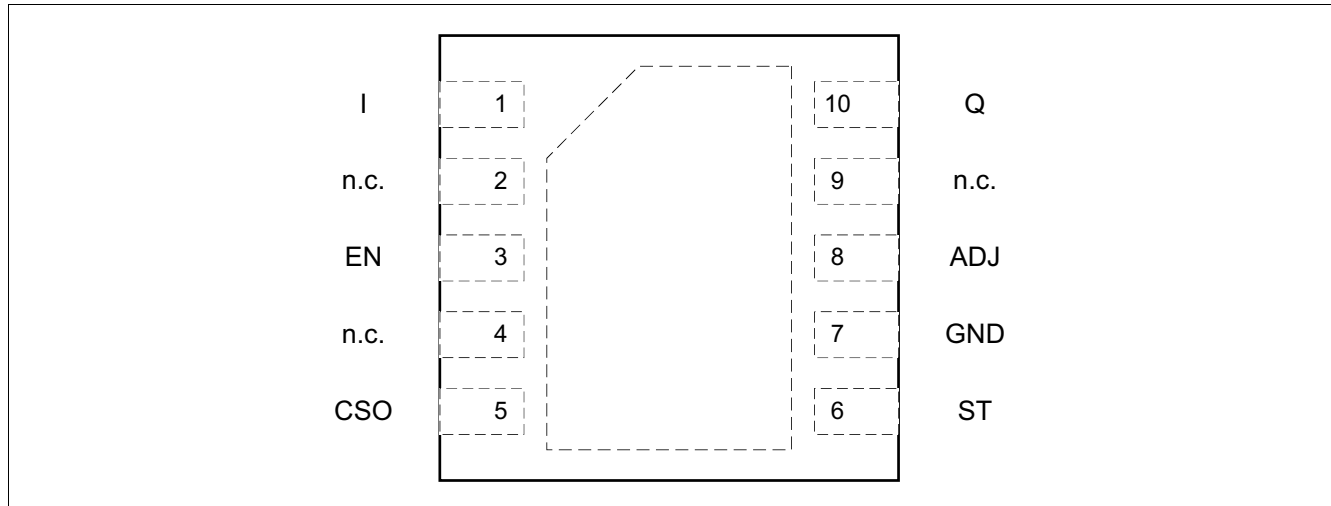


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

Pin	Symbol	Function
1	I	IC supply Place a capacitor from I to GND close to the IC for compensating line influences
3	EN	Enable High signal enables the regulator Low signal disables the regulator Connect to I if the enable function is not needed
5	CSO	Current sense out Current monitor and status output
6	ST	Status output Digital output signal with open-collector output A low signal indicates fault conditions at the regulator's output
7	GND	Ground
8	ADJ	Voltage adjust Connect an external voltage divider to configure the output voltage
10	Q	Regulator output Connect a capacitor between Q and GND close to the IC pins, respecting the values given for its capacitance C_Q and ESR in the table Table 2
	PAD	Heat sink Connect to PCB heat sink area and GND
2, 4, 9	n.c.	Not connected Internally not connected; connect to PCB GND

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings¹⁾

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage ratings							
IC supply I	V_I	-16	-	45	V	-	P_4.1.1
Enable input EN	V_{EN}	-16	-	45	V	-	P_4.1.2
Voltage-adjust input ADJ	V_{ADJ}	-0.3	-	16	V	-	P_4.1.3
Regulator output Q	V_Q	-0.3	-	45	V	$V_Q < V_I + 5\text{ V}$	P_4.1.4
Current-monitor out CSO	V_{CSO}	-0.3	-	5	V	-	P_4.1.5
Status output	V_{ST}	-0.3	-	45	V	²⁾ See also Status output signal	P_4.1.6

Temperatures

Junction temperature	T_j	-40	-	150	°C	-	P_4.1.7
Storage temperature	T_{stg}	-55	-	150	°C	-	P_4.1.8

ESD susceptibility

ESD susceptibility to GND	V_{ESD}	-2	-	2	kV	³⁾ HBM	P_4.1.9
ESD susceptibility to GND	V_{ESD}	-500	-	500	V	⁴⁾ CDM	P_4.1.10
ESD susceptibility pin 1, 5, 6, 10 (corner pins) to GND	$V_{ESD1,5,6,10}$	-750	-	750	V	⁴⁾ CDM	P_4.1.11

- 1) Not subject to production test, specified by design.
- 2) Special care must be taken to control (for example, by optical inspection) the proper handling of ST pin with an external resistor and not connecting directly to a higher voltage level, which allows an uncontrolled current flowing into the pin.
- 3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
- 4) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101.

Notes

1. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.
2. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

General product characteristics

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	$V_Q + V_{dr}$	–	40	V	–	P_4.2.1
Output voltage range	V_Q	5	–	12	V	–	P_4.2.2
Current sense output resistor	R_{CSO}	850	–	25.5	k Ω	–	P_4.2.3
Current sense output capacitor	C_{CSO}	1	–	4.7	μ F	¹⁾	P_4.2.4
Junction temperature	T_j	-40	–	150	$^{\circ}$ C	–	P_4.2.5
Output capacitor requirements	C_Q	1	–	–	μ F	¹⁾²⁾	P_4.2.6
Output capacitor requirements	$ESR(C_Q)$	–	–	10	Ω	¹⁾³⁾	P_4.2.7

1) Not subject to production test, specified by design.

2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

3) Relevant ESR value at $f = 10$ kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

General product characteristics

3.3 Thermal resistance

Table 3 Thermal resistance¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	9	–	K/W	Measured to the exposed pad	P_4.3.1
Junction to ambient	R_{thJA}	–	165	–	K/W	²⁾ Footprint only	P_4.3.2
Junction to ambient	R_{thJA}	–	67	–	K/W	²⁾ 300 mm ² PCB heat sink area	P_4.3.3
Junction to ambient	R_{thJA}	–	56	–	K/W	²⁾ 600 mm ² PCB heat sink area	P_4.3.4
Junction to ambient	R_{thJA}	–	55	–	K/W	³⁾ 2s2p PCB	P_4.3.5

- 1) Not subject to production test, specified by design.
- 2) The specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 μm Cu).
- 3) The specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.

Voltage regulator

4 Voltage regulator

4.1 Description of the voltage regulator

The output voltage V_Q is controlled by comparing the feedback voltage (V_{ADJ}) to an internal reference voltage and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q , the output capacitor ESR, the load current, and the chip temperature. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in [Table 2](#) have to be maintained. For stability details, refer to the typical performance graph [Output capacitor series resistivity ESR\(\$C_Q\$ \) versus output current \$I_Q\$](#) . In addition, the output capacitor may need to be sized larger to buffer load transients.

An input capacitor C_I is not needed for the control-loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals. In general, a buffered supply voltage is recommended for the device. For details, see [Chapter 8.1](#).

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. The integrated safeguards consist of output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, an integrated safe operation monitor lowers the maximum output current for input voltages above $V_{BAT} = 22\text{ V}$.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (for example, output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to a cycling behavior of the output voltage until the fault is removed. However, junction temperatures above 150°C are outside the maximum ratings and therefore significantly reduce the IC lifetime.

The TLF4277-2LD allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This reverse current has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

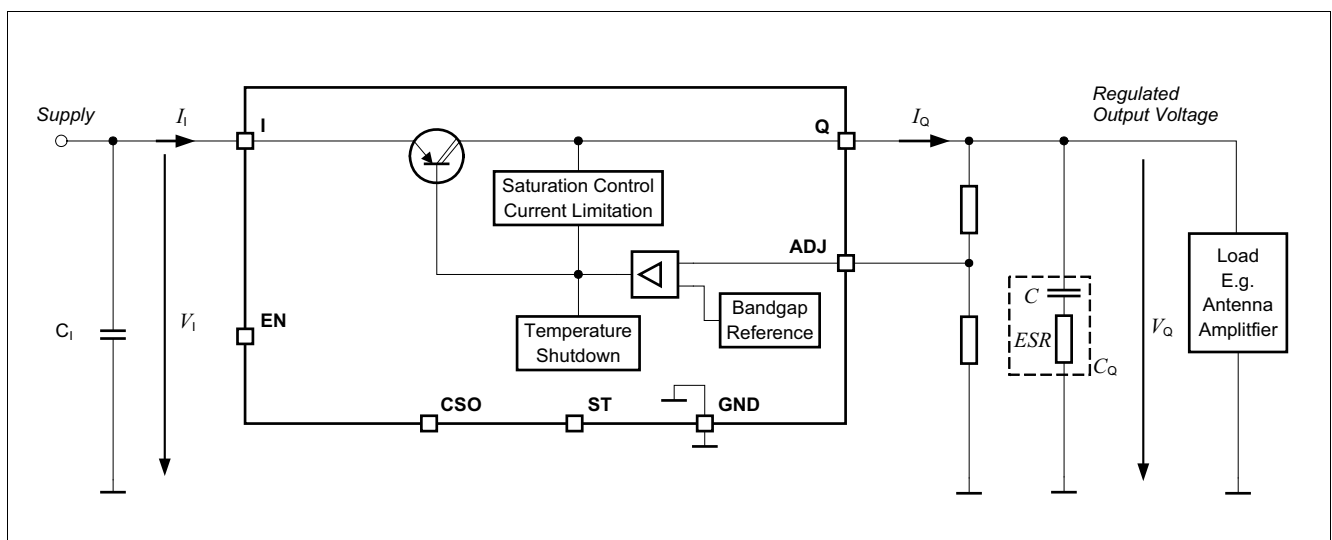


Figure 3 Block diagram of the voltage regulator circuit

Voltage regulator

4.2 Electrical characteristics of the voltage regulator

Table 4 Electrical characteristics of the voltage regulator

$V_{BAT} = 13.5\text{ V}$, $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference voltage	$V_{REF,int}$	-	1.19	-	V	1)	P_5.2.1
Output voltage tolerance	V_Q	-2	-	2	%	2) $1\text{ mA} \leq I_Q \leq 300\text{ mA}$; $9\text{ V} \leq V_{BAT} \leq 16\text{ V}$ $5\text{ V} \leq V_Q \leq 12\text{ V}$ with $V_{BAT} > V_Q + 2\text{ V}$	P_5.2.2
Output voltage tolerance	V_Q	-2	-	2	%	2) $1\text{ mA} \leq I_Q \leq 150\text{ mA}$; $6\text{ V} \leq V_{BAT} \leq 16\text{ V}$ $5\text{ V} \leq V_Q \leq 12\text{ V}$ with $V_{BAT} > V_Q + 1\text{ V}$	P_5.2.3
Output voltage tolerance	V_Q	-2	-	2	%	2)3) $1\text{ mA} \leq I_Q \leq 100\text{ mA}$; $16\text{ V} \leq V_{BAT} \leq 32\text{ V}$ $5\text{ V} \leq V_Q \leq 12\text{ V}$	P_5.2.4
Output voltage tolerance	V_Q	-2	-	2	%	2)3) $1\text{ mA} \leq I_Q \leq 10\text{ mA}$; $32\text{ V} \leq V_{BAT} \leq 40\text{ V}$ $5\text{ V} \leq V_Q \leq 12\text{ V}$	P_5.2.5
Load regulation steady-state	$\Delta V_{Q,load}$	-30	-5	-	mV	$I_Q = 1\text{ mA}$ to 250 mA ; $V_{BAT} = 6\text{ V}$; $V_Q = 5\text{ V}$	P_5.2.7
Line regulation steady-state	$\Delta V_{Q,line}$	-	5	20	mV	$V_{BAT} = 6\text{ V}$ to 32 V ; $I_Q = 5\text{ mA}$; $V_Q = 5\text{ V}$	P_5.2.8
Power supply ripple rejection ¹⁾	$PSRR$	60	65	-	dB	$f_{ripple} = 100\text{ Hz}$; $V_{ripple} = 1\text{ V}_{pp}$; $V_Q = 5\text{ V}$; $I_Q < 100\text{ mA}$	P_5.2.9
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	-	100	250	mV	4) $I_Q = 100\text{ mA}$ $V_Q = 5\text{ V}$	P_5.2.10
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	-	200	500	mV	4) $I_Q = 200\text{ mA}$ $V_Q = 5\text{ V}$	P_5.2.11
Output current limitation	$I_{Q,max}$	301	-	700	mA	$0\text{ V} \leq V_Q \leq 0.95 \times V_{Q,nom}$	P_5.2.13
Reverse current	I_Q	-2	-1	-	mA	$V_{BAT} = 0\text{ V}$; $V_Q = 5\text{ V}$	P_5.2.14
Reverse current at negative input voltage	I_{BAT}	-10	-6	-	mA	$V_{BAT} = -16\text{ V}$; $V_Q = 0\text{ V}$	P_5.2.15
Overtemperature shutdown threshold	$T_{j,sd}$	151	-	200	°C	1) T_j increasing	P_5.2.16
Overtemperature shutdown threshold hysteresis	$T_{j,hy}$	-	15	-	K	1) T_j decreasing	P_5.2.17

1) Parameter not subject to production test; specified by design.

2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.

3) See typical performance graph for details.

4) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

Voltage regulator

4.3 Application information for setting the variable output voltage

The output voltage of the TLF4277-2LD can be adjusted between 5 V and 12 V by an external output voltage divider, closing the control loop to the voltage adjust pin ADJ.

The voltage at pin ADJ is compared to the internal reference of typical 1.19 V in an error amplifier. It controls the output voltage.

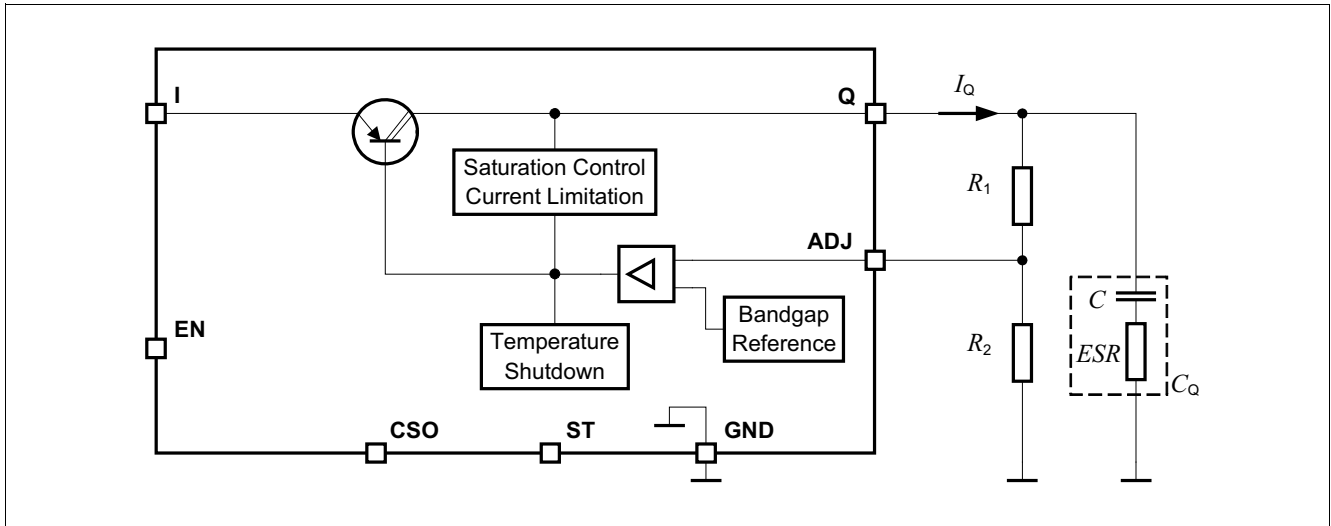


Figure 4 Application detail external components at output for variable voltage regulator

The output voltage is calculated according to [Equation \(4.1\)](#):

$$V_Q = (R_1 + R_2)/R_2 \times V_{REF,int}, \text{ neglecting } I_{ADJ} \quad (4.1)$$

$V_{REF,int}$ is typically 1.19 V.

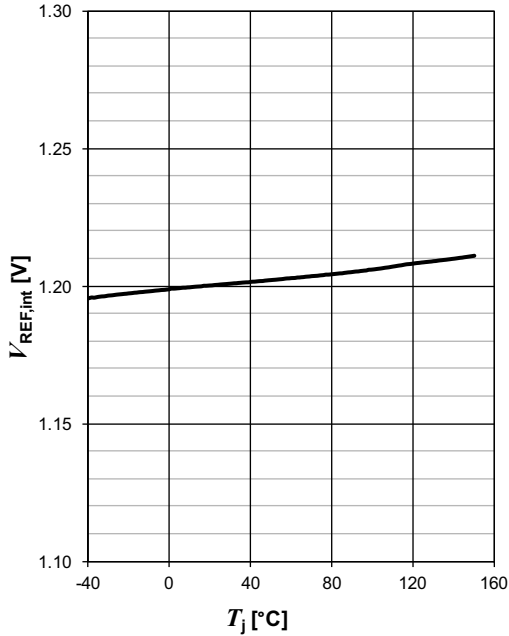
To avoid errors caused by leakage current I_{ADJ} , we recommend to choose the resistor value for $R_2 < 27 \text{ k}\Omega$.

The accuracy of the resistors for the external voltage divider can lead to a higher tolerance of the output voltage. To achieve a reasonable accuracy, resistors with a tolerance of 1% or lower are recommended for the feedback divider.

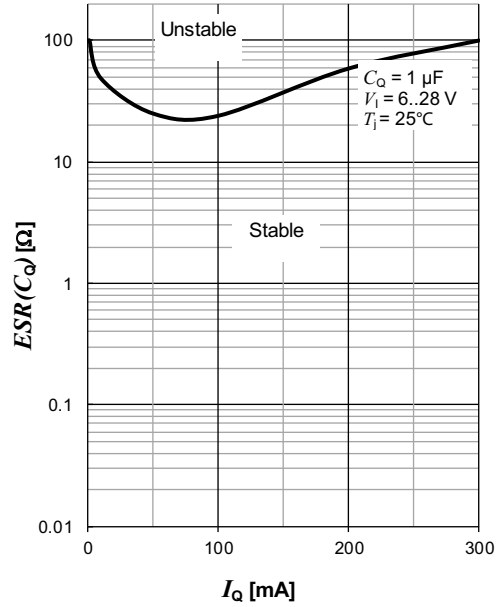
Voltage regulator

4.4 Typical performance characteristics voltage regulator

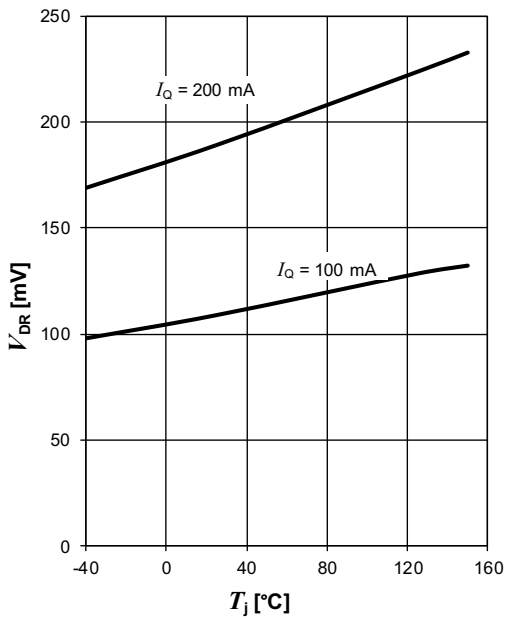
Reference voltage $V_{REF,int}$ versus junction temperature T_j



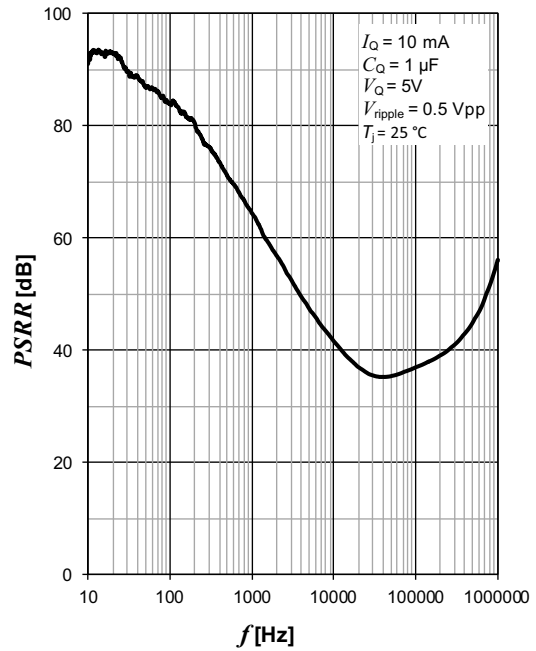
Output capacitor series resistivity $ESR(C_Q)$ versus output current I_Q



Dropout voltage V_{DR} versus junction temperature T_j



Power supply ripple rejection $PSRR$



Current consumption

5 Current consumption

5.1 Electrical characteristics of the current consumption

Table 5 Electrical characteristics of the current consumption

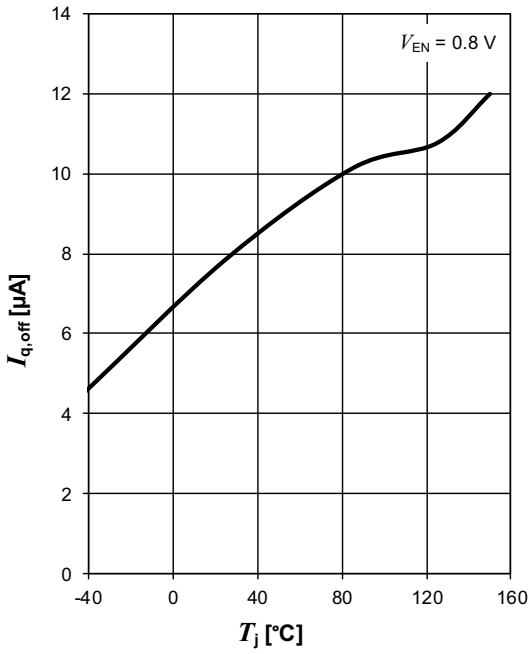
$V_{BAT} = 13.5\text{ V}$, $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground; direction of currents as shown in [Figure 7](#) (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption	$I_{q,on}$	–	150	200	μA	$I_Q \leq 200\ \mu\text{A}$; $T_j \leq 25^\circ\text{C}$; $V_{EN} = 5\ \text{V}$; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.1
Current consumption	$I_{q,on}$	–	–	250	μA	$I_Q \leq 200\ \mu\text{A}$; $T_j \leq 85^\circ\text{C}$; $V_{EN} = 5\ \text{V}$; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.2
Current consumption	$I_{q,on}$	–	1.2	2.6	mA	$I_Q = 50\ \text{mA}$; $V_{EN} = 5\ \text{V}$; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.3
Current consumption	$I_{q,on}$	–	5.5	11	mA	$I_Q = 200\ \text{mA}$; $V_{EN} = 5\ \text{V}$; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.4
Current consumption	$I_{q,off}$	–	–	3	μA	$T_j \leq 25^\circ\text{C}$; $V_{EN} = 0\ \text{V}$ $I_q = I_I - I_Q$	P_6.1.5
Current consumption	$I_{q,off}$	–	–	5	μA	$T_j \leq 85^\circ\text{C}$; $V_{EN} = 0\ \text{V}$ $I_q = I_I - I_Q$	P_6.1.6
Current consumption	$I_{q,off}$	–	–	15	μA	$T_j \leq 85^\circ\text{C}$; $V_{EN} = 0.8\ \text{V}$ $I_q = I_I - I_Q$	P_6.1.7

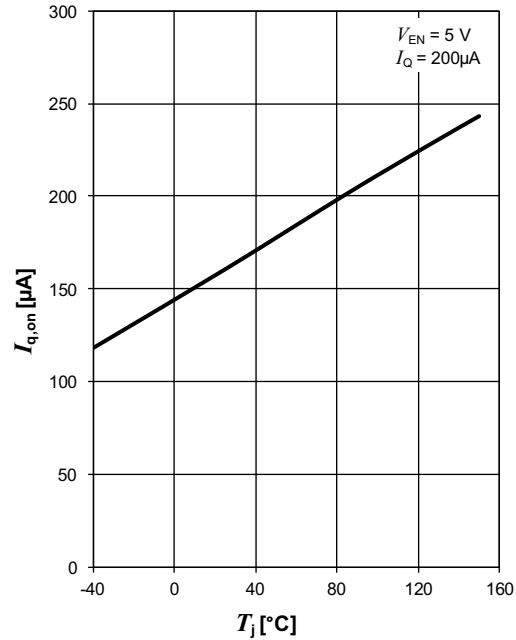
Current consumption

5.2 Typical performance graphs current consumption

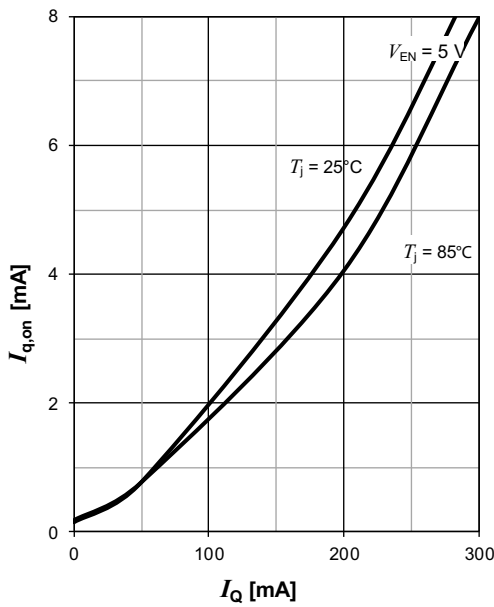
Current consumption $I_{q,off}$ versus junction temperature T_j



Current consumption $I_{q,on}$ versus junction temperature T_j



Current consumption $I_{q,on}$ versus output current I_Q



6 Current and protection monitor functions

6.1 Description current and protections monitor

The TLF4277-2LD provides a set of advanced monitor functionality. The current flowing out of the power stage can be monitored at the CSO output. In addition the current limitation can be adjusted via external resistor. Events of the implemented protection functions are reported through dedicated voltage levels at the CSO output. This information can be processed by an external μC for system analysis and failure identification. The monitored events are overcurrent, overvoltage, and temperature shutdown. In addition, all three fault conditions are routed also to the digital output pin ST.

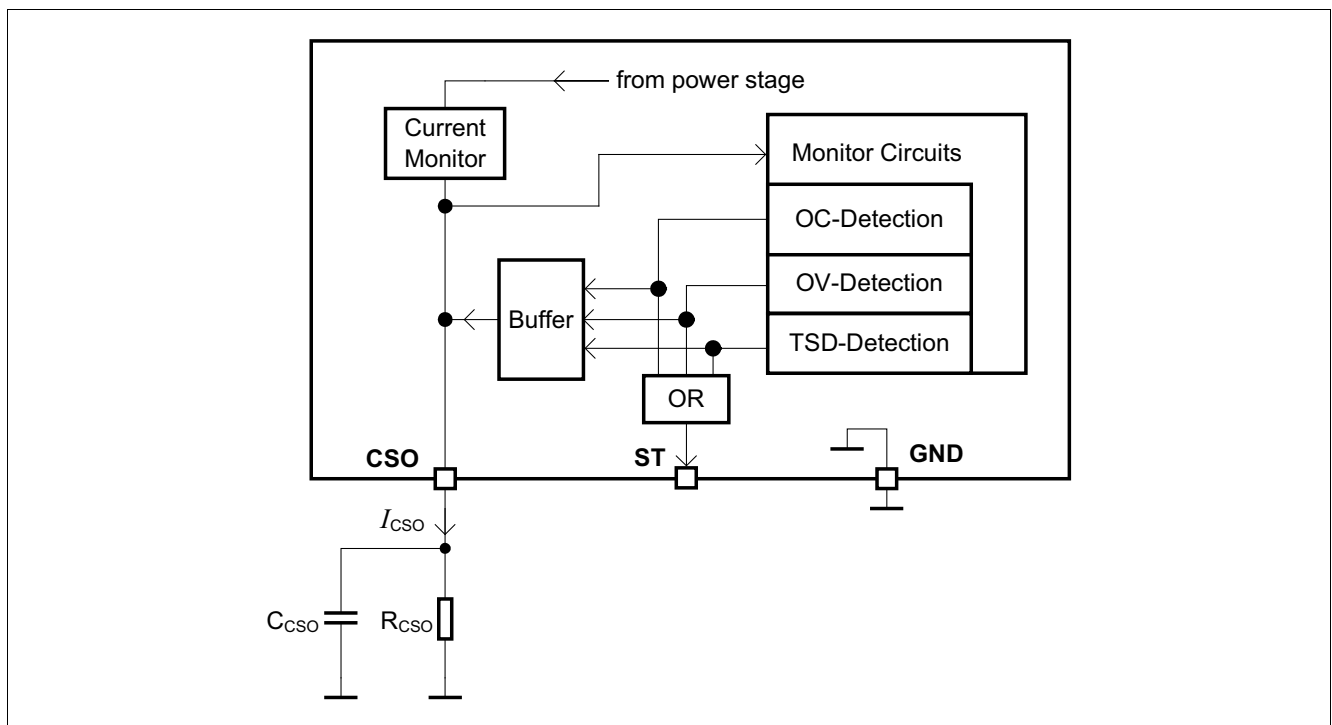


Figure 5 Block diagram of the current and protection monitor

To reduce possible effects from the supply voltage V_{BAT} , additional filtering of the supply voltage is recommended. A 100-nF capacitor should be placed as close a possible to the IC terminal, which is connected to V_{BAT} .

Figure 6 shows the output level at the CSO pin versus the operation or fault condition. The graph is valid for the following setup of external components:

$$C_{\text{CSO}} = 2.2 \mu\text{F}$$

$$R_{\text{CSO}} = 1.5 \text{ k}\Omega$$

Note: In case of high input voltage ($V_i > 20 \text{ V}$), high junction temperature ($T_j > 151^\circ\text{C}$), and CSO pin directly connected to GND without resistor, the return to normal operation from the “thermal shutdown mode” cannot be ensured.

Current and protection monitor functions

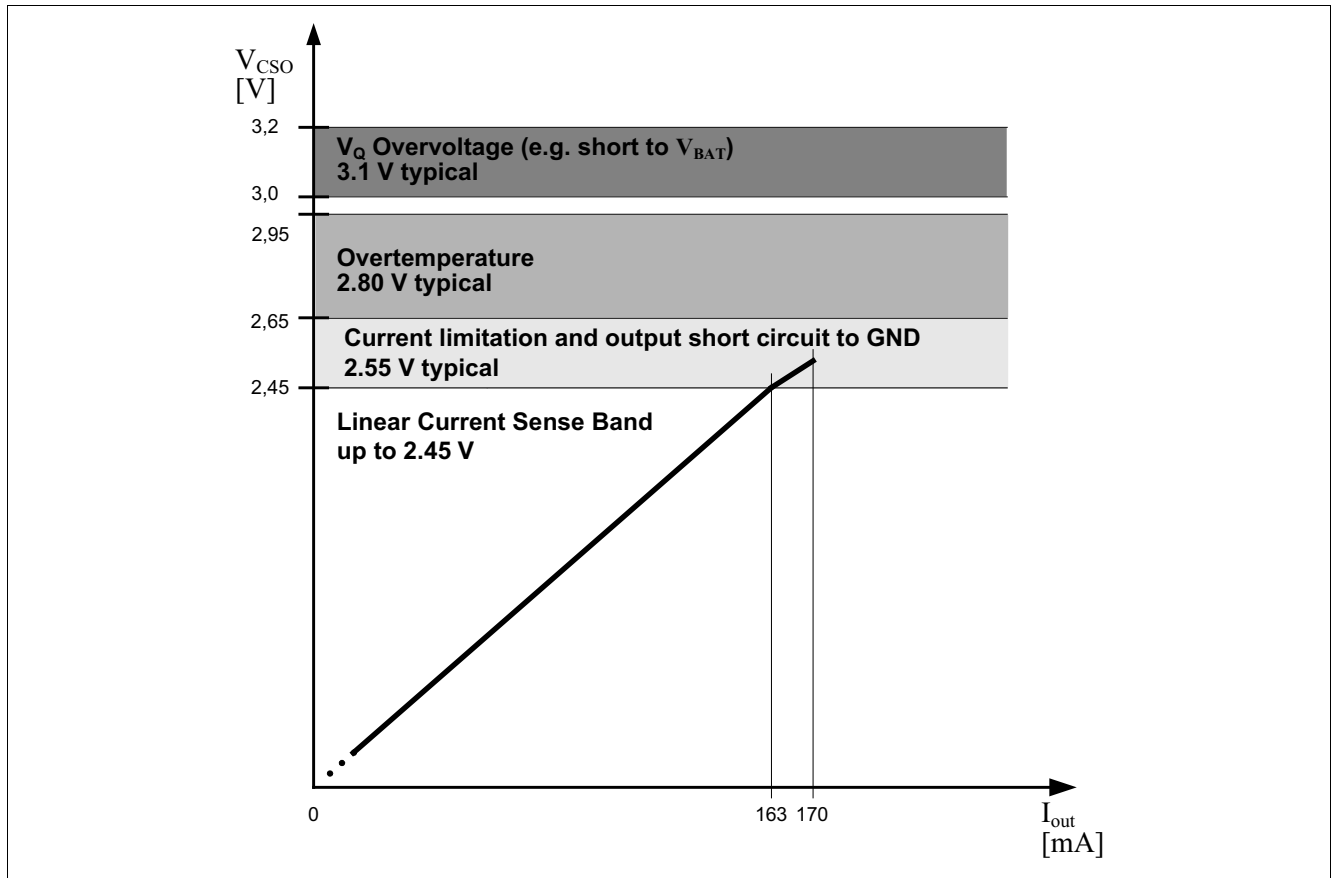


Figure 6 Output levels and functionality of the CSO output

Note: The graph is just an example and only valid for a certain configuration of the external components.

6.1.1 Linear current monitor

Inside the linear current monitor area, the current driven out of the CSO pin is direct proportional to the output current (I_Q).

The level of the current I_{CSO} can be calculated according to **Equation (6.1)**:

(6.1)

$$I_{CSO} = \frac{I_Q}{F_{I_Q/I_{CSO}}}$$

Current and protection monitor functions

6.1.2 Adjustable output-current limitation

The TLF4277-2LD has an adjustable current limitation for the current flowing out of the power stage. If the level of the output current exceeds the defined current-limit threshold ($I_{Q,lim}$), the output current of the TLF4277-2LD will be limited.

Setting of the adjustable current limitation: (6.2)

$$I_{Q,lim} = \frac{2.55V \times F_{I_{Q}/CSO}}{R_{CSO}}$$

A voltage level as defined in **CSO voltage level current limitation** will be applied at the CSO pin. In addition, the ST pin will be set low.

Note: During power-up of the device, the regulator works in output current limitation. Regardless if the output current is limited by the protection function according to **Output current limitation**, or by the adjustable output current limitation according to **Adjustable current-limit range**. If an adjustable current limit is set, the status output pin ST is set to low as long as the adjustable current limitation is active during power-up sequence.

Example: To achieve a current limitation of e.g. 170 mA, the following configuration can be used:

$$I_{Q,lim} = \frac{2.55V \times 100}{1.5k\Omega} = 170mA$$

$$F_{I_{Q}/CSO} = 100$$

$$R_{CSO} = 1.5 k\Omega$$

6.1.3 Overvoltage detection

To detect a possible short circuit of the output to a higher supply rail the TLF4277-2LD has an overvoltage detection implemented. An overvoltage will be detected, if the voltage level at the ADJ pin is 20% higher than the internal reference voltage $V_{REF,int}$ defined in **Reference voltage**.

In case of overvoltage the CSO pin will set to a voltage level as defined in **CSO voltage level overvoltage detected**. In addition the ST pin will be set low.

6.1.4 Thermal shutdown detection

If the junction temperature will exceed the limits defined in the **Overtemperature shutdown threshold**, the TLF4277-2LD will disable the output voltage. In this case, a voltage level as defined in **CSO voltage level overtemperature detected** will be applied at the CSO pin. In addition, the ST pin will be set low.

6.1.5 Status output signal

The status condition pin ST is an open collector output. An external pull-up resistor has to be applied for functionality and to limit the current into the pin (for example, connect via a resistor to Q). Connecting the ST pin directly to a supply voltage may damage the device.

If one or more of the monitored protection functions (overcurrent, overvoltage, and temperature shutdown) is activated, the digital status output pin ST is set to “low”.

Current and protection monitor functions

6.2 Electrical characteristics current monitor function

Table 6 Electrical characteristics current monitor function

$V_{BAT} = 13.5\text{V}$, $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Linear current monitor							
Current-monitor factor Factor = I_Q / I_{CSO}	$F_{I_Q/I_{CSO}}$	95	100	105	–	¹⁾ $I_Q = 10\text{ mA} - 150\text{ mA}$ $T_j = -40^\circ$ to 125°C $V_{IN} = 9\text{ V}$ to 16 V $V_Q = 5\text{ V}$ to 12 V $V_{IN} > V_Q + 2.0\text{ V}$	P_7.1.1
Current-monitor factor Factor = I_Q / I_{CSO}	$F_{I_Q/I_{CSO}}$	90	100	110	–	¹⁾ $1\text{ mA} \leq I_Q \leq 300\text{ mA}$ $V_Q = 5\text{ V}$	P_7.1.5
CSO current at no-load condition	$I_{CSO,off}$	–	–	550	nA	No load connected at Q $R_2 = 27\text{ k}\Omega = 5\text{ V}$	P_7.1.6
Adjustable current limitation							
Adjustable current-limit range	$I_{Q,lim}$	10	–	300	mA	¹⁾ $850\ \Omega < R_{CSO} < 25.5\text{ k}\Omega$ $V_Q < 0.95 \times V_{Q,nom}$	P_7.1.7
Adjustable current-limit tolerance	$I_{Q,lim}$	-10	–	10	%	¹⁾ $10\text{ mA} \leq I_{Q,lim} \leq 300\text{ mA}$ $T_j = -40^\circ$ to 125°C $0.95 \times V_{Q,nom} > V_Q > 3.0\text{ V}$	P_7.1.8
Adjustable current-limit tolerance	$I_{Q,lim}$	-10	–	25	%	¹⁾ $10\text{ mA} \leq I_{Q,lim} \leq 300\text{ mA}$ $T_j = -40^\circ$ to 125°C $0.95 \times V_{Q,nom} > V_Q > 0\text{ V}$	P_7.1.15
CSO voltage level current limitation	V_{CSO,cur_lim}	2.45	2.55	2.65	V	$V_Q < 0,95 \times V_{Q,nom}$	P_7.1.9
Output level overvoltage detected							
CSO voltage level overvoltage detected	$V_{CSO,OV}$	3.0	3.1	3.2	V	$V_{ADJ} > 1.2 \times V_{REF,nom}$	P_7.1.10
Output level overtemperature detected							
CSO voltage level overtemperature detected	$V_{CSO,TSD}$	2.65	2.8	2.95	V	²⁾ $151^\circ\text{C} < T_j < 180^\circ\text{C}$	P_7.1.12
Status output signal							
Status-output digital signal low voltage	$V_{ST,low}$	–	0.2	0.4	V	$I_{ST} \leq 1.8\text{ mA}$	P_7.1.13
Status-output digital signal sink current	I_{ST}	–	–	1.8	mA	–	P_7.1.14

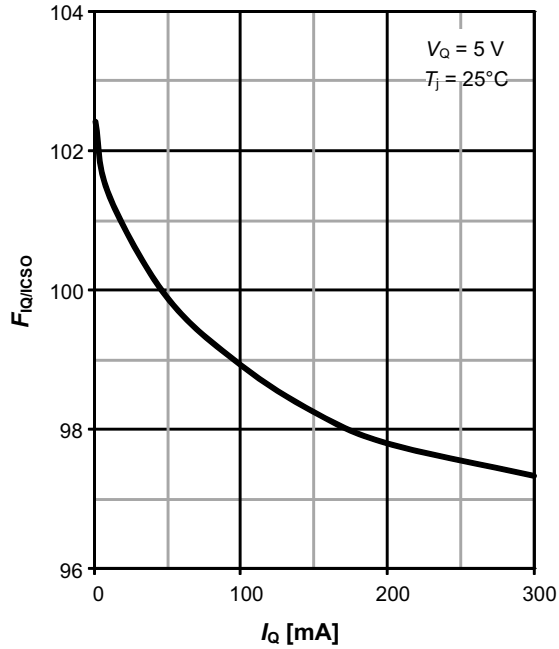
1) Referring to the device tolerance only, the tolerance of the external components can cause additional deviation.

2) Specified by design; not subject to production test.

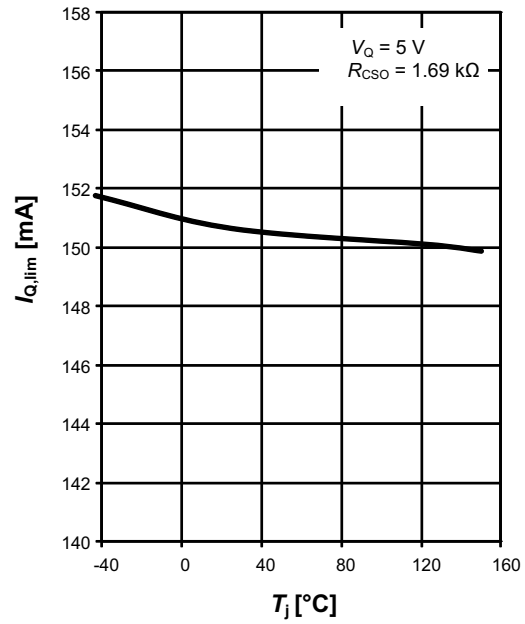
Current and protection monitor functions

6.3 Typical performance graphs current monitor function

Current monitor factor $F_{I_{Q}/I_{CSO}}$ versus output current I_Q



External current limitation $I_{Q,lim}$ versus junction temperature T_j



Enable function

7 Enable function

7.1 Description of the enable function

The TLF4277-2LD can be turned on or turned off via the EN input. With voltage levels higher than $V_{EN,high}$ applied to the EN input, the device will be completely turned on. A voltage level lower than $V_{EN,low}$ sets the device to low-quiescent-current mode. In this condition the device is turned off and is not functional. The EN input has a built-in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input. It has an internal pull-down resistor.

7.2 Electrical characteristics enable function

Table 7 Electrical characteristics enable function

$V_{BAT} = 13.5\text{ V}$, $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, direction of currents as shown in [Figure 7](#) (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable low signal valid	$V_{EN,low}$	–	–	0.8	V	–	P_8.2.1
Enable high signal valid	$V_{EN,high}$	2	–	–	V	See also startup time P_8.2.7	P_8.2.2
Enable threshold hysteresis	$V_{EN,hyst}$	50	–	–	mV	–	P_8.2.3
Enable input current	$I_{EN,high}$	–	–	5	μA	$V_{EN} = 5\text{ V}$	P_8.2.4
Enable input current	$I_{EN,high}$	–	–	20	μA	$V_{EN} < 18\text{ V}$	P_8.2.5
Enable internal pull-down resistor	R_{EN}	0.94	1.5	2.5	$\text{M}\Omega$	$V_{EN} < 5\text{ V}$	P_8.2.6
Startup time	t_{EN}	–	180	–	μs	$C_Q = 1\ \mu\text{F}$; $V_{Q,nom} = 5\text{ V}$; $I_{Q,load} = 150\text{ mA}$; time from $V_{EN} > 2\text{ V}$ to $V_Q = 90\%$ of $V_{Q,nom}$ (0 V to 5 V transition)	P_8.2.7

8.2 Selection of external components

8.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in [Figure 7](#).

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example, ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 μ F to 470 μ F is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to overvoltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

8.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in [Table 2](#). The graph [Output capacitor series resistivity ESR\(\$C_Q\$ \) versus output current \$I_Q\$](#) shows the stable operation range of the device.

TLF4277-2LD is designed to be stable with extremely low-ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins, and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

Application information

8.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_Q \quad (8.1)$$

with

- P_D : continuous power dissipation
- V_I : input voltage
- V_Q : output voltage
- I_Q : output current
- I_q : quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (8.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a : ambient temperature

Based on the above calculation, the proper PCB type and the necessary heat sink area can be determined with reference to the thermal specification in [Table 3](#).

Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 5 \text{ V}$$

$$I_Q = 100 \text{ mA}$$

$$T_a = 85^\circ\text{C}$$

Calculation of $R_{thJA,max}$:

$$\begin{aligned} P_D &= (V_I - V_Q) \times I_Q + V_I \times I_q \\ &= (13.5 \text{ V} - 5 \text{ V}) \times 100 \text{ mA} + 13.5 \text{ V} \times 5.0 \text{ mA} \\ &= 0.850 \text{ W} + 0.068 \text{ W} \\ &= 0.918 \text{ W} \end{aligned}$$

$$\begin{aligned} R_{thJA,max} &= (T_{j,max} - T_a) / P_D \\ &= (150^\circ\text{C} - 85^\circ\text{C}) / 0.918 \text{ W} = 70.8 \text{ K/W} \end{aligned}$$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 70.8 K/W. According to [Table 3](#), at least 300 mm² heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

Application information

8.4 Reverse polarity protection

TLF4277-2LD is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **Table 1** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shutdown circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

8.5 Further application information

For further information you may contact <https://www.infineon.com>.

Package information

9 Package information

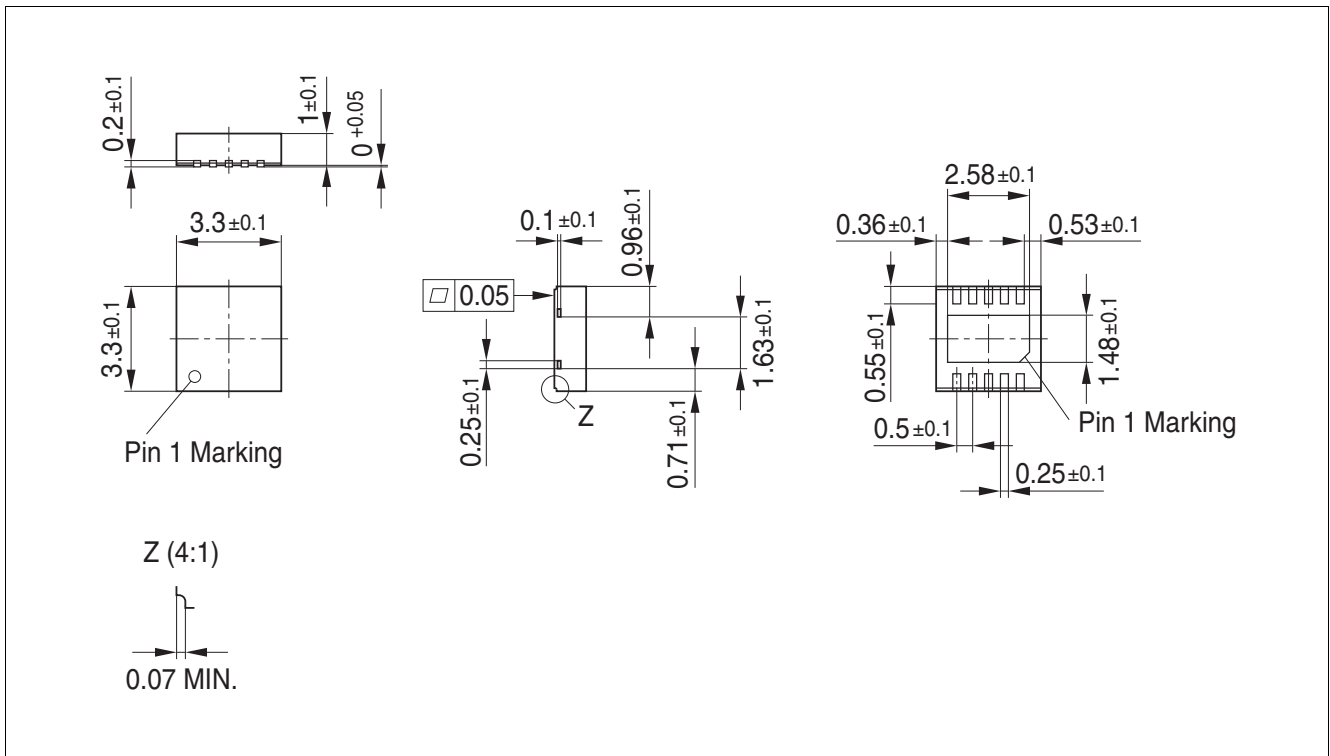


Figure 8 PG-TSON-10¹⁾

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

Revision history

10 Revision history

Revision	Date	Changes
1.02	2023-12-07	Editorial changes
1.01	2016-09-01	Editorial changes
1.0	2016-06-24	Initial version

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-12-07

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2023 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

Z8F56234241

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.