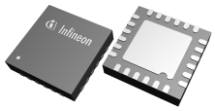
XDP™ XDPP114x product family

Digital power supply controller for PWM and PFM applications

Features



- Digital controller assisted high performance analog front ends and fully programmable ARM® Cortex™-M0 processor
  - 100 MHz clock, 32-bit, 64 kB OTP, 32 kB RAM, 80 kB ROM
- High performance, low latency digital hardware control loop for single rail up to two phases
- High-speed voltage sense
  - 100 MHz 11-bit ADC with 1.25 mV/ LSB
  - Up to 2.1 V differential voltage range
  - 200 MHz edge detection comparator
- High-speed current sense
  - 100 MHz 9-bit ADC with 1 mV/LSB
  - Configurable symmetrical positive and negative input voltage range or asymmetrical input
- 6 high-resolution Digital Pulse Width Modulated (DPWM) remappable outputs
  - 78.125 ps pulse width resolution
  - Adjustable dead-time between pairs for both rising and falling edges with 1.25 ns or 2.5 ns resolution
  - Frequency range: 50 kHz to 2 MHz with 5 ns resolution
- 2 High-speed inputs for external fault shutdown or PWM edge control
- PWM edge alignment
  - Trailing, leading, and dual-edge modulation
- Configurable feedback control
  - Voltage mode, peak current mode
- Configurable modulation methods
  - Pulse width modulation, phase shift modulation, frequency modulation
- Up to 11 GPIO pins
- Synchronization with external clock
- 4-channel, 10-bit, 0.926 Msps general purpose ADC
  - 2.34 mV/LSB, input voltage range 2.4 V
- Communication peripherals
  - 1 MHz I^2C/PMBUS, full duplex SPI, full duplex UART
- 24-pin VQFN packages
- Operating temperature: -40˚C to 125˚C

Typical applications

- Isolated/ non-isolated DC-DC PWM converters
- LLC converters
- Intermediate bus converters for Datacenter / computing system
- Power supplies for Telecom infrastructure/ Brick modules

Product validation

Fully qualified according to JEDEC for industrial applications.

Application features

- Soft start with pre-bias (non-resonant topologies)
- Feed forward compensation for PWM topologies
- Active current sharing
- LLC features
  - Hybrid soft start: PWM or phase-shift at the maximum frequency and frequency sweep
  - Adaptive SR turn-off based on V_{DS} sensing
  - Light load operation including:
    - Burst mode at the maximum frequency
    - Diode emulation (DE) mode
    - Phase Shift duty cycle reduction at the maximum frequency for full-bridge LLC
- High efficiency and light load management
  - Burst mode (except ACF topology)
  - Phase dropping (interleave topologies)
- Flux balancing
- Phase current balancing
- Configurable non-linear PID and Fast Transient Response (FTR)
- Feature rich fault protections
  - Programmable over and under voltage protection (OVP, UVP) thresholds and response
  - Programmable over and under current protection (OCP, UCP) thresholds and response
  - Programmable fast over-current protection and short circuit protection
  - Programmable over and under temperature protection (OTP, UTP) thresholds and hysteresis
  - Programmable positive/ negative peak current limit threshold
  - Internal and external temperature sensor
  - Feedback open loop protection
  - Programmable blanking time

Ordering information

Table 1 Ordering information

Base part number	Package type	Standard pack form and Qty	Application	Orderable part number
XDPP1140-100B	VQFN (24) 4 mm x 4 mm	Tape & reel, 5000	Single phase topologies, supports flux balancing	XDPP1140100BXUMA1
XDPP1148-100B			Single phase or interleaved topologies, supports current balancing between phases	XDPP1148100BXUMA1

Description

The XDPP1140 and XDPP1148 are digital power supply controllers for AC/DC and DC/DC power converters. The controller has high performance analog front end, a unique architecture with optimized power-processing digital blocks, and built-in ready to use firmware which minimize firmware development effort. The state machine based configurable control loop architecture supports various modes of operation including PWM and PFM modulation, voltage mode and peak current mode control.

The XDPP114x includes a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microcontroller sub-system that can be used for enhanced control, real-time monitoring, configuration of peripheral, and managing communications. It also allows firmware-based customization and implementation of housekeeping functions such as sequencing, blackbox data recording and interfacing.

The core power control functions are implemented by dedicated hardware or firmware pre-programmed in the device ROM, allows fast time to market. Additional programs can be stored and executed out of the nonvolatile memory OTP and RAM. Developers have full control of their application and firmware. System designers can develop and compile their customized firmware in any commonly used ARM™ based develop environment.

The XDPP114x supports PMBus™1.4 subsets and includes UART, SPI and I2C communication interfaces. The PMBus™ command set is runtime programmable, which allows config the commands on the fly.

The XDPP114x supports many commonly used AC-DC and DC-DC topologies such as, LLC, hard-switched full bridge and half bridge, phase shifted full bridge, active clamp forward, non-isolated buck, buck-boost, boost, interleaved buck, interleaved buck-boost, and interleaved boost topologies.

Figure 1 shows a typical application of the XDPP1140 device in a full-bridge to full-bridge converter.

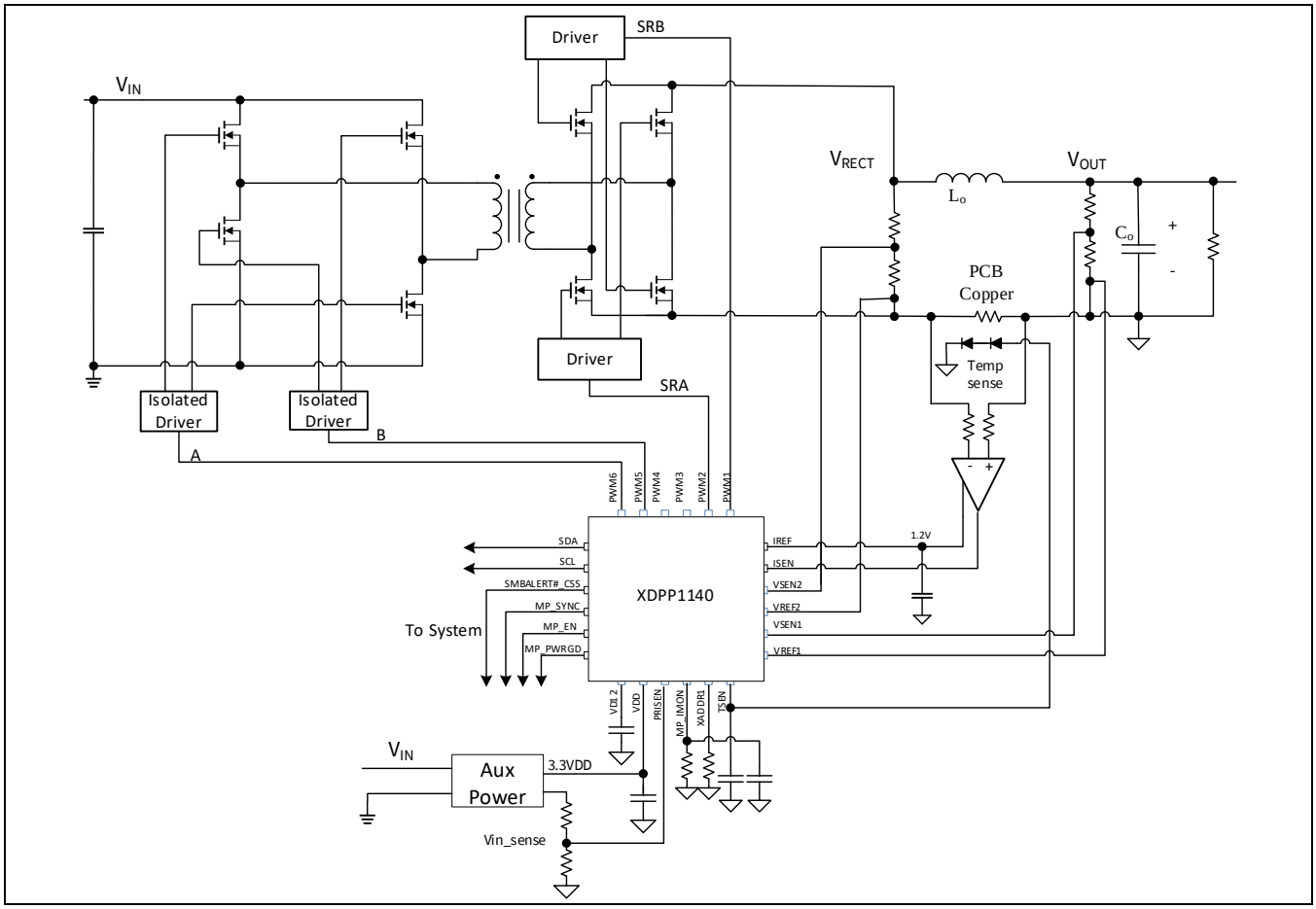


Figure 1 Typical application diagram

Note: *In this datasheet, the reference XDPP114x applies to both the XDPP1140 and XDPP1148 versions of the product. While references to XDPP1140 or XDPP1148 specifically refer to the referenced version of the product.*

Table of contents

Table of contents

1 Block diagram

Figure 2 shows a functional block diagram of the XDPP114x device architecture. Pin name in brackets indicates it is a secondary function of a multi-purpose pin. Details see **Table 7**.

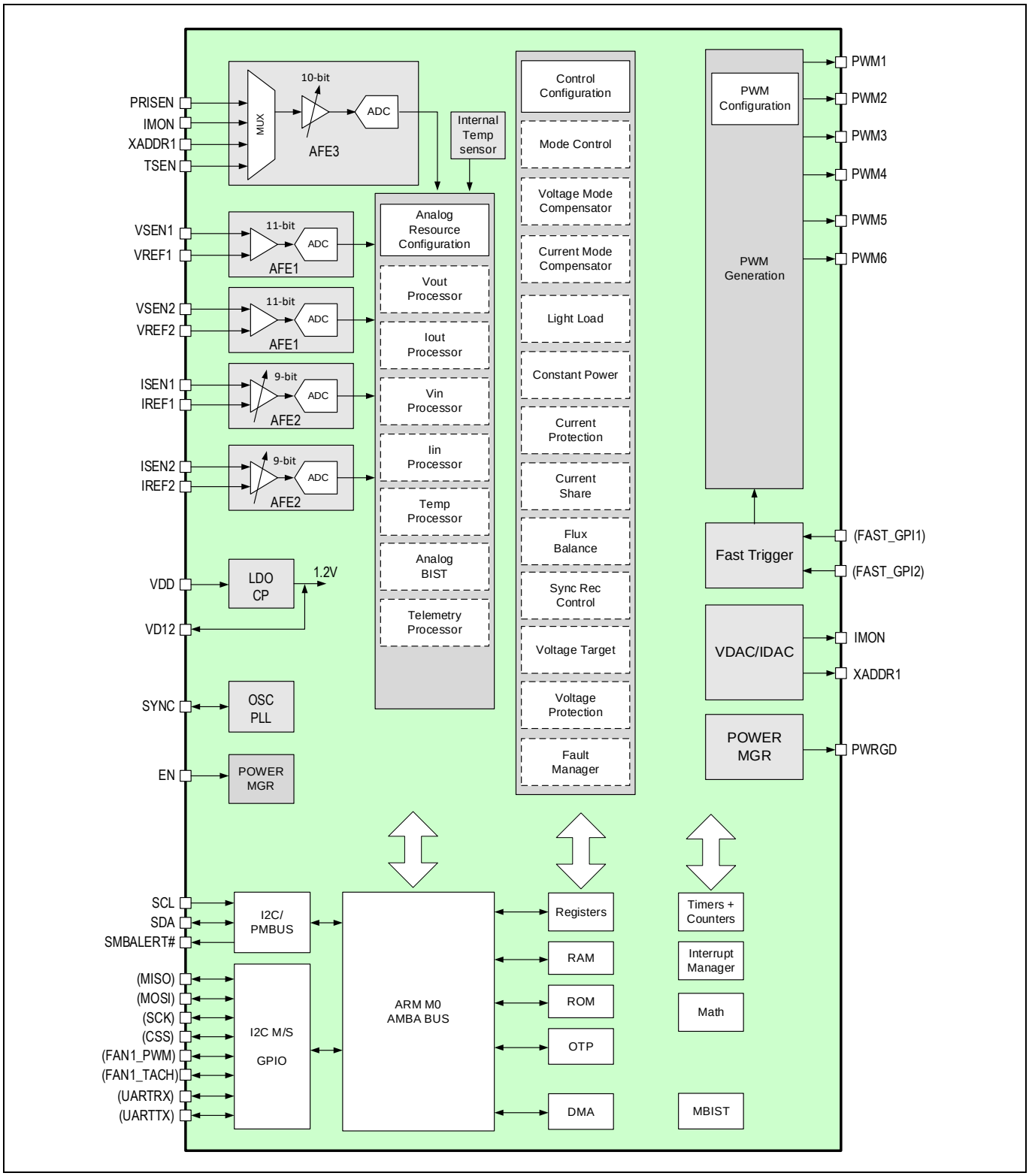


Figure 2 Block diagram

2 Product selection matrix

Table 2 Product selection table

FEATURE	XDPP1140-100B	XDPP1148-100B
ARM M0 core processor	100 MHz	100 MHz
High resolution DPWM outputs (78.125ps resolution)	6	6
Number of voltage sense ADC	2	1
Number of current sense ADC	1	2
General purpose ADC channels	4	4
OTP	64 kB	64 kB
RAM	32 kB	32 kB
ROM	80 kB	80 kB
DPWM switching frequency	Up to 2 MHz	Up to 2 MHz
SPI serial bus	Yes	Yes
UART	Yes	Yes
PMBus	Yes	Yes
Watchdog	Yes	Yes
On chip oscillator	Yes	Yes
Sync in and sync out functions	Yes	Yes
Temperature sense inputs	1	1
Total GPIO (General purpose I/O pins)	11	11
Package offering	VQFN-24 (4x4 mm^2)	VQFN-24 (4x4 mm^2)

3 Pin configuration and functions

3.1 XDPP1140-100B package

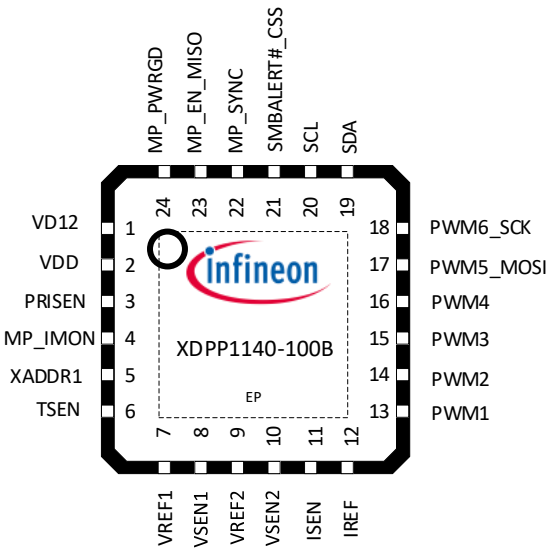


Figure 3 XDPP1140-100B pin assignment

Table 3 XDPP1140-100B pin definition

Pin No.	Name	Primary assignment	Alternate assignment	Configurable GPIO
1	VD12	1.2 V supply bypass.		-
2	VDD	3.3 V main supply input		-
3	PRISEN	Primary voltage sensing input	GPA1	-
4	MP_IMON	Output current monitor	GPA2/ SYNC / FAN1_TACH / Fault / Fast GPI2 / EN	Yes
5	XADDR1	Address 1	GPA3	-
6	TSEN	Temperature sensing input	GPA4	-
7	VREF1	Differential voltage sensing 1, negative input		-
8	VSEN1	Differential voltage sensing 1, positive input		-
9	VREF2	Differential voltage sensing 2, negative input		-
10	VSEN2	Differential voltage sensing 2, positive input		-
11	ISEN	Differential current sensing, positive input		-
12	IREF	Differential current sensing, negative input		-
13	PWM1	PWM1 output	SYNC/ Fast_GPI1	Yes

Pin No.	Name	Primary assignment	Alternate assignment	Configurable GPIO
14	PWM2	PWM2 output	SYNC/ Fast_GPI2	Yes
15	PWM3	PWM3 output	SYNC/ Fast_GPI1 / FAN1_TACH	Yes
16	PWM4	PWM4 output	SYNC/ Fast_GPI2 / FAN1_PWM	Yes
17	PWM5_MOSI	PWM5 output	SYNC/ UARTRX/ Fast_GPI1/ SPI_MOSI	Yes
18	PWM6_SCK	PWM6 output	SYNC/ UARTTX/ Fast_GPI2/ SPI_SCK	Yes
19	SDA	I²C serial data line		-
20	SCL	I²C serial clock line		-
21	SMBALERT#_CSS	PMBus alert	SYNC / Fault / CSS	Yes
22	MP_SYNC	Synchronize pin	FAN1_PWM/ Fast GPI1/ Fault	Yes
23	MP_EN_MISO	Enable_Sleep control	SYNC/ SPI MISO	Yes
24	MP_PWRGD	Power good output	SYNC	Yes
	EP (exposed pad)	Ground pin		-

3.2 XDPP1148-100B package

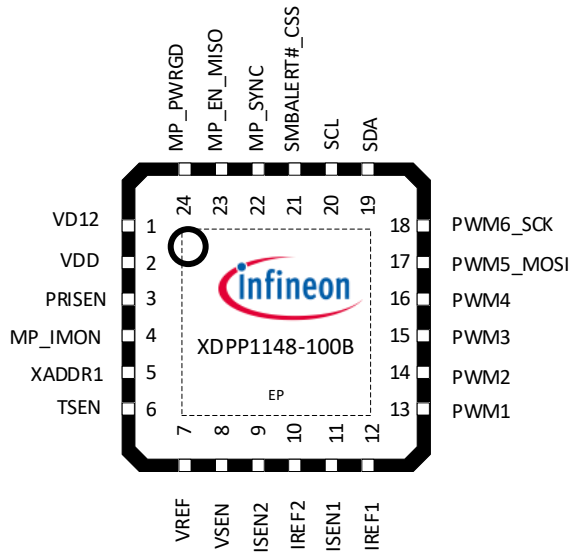


Figure 4 XDPP1148-100B pin assignment

Table 4 XDPP1148-100B pin definition

Pin No.	Name	Primary assignment	Alternate assignment	Configurable GPIO
1	VD12	1.2 V supply bypass		-
2	VDD	3.3 V main supply input		-
3	PRISEN	Primary voltage sensing input	GPA1	-

Pin No.	Name	Primary assignment	Alternate assignment	Configurable GPIO
4	MP_IMON_EN	Output current monitor	GPA2/ SYNC / FAN1_TACH / Fault / Fast GPI2 / EN	Yes
5	XADDR1	Address 1	GPA3	-
6	TSEN	Temperature sensing input	GPA4	-
7	VREF	Differential voltage sensing, negative input.		-
8	VSEN	Differential voltage sensing, positive input		-
9	ISEN2	Differential current sensing of phase 2, positive input		-
10	IREF2	Differential current sensing of phase 2, negative input		-
11	ISEN1	Differential current sensing of phase 1, positive input		-
12	IREF1	Differential current sensing of phase 1, negative input		-
13	PWM1	PWM1 output	SYNC/ Fast_GPI1	Yes
14	PWM2	PWM2 output	SYNC/ Fast_GPI2	Yes
15	PWM3	PWM3 output	SYNC/ Fast_GPI1 / FAN1_TACH	Yes
16	PWM4	PWM4 output	SYNC/ Fast_GPI2 / FAN1_PWM	Yes
17	PWM5_MOSI	PWM5 output	SYNC/ UARTRX/ Fast_GPI1/ SPI_MOSI	Yes
18	PWM6_SCK	PWM6 output	SYNC/ UARTTX/ Fast_GPI2/ SPI_SCK	Yes
19	SDA	I^2C serial data line		
20	SCL	I^2C serial clock line		
21	SMBALERT#_CSS	PMBus alert	SYNC / Fault / CSS	Yes
22	MP_SYNC	Synchronize pin	FAN1_PWM/ Fast GPI1/ Fault	Yes
23	MP_EN_MISO	Enable_Sleep control	SYNC/ SPI MISO	Yes
24	MP_PWRGD	Power good output	SYNC	Yes
	EP (exposed pad)	Ground pin		

Note:

1. *EP is the metal pad under the chip*
2. *SDA, SCL, SMBALERT are Open Drain I/O pins*
3. *All digital GPIO pins are 3.3V level CMOS, the outputs are programmable to be CMOS or Open Drain*
4. *GPA: general purpose analog input pin*

4 Functional description

4.1 Introduction

The XDPP114x is a flexible, feature-rich digital controller, optimized for isolated and non-isolated dc-to-dc converters. The XDPP114x is designed to enable flexibility and provide excellent digital control for all the major fixed frequency topologies: pulse width modulation (PWM) half-bridge (HB), PWM full-bridge (FB), PWM phase-shift full-bridge (PSFB), active clamp forward (ACF), non-isolated Buck, Boost and Buck-boost. It also works for resonant LLC topologies including half-bridge (HB) LLC, full-bridge (FB) LLC, phase-shift full-bridge (PSFB) LLC. The XDPP1148 supports interleaved operation of Buck, Boost and Buck-boost.

The features that require fast response are implemented by state machine in hardware and can be configured over the I^2C port. These features include:

- Digital PID loop filter and compensation
- Pre-bias startup
- Feed-forward compensation
- Non-linear PID fast transient
- Active current sharing
- Current balancing between two phases
- Flux balancing of full-bridge converter
- Burst operation in light load
- Phase shedding

The fault protections are implemented in hardware for the shortest delay time. The fault thresholds, thresholds hysteresis and fault count are configurable. The fault response is managed by firmware for flexibility. The industry standard PMBus interface also provides access to the monitoring and system control functions.

The integrated ARM® Cortex® -M0 microcontroller and built-in non-volatile memory provide extensive programming and customization of functions such as, the frequency dithering, GPIO signal timing, soft start timing and sequencing, dynamic dead-time based on operation, blackbox data recording.

4.1.1 ARM® Cortex™ –M0 core

The XDPP114x chip embeds the smallest ARM processor – the ARM® Cortex®-M0 processor. It is a high performance 32-bit processor with low gate count, minimal power requirements, and reduced code footprint. It is an optimized interrupt controller, allows to be used in hard real-time applications. The ARM® Cortex® -M0 processor clock frequency f_{CLK} is 100 MHz.

4.1.2 Memories

The device has 80 kB Boot ROM that contains the initial firmware startup routines for PMBUS communication. This boot ROM is executed after power-up-reset checks. The XDPP114x also supports customization of the boot program by allowing an alternative boot routine to be executed from the one-time programmable (OTP) nonvolatile memory (NVM). Control registers can be reprogrammed in the field via the serial communication (I^2C) bus and stored into the OTP NVM. For run time data storage and scratchpad memory, a 32 kB RAM is available.

4.1.3 Communication ports

The device provides I²C, SPI, and UART communication ports.

4.1.3.1 I²C/PMBus

All operating parameters in the device are configurable via the I²C serial interface (SDA, SCL). The SDA, SCL support two logic levels, 3.3 V and 1.8 V. By default, the controller uses 3.3 V logic. The device supports all three speeds I²C: standard (100 kHz), fast (400 kHz) and fast mode plus (1 MHz) operating frequency.

The device is compliant to PMBus™ Power System Management Protocol Specification, revision 1.4.1. The I²C/PMBus interface allows to configure the device as well as monitoring fault status, voltage, current, power, and temperature telemetry.

4.1.3.2 SPI

The SPI is high speed communication port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate up to 5 MHz. The SPI port supports two logic levels, 3.3 V and 1.8 V. For 3.3 V output, the SPI pin can be configured as CMOS (push-pull) output or open-drain. For 1.8 V logic, it must be configured to open-drain output and use external pull-up.

The device supports programmable slave or master mode. The SPI is normally used for communication between the XDPP114x and external peripherals. Typical applications include an interface to external I/O or peripheral such as shift registers, SPI EPROMs and analog-to-digital converters. The SPI typically is configured as a master for communicating to external EEPROM. It should be configured to slave mode when receiving control from another microcontroller in the system.

4.1.3.3 UART

A full duplex Universal Asynchronous Receiver/Transmitter (UART) interface is included in the device. The baud rate, word size, and buffer depth are configurable through registers. A loop back feature can also be setup for firmware verification.

The UARTTX and UARTRX pin sets can be configured using assigned GPIO pins. See **Table 7** for the list of GPIO pins and the pre-defined functions of each of them.

4.1.3.4 Address offset

The base address of I²C and PMBus is configured by firmware registers **addr_pin_i2c_address_offset** and **addr_pin_pmbus_address_offset**. By default, the base address of I²C is 0x10, the base address of PMBus is 0x40. Address offset can be added to the base address to differentiate multiple devices that have the same configuration (base address) in system. The XDPP114x uses XADDR1 pin for I²C/PMBus address offset by connecting a resistor from the XADDR1 to ground. The offset decoding is enabled by default with bit [7] of the **addr_pin_i2c_address_offset** set to 0 and bit [7] of the **addr_pin_pmbus_address_offset** set to 0.

The device supports 16-valent or 8-valent address table as shown in **Table 5** and **Table 6**. The bit [1] of firmware register **addr_pin_xv** configs the xValent selection between 16-valent and 8-valent. Set to 0 selects 16-valent, set to 1 selects 8-valent. The default pinset table size is 16-valent. To properly set the device addresses, resistors with 1% tolerance must be connected. The programming resistors are designed to allow using E12 resistors for system cost saving.

The device measures XADDR1 resistor offset during initialization state and does not support on the fly modification. The configuration must be stored in OTP memory and recycling VDD is required to have the modifications taking effect.

Table 5 I²C/PMBus address offset of 16-segment decode

Resistor-to-GND (1%)		Address offset
XADDR	680 Ω	0x00
	1 kΩ	0x01
	1.5 kΩ	0x02
	2.2 kΩ	0x03
	3.3 kΩ	0x04
	4.7 kΩ	0x05
	6.8 kΩ	0x06
	10 kΩ	0x07
	15 kΩ	0x08
	22 kΩ	0x09
	33 kΩ	0x0A
	47 kΩ	0x0B
	68 kΩ	0x0C
	100 kΩ	0x0D
	150 kΩ	0x0E
	220 kΩ	0x0F

Table 6 I²C/PMBus address offset of 8-segment decode

Resistor-to-GND (1%)		Address offset
XADDR	10 kΩ	0x00
	22 kΩ	0x01
	33 kΩ	0x02
	47 kΩ	0x03
	68 kΩ	0x04
	100 kΩ	0x05
	150 kΩ	0x06
	220 kΩ	0x07

4.1.4 GPIO

The device provides up to 11 general purpose inputs/outputs (GPIOs). All the GPIO pins are shared with alternative functions. The GPIO configuration is programmed by the function register of each GPIO pin named xxxx_func. The GPIO polarity is configured by firmware config register **gpio_config_polarity**. When configured as an output pin, the MP_IMON, MP_EN, PWM5_MOSI and PWM6_SCK pins can choose output buffer as CMOS output (push-pull) or open-drain output by setting xxxx_ppen register. All other GPIO pins can be configured as emulated open-drain using firmware register **gpio_config_emu_open_drain**.

The GPIO config only set on initialization. Modifications to gpio_config registers would have to be stored in OTP and will take effect after power cycling the V_{DD} or resetting FW.

Table 7 GPIO and I²C/SPI multi-purpose pin

Name	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
MP_IMON	A: IMON	IO: GPIO[3]	IO: GPIO[11]	IO: SYNC	I: FAN1_TACH	O: GENERIC_ FAULT	I: FAST_GPI2	IO: GPIO[0] (EN)
PWM1	O: PWM1	IO: GPIO[5]	IO: GPIO[13]	IO: SYNC	na	na	I: FAST_GPI1	na
PWM2	O: PWM2	IO: GPIO[7]	IO: GPIO[15]	IO: SYNC	na	na	I: FAST_GPI2	na
PWM3	O: PWM3	IO: GPIO[6]	IO: GPIO[14]	IO: SYNC	I: FAN1_TACH	na	I: FAST_GPI1	na
PWM4	O: PWM4	IO: GPIO[2]	IO: GPIO[10]	IO: SYNC	O: FAN1_PWM	na	I: FAST_GPI2	na
PWM5_MOSI	O: PWM5	IO: GPIO[3]	IO: GPIO[11]	IO: SYNC	I: UARTRX	I: S_MOSI	I: FAST_GPI1	O: M_MOSI
PWM6_SCK	O: PWM6	IO: GPIO[4]	IO: GPIO[12]	IO: SYNC	O: UARTTX	I: S_SCK	I: FAST_GPI2	O: M_SCK
SMBALERT#_ CSS	IO: SMBALERT_N	IO: GPIO[6]	IO: GPIO[14]	IO: SYNC	O: GENERIC_ FAULT	I: S_CSS	na	O: M_CSS
MP_SYNC	na	IO: GPIO[7]	IO: GPIO[15]	IO: SYNC	O: FAN1_PWM	O: GENERIC_ FAULT	I: FAST_GPI1	na
MP_EN_MISO	IO: GPIO[0](EN)	IO: GPIO[10]	IO: GPIO[8]	IO: SYNC	na	O: S_MISO	na	I: M_MISO
MP_PWRGD	IO: GPIO[1](PWRGD)	IO: GPIO[12]	IO: GPIO[9]	IO: SYNC	na	na	na	na

Note:

1. Analog functions prefixed with "A:"
2. Digital inputs prefixed with "I:", outputs prefixed with "O:", inouts prefixed with "IO:"
3. Input priority by lowest pin # (e.g., if MP_IMON and PWM6_SCK both programmed to SYNC, the input is taken from MP_IMON due to lower pin #)

4.1.5 Register map

The device is configured by application specific parameter settings loaded into control registers. The direct I²C register access is disabled by default with the bit [4] of **vid_resolution** set to 1. The access to control register map can be achieved via PMBus. The MFR_REG_WRITE, MFR_REG_READ and the MFR_AHB_ADDRESS PMBus commands are used write\read register parameters. The access to register map is supported by the XDP designer GUI without extra steps.

The control registers are not pre-programmed at the factory. Control registers should be programmed in each specific application and stored into the on-chip nonvolatile memory (NVM), which is then downloaded to the control registers during initialization of the controller as it powers up. The controllers support multiple reprogramming cycles which is easily accomplished with the GUI or System Programmer software.

The controllers also support storing multiple configurations in NVM. It can store up to 16 configurations, and these configurations may be reprogrammed if needed.

4.2 Analog blocks and subsystems

4.2.1 Power supply

Operating from a single +3.3 V (VDD) supply to the controller, an on-chip low drop-out (LDO) regulator generates an internal +1.2 V voltage at VD12 pin. Both VDD and VD12 pin should have 1 µF + 0.1 µF ceramic bypass capacitors for noise filtering. Place the bypass capacitors as close as possible to VDD and VD12 pins. Do not apply voltage to or ground VD12 pin. VD12 pin can be used as 1.2 V reference of the current sense input, but not intend to drive a load.

The device can be put into sleep mode to reduce quiescent current and system standby power. The sleep mode current consumption is $I_{DDsleep}$. It is capable wakeup from sleep mode after t_{wakeup}. If deep sleep mode is not desired, it can be disabled and allows faster response to the EN input. The EN logic can be configured to be active-high or active-low.

4.2.2 Oscillator and PLL

An internal PWM oscillator running at f_{OSC} is incorporated in the device, and the frequency programming resolution is 5 ns. With a 6-bit interpolator, the XDP device offers high PWM resolution as small as 78.125 ps. Using a 12-bit time-based period and frequency control, the maximum pulse width that the device supports is 20.48 µs (4096 x 5ns); this sets the minimum switching frequency to approximately 50 kHz. The maximum switching frequency is 2 MHz. For LLC topologies, the frequency adjusting resolution is 2.5 ns.

A typical LLC frequency modulation waveform is shown in **Figure 5**. The top axis shows compensated error signal (that is, PID output). The second axis shows the resulting pwm waveform of even cycle, followed by the pwm signal of odd cycle. The lower the PID output, the higher the switching frequency. The signals on the next two axes are PWM outputs which have hatched lines indicating where dead-time is applied to the signals. The bottom two axes are the secondary SR PWM waveforms which follows primary PWM with maximum ON time limitation.

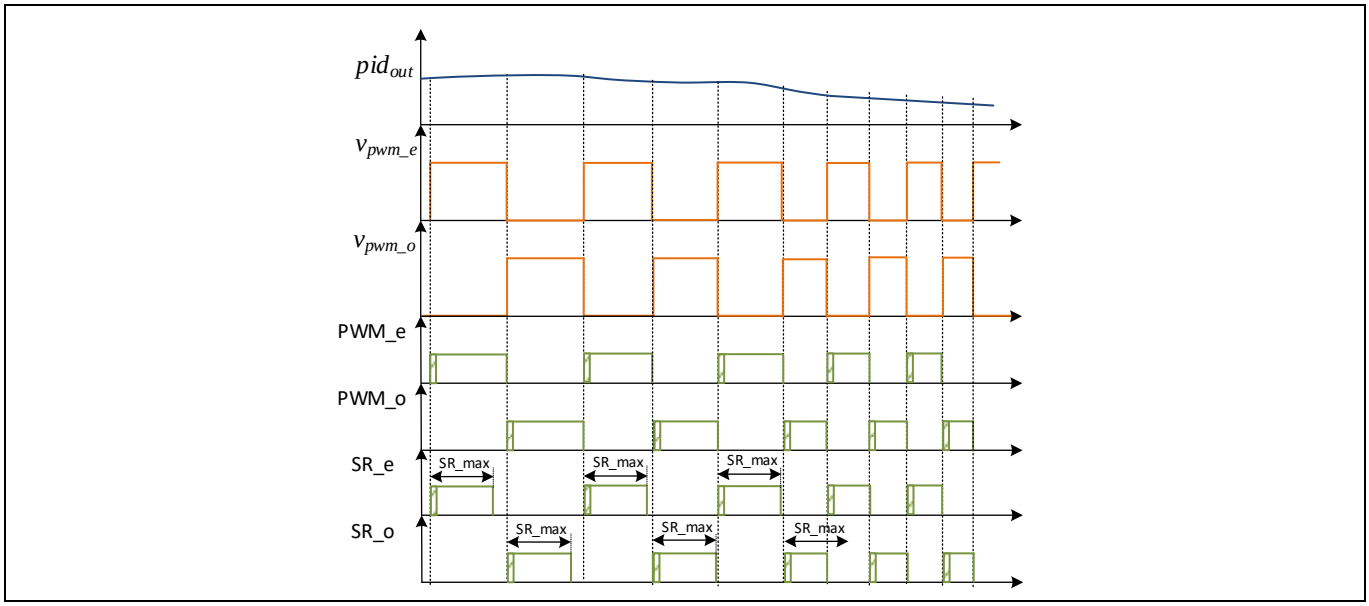


Figure 5 PWM generation of LLC topology

A typical PWM generation waveform is shown in **Figure 6**. The top axis shows analog behavioral waveforms of a dual-edge modulator (Vmod) and compensated error signal (that is, PID output). The second axis shows the resulting PWM waveform. The signals on the bottom four axes have hatched lines indicating where dead-time is applied to the signals.

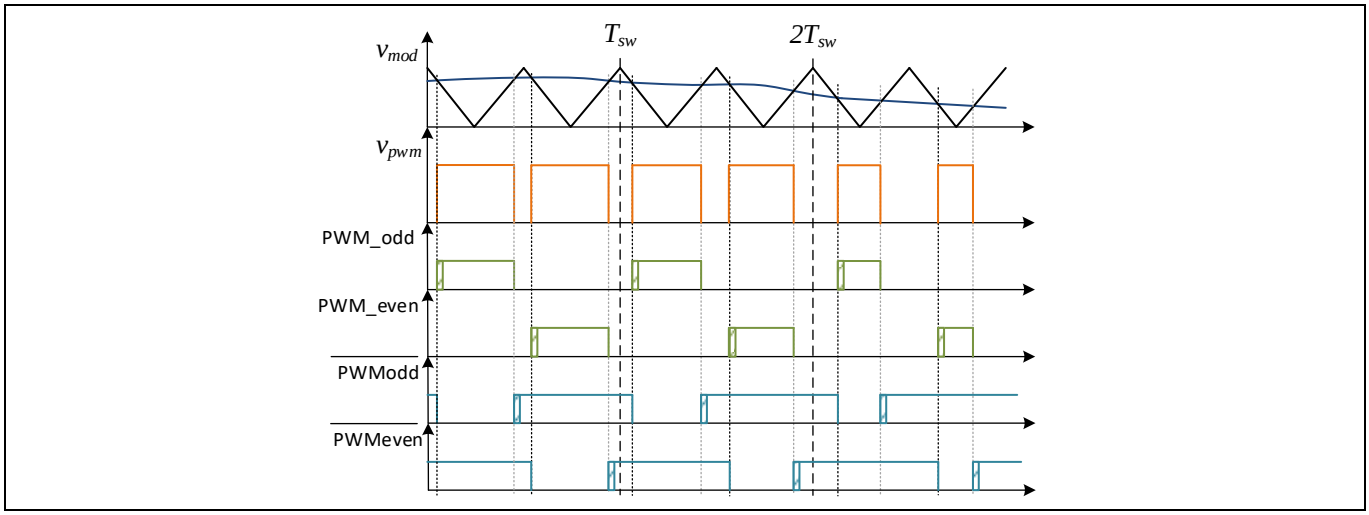


Figure 6 PWM Generation of PWM topology

Dead-time refers to the amount of time between the turning-off of one switch to the turning-on of another switch where both are off to prevent unintentional short circuit conditions. The standard way of implementing dead-time is to use leading edge-blanking. Each signal of the PWM generator is capable of blanking the rising edge by a programmable amount. The device supports two sets of dead-time resolutions and ranges, configured by register **deadtime_lsb_sel**, for 0-318.75 ns in 1.25 ns increments or 0-637.5 ns in 2.5 ns increments. The device also supports to adjust the falling edge of each PWM if additional blanking time is required. The value of dead-time is changeable during normal operation to allow power supply efficiency optimization.

PWM outputs are 3.3 V compatible signals which are set to high impedance during reset, configuration, and initialization. The PWM outputs that are mapped to a Loop to drive MOSFETs is pulled to the state defined in the configuration after firmware completed the initialization. The PWM OFF state level can be set low or high by **pwm_state_shutdown** register, and enabled by **en_pwm_state_shutdown**. By default, the PWM OFF state is disabled and all the PWMs that are mapped to a Loop stays low during shutdown.

The multi-purpose MP_SYNC pin can be configured as an input to allow synchronization to an external clock signal, or as an output to provide a clock that other converters synchronize to. For the best flexibility, all GPIO pins can be configured as SYNC pin.

When SYNC pin is configured as an input, the PLL receives a periodic signal. The input signal is limited to ±12.5% of the programmed switching period to lock the sync clock. Once the frequency is locked, the system can remain in sync for a maximum of ±25% of the programmed switching period.

The SYNC output signal is a square waveform with the rising edge aligned with PWM signal per topology and type of modulation. The sync function would provide a signal indicating successfully synchronization, as well as a fault if it cannot synchronize.

4.2.2.1 The 3rd ramp

Besides the two regular oscillator ramps which used to generate PWM outputs for up to two phases, the device also provides a third ramp. The frequency of the third ramp can be configured independently to the first two regular ramps (ramp0 and ramp1). It can also be synchronized with the ramp0 or to an external frequency if desired. The third ramp is not associate with any close loop control thus only supports open loop operation. The rising edge and the falling edge of the third ramp can be programmed independently by FW patch.

With the third ramp, the device could drive interleaved Buck or interleaved 3-level buck converter with a cascade open loop stage.

Table 8 PWM ramp and topology supported

Features	XDPP1148-100B	XDPP1140-100B	XDPP1100-Q024	XDPP1100-Q040
Number of loops	1	1	1	2
Number of ramps	2+1	2+1	2	2
Number of VS ADC	1	2	2	2
Number of IS ADC	2	1	1	2
Topology				
HB/CT; HB/FB	✓	✓	✓	✓
FB/CT; FB/FB (VMC with Flus balance)		✓	✓	✓
FB/CT; FB/FB (PCMC)	✓			✓
ACF	✓	✓	✓	✓
PSM-FB/CT; PSM-FB/FB	✓	✓	✓	✓
LLC-HB; LLC-FB; LLC-PSFB; secondary CT or FB	✓	✓		
Buck	✓	✓	✓	✓
Buck-boost	✓	✓	✓	✓
Boost	✓	✓	✓	✓
Interleaved Buck	✓			✓
Interleaved Buck-boost	✓			✓
Interleaved Boost	✓			✓
Interleaved HB/CT; HB/FB; FB/CT; FB/FB; PSM-FB/CT; PSM-FB/FB				✓
Interleaved ACF				✓
Dual loop (single phase of each loop)				✓
Interleaved Buck + open loop converter	✓			
Interleaved 3-level Buck+ open loop converter	✓			

4.2.3 Voltage sense AFE1

The XDPP1140 offers two dedicated high speed voltage analog/digital converters (ADC) as Analog Front End (AFE1), while the XDPP1148 offers one dedicated high speed VADC. The voltage sense AFE1 can be used as voltage sense processor (VSP) or rectified voltage sense processor (VRSP).

The major functions of the VSP and its associated blocks are:

- Voltage ADC full rate interface to the digital domain
- Voltage ADC gain and offset trim (digital trim)

- Voltage scaling (external resistor divider)
- Input or output voltage computation (configurable input or output sense)
- Over/Under Voltage Protection comparators and fault
- Fast transient (FTR) mode and FTR exit comparators
- Burst mode and burst mode exit comparators

The VRSP and its associated blocks have the following functions in addition to the above:

- 200 MHz edge comparator with digital de-glitcher
- Measure V_{RECT} voltage of the even and odd half cycles of bridge topologies
- Measure V_{RECT} voltage on the even cycle for non-bridge topologies
- Average the measured even and odd V_{RECT} voltage
- Flux balancing circuit
- Input voltage processing

The simplified VSADC block diagram is shown **Figure 7**.

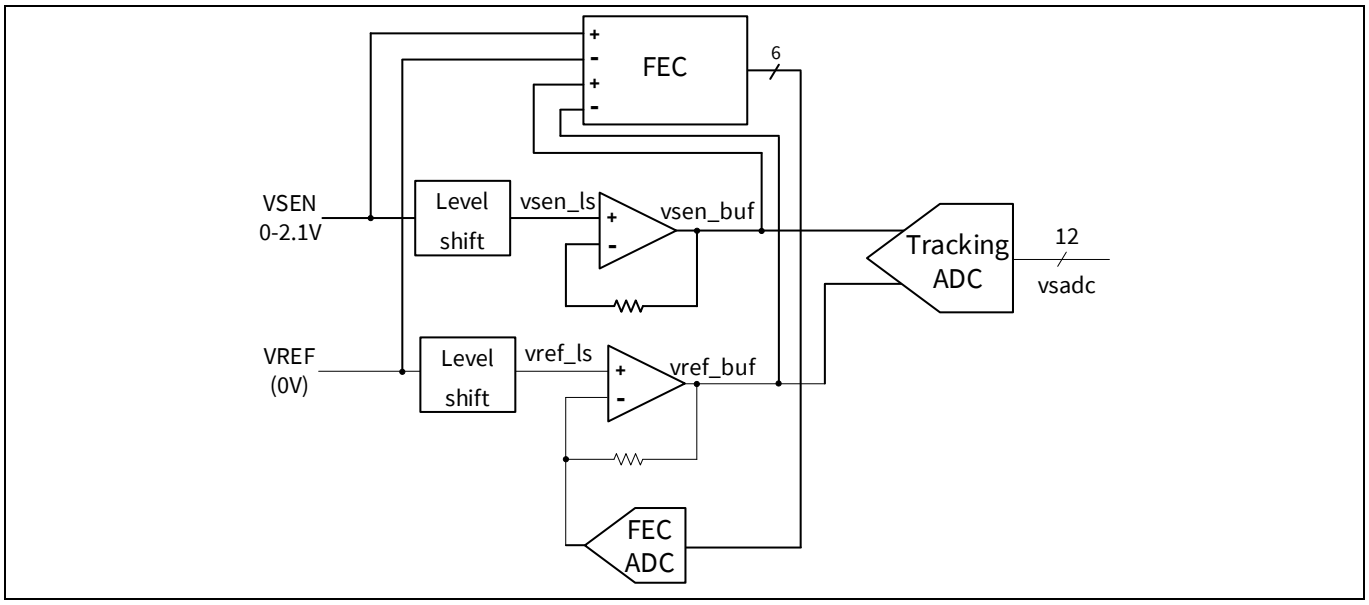


Figure 7 Voltage sense ADC block diagram

The level shifters allow wide input voltage range, 0.0 to 2.1 V, as well as provide a high input impedance. The unity gain buffers provide additional drive strength to the tracking ADC input stage. The front end offset compensator (FEC) is to reduce the effects of temperature, stress and lifetime offset-drift in the AFE.

Simplified block diagram of the tracking ADC is shown in **Figure 8**. The summing amplifier amplifies the difference between the buffered differential sensed voltage and the DAC output voltage.

The output of the summing amplifier drives the comparator whose output determines the size and direction of the next step for the tracking integrator. The tracking integrator output represents the analog to digital converted sensed voltage. It is also used to drive the DAC whose output is summed in the summing amplifier.

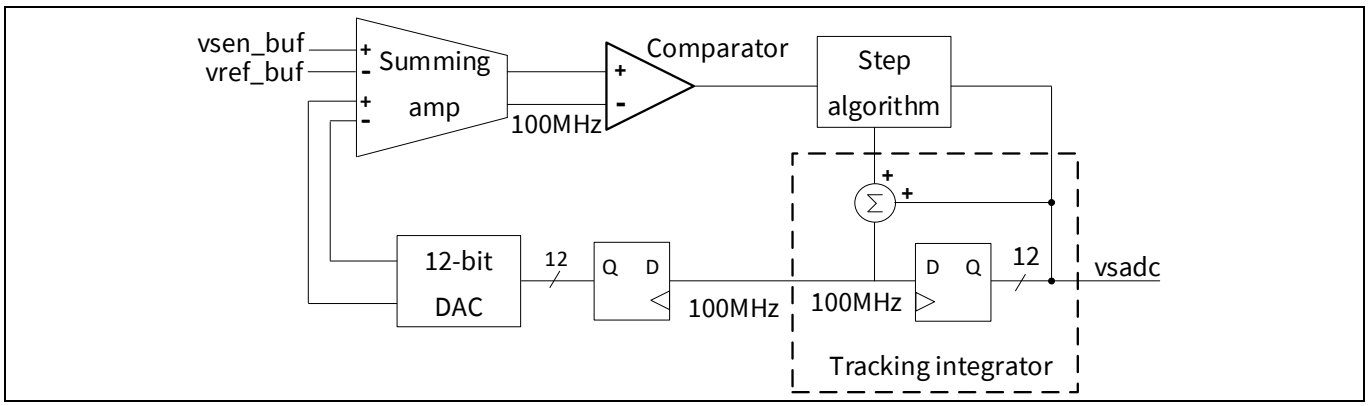


Figure 8 Tracking ADC block diagram

Tracking ADC resolution is 12 bits with an input referred LSB weight of 1.25 mV. Note that the AFE input range is restricted to maximum of 2.1 V, meaning only the lower 11 bits of the ADC output are actually used. For output voltage sensing, 3-bit modulation is added to the reference voltage to achieve 156.25 µV resolution.

The voltage sense input has a nominal input impedance of 1 MΩ. The ADC is clocked at 100 MHz and a voltage sense front-end amplifier process the voltage at 50 MHz. There is no need for an anti-alias filtering, but it may be advantageous to add a higher bandwidth external RC filter network to increase the attenuation of high frequency noise that may couple onto the voltage sense lines. This additional filter provides minimal phase margin impact on the feedback loop. If such an additional filter is used, it is recommended that values of R_{EXT} = 10 Ω and C_{EXT} = 220 pF be used.

The VRSP is responsible for controlling the VSEN1 or VSEN2 ADC when they are used to measure the rectified voltage waveform (V_{RECT}). V_{RECT} sensing is often used to sense the input voltage indirectly from the secondary side of transformer. **Figure 9** presents waveforms to illustrate how sampling of the V_{RECT} waveform. Noise has been added to the ideal V_{RECT} waveform to highlight the importance of sampling window timing. The AFE1 has an edge detector working at 200 MHz clock. It senses the rising and falling edges of V_{RECT} waveform. T_{detect} waveform is the output of edge detector logic. The rising-edge of the rectified voltage waveform is detected and some programmable blanking window is added to it. The blanking time should be configured longer than the voltage spike and ringing duration. The blanking time should also be set longer than 250 ns for the tracking ADC to settle. After the blanking window, sampling of the rectified voltage can occur (shown as the T_{sample} waveform). The comparator for the VSEN ADC is prepositioned to the value of the last cycle to minimize the time required for the ADC to properly track the voltage. The sampling window ends when the associated PWM signal goes low.

The input voltage is calculated based on V_{RECT} sensed voltage, V_{RECT} resistor divider scale and the transformer turns ratio. Faults and warnings including input overvoltage and undervoltage would be detected by the VRSP when it is being used for input voltage sensing. These are set by PMBus commands, and the response is handled by the CPU.

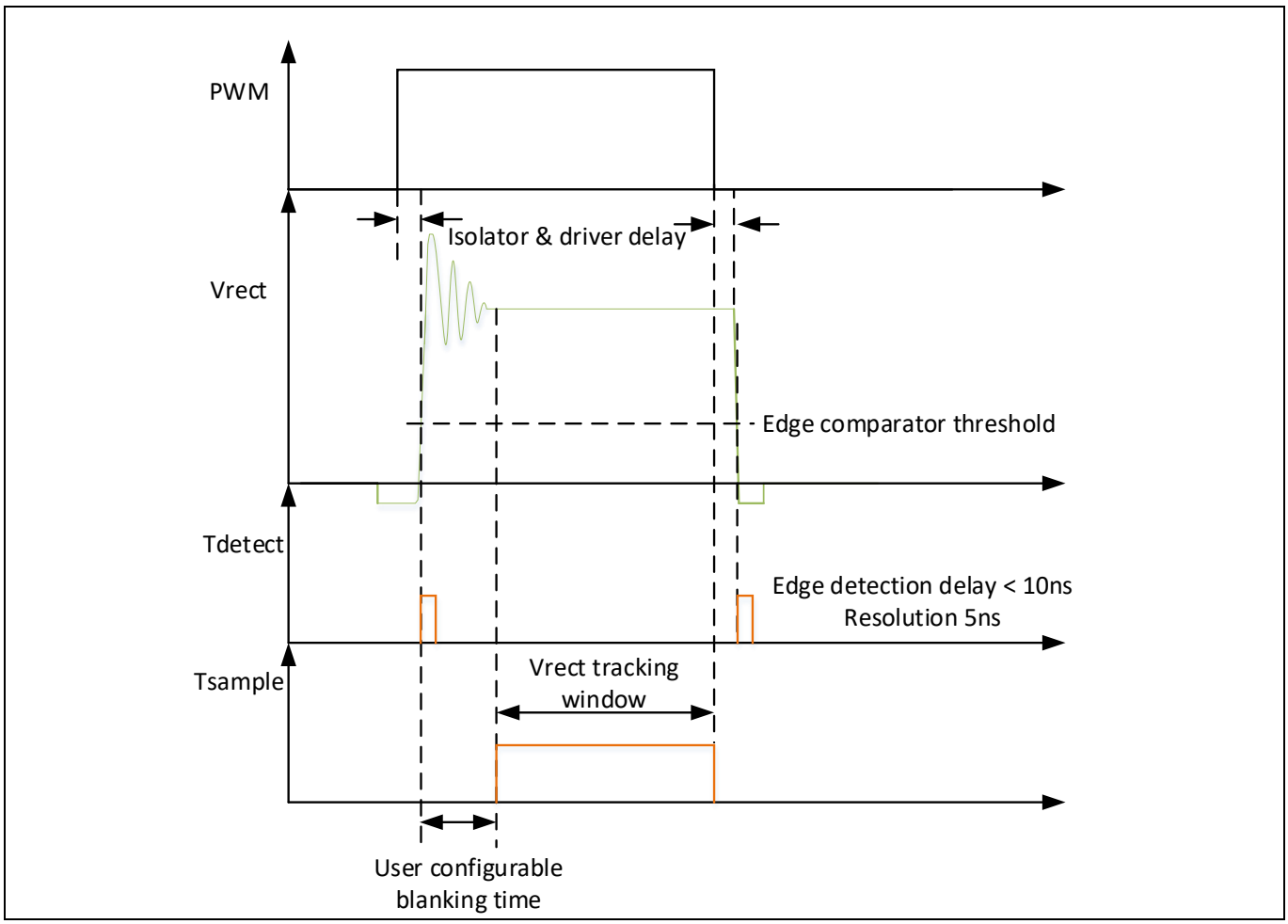


Figure 9 VRSP sampling window

The timing of the rising and falling edges of the rectified voltage waveform, along with the magnitude, is used for transformer protection, that is, in full-bridge voltage mode converter, the V_{RECT} timing and amplitude is used for volt-second flux balancing. To avoid waveform distortion or timing delay, it is not recommended to add any filter to the input of VSEN when it is used V_{RECT} sensing mode.

4.2.4 Current sense AFE2

The dedicated differential current sense ADC (AFE2) is designed to sense current via low ohmic sense resistor or PCB copper trace, as well as sense primary current through current sense transformer. The ISADC (ISEN1, ISEN2) is 9-bit ADC. It operates at 100 MHz and could provide high speed short circuit protection (SCP). The resolution of current sense ADC is 1 mV/LSB. The reference level (common mode voltage at IREF pin) is 1.2 V.

The device supports both primary and secondary current sense. When sensing primary current through current transformer, symmetric positive and negative input voltage range (+/- 256 mV) is enabled. This feature does not require rectifying the signal, thus simplify external circuit. When sensing secondary current, a configurable digital offset could be used to adjust the voltage level at 0 A, thus allowing to increase the effective positive input voltage range. The maximum digital offset voltage is 252 mV.

Simplified block diagram of the current sense ADC is shown in **Figure 10**.

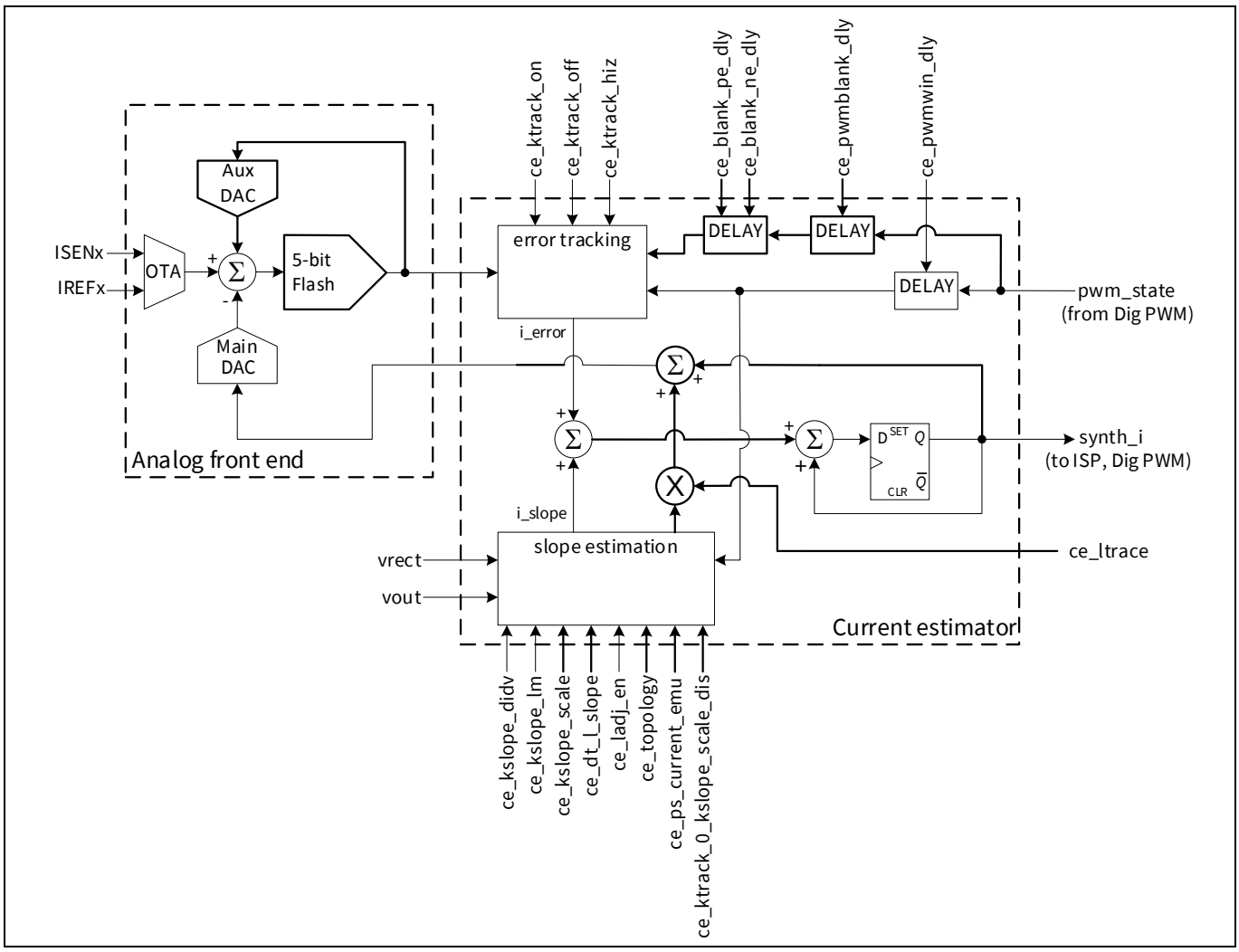


Figure 10 Simplified block diagram of the current sense ADC

For PWM topologies, the current estimator provides a digital reconstruction of the secondary side inductor current or the primary side current, depending on the current sense input pin configuration. The shape of this current is obtained through slope estimation function. Based on the state of the PWM pulse, the controller continuously predicts each individual phase DC and ripple current. The result of the prediction is combined with the actual measured phase current to be processed by the controller. Hence, the instantaneous noise in the measurement can be filtered out without losing the valuable ripple current information.

For LLC topology, the current estimator circuit is bypassed. The output of the current sense block purely relies on ADC sensing. The ADC is capable tracking sinusoid current waveform with slew rate up to 1.6 mV/ns. The current sense processor (ISP) mode is configured by **isp0_mode** and **isp1_mode** registers.

If PCB copper traced is used for current sensing, temperature compensation should be considered to compensate the temperature shift of the copper trace. The controller continuously monitors temperature and uses this information to digitally compensate for resistance changes over temperature. The built-in temperature coefficient is 0.39% Ampere/ °C for copper material. Customized temperature coefficient can be achieved using FW patch.

The controller provides several mechanisms for improving the current sense accuracy. To reduce the effect of board noise on the current sense, leading edge blanking and trailing edge blanking time are implemented at PWM transition. The blanking time can be configured from 0 to 280 ns. In addition, the controller makes

multiple current measurements and the readings are averaged over every switching cycle. To improve the current sense accuracy, the controller also allows to compensate the parasitic inductance of current sense resistor.

The polarity of the current sense can be configured through the ISP digital processor. Write 1 to **isp0_invert_input** or **isp1_invert_input** inverts the polarity. When the polarity is inverted, the current estimator is disabled and current sense relies on the ADC only. The default config is non-inverted.

The major functions of the current sense processor (ISP) and its associated blocks are:

- Current ADC full rate interface to the digital domain
- Current ADC gain and offset trim (digital trim)
- Current scaling
- Output current computation
- Output current shunt temperature compensation
- Output Over/Under Current Protection comparators and fault
- Input current computation
- Input Over Current Protection comparators and fault
- Cycle-by-cycle peak current limit

4.2.5 General purpose AFE3

The general-purpose ADC AFE3, also referred to as telemetry ADC (TS ADC), is a 10-bit, high speed analog to digital converter. Voltage resolution of the general-purpose ADC is 2.344 mV, with a sample frequency 0.926 MHz. The general-purpose ADC block consists of 8 channels with 4 channels externally accessible through pins PRISEN, MP_IMON, TSEN and XADDR1 as shown in **Figure 11**. It can be configured to digitize voltage, impedance, and temperature.

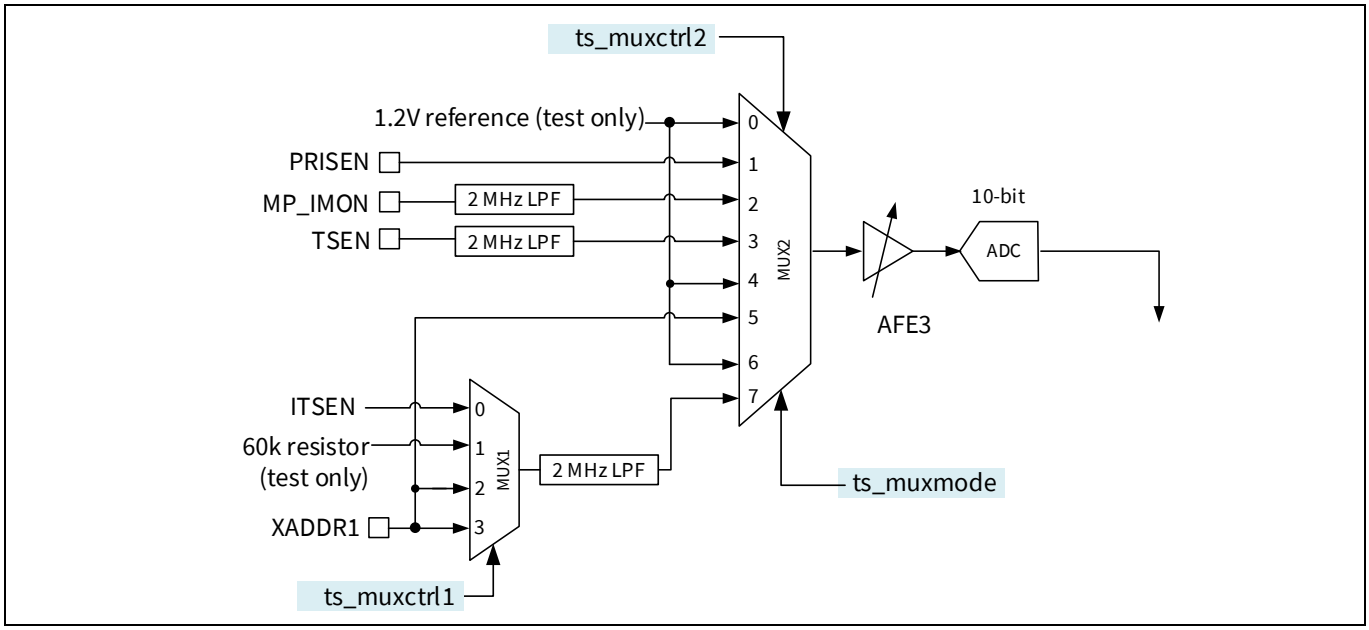


Figure 11 Telemetry ADC block

The conversion sequence of channels can be customized or can be set to auto sequencing per mux control registers **ts_muxctrl1**, **ts_muxctrl2**, **ts_muxmode**.

4.2.5.1 IMON and active current sharing

IMON pin has an analog DAC current source representing the output current. IMON could be used for output current monitor, and for active current sharing in multi parallel modules application. An internal current proportional to the output current is sourced from IMON pin. IMON current DAC (IDAC) is 6-bit DAC with output current range in 0 to 640 µA. There are 4-bit accumulated dithering driving an extra LSB input to the DAC for extra resolution (total 6+4 bit). The gain of the current source is configurable which allows to scale the current source per application. At no load, this source current is 160 µA. IMON source current lower than 160 µA indicates negative current in this module.

Connecting a 2.2 kΩ precision resistor (R_{ishare}) between IMON and a GPIO pin. The GPIO pin is used as a switch to disconnect the R_{ishare} when the converter is not in regulation such as in off state or in fault shutdown. Use register **gpio_config_ishare_imon_disconnect_select_loop0** to assign a GPIO for this function. When the converter is in regulation and the current sharing is active, the GPIO pin connects the R_{ishare} to ground, thus IMON pin presents a voltage proportional to output current. Connecting the IMON of multi converters to the I_{share} bus, the voltage of I_{share} bus represents the average current of the parallel modules.

Each power supply converter would compare its own output current with the average current and adjust output voltage accordingly to reduce the error. To prevent oscillation on small error current, a dead zone applies to the current sharing block. When the error current is less than the dead zone, current sharing is inactive. At full load, the IMON voltage is 1.408 V (640 µA x 2.2 kΩ); and at 0 A load, IMON voltage is 0.352 V (160 µA x 2.2 kΩ).

To smooth the IDAC dithering ripple, it is suggested to put at least 1 nF capacitor between IMON pin and ground. The device has an internal low pass filter to config the bandwidth for the current sharing.

The device provides both positive and negative clamps to voltage adjustment during active current sharing. This guard bands the output voltage in a safe range. If the output voltage reaches the clamping level and the current error is still larger than the dead zone, current share fault is reported.

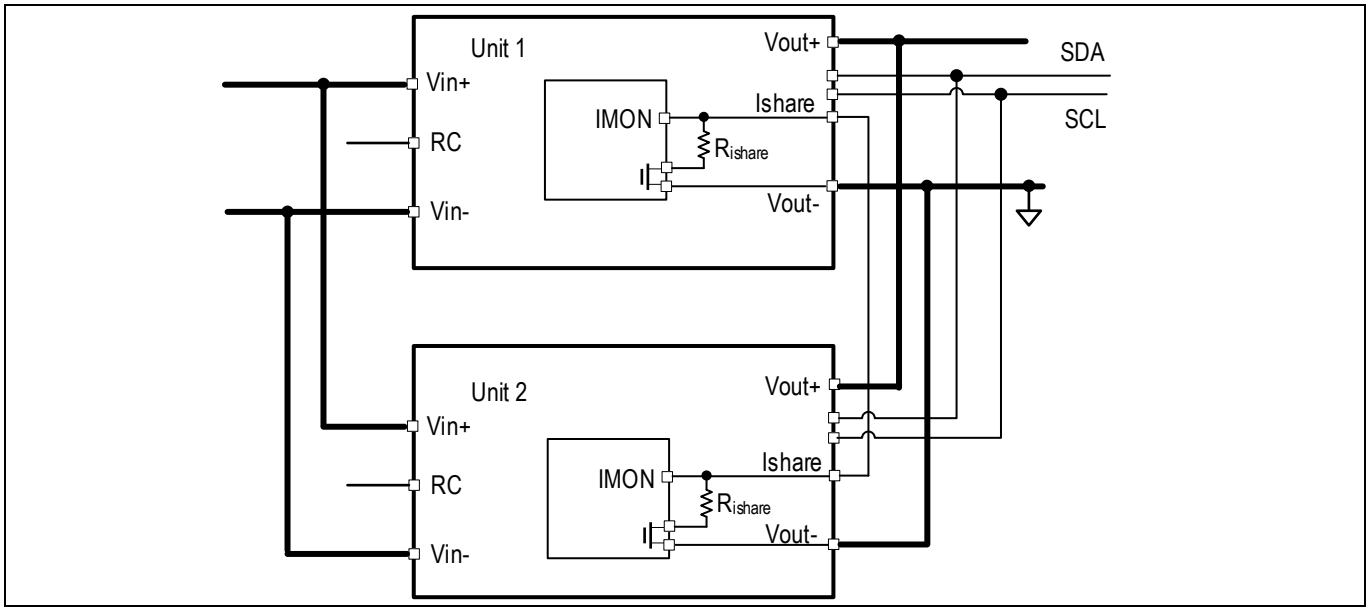


Figure 12 Parallel module current sharing

4.2.5.2 Temperature sense

The device supports both, external and internal temperature sensing for protection and monitoring. External temperature sensing is performed with a temperature sensor connected between TSEN and ground. The device supports sensing temperature by diode forward voltage drop. It is recommend using two diodes in series to provide higher resolution. The temperature sensor should be placed close to and tightly coupled to the element of interest, for example the power stage components or the current sense resistor.

Figure 13 shows the TSEN pin connects to two diodes in series to ground for temperature sense. It also can be configured to use NTC thermistor by replacing the series diodes with a 47 kΩ NTC in parallel with a 12 kΩ resistor. The NTC based temperature sense is backward compatible with the XDPP1100-Q024 solutions. The temperature is sensed by injecting a 100 µA current and measuring the voltage on TSEN. The temperature is used to effectively compensate for the temperature coefficient of the current sense element and to provide over temperature protection by generating warning and fault signals. If the temperature sensor is not required, the TSEN pin must be tied to GND.

When using two-diode voltage drop or V_{BE} for temperature sensing, the offset and gain can be configured based on the actual diode used. It also supports customized temperature lookup table if other temperature sense device is preferred, such as PTC thermistor temperature sense.

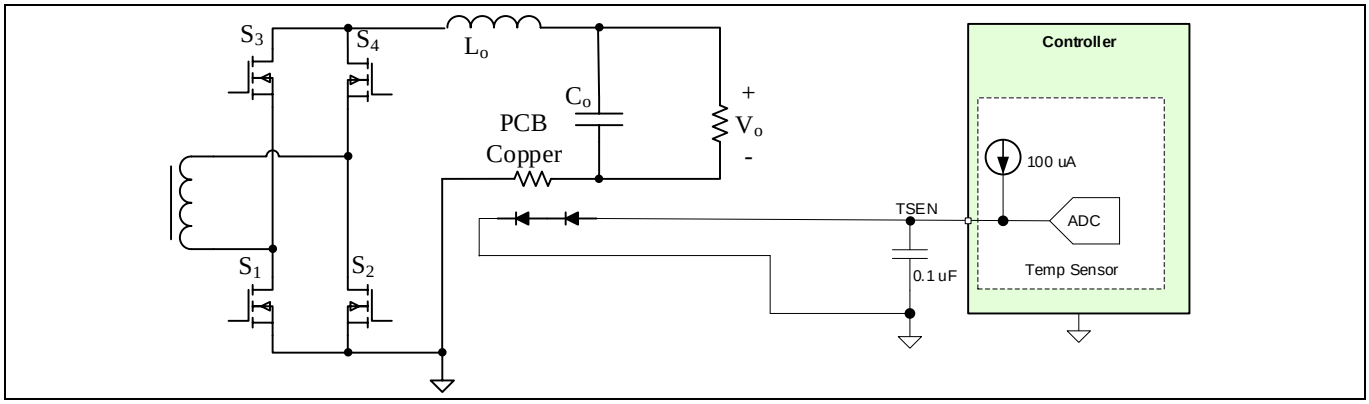


Figure 13 Temperature sensing

A noise decoupling cap is recommended and should be placed between the TSEN pin and GND next to the IC.

The internal temperature sensor is a PTAT (Proportional to Absolute Temperature) voltage generated within the controller die which reflects the junction temperature of the controller.

4.2.5.3 PRISEN

PRISEN is used to sense primary voltage for input voltage telemetry and feedforward compensation. In isolated converter, the V_{IN} voltage should be sensed at primary side and feed to the device through isolated amplifier or auxiliary transformer. The slope and offset of the PRISEN are configured by **vin_pwl_slope** and **vin_trim** registers.

The XDPP1140 has the option to use either PRISEN or VSEN for input voltage sense, configured by register **tlm_vin_src_sel**.

When using PRISEN for V_{IN} sense: The PRISEN is always enabled even when converter is in OFF mode. The general ADC has 0.926 MHz sample rate, and the ADC is shared with three other inputs (temperature sense TSEN, IMON, XADDR1), thus the feedforward response is slower than the VSEN based input voltage sensing.

When using VSEN for V_{IN} sense (only available for XDPP1140): uses high speed ADC VSEN1 or VSEN2 selected by register **vsen_select**. The VSEN ADC has 50 MHz sample rate, provides very fast feedforward response and OV/UV protection. When using VSEN (1 or 2) for V_{IN} telemetry, it can be configured to sense DC input voltage by setting the **vsen_vrect_mode** register to “VIN mode”, or set to “V_{RECT} mode” when sensing at transformer secondary winding. When set to “V_{RECT} mode”, the V_{IN} telemetry is active only after the converter starts switching.

The PRISEN and VSEN voltage sensing could be combined for the best system performance. The XDPP1140 allows to configure the input voltage telemetry and input voltage feedforward independently. Using PRISEN for input voltage telemetry allows continuous input voltage monitoring and pre-startup protections, using V_{RECT} sensing through VSEN for fast feedforward response and flux balancing functions.

4.2.6 Fast trigger input

The device has up to 2 fast trigger inputs – GPI1 and GPI2 - which can be used as external fault shutdown control to increase system reliability; or used for special timing control such as the SR timing of LLC.

Any PWM pin can be configured as the fast trigger input, see **Table 7**.

4.2.7 Fast fault output

The XDPP114x could config MP_IMON, MP_SMBALERT# or MP_SYNC pin as fault output pin. The fault output will change polarity when a loop fault or a common fault is triggered. The response time from fault triggering to the fault pin reporting is less than t_{FSF}. The list of fault and fault mask bit assignment are described in chapter **4.4**. To disable the fault pin responding to a particular fault, set the assigned bit of the **fault_gpio_mask_loop** or the **fault_gpio_mask_com** to 1.

4.3 Control loop subsystems

4.3.1 State diagram

The state diagram is shown in **Figure 14**.

Controller operation is initialized by a power-on UVLO circuit. During controller configuration, the content of the OTP NVM is downloaded onto the control registers. During this period, the GPIO pins are held in high impedance (Hi-Z) state, allowing board pull-up or pull-down resistors to set the correct default levels for static input signals such as the I^2C address (XADDR1).

During the Initialization state, the controller measures the internal and external temperatures, input and output voltage, and executes the various calibration routines within the IC. Prior to exiting the Initialization state, the controller performs the external resistor pin set measurements used to set the I^2C serial addresses. Once a valid I^2C address has been determined, communication with the controller can established via the I^2C bus of the controller.

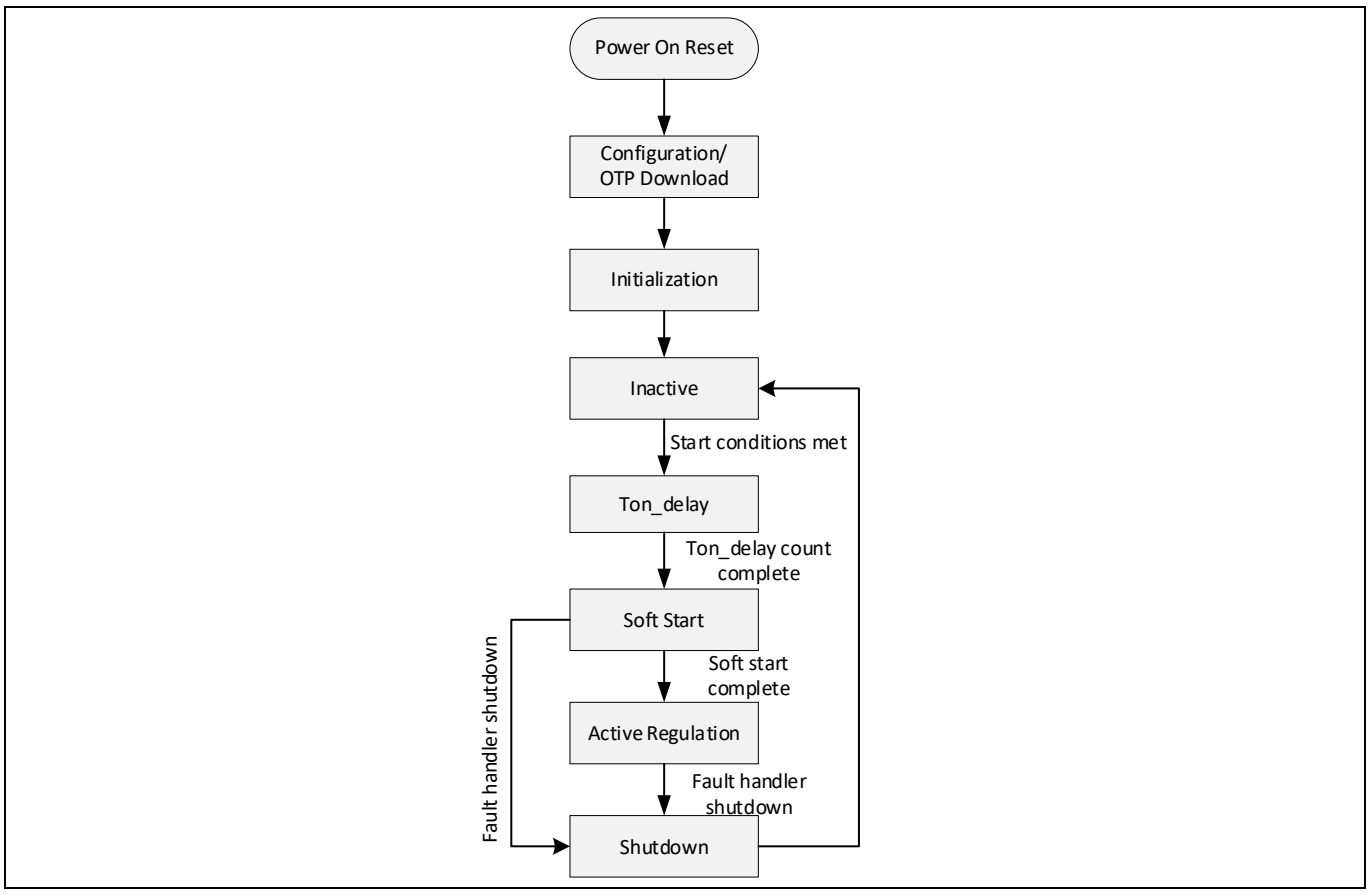


Figure 14 State diagram

Upon completion of the Initialization process, the controller will enter the Inactive state. Controller will verify that the following conditions are satisfied before initiating the system:

1. Valid VDD: The voltage applied to VDD must exceed VDD UVLO rising threshold ($V_{DD\ rising}$) for the internal power valid signal to be asserted. Otherwise, a VDD UVLO fault will be issued.
2. No shutdown faults are asserted that are defined in the programmed shutdown mask.
3. Enable is asserted if the ON_OFF_CONFIG is set to “response to EN”. It is recommended that EN be asserted only after VDD, V_{IN} and power supplies for the power stages are ready.
4. TSEN input and the internal temperature are within operation range.

Once the above startup conditions are satisfied, the controller will wait for a programmable period of time (TON_DELAY) before ramping up the output voltage.

4.3.2 Soft start

4.3.2.1 Soft start for non-resonant topologies

For non-resonant topologies, prior to entering the active regulation state, the controller performs a controlled, monotonic soft start ramp of the voltage output. During Soft Start, the controller will perform a pre-bias condition measurement of the output voltage. The controller could disable synchronous rectifier outputs (diode emulation mode) so that it will not sink current from the pre-biased output. The diode emulation mode in startup can be configured using PMBus command FW_CONFIG_REGULATION. Soft start is performed by actively regulating the output voltage while digitally ramping up a reference voltage from the measured pre-

biased voltage to its final target value. Target output voltage, slew rate, turn-on rise time, as well as number of turn-on trials can be configured during a soft start ramp.

The transition from diode rectification (DE) to synchronous rectification (SR) is seen by the control loop as a load release. To avoid voltage glitch, the control loop resets the PID accumulate error and use the feed-forward duty-cycle when the SRs are enabled. This feature applies to the voltage mode control and is configured by setting **sr_on_mode** to 0 and **pid_reset_accum_en** to 1. With the reset of PID accumulator, by the time the SRs turned on, the loop has a corrected duty-cycle immediately, provides smooth transition from DE to SR mode.

The controller could also gradually increase SR duty-cycle, from a configurable minimum SR pulse width to the full pulse width. See SR soft turn-on in section **4.3.21**.

When the converter completes the initial output ramp to the target output voltage, it enters active regulation state. The power good signal PWRGD is asserted indicating the output voltage is within the regulation window.

4.3.2.2 Soft start for LLC converters

The soft start of LLC converter includes three stages. During the first stage, duty-cycle is ramped up from low to high, while switching at the soft-start initial switching frequency. The LLC start duty-cycle (**llc_ss_duty_start**) and LLC maximum duty-cycle (**llc_ss_duty_max**) are configurable. The LLC soft-start initial switching frequency is configured by **vc_llc_rampstep_start** by defining the rampstep ratio to the minimum switching frequency **pid_llc_tmax**. The duty-cycle ramp time is configured by **llc_ss_duty_step** and **llc_ss_duty_steptime**.

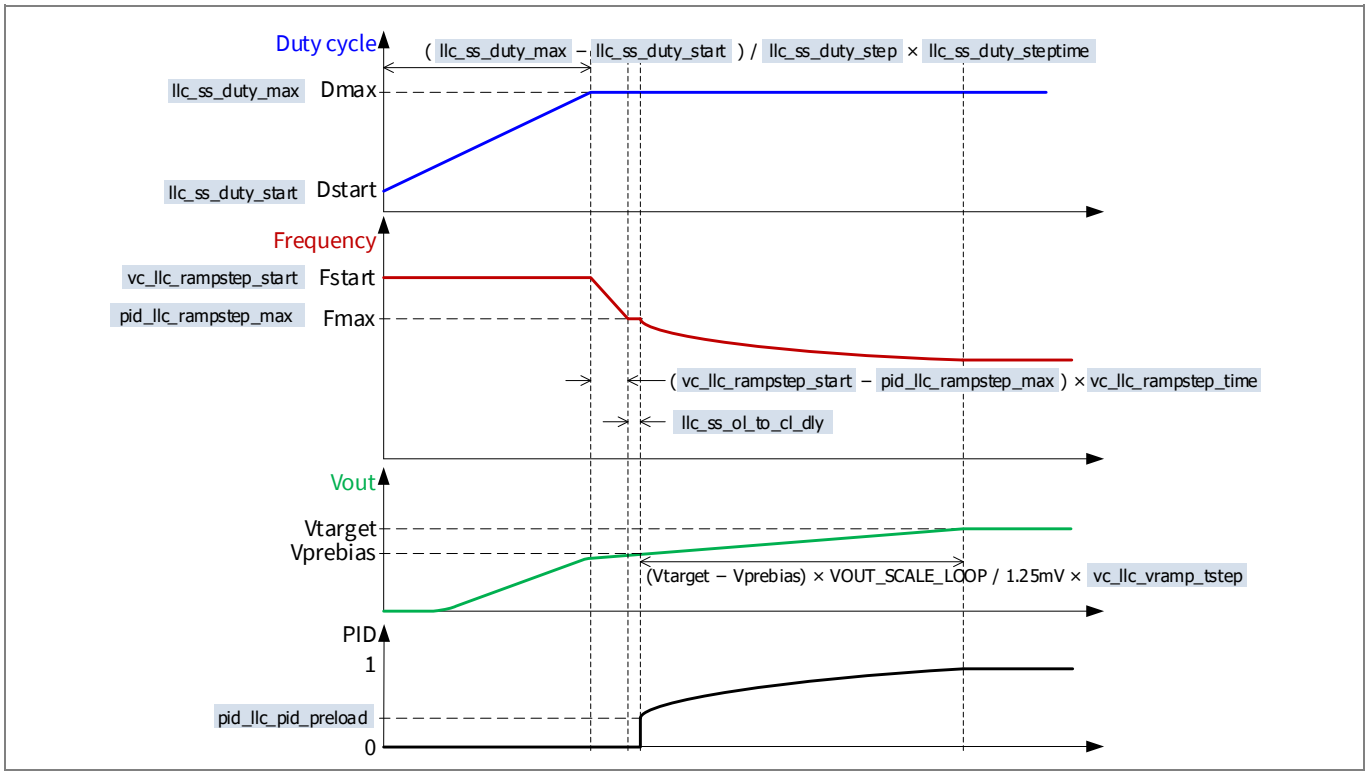


Figure 15 Soft Start of the LLC converter

After duty-cycle reaching the maximum duty-cycle, the converter enters the second stage where the duty-cycle stays at maximum, and switching frequency ramps from the initial soft-start frequency to the maximum switching frequency of LLC. The initial soft-start frequency (by **vc_llc_rampstep_start**) can be set different to the LLC maximum frequency (by **pid_llc_rampstep_max**). If the soft-start frequency is higher than the LLC

maximum frequency, the transition time from the soft-start frequency to the max frequency is defined by **vc_llc_rampstep_time**. If the soft-start frequency is equal or lower than the LLC maximum frequency, the second step is skipped. An optional delay before the start of the third stage is configured by register **llc_ss_ol_to_cl_dly**.

In the third stage, the closed-loop voltage regulation starts. The voltage reference of the control loop ramps from the measured prebias to the final target, and the switching frequency is modulated automatically by the control loop. The voltage slew rate is configured by **vc_llc_vramp_tstep**.

4.3.3 Shutdown

The shutdown state can be entered from either soft start or active regulation states through intervention (de-asserting EN) or through a detected fault. Here are the examples of some fault conditions: over-temperature (OTP), over current (OCP), input under voltage (VIN UVP), input over voltage (VIN OVP), output overvoltage (VOUT OVP), flux balance fault.

The device supports two selectable shutdown options in response to de-assertion of EN. The first option is a closed-loop shutdown where the controller ramps down the output voltage at a configurable slew rate. The second option is a hot-shutdown (Hi-Z) response, where the output stage power FETs are immediately switched off. If immediate shut-down is required, TOFF_DELAY should be set to 0 ms. For cases where the shutdown is caused by a fault, the resultant shutdown response is always Hi-Z.

Once shutdown has occurred, firmware will handle the subsequent response. The shutdown may be final; or the converter may enter a finite or infinite hiccup mode.

4.3.4 Voltage mode control (VMC)

Voltage mode control (VMC) is the most fundamental control mode supported in the XDPP114x and is shown in **Figure 16**. The output voltage is compared to its desired voltage (V_{ref}) to generate an error voltage that is fed into the PID compensation network. The output of the PID is used by the PWM Gen block to create the required signals for the given topology.

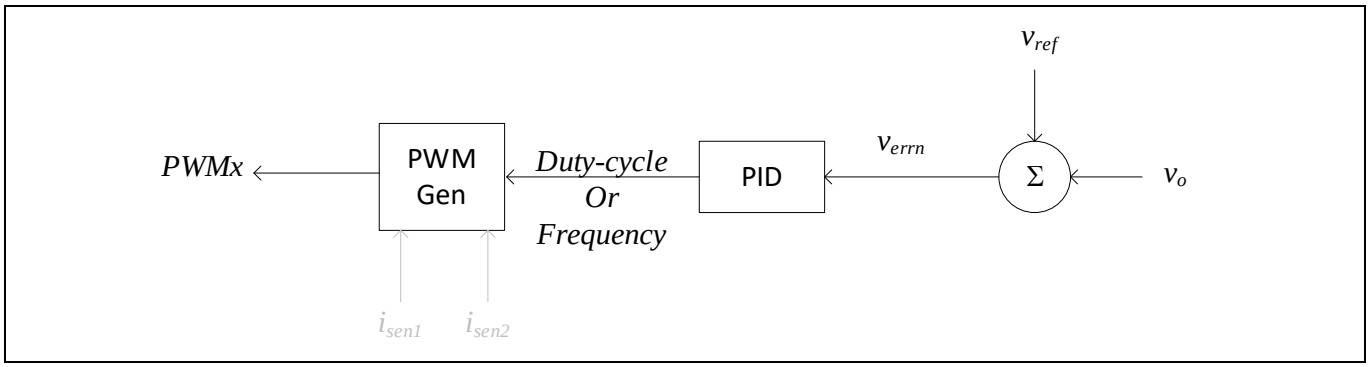


Figure 16 Voltage mode control loop

VMC supports trailing-edge (TE) modulation, leading-edge modulation (LE), and dual-edge modulation (DE) for non-resonant topologies as shown in **Figure 17**. It only supports trailing-edge modulation for LLC topologies. The modulation mode is configured by register rampX_m_flavor.

The first modulation waveform in **Figure 17** a) shows the trailing edge (TE) modulation case. The PWM pulse has a fixed leading edge and a modulated trailing edge.

The second modulation scheme is leading edge (LE) modulation, shown in **Figure 17** b). The PWM pulse has a fixed trailing edge and a modulated leading edge.

The last modulation scheme is dual edge (DE) modulation, shown in **Figure 17** c). In this modulation, the timing markers t1 and t2 are both modulated.

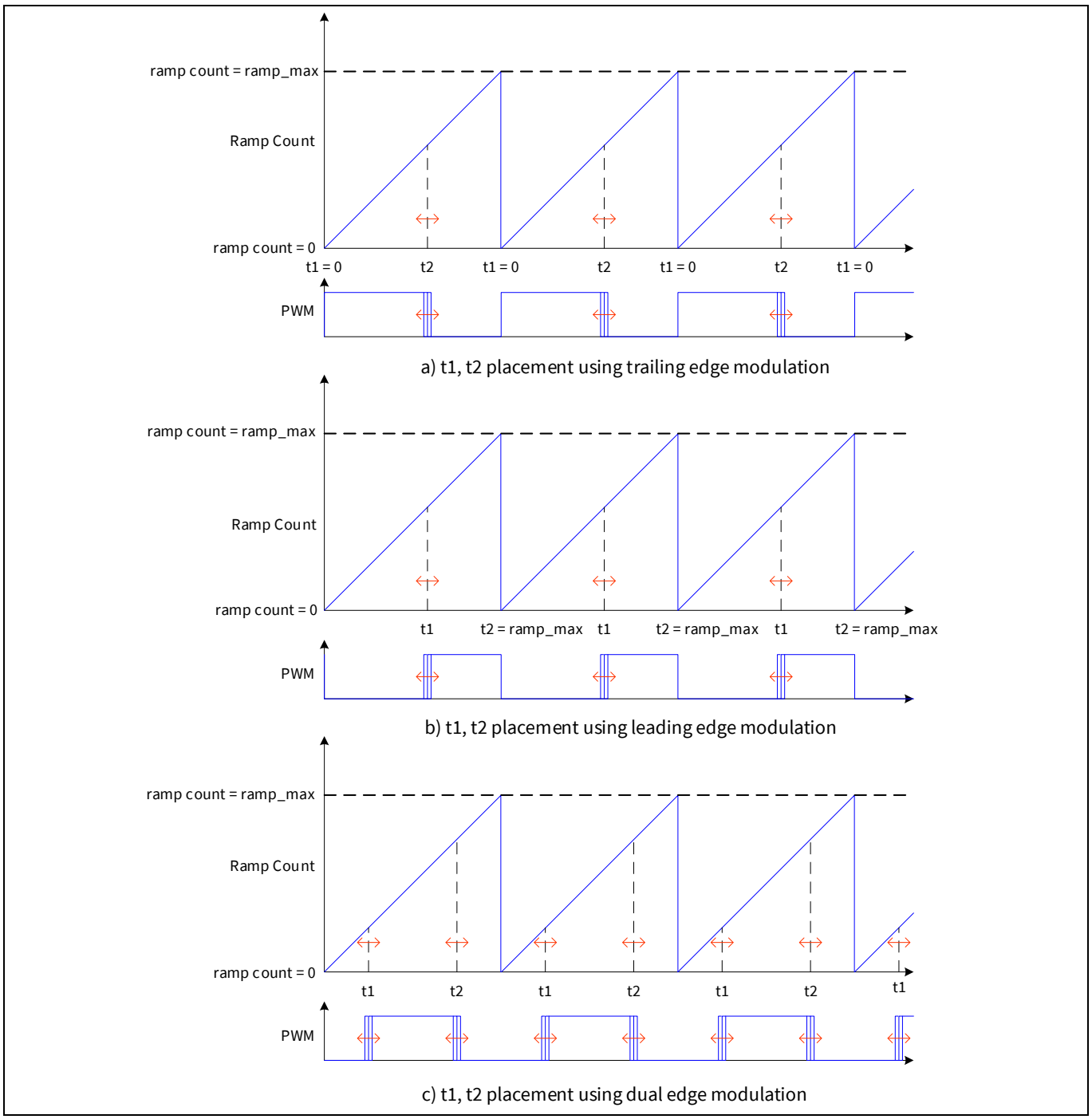


Figure 17 T1 and t2 placement for TE (a), LE (b) and DE (c) modulations.

4.3.5 Peak current mode control (PCMC) non-resonant topologies

In peak current mode control (PCMC), the current is sensed and shut off when it reaches a given threshold. The compensated error voltage defines that threshold value. What is important to note is that to implement

primary side PCMC, the sensed current is not the output current (as in VMC). Instead, the current in the primary devices is sensed and fed across the isolation barrier by a current transformer or isolation amplifier. Secondary side PCMC is compensated similarly to primary side PCMC, the main difference being the sense current in this case is the output (inductor) current. Only the non-resonant topologies support the PCMC.

With PCMC, the derivative of the compensator network is not needed, leaving only a PI for the compensation network.

One issue with PCMC is subharmonic oscillation with duty cycles greater than 50% causing disturbances to grow instead of decay. To overcome this, an auxiliary ramp is added. The slope of the ramp is configurable by register **compensation_slope** from V_o/L, $V_o/2L$, $V_o/4L$, $2V_o/L$, $4V_o/L$, $8V_o/L$.

During startup and controlled shutdown when the duty-cycle is narrow, primary current signal is very small. It is suggested to enable the minimum pulse width register (rampX_min_pw_state = 1) to avoid cycle skipping.

PCMC only supports trailing edge modulation.

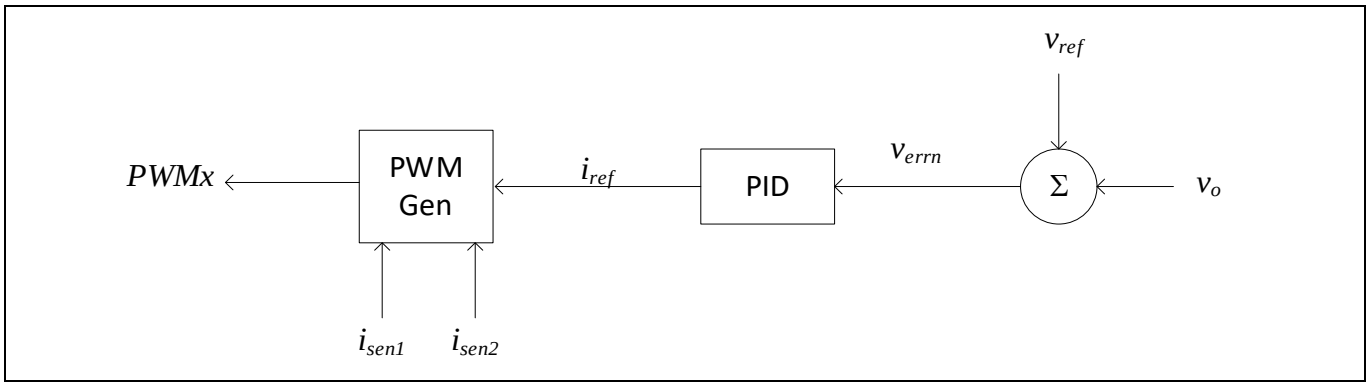


Figure 18 Peak current mode control loop

4.3.6 PID and control loop

The control loop implements a fixed switching frequency, digital PID voltage loop, and dual-edge PWM architecture. During operation, the output voltage is sensed differentially and digitized by a precision analog-to digital converter (ADC). The voltage is compared to reference voltage to generate an error voltage. The resultant digital error signal is then fed into a digital PID compensator with the effective transfer function given by:

$$H_{PID}(z) = \left[\left(K_P + K_D(1-z^{-1})\right)\left(\frac{K_{fp2}}{1-(1-K_{fp2})z^{-1}}\right) + \frac{K_i}{1-z^{-1}}\right]\left[\frac{K_{fp1}}{1-(1-K_{fp1})z^{-1}}\right]z^{-1}$$

The locations of the poles and zeroes are determined by the digital loop coefficients Kp, Ki, Kd, and Kfp, which are the PID (proportional, integral, derivative) and low pass filter pole terms, respectively. It creates the equivalent of type III compensation network. In current mode control, phase lead is not required, so the derivative term Kd should be zeroed out by setting the **pid_kd_index_1ph** to 0.

Two extra sets coefficients of Kp, Ki, Kd are provided (pid_nl_neg_verr_xxx and pid_nl_pos_verr_xxx) to set non-linear loop compensation when the error voltage exceeds customized thresholds in the negative or positive directions.

For non-resonant topologies, the output of the digital PID compensator is converted to a PWM pulse using a digital dual-edge pulse width modulator. The maximum duty cycle limit is programmable up to 99.5%. In addition to using the PID compensator for regulation, the controller has nonlinear control mechanisms such as

fast transient response (**4.3.13**, **4.3.14**), and input voltage feedforward (**4.3.15**), to minimize voltage excursions during transient events. For LLC topologies, the PID output controls switching frequency. See additional information in **4.3.7**.

4.3.7 Frequency modulation (LLC)

Frequency modulation is commonly used for closed-loop LLC topology. When enabled by register **llc_mode**, the PID output is used to control the rate (stepsize) of the internal ramp, which in turn determines the switching frequency. As shown in **Figure 19**, the minimum (Fmin) and maximum (Fmin + Fgain) frequencies are configurable by registers **pid_llc_tmax** and **pid_llc_rampstep_gain**. Optionally, the clamps for max and min frequencies (Fmax and Fmin_clamp) are also configurable.

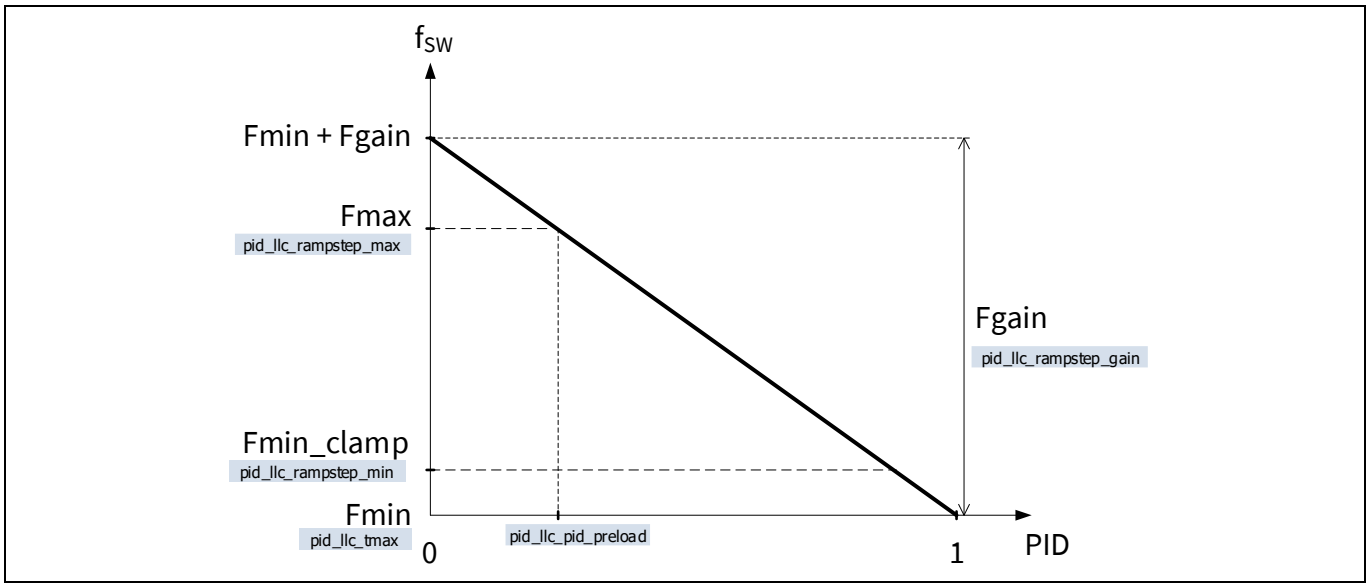


Figure 19 PID output controls ramp stepsize in frequency modulation

4.3.8 Full-bridge LLC phase shift mode

In addition to frequency modulation, phase shift can also be applied in LLC converters with full-bridge primary. This could be useful to improve the light load performance and/or regulation range. When enabled, once Fmax is reached, PID output controls pulse width (t2), as shown in **Figure 20**. The reduction of duty cycle is effectively the increase of phase shift, when the PWMs for primary legs are assigned according to phase-shift full-bridge LLC. That is, one primary leg assigned to t1, and the other leg assigned to t2. Note that in this case, the LLC maximum duty-cycle (**llc_ss_duty_max**) needs to be the maximum 99.9756%.

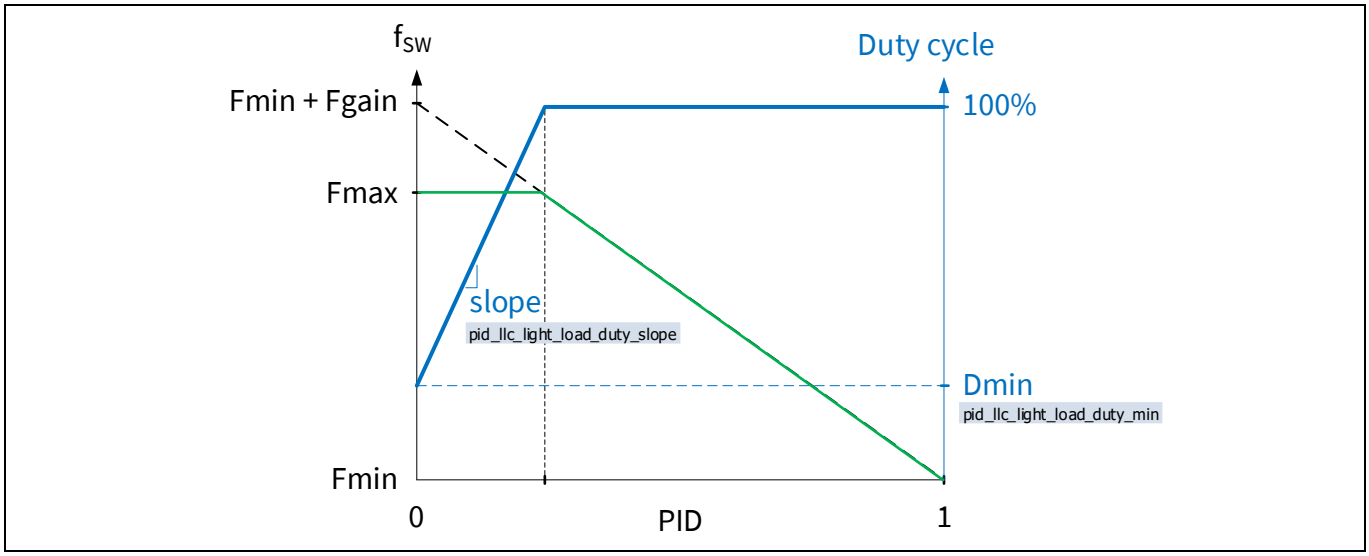


Figure 20 Phase shift control after reaching maximum frequency

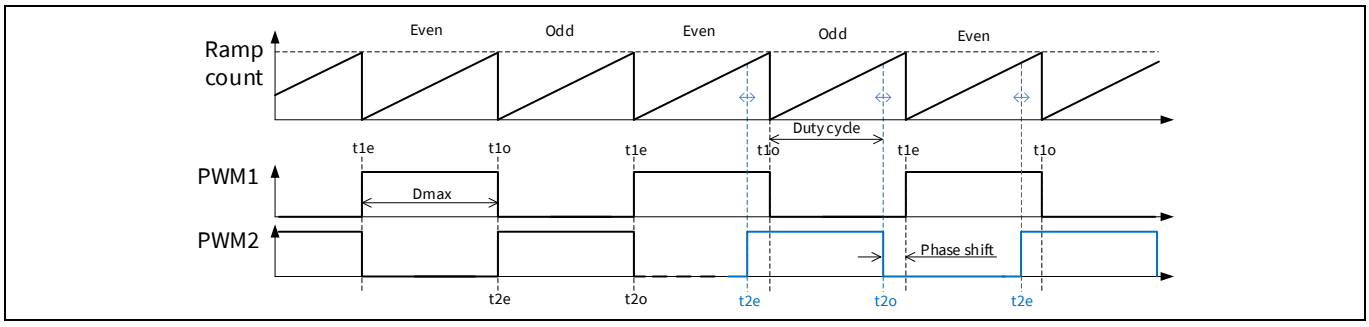


Figure 21 Primary PWM timing in phase shift LLC

4.3.9 LLC SR timing control

In LLC converter the secondary current is not exactly in phase with primary PWM. Therefore, the SR PWM timing of LLC topology requires special control. The XDPP114x offers two types of SR timing control for LLC. They are described in below.

4.3.9.1 Fixed maximum on-time of SR

The SR rising edge is aligned with primary PWM rising edge. Configure SR turn-on delay using dead-time registers for up to 318.75 ns (or extended range of 637.5 ns by reducing the resolution). The turn-off of SR has two scenarios, as shown in **Figure 22**.
A) when the switching frequency is lower than the resonant frequency (F_{RES}), the maximum SR pulse width is limited to the half of the resonant period.
B) if the switching frequency is equal or higher than the resonant frequency, the SR falling edge is aligned with primary PWM falling edge.

The resonant frequency is a parameter (1/ **llc_tres**) that is defined by user based on system design. Additional adjustment to the turn-off is configured by **llc_tdtprim_plus_tiso** and **toff_dly_t3**.

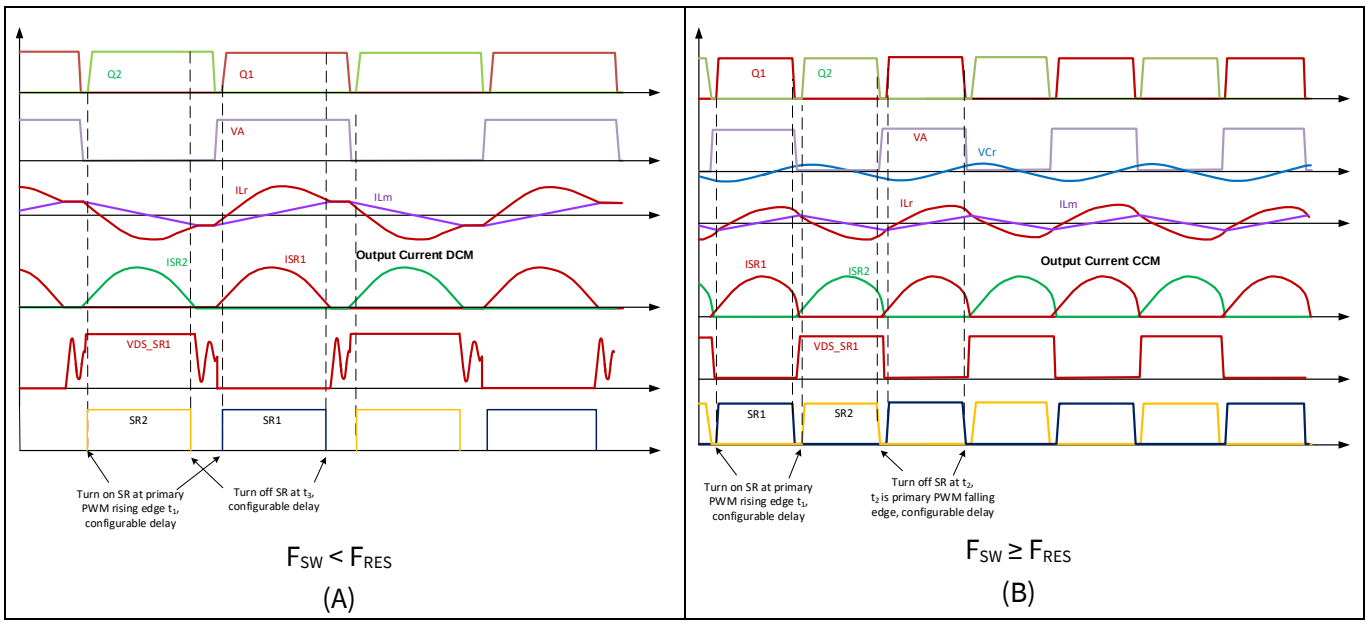


Figure 22 LLC waveforms with fixed maximum SR on time

4.3.9.2 Adaptive SR maximum on-time

The adaptive SR timing control is achieved by sensing the SR V_{DS} voltage. As shown in **Figure 23**, the V_{DS} voltage is first level-shifted and clamped by a small signal MOSFET (such as BSS123N), and send to a comparator with threshold configurable by the resistor divider. The comparator measures the SR body diode conduction time and generates corresponding pulses. As shown in **Figure 24**, the duration between the rising edges of the first body diode conduction pulse before SR PWM turning on, to the falling edge of the second body diode conduction pulse after SR PWM turning off, indicates the half of the resonant period in below resonant operation. This signal is sent to the fast GPI1 input and is processed by the device to adjust the maximum SR pulse width.

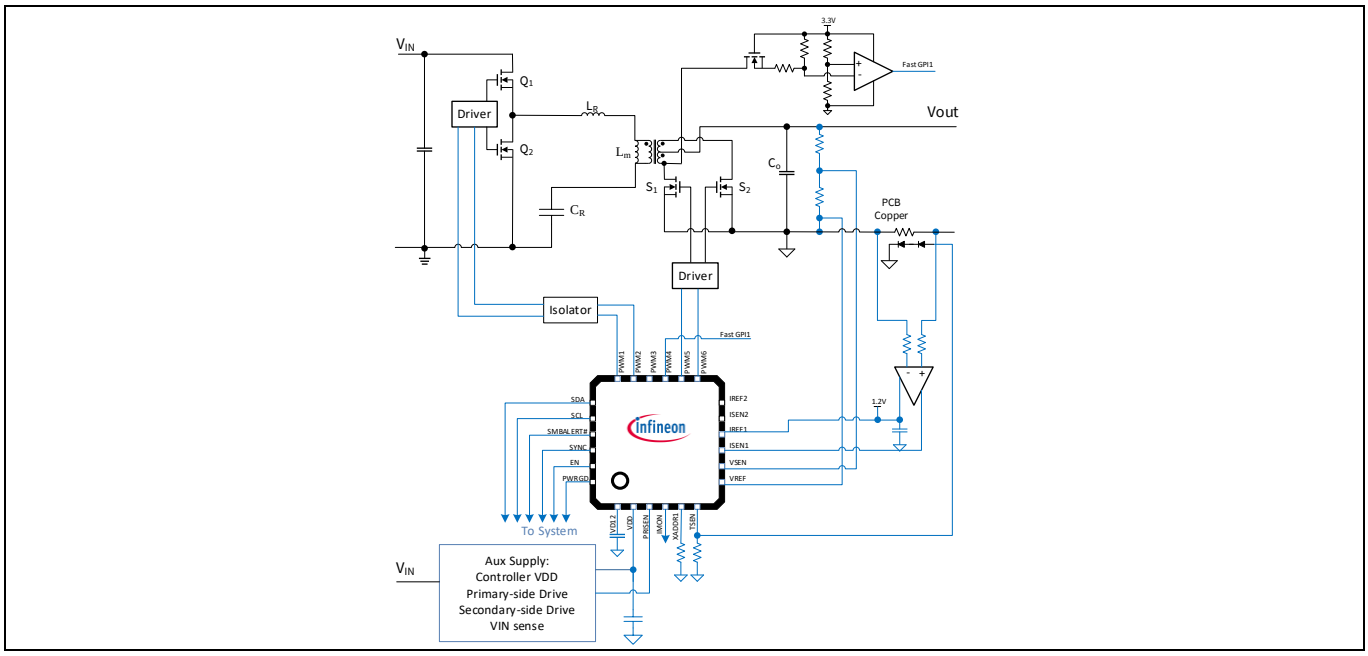


Figure 23 LLC with SR VDS sensing

The device supports negative delay (**toff_dly_t3**) at the SR PWM falling edge, which truncates or subtracts the SR on pulse-width. Negative delay range -315 ns to 0 ns, resolution -5 ns.

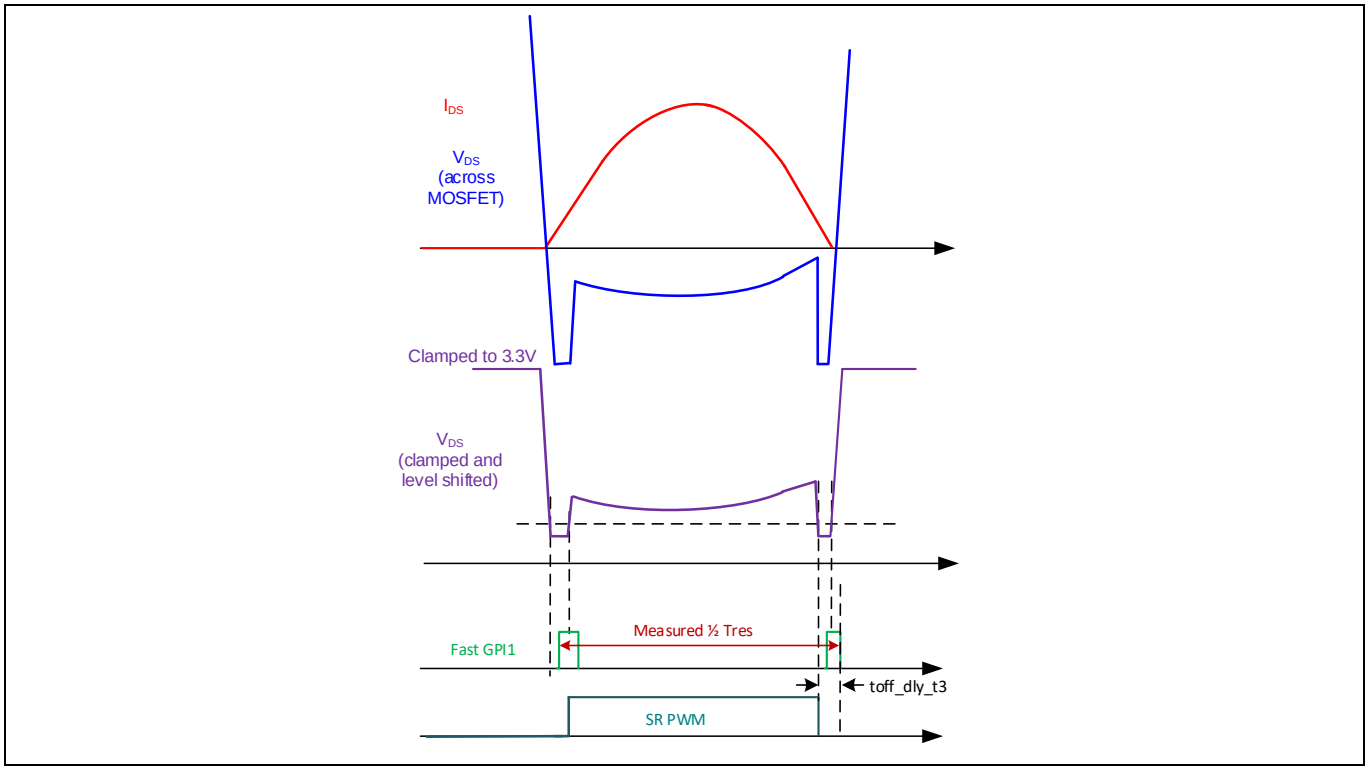


Figure 24 SR VDS sensing and fast GPI1 waveform in below resonant operation

4.3.10 Current sense estimator for non-resonant topologies

The current sense estimator (CE) samples the inductor current and provides slope estimation and tracking. Based on the state of the PWM pulse, the controller continuously predicts DC and ripple current. The result of the prediction (estimation) is combined with the actual measured current (tracking) to be processed by the controller. The percentages of tracking in this combination can be configured for three individual PWM states: HiZ, off, and on state by registers ceX_ktrack_hiz, ceX_ktrack_off, and ceX_ktrack_on, respectively.

The current estimator implements different equations for buck-derived, boost and buck-boost topologies. For output current sensing in isolated buck-derived topologies, slopes during the energy transfer interval depend on the value of the rectified voltage, which is a function of input voltage and transformer turns ratio, the filter inductance, and the output voltage. The freewheeling interval can be split up into two parts: the first where the SR body diode conducts, and the second where the SR is on so the channel conducts. In the first case, the slope is a function of the output voltage, inductor, and forward voltage of the diode. In the second case, the slope is a function of the output voltage and filter inductance. Register ceX_kslope_didv defines the normalized output inductor value for slope estimation.

The output current could be sensed before the output capacitor bank, which is the inductor current with ripple; or could be sensed after the output capacitor which is DC current without ripple. Sensing the inductor current enables the capability of secondary peak current mode control. Sensing DC output current precludes the use of secondary PCMC and cycle-by-cycle peak current limit.

When used for primary-side PCMC, the CE estimates the slope of the current during the energy transfer interval. The slope is a function of input voltage, output inductance, output voltage, turn ratio N, and magnetizing inductance of the transformer. The primary-side current is sensed through a current transformer and fed to the

ISEN inputs; which means the turn ratio of the current transformer, along with its termination resistor introduces a gain scaling term. Register ceX_kslope_lm defines the normalized transformer primary magnetizing inductance.

If the ripple current magnitude falls outside of a configurable range, a current sense tracking fault will be issued. The enable of current track fault is configurable.

The CE supports compensation of the following non-idealities associated with typical DC-DC converter current sense schemes:

- The step induced by the parasitic inductance of the current sense trace resistance
- Output inductance variation with output current
- Leading-edge and falling-edge blanking time due to noise after PWM toggles

4.3.11 Load-line (Droop)

The device supports VOUT_DROOP in LINEAR11 format. The droop is used for current sharing purpose when multiple converters are connected in parallel. The output voltage reduces when output current increases, the actual output voltage is set based on PMBus command, VOUT_COMMAND – READ_IOUT * VOUT_DROOP.

The multi-segment droop is implemented for constant current and constant power operation. Multi-segment droop is a type of non-linear droop that allows to define different droop resistance under different load current. If the load-line resistor is set high, output voltage will sag quickly when the current exceeds the set threshold, behavior similarly to constant current (CC) or constant power (CP) operation.

Figure 25 shows the behavior of multi-segment load-line. A load-line value of $R_{LL,neg}$ is used when the output current I_o is less than zero. This is meant to help current balancing in parallel module application. $R_{LL,1}$ is the regular droop resistance that defined by standard PMBus command VOUT_DROOP. From I_{thr_seg2} to I_{thr_seg3}, $R_{LL,2}$ is used to emulate constant current operation. From I_{thr_seg3} until the overcurrent shut down threshold $I_{OC,SD}$, $R_{LL,3}$ is used for approximate constant power operation. $I_{OC,SD}$ equals to the IOUT_OC_FAULT_LIMIT.

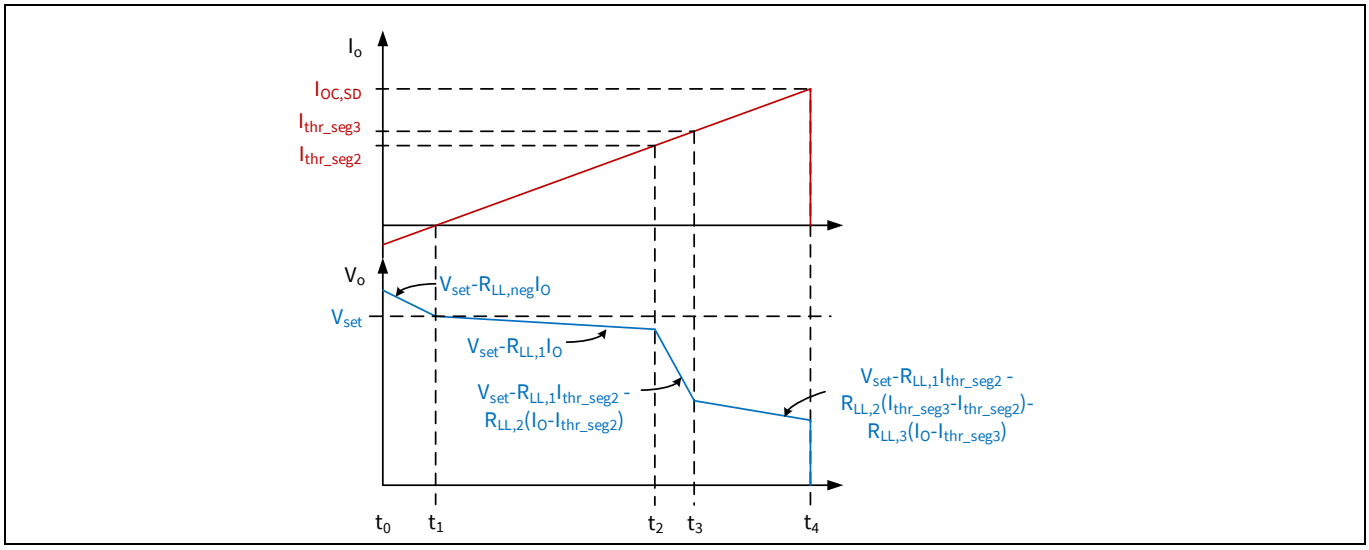


Figure 25 Load-line implementation for over-current protection

4.3.12 AC droop

For applications which cannot tolerate the DC voltage drop that introduced by the load-line at heavy loads, the controller can still provide some load-line benefits with its AC droop feature. Instead of dropping the DC target

based on the load current, AC droop temporarily adds this load-line offset through a programmable band pass filter. At either low or very high load transient frequencies, the load-line is blocked by the filter. At near mid-band, a non-zero load-line is in effect.

4.3.13 Fast transient response (FTR) for bridge topologies

The device implements fast transient response to half-bridge and full-bridge topologies. Upon the detection of a positive load transient the converter effectively saturates the rectified voltage by changing the switching period from T_{sw} to $2T_{on}$ where T_{on} is the product of duty-cycle D and switching period. Since duty-cycle varies with input voltage, the operating frequency during the transient is also dependent on input voltage.

Transient detection can be achieved by threshold voltage detection in the Vo sense as shown in **Figure 26**, or threshold of the derivative of the error voltage (not shown), or a combination of the two. The peak inductor current (i_L) depends on the load step Δi_o and input voltage (which determines the rate of rise of the inductor current.

Output voltage starts recover after a couple of FTR cycles when the current in output inductor is higher than load current. To avoid overshoot, the converter should exit FTR mode before V_{OUT} getting back to the set target voltage. The device exits FTR mode at a configurable error voltage threshold which is always below target V_{OUT}. The error voltage is defined as (target voltage - sense voltage). When the error voltage is smaller than the set threshold, the controller exits FTR mode. At FTR exit, the device would complete the present FTR cycle then resume switching period back to T_{SW}, the linear loop then takes over for regulation.

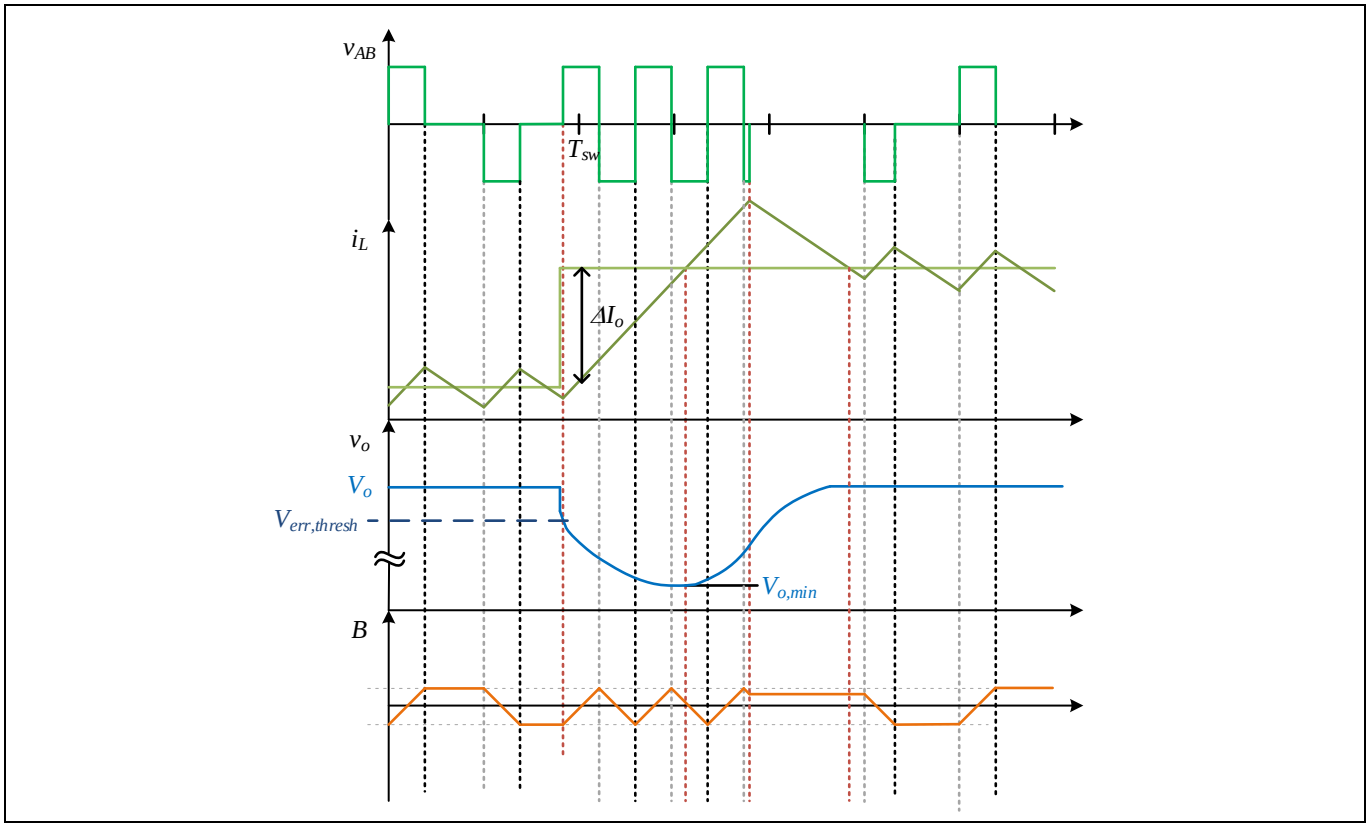


Figure 26 Waveforms of fast transient response with transformer protection

4.3.14 Fast transient response (FTR) for buck

The triggering of FTR of a buck converter is the same as the bridge topologies. The magnitude and slope of the error voltage of the output is monitored. The FTR function will increase the duty-cycle during a positive load transient to reduce output undershoot. The FTR duty-cycle is configured by rampX_ftr_duty_sel register. The overshoot fast transient response (OVS_FTR) function will reduce pulse width at a negative load transient to reduce output overshoot. The PWM pulse in OVS_FTR jumps to the minimum pulse width defined by command MFR_MIN_PW. The buck FTR is enabled by bit [5] of rampX_ftr_duty_sel.

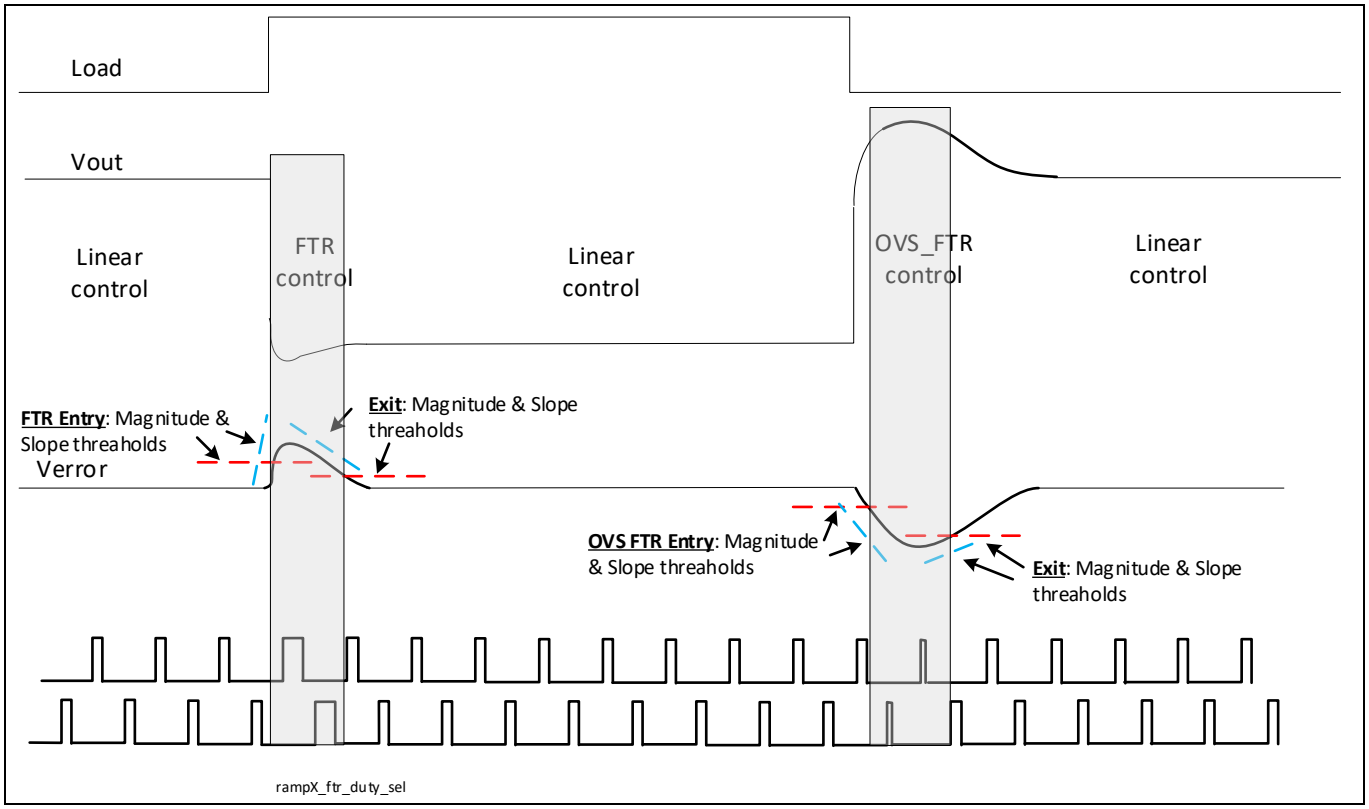


Figure 27 FTR of Buck topology

4.3.15 Input voltage feedforward

Input voltage feedforward involves using input and output voltage measurements to set the nominal duty cycle for the given conditions. Upon sensing a changing of input voltage, the controller could quickly compensate duty cycle based on input voltage, output voltage, and the SRs condition. In an input voltage transient condition, feedforward response is much faster than output linear loop. In isolated converter with controller sitting at the secondary side, fast and accurate V_{RECT} sensing is critical to achieve high performance feedforward.

The controller allows to config one of the following sources for the feedforward computation.

- Sensed V_{IN} on the VSEN input configured by **vsen_select** (VSEN1 or VSEN2)
- Sensed V_{IN} on the PRISEN input (Telemetry sense V_{IN})
- **pid_ff_vrect_override** is provided for FW override of sensed V_{RECT}

Feedforward duty cycle calculation varies with topology, as defined in the equations below. The input voltage is measured, while target output voltage ($V_{o,target}$) and turns ratio are register settings.

$$D_{HB} = \frac{2 \times N \times V_{o,\,target}}{V_{in}}$$

$$D_{FB,\,ACF} = \frac{N \times V_{o,\,target}}{V_{in}}$$

$$D_{Buck} = \frac{V_{o,\,target}}{V_{in}}$$

$$D_{Buck\_boost} = \frac{V_{o,\,target}}{V_{in} + V_{o,\,target}}$$

$$D_{Boost} = \frac{V_{o,\,target} - V_{in}}{V_{o,\,target}}$$

HB: Half-bridge, FB: Full-Bridge, ACF: Active Clamp Forward, N: transformer turns ratio N_p:N_s

4.3.16 Current balancing of XDPP1148

Current balancing is required for interleaved topologies. The circuit receives the cycle-averaged current from the ISEN1 and ISEN2 inputs. The difference between these current inputs is computed and used as the input to a PI compensation filter. The filter output, adjusts the duty-cycle of the PWM ramp0 up to ±25 percent.

An enable threshold applies to current balancing block. Current balancing only activates when the total current is higher than the enable threshold which has options of 0 A, 3 A and 5 A.

4.3.17 Current sharing

Current sharing refers to balancing the current of individual power supplies that provide a common output voltage. One way to implement current sharing is to use IMON (section **4.2.5.1**), shown in **Figure 12** where the Ishare pin of each converter are connected and feed an external resistor R_{ishare}. The IDAC generates a current proportional to the load current of the module. The sum of the currents creates a voltage across the resistor that is measured by the general ADC and used to identify how equal the current is shared between the two modules. Current sharing is a slow loop (ex. 10% of voltage loop bandwidth).

The second method of current sharing is passive and uses load-line (Section **4.3.11**).

4.3.18 Flux balancing of XDPP1140

In full-bridge (FB) converters, timing mismatch can cause the applied volt-seconds across transformer during one half cycle to be greater than the volt-seconds during the opposite half cycle. This places a dc voltage across the transformer core leading to saturation due to ‘flux walkaway.’ To avoid this, PWM timing must be adjusted to balance each half cycle to account for practical timing differences.

The XDPP1140 supports volt-second based flux balancing for FB in voltage mode control. It uses input voltage measurement and timing measurement during each half cycle. Error between the volt-second product of each half cycle is fed to a PI compensation network for duty cycle augmentation. The adjustment applies to odd half-cycles.

The XDPP1140 uses the rectified voltage (V_{RECT}) for voltage and timing measurement. The high-speed edge comparator has 5 ns accuracy for timing measurement, enables high performance flux balancing. The edge comparator has two configurable reference voltage thresholds: 500 mV and 300 mV. To have proper voltage sensing, the V_{RECT} voltage should be scaled properly. The recommended voltage range of VSEN is 600 mV to 2 V.

The device supports flexible balances solutions, including volt-second balance, voltage mode balance, and time-only balance. The allowed maximum duty-cycle correction is configurable with resolution 0.09766 %. To avoid balancing error in DCM operation, the flux balance can be disabled in DCM with a configurable output current threshold. The flux balancing is disabled in burst mode.

Failure to achieve flux balance within a programmable number of cycles would generate a fault. More details of flux balancing and flux balance fault protection can be found in application note.

For V_{RECT} sensing, do not put filter cap to VSEN pin to avoid waveform distortion. Route the VSEN and VREF in pairs for Kelvin sensing; keep the route away from other switching node to avoid noise coupling.

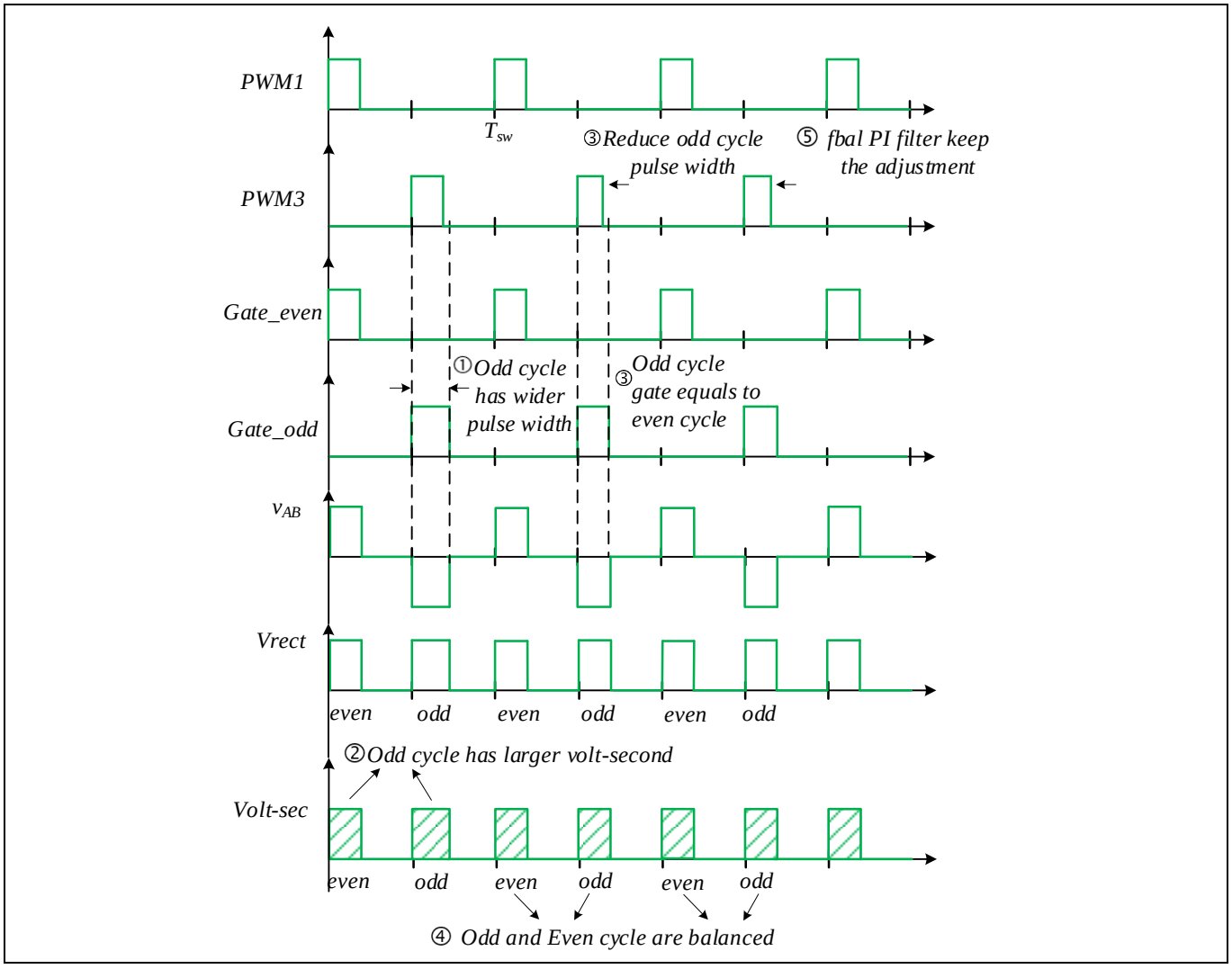


Figure 28 Volt-second flux balancing

4.3.19 Burst mode

4.3.19.1 Burst mode for non-resonant topologies

To increase light load efficiency, converter could enter burst mode to reduce switching losses. For non-resonant topologies (except ACF topology), when the load current falls below the burst entry current level, the converter should enter burst mode operation. Converter stops switching when entering burst (burst-off). Switching is resumed when output voltage drops to a target level (burst-on). This target level defines output

voltage ripple in burst mode. In burst mode, PID output is frozen to the value prior entering burst. Thus during burst-on period, the converter works in constant on time mode. The SRs are turned off during burst mode. The frequency of the PWM bursts will be same as the switching frequency. The number of switching cycle in burst-on is configurable, from minimum one cycle up to 16 switching cycles. Burst mode exits either due to a side by side burst-on event (the burst-off time is less than half of the switching period) or by output current exceeding the burst exit threshold **burst_exit_ithr,** enabled by **burst_exit_ithr_en**. During burst mode, a stronger low pass filter **tlm_kfp_iout_burst** can be configured to smooth the IOUT telemetry.

Representative waveforms are shown in **Figure 29**. More details of the burst operation can be found in application note.

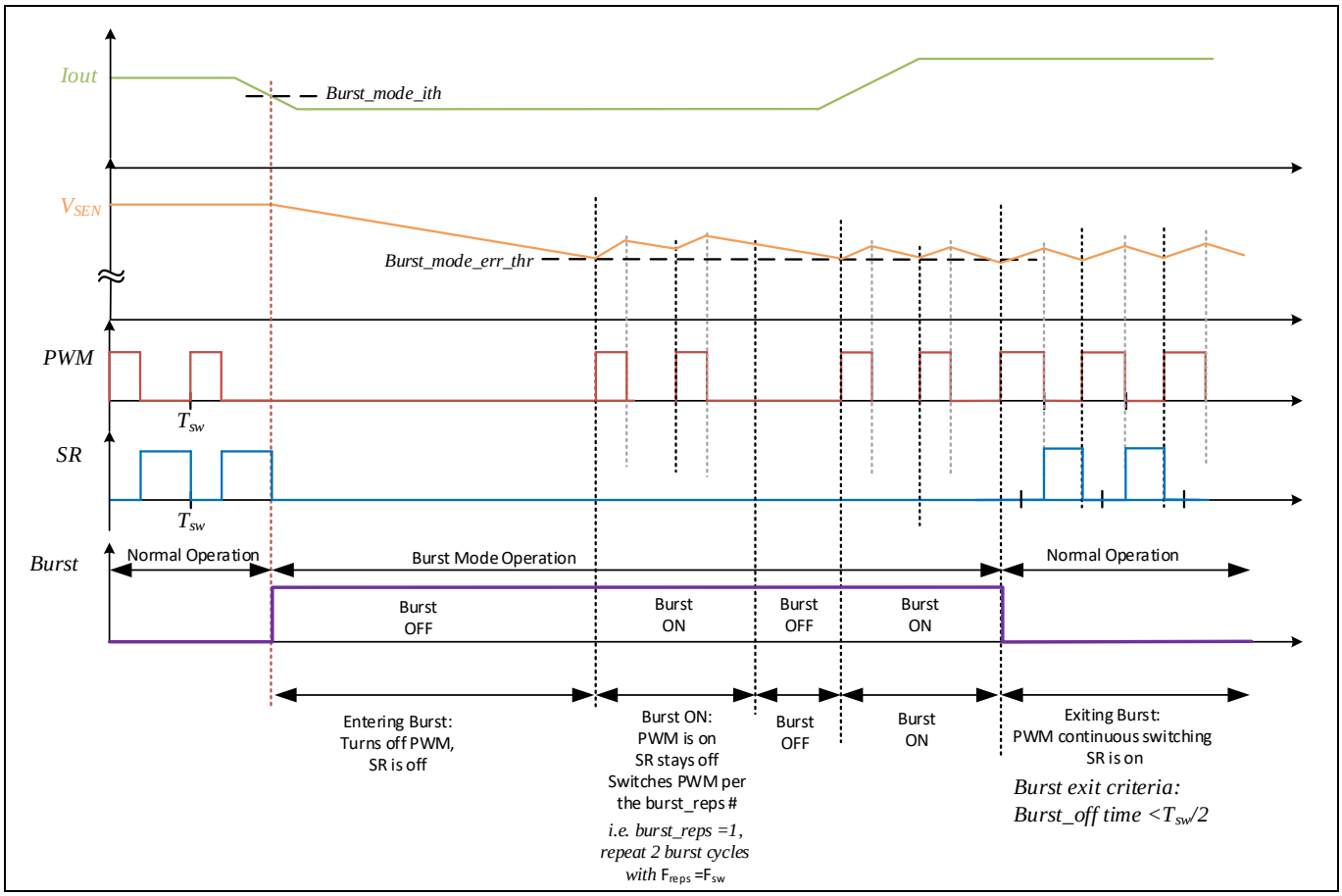


Figure 29 Waveforms in burst mode operation (non-resonant topologies)

4.3.19.2 Burst mode for LLC topologies

At high line and light load, the LLC converter switching frequency increases towards the maximum frequency F_{SW_MAX}. The converter enters burst mode if the F_{SW} hits the F_{SW_MAX} while the output voltage is at the maximum allowed error threshold. The burst entry condition can also be based on load current (light load) with configurable threshold. In burst mode, SRs can be turned off or keep on based on configuration. The primary PWM stops switching until the sensed output voltage drops to a target level (**burst_mode_err_thr**), then primary PWM resumes at F_{SW_MAX} frequency (burst-on) for user defined number of switching cycles. In a single burst-on, the number of switching cycles can be set from one cycle up to 16 cycles. The primary PWM stays off afterward (burst-off) until sensed output voltage drops to **burst_mode_err_thr** again.

In the burst mode, switching frequency is F_{SW_MAX}. The last PWM pulse has half of the regular pulse width (1/4 T_{SW}) when entering the burst mode. This makes the primary magnetizing current and resonant current nearly zero during the burst on to burst off transition. The first burst-on pulse is always on the same side and is also half of the regular pulse width. The magnetizing current "continuous" in the same di/dt direction as the last pulse.

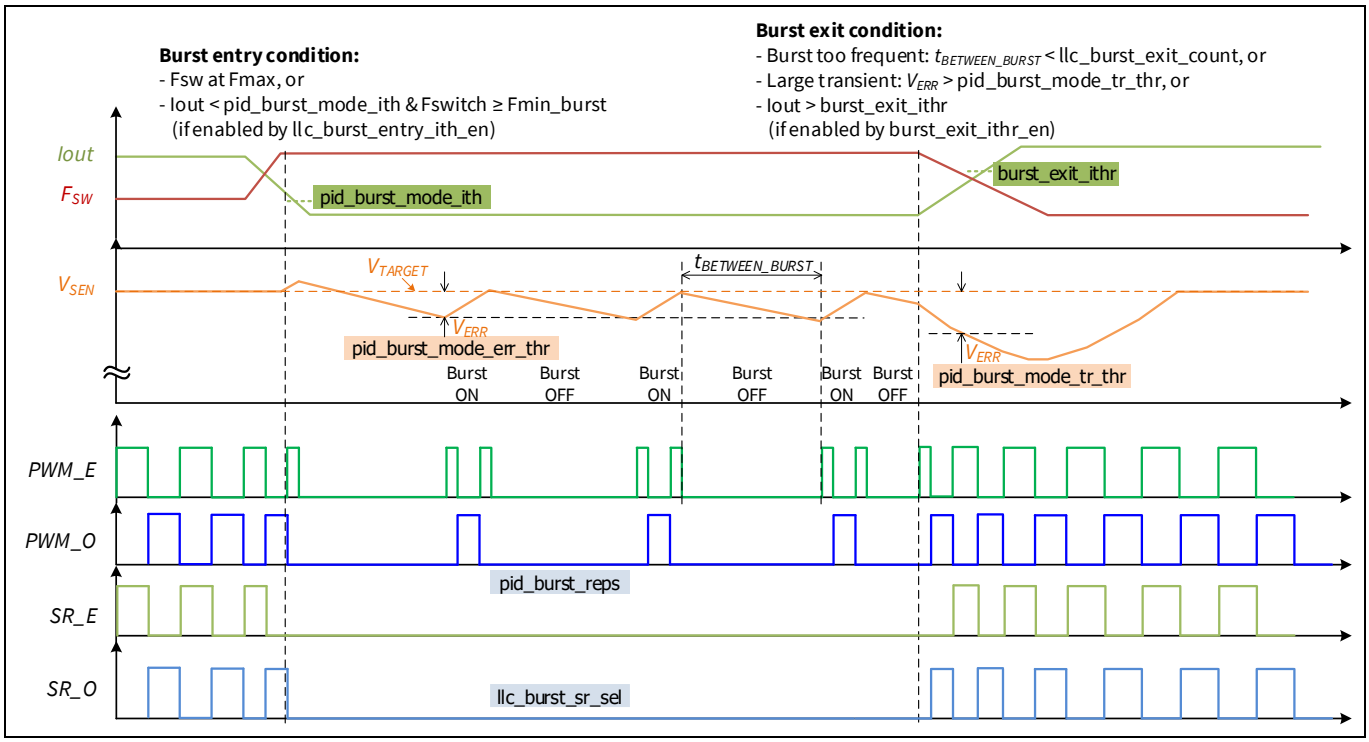


Figure 30 LLC burst mode

Exist of burst mode happens when the control loop reduces switching frequency as load increasing, or when load transient happens.

4.3.20 Phase shedding

At light load, the interleaved topologies could drop one phase when output current is lower than phase shedding threshold. The phase shedding and resume are implemented in hardware for fast response.

4.3.21 SR soft turn-on

The SR could be disabled during the prebias startup or in light load DE mode to avoid negative current in the SR MOSFETs. SRs usually enables at the end of soft-start or when existing DE mode. To have a smooth transition when enabling SR, the duty-cycle of the SR pulse could be configured to increase from minimum pulse width to the full pulse width.

Figure 31 shows SR soft turn-on in DE mode startup of a hard-switching bridge topology. At the end of V_{OUT} startup ramp, the converter exists DE mode and starts driving SR MOSFETs. The SR rising edge is aligned with the corresponding primary PWM rising edge. The SR pulse width increases gradually from the minimum SR pulse width (configurable) to the full duty-cycle of the primary PWM. The number of steps is configurable. When the SR duty-cycle is the same as the primary PWM, the controller turns on SR with full pulse width in the next cycle.

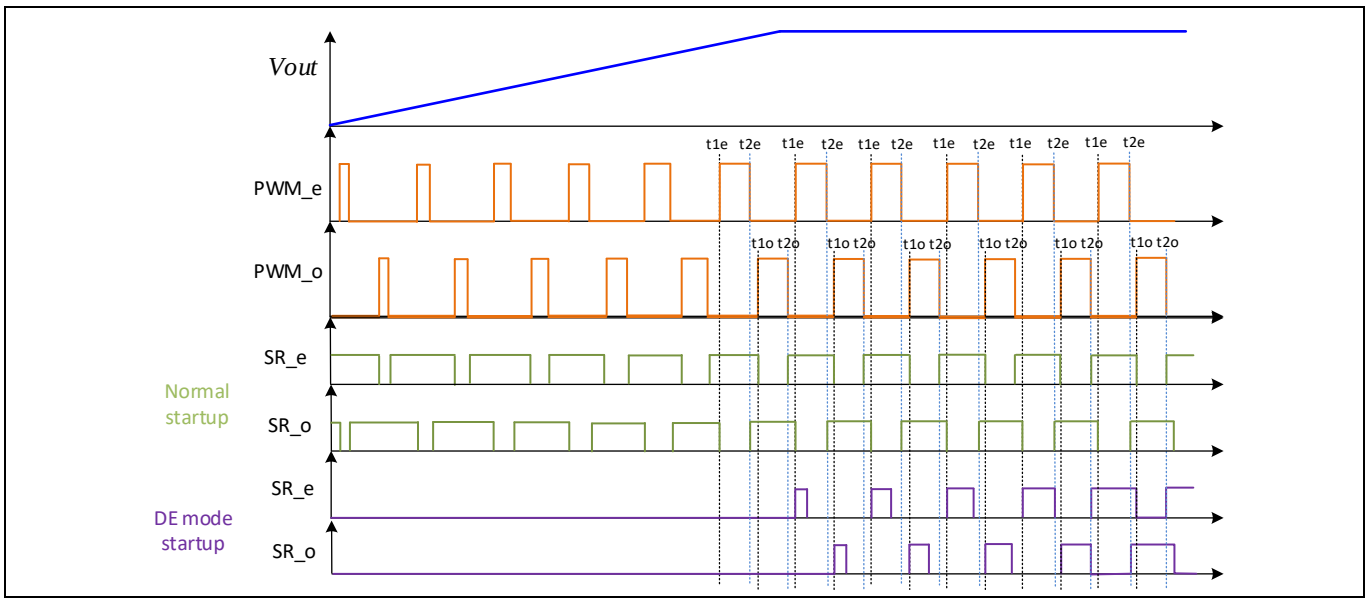


Figure 31 SR soft turn-on of PWM bridge topologies in DE mode startup

The SR soft turn-on from DE mode of LLC converter is shown in **Figure 32**.

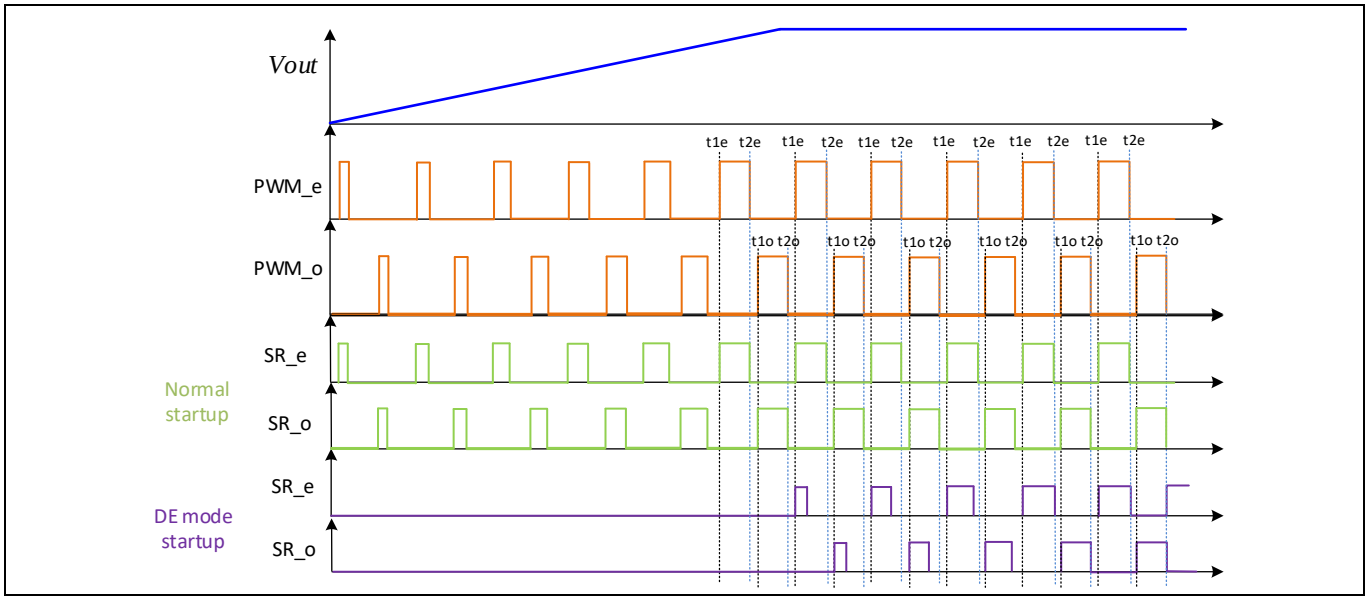


Figure 32 SR soft turn-on of LLC topology in DE mode startup

4.4 Protection and fault

The fault protection system has the following functions:

- Controller VDD under-voltage lock out (VDD UVLO)
- Input under/over-voltage protection (VIN_UV/VIN_OV)
- Input over current protection (IIN_OC)
- Input over power warning (PIN_OP)
- Output under/over-voltage protection (VOUT_UV/VOUT_OV)

- Output under/over-current protection (IOUT_UC/ IOUT_OC)
- Output over power warning (POUT_OP)
- Pulse-by-pulse peak current limit protection (PCL)
- Short circuit protection (SCP)
- Internal/external temperature protection (OT/ UT)
- Flux balance fault
- Sync fault
- Current sharing fault
- First to assert SMBALERT#
- Configuration (CRC) failure
- I^2C communication failure

The hardware (HW) protection block diagram is shown in **Figure 33**. The controller implements all the fault protections without the need of using external comparators.

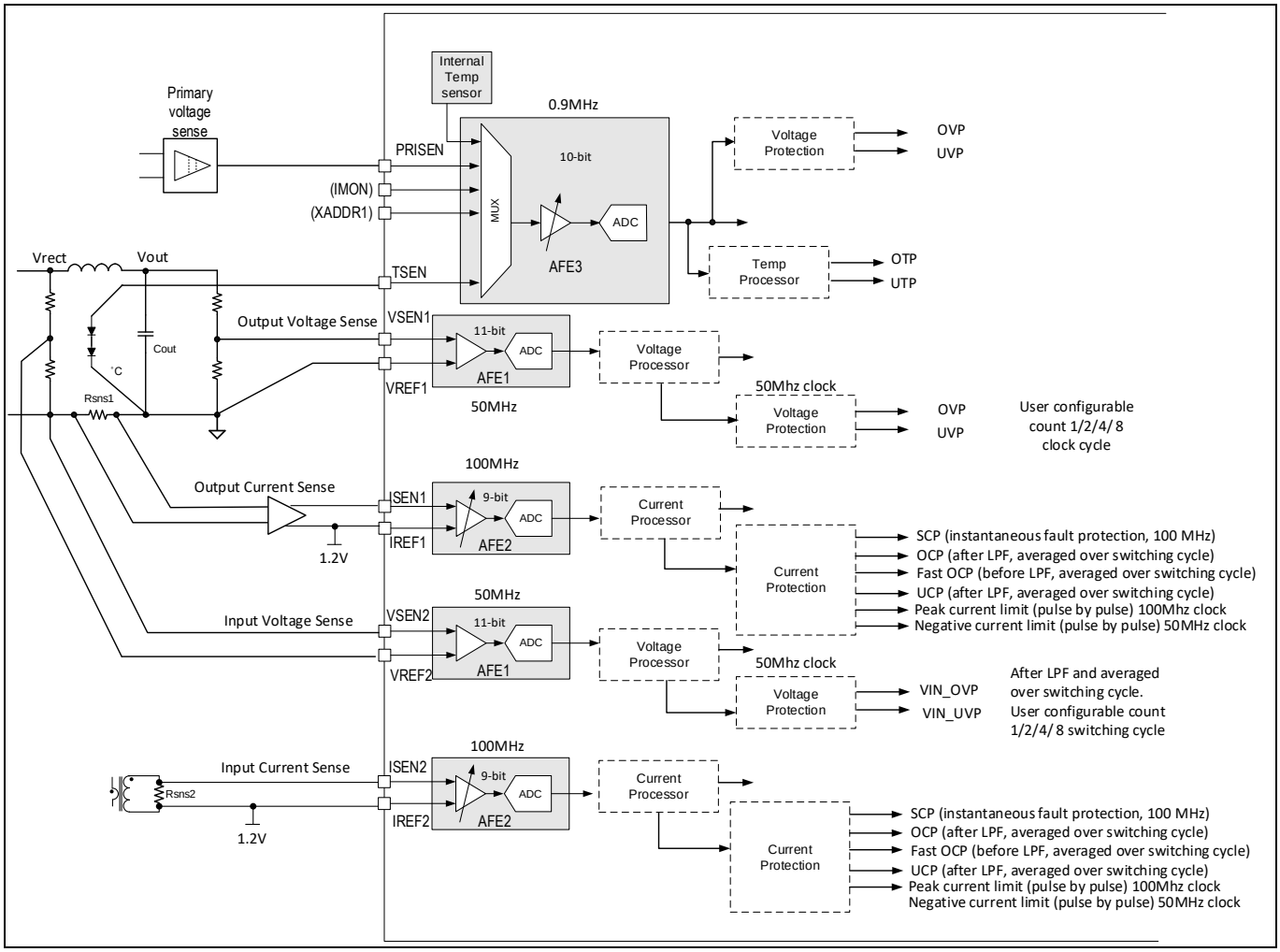


Figure 33 Protection block diagram

The list of HW fault, FW fault and common fault are shown in **Table 9**, **Table 10**, and **Table 11**. The device uses register fault_enable_mask_loop_xxx to config fault mask which allows to enable/disable an individual fault. More details of the fault protections can be found in application note.

Table 9 HW fault mask bit assignment by fault_enable_mask_loop_hw_loop0

Bit	Fault	Bit	Fault
0	Reserved	1	VOUT_OV_FAULT
2	VOUT_OV_WARN	3	VOUT_UV_FAULT
4	VOUT_UV_WARN	5	IOUT_OC_LV_FAULT
6	VIN_OV_FAULT	7	VIN_OV_WARN
8	VIN_UV_FAULT	9	VIN_UV_WARN
10	MFR_IOUT_OC_FAST	11	IOUT_OC_FAULT
12	IOUT_CONSTANT_CURRENT	13	IOUT_OC_WARN
14	IOUT_UC_FAULT	15	IIN_OC_FAULT
16	IIN_OC_WARN	17	OT_FAULT
18	OT_WARN	19	UT_FAULT
20	UT_WARN	21	Unused
22	VDD UVLO fault	23	SYSTEM_RESET_EVENT
24	EXTERNAL_FAULT	25	ISP0_SCP_FAULT
26	ISP1_SCP_FAULT	27	CURRENT_SHARE_FAULT
28	SYNC_FAULT	29	ANA_VOUT_OV_FAULT
30	VOUT_MAX_MIN_WARN	31	FW_FAULT_PIN_SET

Table 10 FW fault mask bit assignment by fault_enable_mask_loop_fw_loop0

Bit	Fault	Bit	Fault
0	RESERVED_FW_NO_FAULT	1	COMMON_FAULT
2	TON_MAX_FAULT	3	TOFF_MAX_WARN
4	VIN_INSUFFICIENT	5	PIN_OP_WARN
6	POUT_OP_WARN	7	ESTIMATED IIN OC FAULT
8	ESTIMATED IIN OC WARN	9	INVALIDATED_CORRUPTED_SNAPSHOT
10-31	Spares for user		

Table 11 Common fault mask bit assignment by fault_enable_mask_loop_common

Bit	Fault	Bit	Fault
0	unused	1	ISEN1 tracking fault
2	ISEN2 tracking fault	3	Flux balance fault
4	ISEN1 PCL fault	5	ISEN2 PCL fault
6	VSEN open fault (PID Duty detection)	7	LLC burst mode warning
8	LLC open loop warning	9	unused
10	POR VDDA fault	11-31	unused

5 Electrical characteristics

5.1 Absolute maximum ratings

Subjecting the controller to stresses above those listed in **Table 12** Absolute Maximum Rating may cause permanent damage to the device. These are absolute stress ratings only and functional operation of the device is not implied or recommended at these or any other conditions in excess of those given in the *Recommended Operating Conditions* sections of this specification. Exposure to absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 12 Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit	Note or condition
VDD Supply voltage	V_{DD}	-0.3	4	V	Instantaneous voltage, see Note
			3.7	V	Continuous voltage
VSEN1, VSEN2, VSEN		-0.3	3.7*	V	*The lesser of 3.7 V or VDD + 0.2 V
VREF1, VREF2, VREF		-0.3	0.5	V	
ISEN1, ISEN2, IREF1, IREF2, ISEN, IREF		-0.3	3.7*	V	*The lesser of 3.7 V or VDD + 0.2 V
1.2 V Supply	I_{VD12}	-1	1	mA	Do not drive or load this pin
All other pins		-0.3	3.7*	V	*The lesser of 3.7 V or VDD + 0.2 V
Operating junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-65	150	°C	

Note: The absolute maximum VDD supply voltage is 4.0 V with the conditions that the junction temperature range is maintained between -40 ˚C < T_J < +125 ˚C and the product is not operated at the absolute maximum VDD supply voltage for more than 24 hours cumulatively over the lifetime of the product.

5.2 ESD and MSL rating

Table 13 ESD and MSL ratings

ESD	Charge Device Model	Class C3 (1000V) (per JEDEC standard JS-002)
	Human Body Model	Class 2 (2000V) (per EIA/JEDEC standard EIA/ JS-001)
Moisture Sensitivity Level		MSL2 (per IPC/JEDEC J-STD-020E)

5.3 Thermal characteristics

Table 14 Thermal Impedance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Thermal resistance, junction to ambient, at 0 lfm	$R_{\theta JA}$	-	53.5	-	°C/W	QFN-24 4x4
Thermal resistance, junction to ambient, at 200 lfm	$R_{\theta JA}$	-	36.9	-		QFN-24 4x4
Thermal resistance, junction to Ambient, at 500 lfm	$R_{\theta JA}$	-	30.3	-		QFN-24 4x4

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Thermal resistance, junction to case (bottom)	$R_{\theta JCB}$	-	3.6	-		QFN-24 4x4
Thermal resistance, junction to case (top)	$R_{\theta JCT}$	-	33.1	-		QFN-24 4x4

5.4 Recommended operating conditions

The recommended operating conditions are shown for which the DC electrical characteristics are valid.

Table 15 Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Supply voltage	V_{DD}	2.97	3.3	3.63	V	
Junction temperature	T_J	-40	25	125	°C	

5.5 Electrical characteristics

VDD = 2.97 V to 3.63 V, 1 µF capacitor from VDD to GND, 1 µF capacitor from VD12 to GND, T_J = -40 °C to 125 °C unless otherwise specified.

Table 16 Electrical characteristics of power supply section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Supply current	I_{DD0}	-	8	-	mA	In off mode with telemetry disabled
Supply current	I_{DD1}	-	21	–		4 PWMs switching at 250 kHz without any load
VDD UVLO threshold	$V_{DD\ rising}$	-	2.78	2.95	V	
	$V_{DD\ falling}$	2.5	2.7	-		
VDD UVLO hysteresis	$V_{DD\ hyst}$	-	80	-	mV	
Sleep mode current	$I_{DDsleep}$	-	1	-	mA	Not regulating, clocks stopped, peripherals disabled, responsive to sleep pin. Note **6**
Sleep mode wakeup time	t_{wakeup}	-	150	-	µs	The wakeup event is toggling sleep pin. Wakeup time is measured from the wakeup event to the first instruction executed by the CPU. Note **6**

Table 17 Voltage ADC AFE1 section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Input differential voltage range	VSENx-VREFx	0.25	-	2.1	V	Note **6**
Error voltage digital resolution	V_{RSL1}	-	1.25	-	mV	Note **6**
Input impedance	R_{EA1}	-	> 1	-	MΩ	Note **6**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Sample rate	f_{ADC1}	-	100	-	MHz	
VS ADC accuracy	A_{AD1_1}	-1	-	1	%	Setpoint 1.6 V to 2.1 V, -40 °C <T_A < 125 °C, 2.97 V < V_{DD} < 3.63 V, Note 5
	A_{AD1_2}	-1	-	1	%	Setpoint 1.2 V -40 °C <T_A < 125 °C, 2.97 V < V_{DD} < 3.63 V
	A_{AD1_3}	-1.5	-	1.5	%	Setpoint 0.8 V, -40 °C <T_A < 125 °C, 2.97 V < V_{DD} < 3.63 V
	A_{AD1_7}	-2.3	-	2.3	%	Setpoint 0.5 V, -40 °C <T_A < 125 °C, 2.97 V < V_{DD} < 3.63 V
	A_{AD1_4}	-	±0.45	-	%	Setpoint 1.6 V to 2.1 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ, Note 5
	A_{AD1_5}	-	±0.45	-	%	Setpoint 1.2 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ
	A_{AD1_6}	-	±0.8	-	%	Setpoint 0.8 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ
	A_{AD1_8}	-	±1.15	-	%	Setpoint 0.5 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ

Table 18 Current ADC AFE2 section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or conditions
Input differential voltage range	ISENx-IREFx	-256		256	mV	
Input common voltage range	V_{COM}	1.0	1.2	1.32	V	Note 6
Error voltage digital resolution	V_{RSL2}	-	1	-	mV	Note 6
Input impedance	R_{EA2}	-	> 1	-	MΩ	Note 6
IS ADC offset	$V_{OFFSET2}$	-2.5	-	2.5	LSB	
Sample rate	f_{ADC2}	-	100	-	MHz	
Tracking slew rate	TSR	-	-	1.6	mV/ns	Note 6
IS ADC accuracy	A_{AD2_1}	-	±4	-	%	±100 mV differential input, Typ = 3 σ
	A_{AD2_2}	-	±2.2	-	%	±256 mV differential input, Typ = 3 σ

Table 19 General ADC AFE3 section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Input differential voltage range	V_{ADC3}	-	0 – 2.4	-	V	Note 6
Error voltage digital resolution	V_{RSL3}	-	2.344	-	mV	Note 6
Input impedance	R_{EA3}	-	> 1	-	MΩ	Note 6

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
TS ADC offset error	$V_{OFFSET3}$	-2	-	2	LSB	
Sample rate	f_{ADC3}	-	0.926	-	MHz	
TS ADC Gain error	A_{AD3_1}	-1	-	1	%	

Table 20 IMON DAC section

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Output current range	I_{DAC}	-	0-640	-	µA	Note **6**
Output current resolution	I_{DAC_RSL}	-	10	-	µA	Note **6**
TSIDAC accuracy	A_{DAC}	-3	-	3	%	Tested at 100 µA

Table 21 XADDR1 pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Current measurement	I_{XADDR}	-	0-640	-	µA	Note **6**

Table 22 GPIO Inputs/Outputs (IMON, EN)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Low-level output voltage	V_{OL}	-	-	0.4	V	I_{OL} = 5 mA
High-level output voltage	V_{OH}	2.6	-	-		I_{OH} = -5 mA
Low-level input voltage	V_{IL}	-	-	1.0		Note **7**
High-level input voltage	V_{IH}	2.1	-	-		Note **7**
Leakage current	I_{OZ}	-1	-	1	µA	

Table 23 GPIO Inputs/Outputs (PWM1-6, PWRGD, SYNC)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Low-level output voltage	V_{OL}	-	-	0.4	V	I_{OL} = 5 mA
High-level output voltage	V_{OH}	2.6	-	-		I_{OH} = -5 mA
Low-level input voltage	V_{IL}		-	0.3 VDD		
High-level input voltage	V_{IH}	0.7 VDD	-	-		
Leakage current	I_{OZ}	-1	-	1	µA	

Table 24 SDA, SCL, SMBALERT pins

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 20 mA
Low-level input voltage	V_{IL}	-	-	1.0		
High-level input voltage	V_{IH}	2.1	-	-		Configured as 3.3 V buffer
Low-level input voltage	V_{IL}	-	-	0.6		
High-level input voltage	V_{IH}	1.35	-	-		Configured as 1.8 V buffer
Leakage current	I_{OZ}	-1	-	1	µA	
Pin capacitance	C_{PIN}	-	1.5	-	pF	Note **6**

Table 25 System performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Processor master clock	f_{CLK}	-	100	-	MHz	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Internal oscillator frequency	f_{OSC}	195	200	205	MHz	T_A = 25 °C
		190	200	210	MHz	-40 °C <T_A < 125 °C
Switching frequency	f_{SW}	-	50 - 2000	-	kHz	Note 6
Switching period programming resolution	t_{RSL1}	-	5	-	ns	Note 6
Switching period regulation resolution	t_{RSL2}	-	2.5	-	ns	Note 6
Sync frequency range		-	+/- 12.5	-	%	With respect to switching period. Note 6

Table 26 Temperature sensor

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Input voltage range	V_{TSEN}	-	0 – 2.4	-	V	Note 6
Bias current	I_{TSEN}	-	100	-	µA	Source current to measure external V_{BE}, NTC or PTC resistor, can be disabled
Accuracy of internal temperature sensor	e_{TEMP}	-	±5	-	˚C	Note 6

Table 27 Fast GPIO

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
Fast GPI response time	t_{FSD1}	-	50	-	ns	From fast GPI input falling/rising edge to PWM i/o change (synchronization), with zero programmed deadtime. Note 6
Fast GPI response time	t_{FSD2}	-	150	-	ns	From fast GPI input rising edge to PWM falling edge (PWM going to inactive /shutdown) with zero programmed deadtime. Note 6
Minimum input pulse width	t_{FPW}	25	-	-	ns	Note 6
Fast fault output response time	t_{FSF}	-	50	-	ns	From fault triggering to rising edge of Fault pin, Note 6

Note:

5. *Production test limits verified at 0.5V, 0.8V, 1.2V, 1.6V. Full range not subject to production test.*
6. *Not subject to production test - verified by design and/or characterization*

7. *The enable signal cannot linger between the V_{IL} and V_{IH} thresholds. The EN pin is intended to operate as a switch with the pin voltage either above or below the thresholds.*

6 Package information

6.1 QFN 4x4 – 24pin

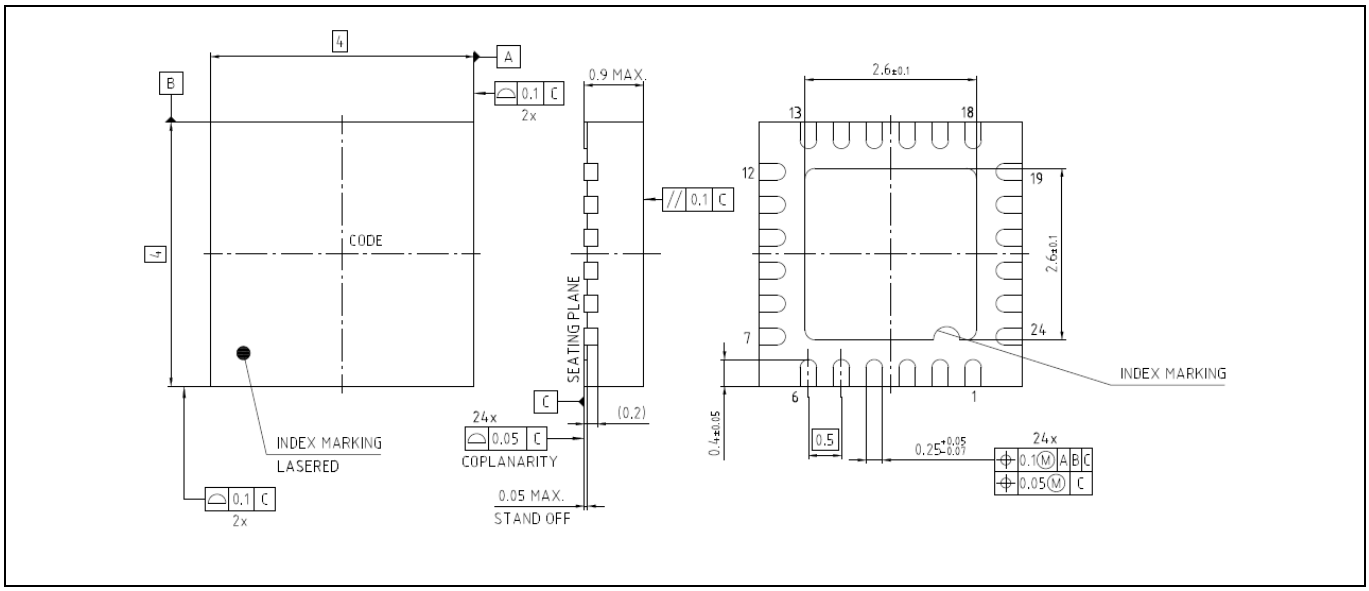


Figure 34 PG-VQFN-24-20

Green Product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pbfree finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

6.2 Part marking

The part marking shows in Figure 35.

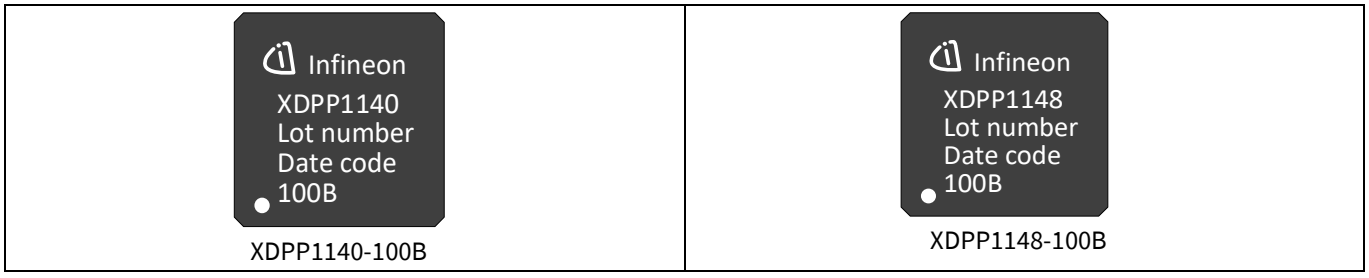


Figure 35 Package Marking

Examples of Lot number and Date code:

Lot number: 1YUS1ANNB03

Date code: H2018B03

The B03 at the end of date code is the last 3 digits of the lot number.

7 Nomenclature

Table 28 Definitions of acronyms, symbols and terms

Acronym, symbol, or term	Definition
ACF	Active Clamp Forward
ADC	Analog-to-Digital Converter
AFE	Analog Front End
DAC	Digital-to-Analog Converter
DCM	Discontinuous Conduction Mode
DCR	DC resistance
DE	Diode Emulation
FB	Full-Bridge
FTR	Fast Transient Response
F_{RES}	LLC resonant frequency
F_{SW}	Switching frequency of converter
FW	Firmware
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HB	Half-Bridge
HiZ	High impedance
HW	Hardware
LLC	A resonant topology made up of two inductors (LL) and one capacitor (C)
LSB	Least Significant Bit
N_p	Number of turns of the transformer primary winding
N_s	Number of turns of the transformer secondary winding
NTC	Negative Temperature Coefficient
OCP	Over-Current Protection
OTP	One-Time Programmable memory
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
OVS_FTR	Over-Shoot Fast Transient Response
PCB	Printed Circuit Board
PCL	Peak Current Limit
PCMC	Peak Current Mode Control
PFM	Pulse Frequency Modulation
PID	Proportional, Integral, Derivative coefficient
PI filter	Proportional Integral filter
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation

Nomenclature

Acronym, symbol, or term	Definition
SCP	Short-Circuit Protection
SR	Synchronous Rectification
T_{SW}	Switching period of converter
UCP	Under-Current Protection
UTP	Under-Temperature Protection
UVP	Under-Voltage Protection
V_{IN}	Input voltage
VMC	Voltage Mode Control
V_{DS}	MOSFET Drain to Source Voltage
V_{OUT}	Output voltage
V_{RECT}	Transformer secondary rectified voltage

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