XDPS2221 PFC + Hybrid-Flyback - Combo Controller

Datasheet

Product Highlights

- Digital combo controller for PFC-boost and dc-dc hybrid-flyback in DSO-14 (150mil) package
- Novel ZVS hybrid-flyback (asymmetrical half-bridge) topology for ultra-high system efficiency
- Integrated gate drivers supporting GaN and Si switches
- 600V high voltage start-up cell for fast VCC charging
- Burst mode operation control for lowest no-load stand-by power
- Adaptive PFC bus voltage and PFC enable/disable control to maximize average and light load efficiency
- Configurable parameters for protection modes and system performance
- Pb-free lead plating, halogen-free (according to IEC61249-2-21), RoHS compliant

PFC control

- Configurable PFC QRM operation for improved average efficiency
- Pulse skipping for improved light load efficiency
- Automatic PFC disable/enable-control depending on operating conditions
- Adaptive PFC bus voltage level following operating conditions

Hybrid-flyback control

- Peak current mode control for robust and fast input and load control
- ZVS operation of high-side and low-side switch (with ZVS pulse insertion in DCM)
- Configurable multimode operation for improved average and light load efficiency

Description

The XDPS2221 PWM controller is a highly integrated device combining a multimode ac-dc PFC controller and a multimode dc-dc hybrid-flyback controller. The integration of PFC and hybrid-flyback into a single package enables the reduction of external bill of material components and optimizes the system performance by harmonized operation of the two stages.

Ordering Information

Product Name	Marking	Ordering Code	Firmware Version	Package
XDPS2221	XDPS2221	SP005630569	3.1.4	PG-DSO-14

Potential Applications

Ultra high power density chargers / adapters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

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1 Pin Configuration and Functionality

The pin configuration is shown in the figure below and the functions are described in the following table.

Table 1 Pin Definitions and Functions

Symbol	Pin	Type	Function
PFCGD	1	O	**PFC gate driver** This pin drives the PFC transistor via a gate resistor.
CS	2	I	**Hybrid-flyback current sense** Input pin for current sensing during the hybrid-flyback high-side gate driver turn-on phase.
VCC	3	I	**Power supply** This pin supplies the IC. During start-up VCC is supplied from the AC via the HV-pin, while during normal operation VCC is supplied from the auxiliary winding to the hybrid-flyback stage.
GND	4	O	Ground level of the IC for supply voltage, gate drive and sense signals.
ZCD	5	I	**Hybrid-flyback zero crossing detection** This pin provides zero crossing detection after low-side gate driver turned off and during pause phase in burst mode. Furthermore, the reflected output voltage at the auxiliary winding can be measured during low-side gate driver turn-on phase.
PFCVS	6	I	**PFC bus voltage sense** This pin is connected to a high impedance resistor divider from the PFC controller output for bus voltage sensing.
HV	7	I	**High voltage input** The HV pin is connected to the input AC voltage. An internal HV startup-cell is used for initial VCC charging and AC brown-in detection.
MFIO	8	I	**Multi-functional Input Output** This pin is connected to GND through an external NTC resistor used to detect ambient temperature. Furthermore, UART communication for parameter configuration and error code reporting is provided by this pin.
FB	9	I	**Feedback** This pin receives feedback from the secondary side via an optocoupler.
PFCCS	10	I	**PFC current sense and PFC zero crossing detection** This pin is configured for PFC current sensing in combination with zero crossing detection of the PFC choke current.
LSGD	11	O	**Hybrid-flyback low-side gate driver** This pin drives the low-side transistor of the hybrid-flyback half-bridge.
HSGND	12	I	**High-side Ground** Ground reference node for hybrid-flyback floating high-side driver domain.
HSVCC	13	I	**High-side power supply** Power supply input for hybrid-flyback floating high-side driver domain.

(table continues...)

1 Pin Configuration and Functionality

Table 1 (continued) Pin Definitions and Functions

Symbol	Pin	Type	Function
HSGD	14	O	**High-side gate driver** This pin drives the high-side transistor of the hybrid-flyback half-bridge from the floating driver domain.

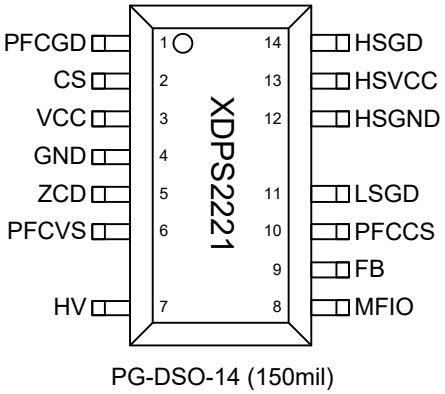

Figure 1 Pin configuration

2 Representative Block Diagram

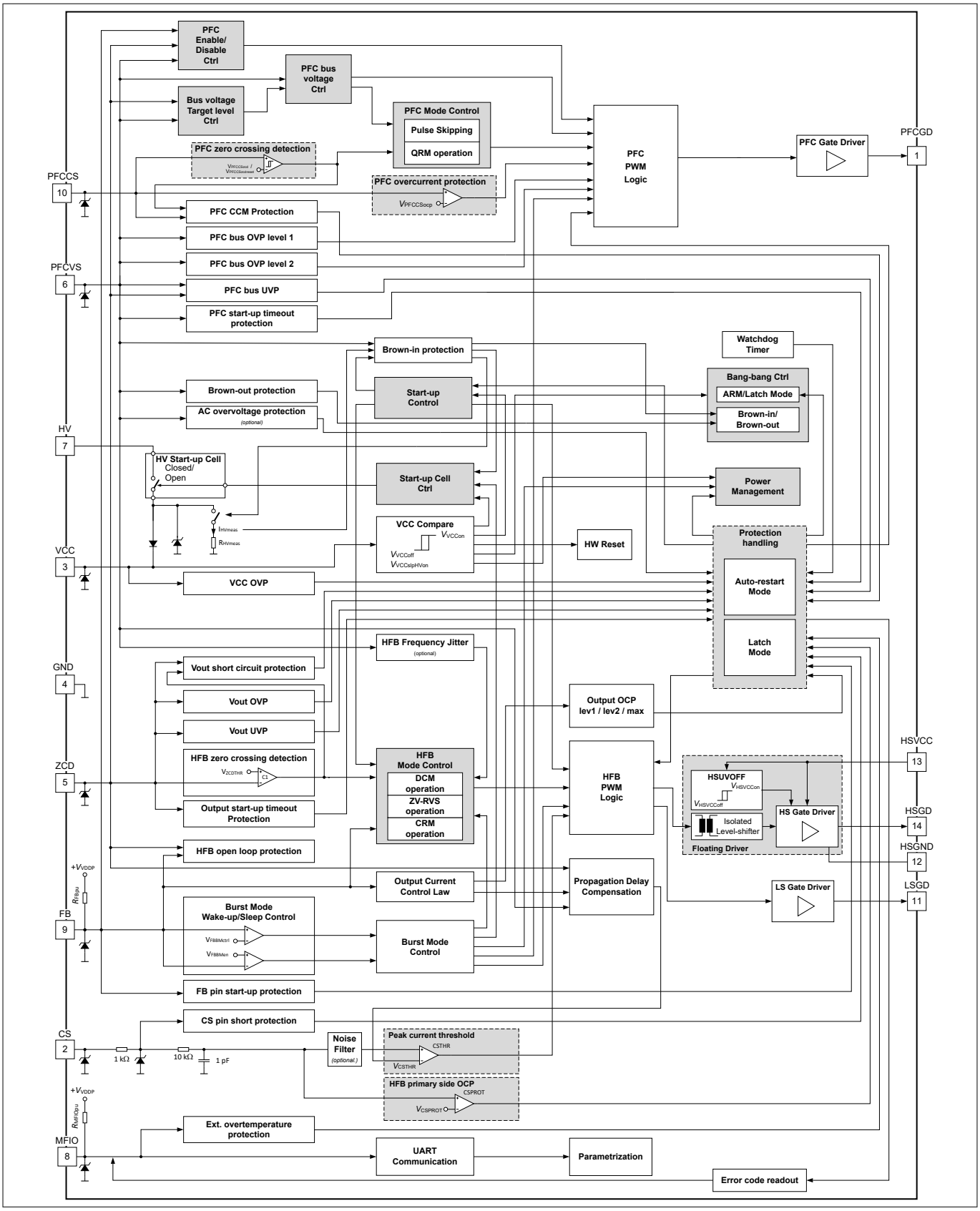

Figure 2 Block diagram

3 Introduction

The XDPS2221 PWM controller is a highly integrated device combining a multimode ac-dc PFC controller and a multimode dc-dc hybrid-flyback controller. The integration of PFC and hybrid-flyback into a single controller enables reduction of external parts and optimizes performance by joint operation of the two stages. It is meant to be used in USB-PD chargers / adapters with wide output voltage up to 28 V.

The system efficiency can further be increased using Infineon CoolMOS™, CoolGaN™ and OptiMOS™ transistors. Below a typical application schematics in a USB-PD application are depicted.

Figure 3 shows the potential application schematic using CoolGaN™ and OptiMOS™ transistors for highest efficiency and power density.

Figure 4 shows the potential application schematic using CoolMOS™ and OptiMOS™ transistors.

3 Introduction

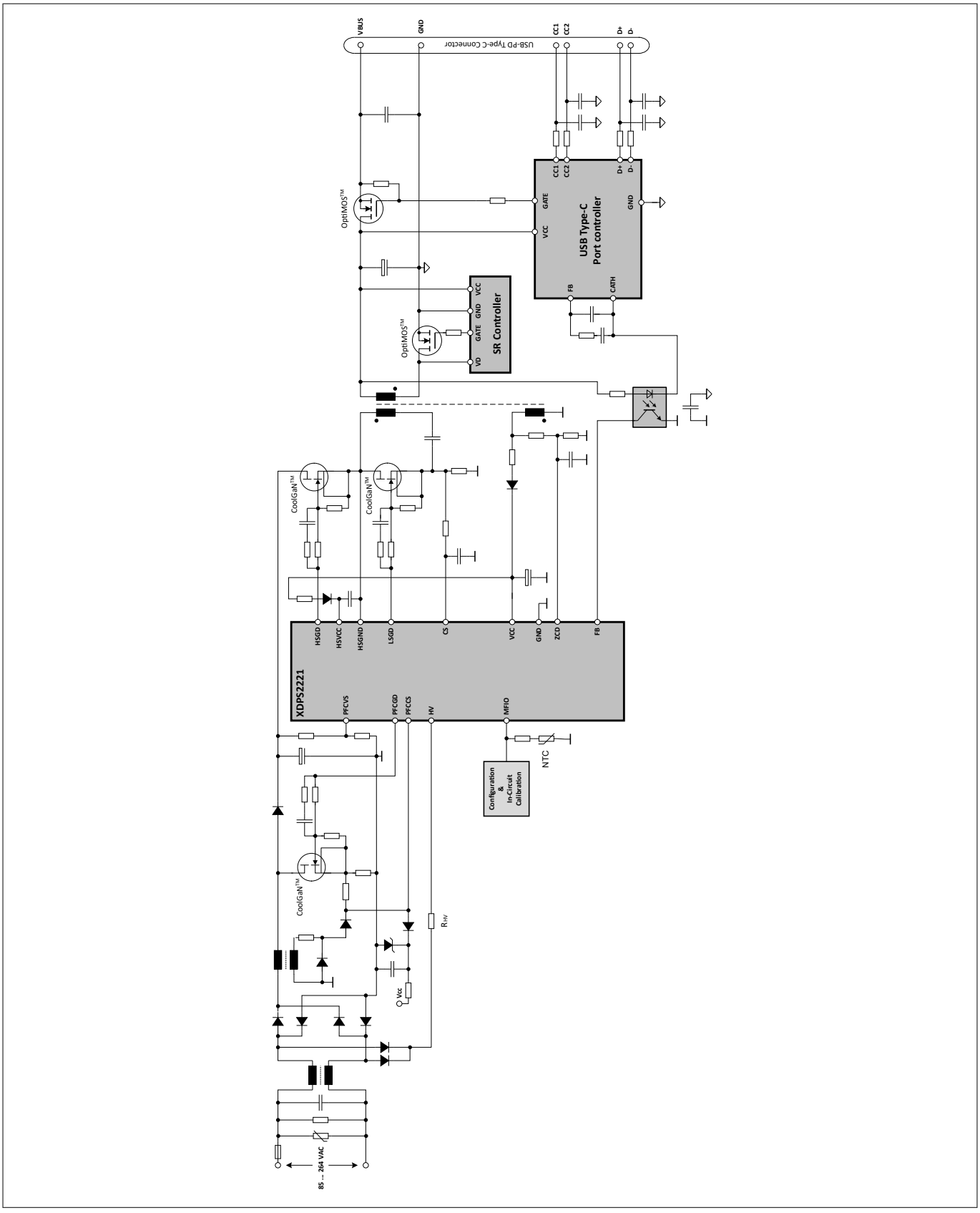

Figure 3 Typical application in combination with CoolGaN™ transistors

3 Introduction

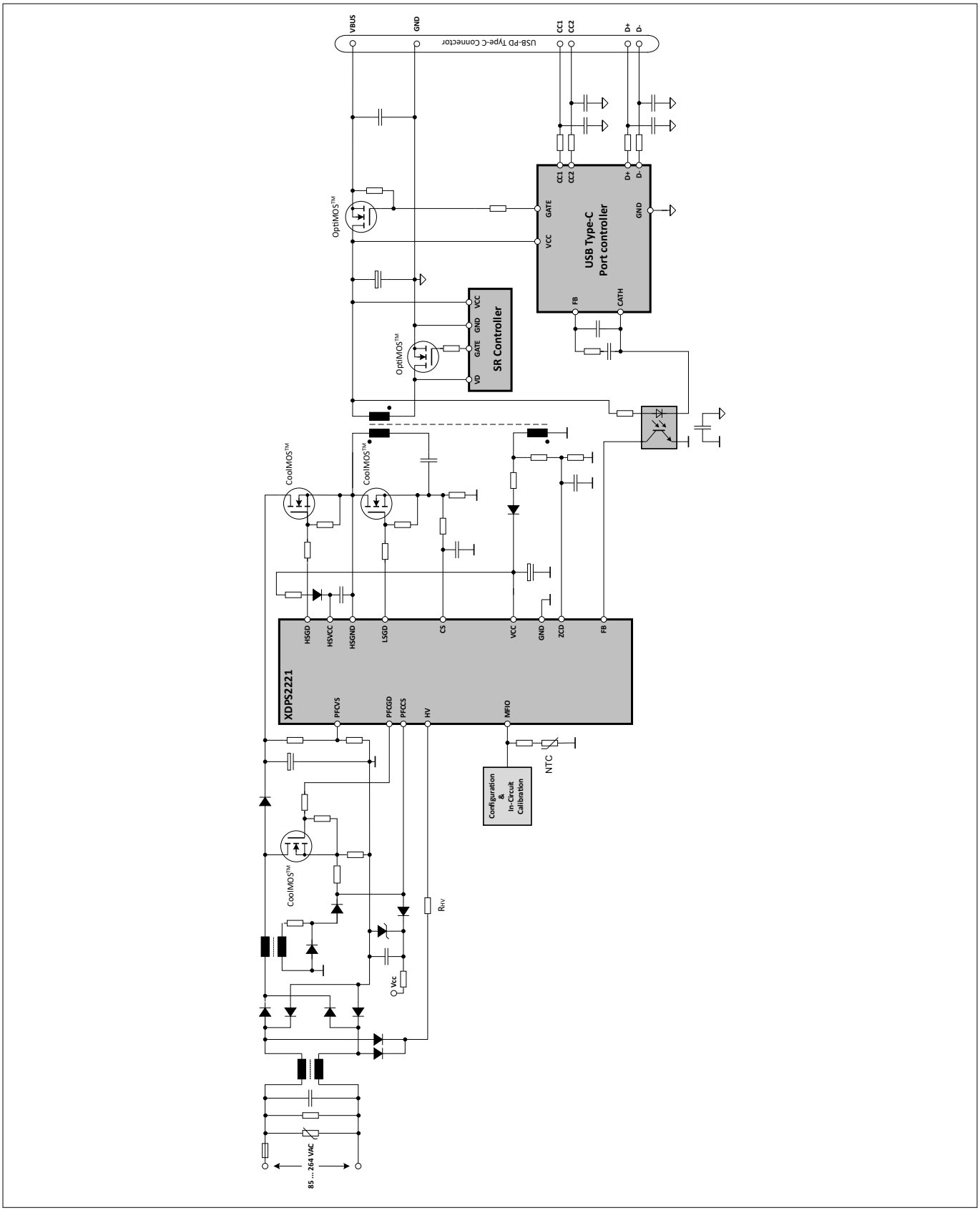

Figure 4 Typical application in combination with CoolMOS™ transistors

4 Functional description

4.1 Power-supply and high voltage start-up cell management

The power supply management ensures a reliable and robust IC operation. Depending on the operation mode of the control IC, the power supply management unit runs in different ways for VCC supply, which are described as in the sequel.

4.1.1 VCC capacitor charge-up and start-up sequence

At VCC start-up the capacitor C_{VCC} is charged by the internal HV start-up cell via HV pin (see Figure 5). The internal HV start-up cell is turned on for V_{VCC} lower than the IC deactivation voltage threshold V_{VCCoff}. Once the voltage at pin VCC exceeds the threshold V_{VCCon} at time t0 the HV start-up cell is turned off and the IC is starting up (see Figure 6).

The IC operation is started at time t1 and the start-up conditions are validated afterwards.

Following conditions need to be fulfilled to start the hybrid-flyback operation at time t2 (hybrid-flyback switching is indicated by signal V_{HBGD}):

1. Two-level brown-in condition with $V_{in} > V_{inbi}$ and $V_{bus} > V_{busbi}$ (see Chapter 4.5.2.4))
2. No input overvoltage with $V_{bus} < V_{busACovp}$ (see Chapter 4.5.2.8)
3. Feedback signal out of regulation range with $V_{FB} > V_{FBBMctrl}$
4. No overtemperature condition with $R_{MFIO} > R_{MFIOOTPrel}$. (see Chapter 4.5.2.17)

The conditions need to be met within the time period t_{HVbito}. With hybrid-flyback switching, the the external VCC self-supply takes over the IC supply. In case one of those conditions is not met the IC enters bang-bang during brown-in phase (see Chapter 4.1.2).

Note: In the typical application the output voltage target value is set by the USB-PD controller. At start-up, no load is applied and the target value is first set by the USB-PD controller to e.g. $V_{out,set1} = 5$ V and only after having reached a stable output voltage condition the USB-PD controller activates the load and sets the proper output voltage required by the attached device.

PFC operation depends on operating conditions and might not be required at start-up. Hybrid-flyback operation starts first, if required, PFC operation comes up afterwards. Figure 6 shows a situation with an output voltage request from USB-PD controller with $V_{out,set2} > V_{out,set1}$ after a while. In this case PFC operation is started at t_4.

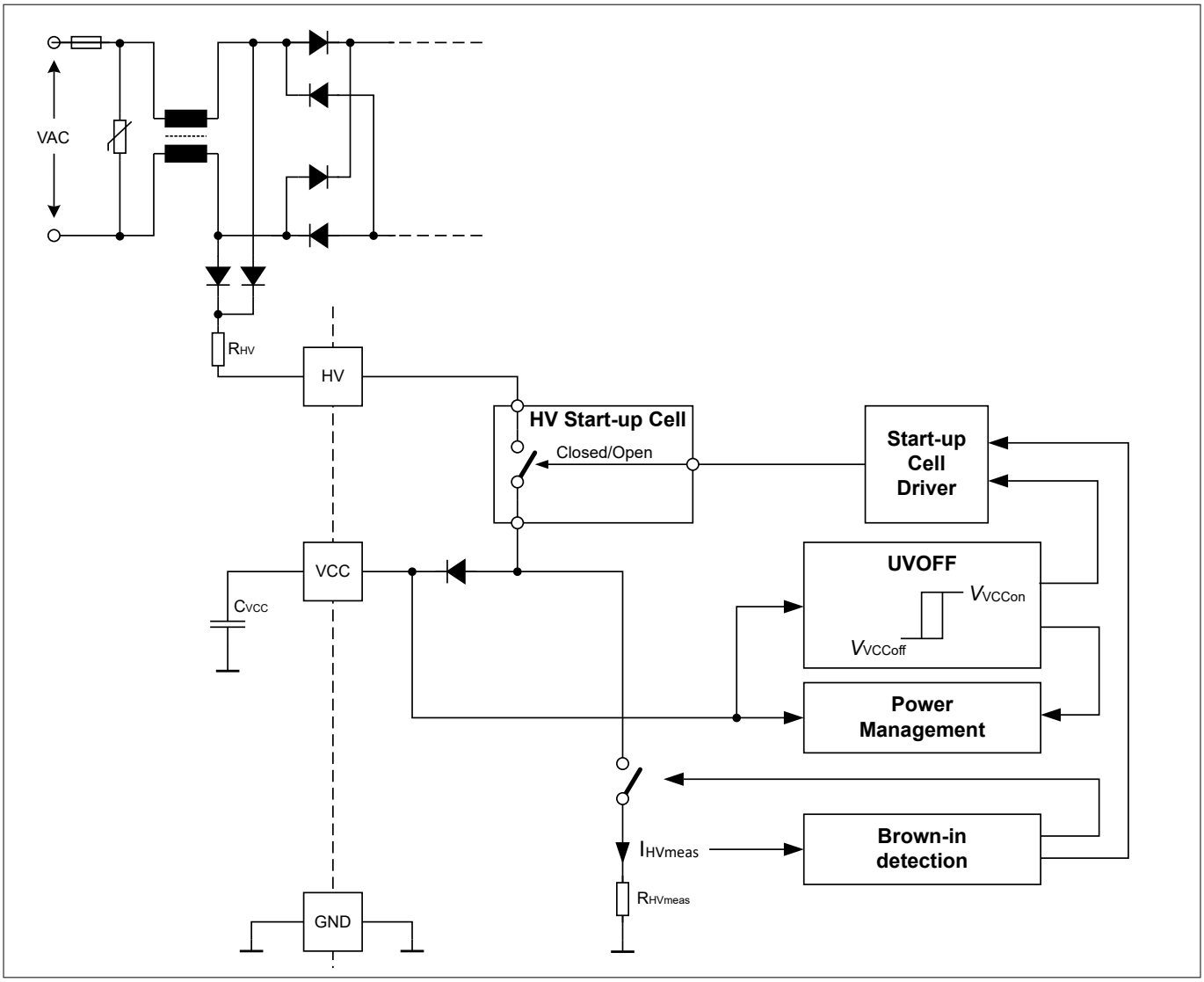

Figure 5 **HV control for start-up and brown-in detection**

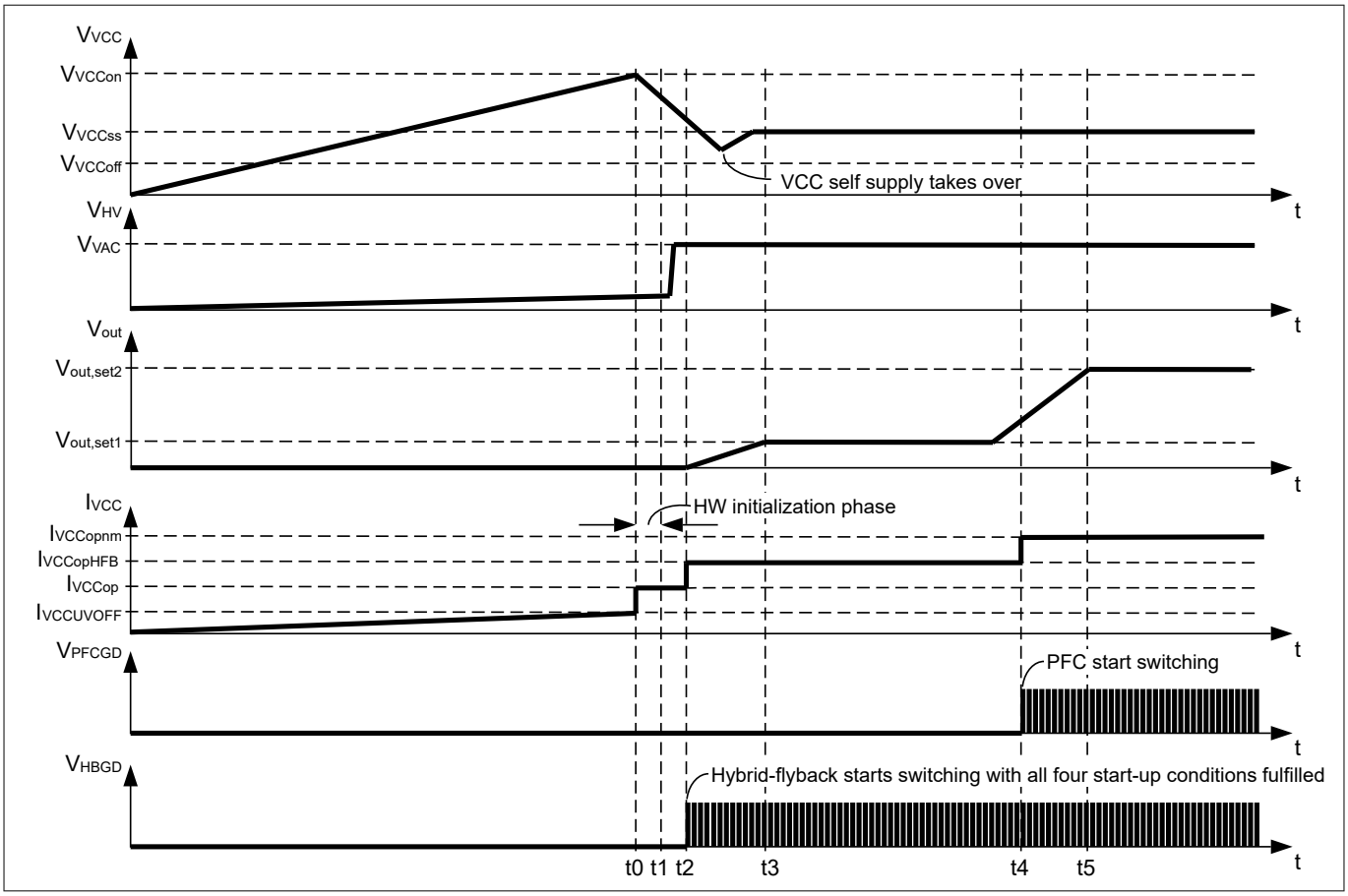

Figure 6 Typical start-up sequence

4.1.2 Bang-bang mode operation during brown-in phase

In order to support a fast activation as soon as brown-in condition is fulfilled, the VCC voltage is kept at a high level. A bang-bang mode operation for the start-up check phase is ensuring a high VCC level.

For example, after a brown-out event the IC enters a sleep mode with reduced current consumption I_{VCCBB}. The HV start-up cell turns on and tries to charge up the VCC voltage to the threshold V_{VCCon}. When AC input voltage comes back V_{VCC} can reach V_{VCCon} and the IC gets active for brown-in detection for a short time. If AC input voltage is high enough the IC detects the brown-in condition.

4.1.3 Bang-bang mode during protection mode operation

In auto-restart operation, the the HV start-up cell is regularly turned on after a time period $t_{ARMbase}$ and turned off when reaching VCC pin voltage threshold V_{VCCon}. During this bang-bang mode operation the VCC is kept at a high voltage level in order to support a proper restart operation (see Figure 7). A system restart happens after the auto-restart time t_{arm} is expired.

In latch mode operation, the HV start-up cell is turned on at VCC pin voltage threshold $V_{VCCslpHVon}$ and turned off when reaching VCC pin voltage threshold V_{VCCon} (see Figure 8). A reset can only be achieved by disconnecting the AC line once the VCC voltage drops below the threshold V_{VCCoff}.

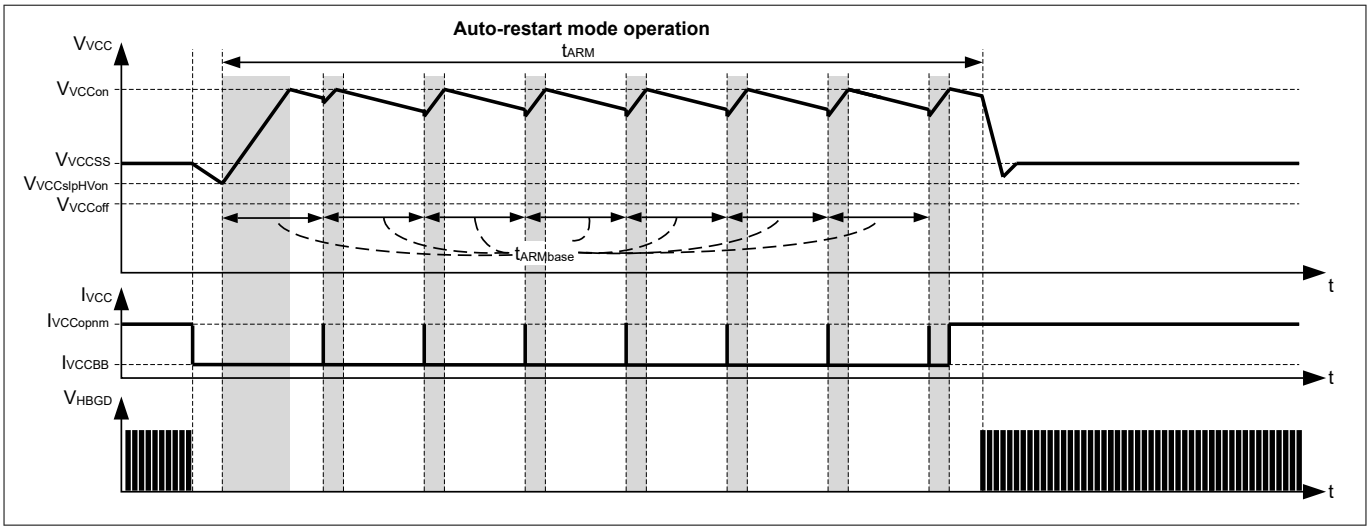

Figure 7 Auto-restart mode operation

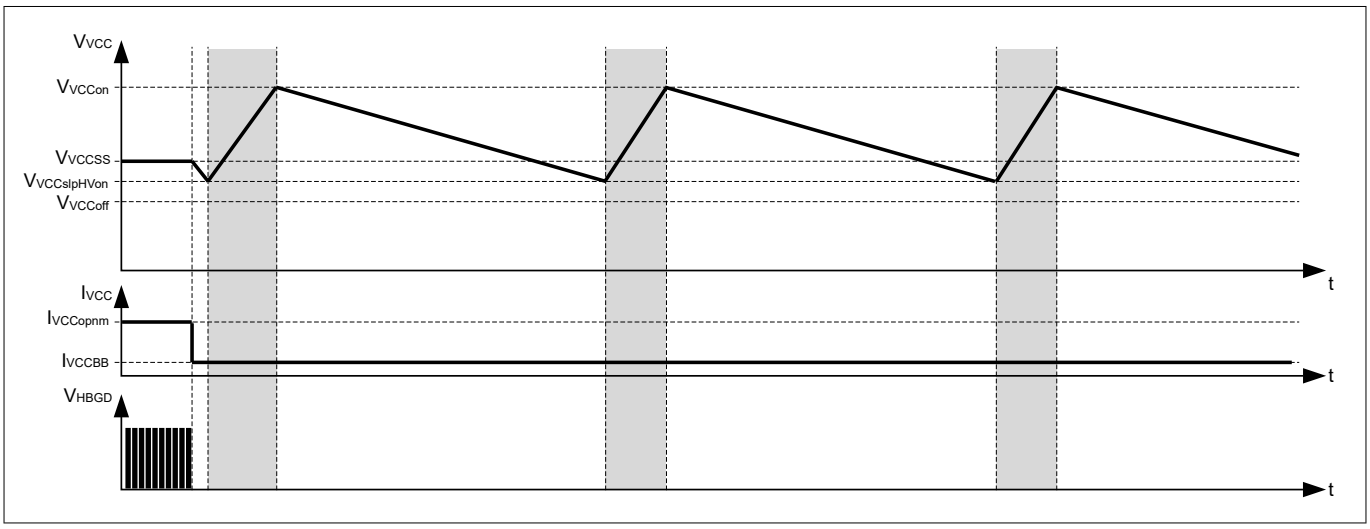

Figure 8 Latch mode operation

4.1.4 VCC supply during burst mode (BM) operation

During burst mode operation the IC enters repeatedly a power saving mode, in which the IC current consumption is reduced to $I_{VCCBMpsm}$. During the burst active time, VCC should be supplied externally from the auxiliary winding.

In burst-mode the controller can also be configured to use the HV start-up cell to support VCC supply. When enabled and the VCC voltage drops below the threshold $V_{VCCslpHVon}$, the HV start-up cell is activated and charges the VCC capacitor.

4.2 PFC control

The PFC controller turns on and off the PFC gate driver PFCGD so that a desired bus voltage V_{bus} is maintained while the AC input current I_{AC} follows the instantaneous line input voltage V_{AC} resulting in high power factor and low harmonic content. The operation mode is based on quasi-resonant operation mode (QRM), thus critical conduction mode, but with valley switching and valley skipping. The oscillation of the switch voltage $V_{PFC,ds}$ after choke current demagnetization is detected via an integrated zero crossing detection (ZCD) mechanism. The ZCD-function is combined with a PFC overcurrent protection at pin PFCCS. Figure 9 shows the PFC circuit arrangement including the AC input stage and the PFC control part of the IC.

4 Functional description

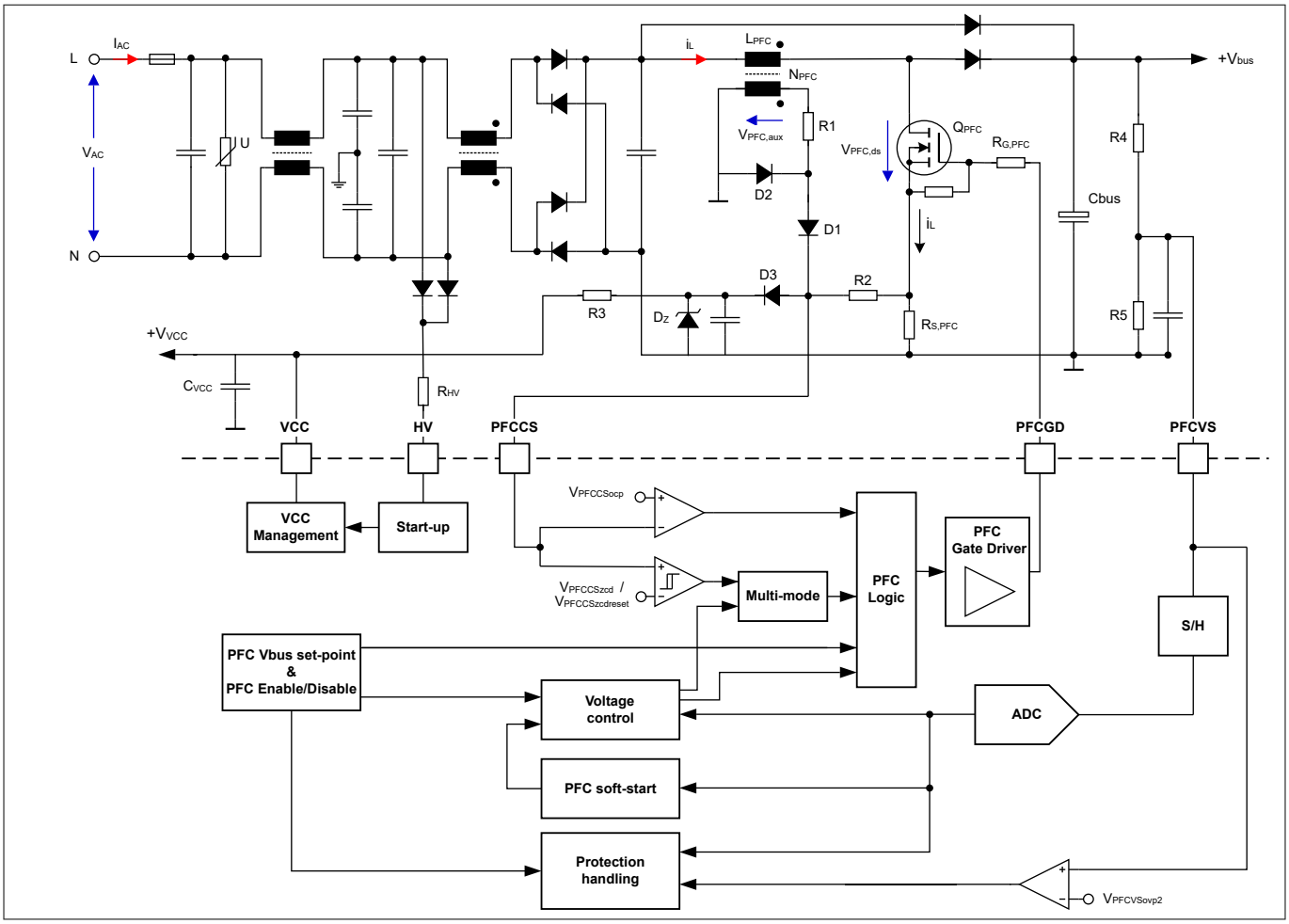

Figure 9 QRM-PFC circuit arrangement and associated PFC control

The PFC controller is operating in quasi-resonant mode (QRM) with valley switching. Typical waveforms are depicted in Figure 10. In the shown case, the PFC is turned on in the third valley.

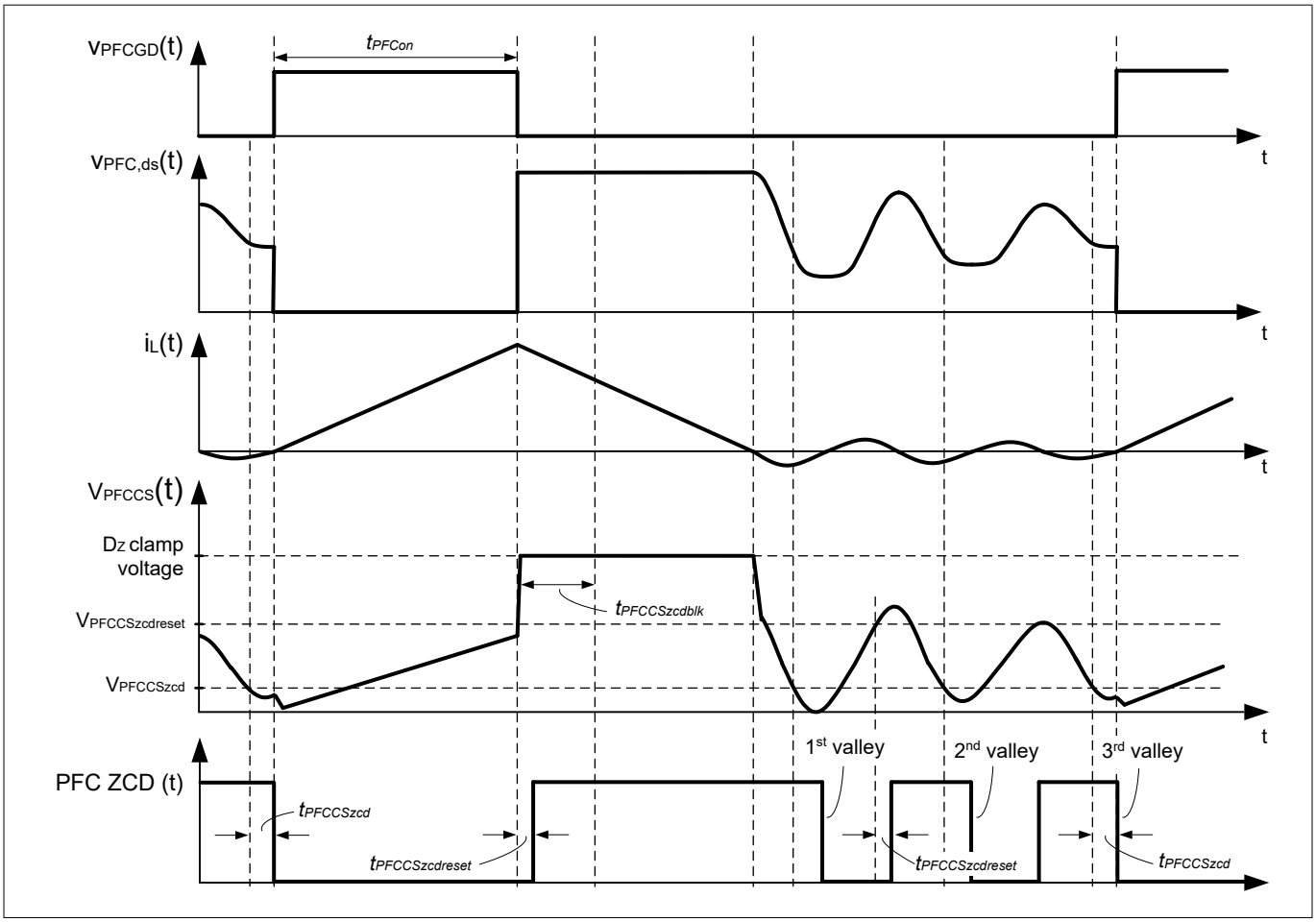

Figure 10 PFC switching cycle with transistor turn-on in the 3rd valley (QRM3)

4.2.1 Combined current sense (CS) and zero crossing detection (ZCD) function

The PFC stage uses a combined current sense (CS) and zero crossing detection (ZCD) functionality at pin PFCCS. During the PFC gate driver on-time the pin acts as a current sense (CS), while during the gate driver off-time the pin acts as a zero-crossing-detector (ZCD) for valley switching. Please refer to Figure 9 for the related circuitry for ZCD and CS.

Valley detection is done through an external circuit connected to the auxiliary winding of the PFC inductor. A hysteretic comparator with a lower threshold of $V_{PFCCSzcd}$ for falling edges and an upper threshold $V_{PFCCSzcdreset}$ for rising edges of the signal at PFCCS is used. A ZCD event is triggered in case V_{PFCCS} falls below the threshold $V_{PFCCSzcd}$. In case the target valley is reached, the gate driver output PFCGD only goes high after the delay time $t_{PFCCSzcd}$. However, a (new) ZCD event can only be detected after the voltage at PFCCS was above the upper comparator threshold $V_{PFCCSzcdreset}$ for longer than the configurable filter and delay time $t_{PFCCSzcdreset}$. For ringing suppression due to switching, the ZCD signal is blanked for $t_{PFCCSzcdblk}$ after PFGGD falling edge. The signal showing the hysteretic comparator output in Figure 10 illustrates this mechanism.

The measured voltage at the shunt resistor $R_{S,PFC}$ during the PFC gate driver on-time is used for PFC overcurrent limitation. Once the voltage at pin PFCCS exceeds the overcurrent threshold $V_{PFCCSocp}$ for longer than the blanking time $t_{PFCCSocp}$ the PFC gate PFCGD is turned off.

4.2.2 Multimode operation and frequency law

The PFC controller provides various modes of operation. When going from full to no load several operation modes are used in order to optimize efficiency and EMI behavior.

A PFC converter is used to emulate a resistive load $R_e = V_{AC,rms} / I_{AC,rms}$ to the AC input. The output of the PFC bus voltage controller $t_{PFCon,des}$ is inversely proportional to the emulated resistive load R_e. Thus, $t_{PFCon,des}$ varies as the AC line voltage magnitude varies and is proportional to the RMS input current $I_{AC,rms}$.

The frequency law depicted in Figure 11 indicates the operation mode for the complete range, which can be $t_{PFCon,des}$ or $I_{ac,rms}$ range. A limitation within a minimum switching frequency $f_{swPFCmin}$ and a maximum switching frequency $f_{swPFCmax}$ is applied in every switching cycle. In QRM exceeding the thresholds $f_{swQRmax}$ and $f_{swQRmin}$ for longer than the given blanking time lead to a change of valley to bring the switching frequency back into the range from $f_{swQRmin}$ and $f_{swQRmax}$ (see Chapter 4.2.2.1).

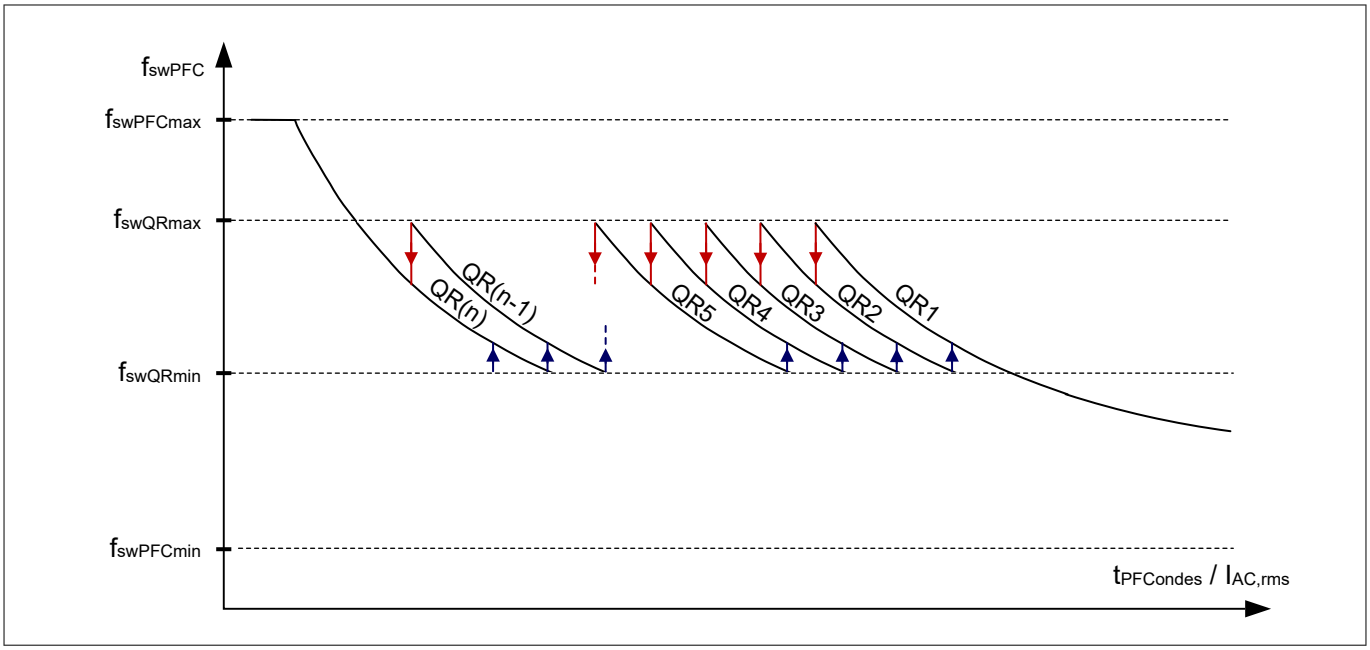

Figure 11 Frequency law

4.2.2.1 Quasi-resonant mode (QRM)

In quasi-resonant operation mode (QRM) the PFC switch is turned on in the valley of the oscillation seen at the switch's drain-source voltage after demagnetization. QRM reduces PFC transistor switching losses and ensures highest possible efficiency of the system.

In QR1 operation the first valley is used. The transistor is turned on as soon as the first ZCD event is detected.

With decreasing load or increasing input voltage switching frequency is increasing and the maximum switching frequency $f_{swQRmax}$ is hit. In this case the valley number should be increased. With load getting higher or input voltage decreasing, the lower frequency limit $f_{swQRmin}$ will be hit and the valley number should be decreased.

However, in order to prevent valley number change within each AC half cycle, valley change blanking times $t_{QRblkinc}$ and $t_{QRblkdec}$ apply.

In order to ensure good ZCD detection before the PFCCS signal gets too small in amplitude, only 1st valley (QR1) to a configurable n^{th} valley $N_{PFCvalleymax}$ are supported. In case $N_{PFCvalleymax}$ is reached the frequency is only limited by $f_{swPFCmax}$.

The time during QR valley oscillation, when neither PFC switch nor PFC diode is conducting, is responsible for some AC input current waveform distortion and affects the PFC THD performance. The multimode PFC controller uses an algorithm that optimizes the applied on-time on a cycle by cycle basis so as to ensure good input current shaping and improve PFC THD performance.

4.2.2.2 Low power mode

In softstart and steady operation, as soon as the on-time $t_{PFCondes}$ determined by the bus voltage controller is less than a value $t_{PFConskip}$ the switching pulse is skipped and PFC gate driver is not switching. Depending on the configuration of parameter $CFG_{PFContime}$, the value of $t_{PFConskip}$ is equal to a constant on-time $t_{PFConmin}$, with $t_{PFConmin} \geq t_{PFCCSleb}$, or it can be set to be scaled with the AC line rms voltage.

At low output load, the combo controller IC goes into burst mode. The PFC burst mode operation is synchronous to the hybrid-flyback burst mode operation.

4.2.3 PFC bus voltage sensing and regulation

The controller senses the PFC output voltage V_{bus} via pin PFCVS. The bus voltage is maintained by a nonlinear PIT1 controller that calculates the desired on-time $t_{PFCondes}$ in response to the sensed voltage.

The PFC on-time from regulation $t_{PFCondes}$ is limited to a configurable minimum value $t_{PFConmin}$ and a maximum value $t_{PFConmax}$.

The PFC target bus voltage and the bus voltage undervoltage protection level V_{busUVP} are set dynamically by the controller. In case the bus voltage V_{bus} drops and is getting close to V_{busUVP}, the controller reacts and increases the on-time to the maximum on-time $t_{PFConmax}$ in order to boost up the bus voltage.

In order to compensate for the AC line gain dependency of the boost power stage, the PIT1-controller processes the previous sample of $t_{PFCondes}$ in nonlinear way. This is used as a kind of AC input feedforward-control.

4.2.4 PFC bus voltage target setting

In contrast to a conventional PFC boost converter, the bus voltage target level $V_{bustarget}$ is not fixed but changing with operation conditions. On the one hand, the hybrid-flyback stage is requesting some bus voltage target level depending on the output voltage V_{out}. On the other hand, the PFC itself can set a target bus voltage level following the AC peak voltage. This feature is described in more detail in Chapter 4.4.3.

4.2.5 PFC soft-start

Each time the PFC is enabled, the PFC initiates a soft start to minimize the switching stress on the power MOSFET, diode and inductor. During a soft start, the PFC operates in QR1-mode. The soft-starts ends as soon as the bus voltage has reached 93.75% of the target value $V_{bustarget}$ or when PFC pulse skipping mode is entered. The initial on-time depends on the configuration of parameter $CFG_{PFContime}$: It is either fixed or will be scaled with the AC line rms voltage.

4.2.6 PFC gate driver

A PFC gate driver is integrated in the controller at pin PFCGD. In order to drive discrete GaN-HEMT devices, a dedicated external RC-network is recommended.

4.2.7 PFC disable

The PFC can be disabled completely and permanently by configuration. At the same time all PFC related protections are automatically disabled. The hybrid-flyback and related house-keeping functions are still enabled.

The controller with disabled PFC functionality is meant to be combined with a separate, standalone PFC controller providing a regulated bus voltage V_{bus} which is high enough for reliable operation of the hybrid-flyback in all operation conditions. Otherwise, PFC bus undervoltage protection will trigger (see Chapter 4.5.2.9).

4.3 Hybrid-flyback control

The hybrid-flyback converter is based on a resonant asymmetrical half-bridge topology with flyback output. Figure 12 shows the hybrid-flyback stage with the associated control blocks.

The hybrid-flyback power stage can achieve zero voltage switching (ZVS) operation on primary side and zero current switching (ZCS) operation on secondary side under all conditions of bus voltage V_{bus} and output voltage V_{out} with proper system design. In order to achieve ZVS operation, two control methods are implemented:

- Continuous resonant mode (CRM) operation
- Zero voltage resonant valley switching (ZV-RVS) operation

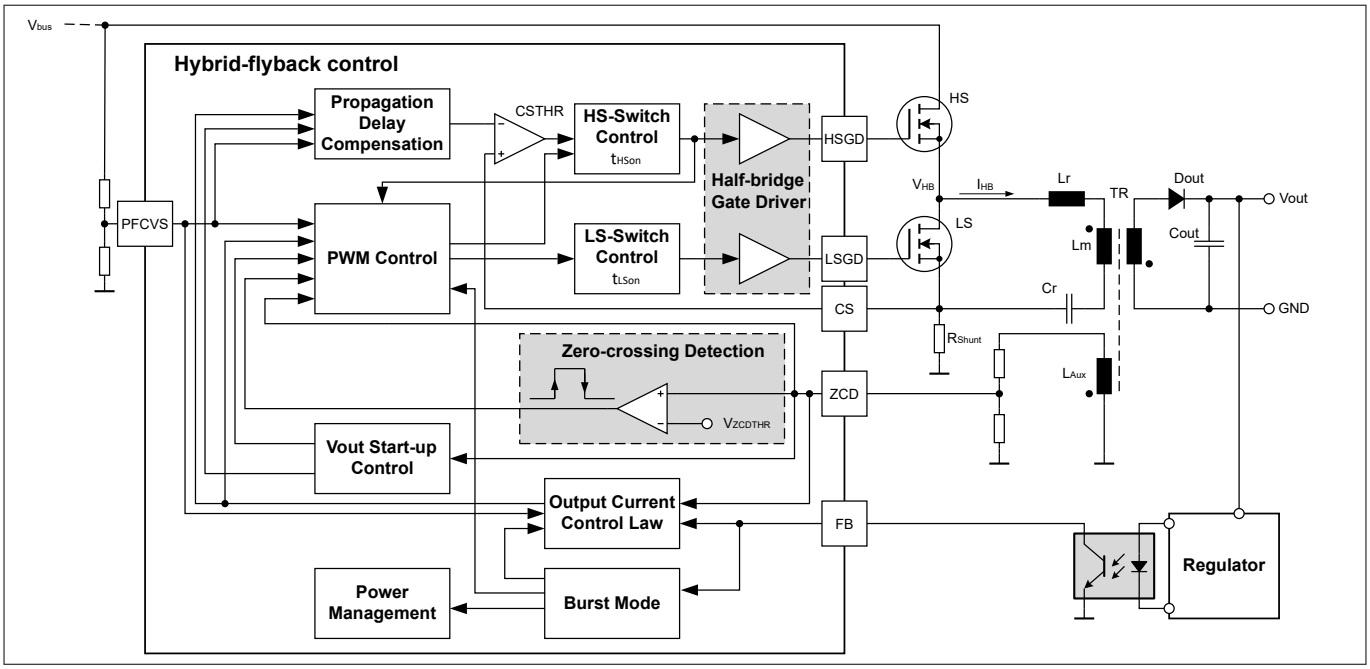

Figure 12 Hybrid-flyback circuit arrangement with associated control blocks

The output current control uses the CSTHR-comparator for peak current control via high-side switch on-time t_{HSon}.

4.3.1 PWM control schemes

In the following chapter the pulse width modulation (PWM) control methods for the different control modes and the associated mode transition are discussed. Depending on load, output voltage and bus voltage the control scheme is adjusted to ensure ZVS operation for both low-side and high-side switches.

4.3.1.1 CRM control scheme

In continuous resonant mode (CRM) the switching of high-side switch HS and low-side switch LS is done in a continuous alternating manner with short dead-times t_{deadHS} for the high-side switch turn-on and t_{deadLS} for the LS switch turn-on.

It targets a ZVS operation for every half-bridge switching cycle by tuning the negative current level I_{MAGneg}.
In Figure 13 typical waveforms are shown. The dead-time t_{deadLS} between HS and LS switch is fixed as the peak current is high enough to provide proper ZVS operation for LS switch.

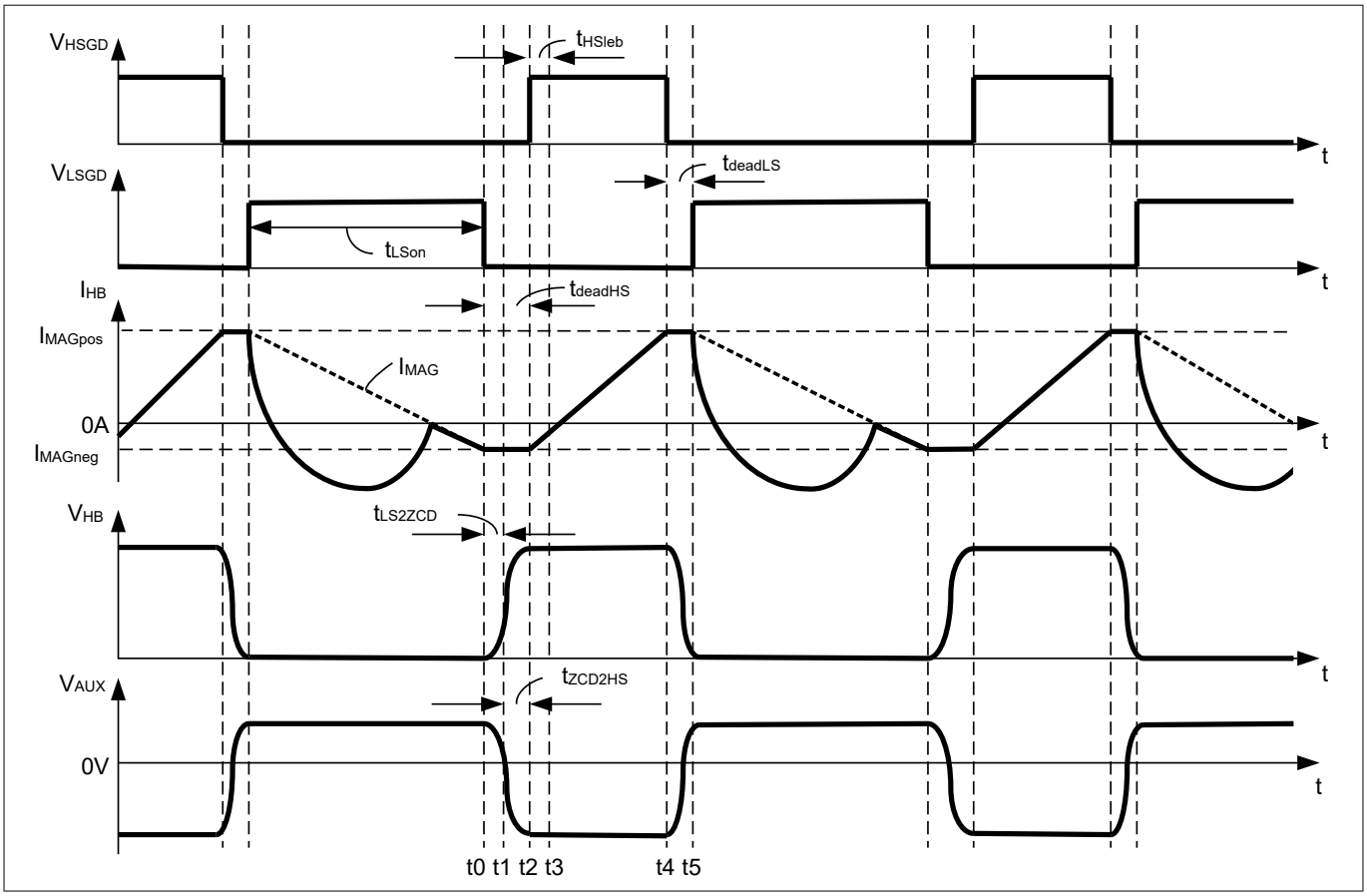

Figure 13 Half-bridge timings for CRM operation

In CRM operation the dead-time t_{deadHS} consists of two time intervals:

$$t_{deadHS}(CRM) = t_{LS2ZCD} + t_{ZCD2HS}$$

Equation 1

The LS on-time is adjusted cycle-by-cycle for a target delay time t1 - t0 = $t_{LS2ZCD}(V_{bus})$, based on the configurable corners $t_{LS2ZCDmax} = t_{LS2ZCD}(V_{bus} = V_{Cr})$ and $t_{LS2ZCDmin} = t_{LS2ZCD}(V_{bus} = V_{busACovp})$.

The configurable time period t2 - t1 = t_{ZCD2HS} is delaying the HS switch turn-on at time t2 so that HS ZVS is possible.

The HS switch is activated when the deadtime t_{deadHS}(CRM) is over or when the switching period exceeds 327 μs_{typ}.

After the HS switch is activated, the peak current control determines the HS on-time. The magnetizing current can be measured after a leading edge spike blanking period t_{HSleb}, which therefore determines the minimum on-time of HS switch operation.

4.3.1.2 ZV-RVS control scheme

When decreasing the load the amount of circulating magnetization energy is increasing compared to the transmitted energy in CRM operation. When decreasing V_{out} the demagnetization time is becoming much longer than half of the resonant period of the LrCr tank, which can lead to further resonant half-bridge oscillations. Turning off the LS switch during an ongoing I_{HB} oscillation can lead to oscillations on the secondary side due to the secondary side leakage inductance.

To overcome these issues the zero voltage resonant valley switching (ZV-RVS) mode is provided. It keeps the peak magnetizing current in the desired range while maintaining soft switching of both HS and LS switch. Lower load is addressed by lower switching frequency. Figure 14 shows typical waveforms when operating in the second valley.

Compared to CRM, there are two LS pulses during HS off-time with a wait gap $t_{waitgap}$ in-between. The first LS pulse demagnetizes the LrCr tank and charges the output capacitor on the secondary side. The waiting time gap $t_{waitgap}$ is inserted at time t0 after a HS and LS switch half-bridge cycle. During the wait gap, a free-wheeling oscillation takes place which is sensed by pin ZCD with a comparator. The second LS pulse, the so-called ZVS pulse t_{ZVS}, starts shortly after the first or a later rising edge detection of the ZCD comparator at time t1 and a configurable delay time period $t_{ZCDfilRVS}$ so that the LS switch turns on at a valley of the drain-source voltage and zero magnetizing current. Hence, a resonant valley switching (RVS) operation is achieved. Selecting a later valley increases the wait gap duration $t_{waitgap}$ and lowers the switching frequency. The ZVS pulse further demagnetizes the the LrCr tank to a negative value I_{MAGneg} for zero-voltage switching (ZVS) of the HS switch. The required ZVS pulse length t_{ZVS} is determined by the target negative magnetization level I_{MAGneg}, the transformer magnetizing inductance Lm and depends on the output voltage Vout. The minimum ZVS pulse length occurs at lowest input and highest output voltage. In addition a lower limit t_{ZVSmin} applies.

During the first switching cycles of the hybrid-flyback start-up the dead-time for turning on the HS switch after the ZVS pulse is fixed with using the value $t_{deadHSRVS}$. The subsequent dead-time t_{deadLS} is same as in CRM operation.

Selecting the appropriate valley and adjusting the magnetizing peak current within the desired range controls the load.

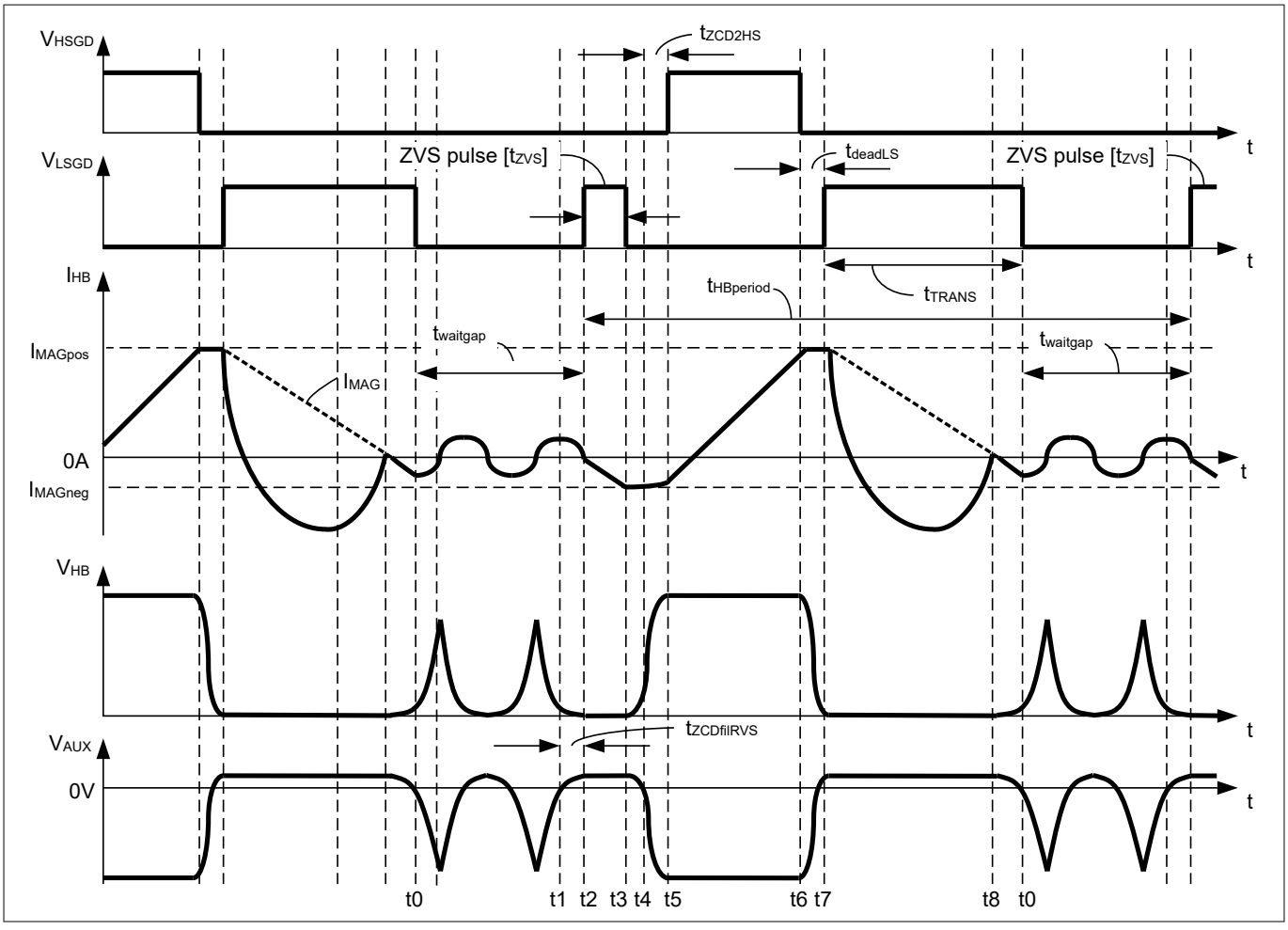

Figure 14 Hybrid-flyback operating in zero voltage resonant valley switching mode (ZV-RVS)

4.3.1.3 Valley skipping control

When operating in ZV-RVS mode, valley detection is taking place to determine the time for turning on the ZVS pulse. The waiting time $t_{waitgap}$ is controlled based on the target number of detected valleys.

The target valley number is chosen so that the magnetizing peak current is in the desired range to ensure an optimum operation. If the target valley cannot be detected, the controller will enter DCM operation with a similar fixed frequency.

4.3.1.4 DCM control scheme

ZV-RVS mode operation at light-load is limited by the maximum number of detectable zero-crossings at ZCD due to decreasing oscillation magnitude with prolongation of the inserted waiting time gap $t_{waitgap}$. When further reducing the output current the waiting time gap $t_{waitgap}$ is further increased until the ZVS pulse is initiated without zero-crossing detection. The subsequent half-bridge cycle is then again performed under ZVS condition. Increasing $t_{waitgap}$ takes only place until the half-bridge period $t_{HBperiod}$ reaches the associated minimum half-bridge switching frequency $f_{swDCMmin}$.

4.3.1.5 Mode transition between CRM and ZV-RVS

The mode transition control is based on the target peak current I_{MAGpos} and the voltage measured at ZCD pin. First, a transition from CRM to ZV-RVS mode and vice versa is only possible in case the output voltage, sensed via ZCD, has a certain value. The transition from ZV-RVS to CRM is only possible with a detected output voltage greater than $V_{outRVS2CRM}$ (in order to have some hysteresis, the transition from CRM back to ZV-RVS only happens for an output voltage smaller than $V_{outCRM2RVS}$). Second, the feedback signal V_{FB} is determining the internal current set-point I_{SET} and compared with the internal thresholds for changeover.

4.3.2 Output control

Similar as in standard flyback controllers primary peak current control is implemented to support a 1st order system for easier control loop compensation. The input power per half-bridge switching cycle is depending on the voltage at the resonant capacitor C_r that is charged by the half-bridge current I_{HB} during the on-time t_{HSon}. The input power in CRM-mode can be calculated as shown in the following equation:

$$P_{in} = \frac{1}{2} \cdot V_{Cr,avg} \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 2

$V_{Cr,avg}$ is the average voltage on the resonant capacitor C_r , which is the reflected output voltage V_{out} multiplied with the transformer turns ratio. The output voltage is reflected at winding L_{AUX} during the on-time period of LS switch.

$$V_{Cr,avg} = N \cdot V_{out}$$

Equation 3

Assuming an ideal system leads to a direct correlation between input half-bridge current I_{HB} and average output current I_{out}:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{1}{2} \cdot N \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 4

Compared to CRM operation the ZV-RVS mode is adding waiting time gaps $t_{waitgap}$, where no energy transfer is happening. The average output current I_{out} is decreasing with increasing $t_{waitgap}$ according to

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{t_{HBperiod} - t_{waitgap}}{t_{HBperiod}} \cdot \frac{1}{2} \cdot N \cdot \left(I_{MAGpos} + I_{MAGneg}\right)$$

Equation 5

The output current is only controlled by means of the positive magnetization current level I_{MAGpos}. During continuous operation the output current I_{out} is controlled by means of a linear relationship between the feedback voltage at FB pin and the associated internal current set-point I_{SET}, which is described in Chapter 4.3.2.1. The negative current I_{MAGneg} is chosen so that ZVS of the HS is achieved. The value of I_{MAGneg} is a function of V_{bus}.

The output voltage is measured via pin ZCD at the auxiliary winding and is used for protection features, for compensation to ensure ZVS operation over wide output voltage range (see Chapter 4.3.2.3) as well as for estimating the average voltage $V_{Cr,avg}$ on the resonant capacitor according to Chapter 4.3.2. The internal averaging uses a filter with configurable filter time constant $T_{CVzcdavg}$.

4.3.2.1 Output current control law

The positive magnetization level I_{MAGpos} equals the positive half-bridge peak current that is controlled via CS pin at the shunt resistor R_{Shunt}:

$$V_{CSpeak} = I_{MAGpos} \cdot R_{Shunt}$$

Equation 6

Peak current regulation is prone to error due to noise. CS pin related PCB design should consider this sensitivity. An external high-frequency R-C-filter at CS pin is recommended. In addition, a digital filter using a configurable filter time $t_{CSTHRfil}$ can be set to blank the CSTHR comparator event.

Figure 15 shows the control path from feedback signal input at FB pin to peak current setting at CS pin. The requested output current equals to the internal I_{SET} for the corresponding feedback signal. The required peak current setting is then calculated based on V_{bus} measurement and mode operation.

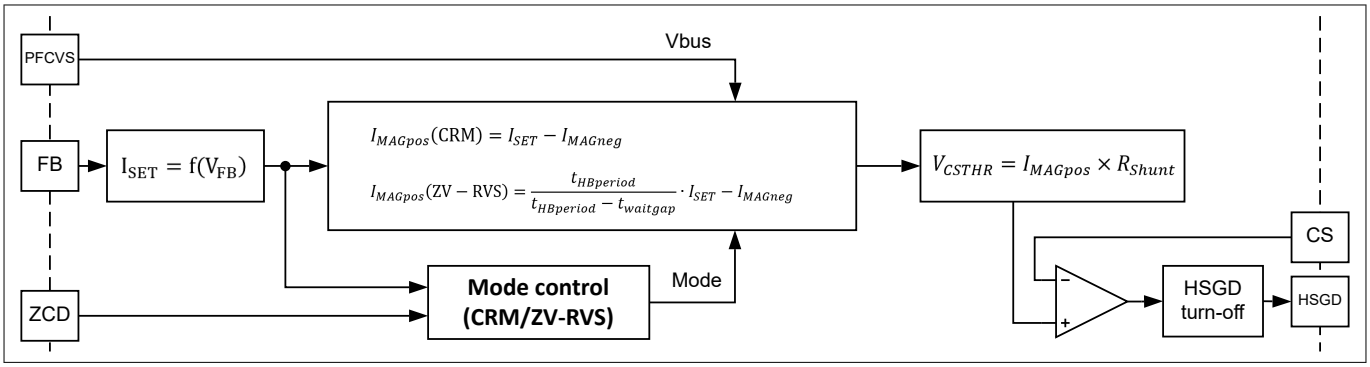

Figure 15 Control path from feedback input to peak current setting

The feedback pin has a pull-up resistor R_{FBpu} to V_{FBoc}. The value of the pull-up resistor R_{FBpu} is configurable. The feedback voltage V_{FB} has a linear correlation with the output current I_{out} between burst mode entry current level $I_{outBMen}$ and the maximum output current $I_{outOCPmax}$. Figure 16 shows the relationship between output current and feedback voltage.

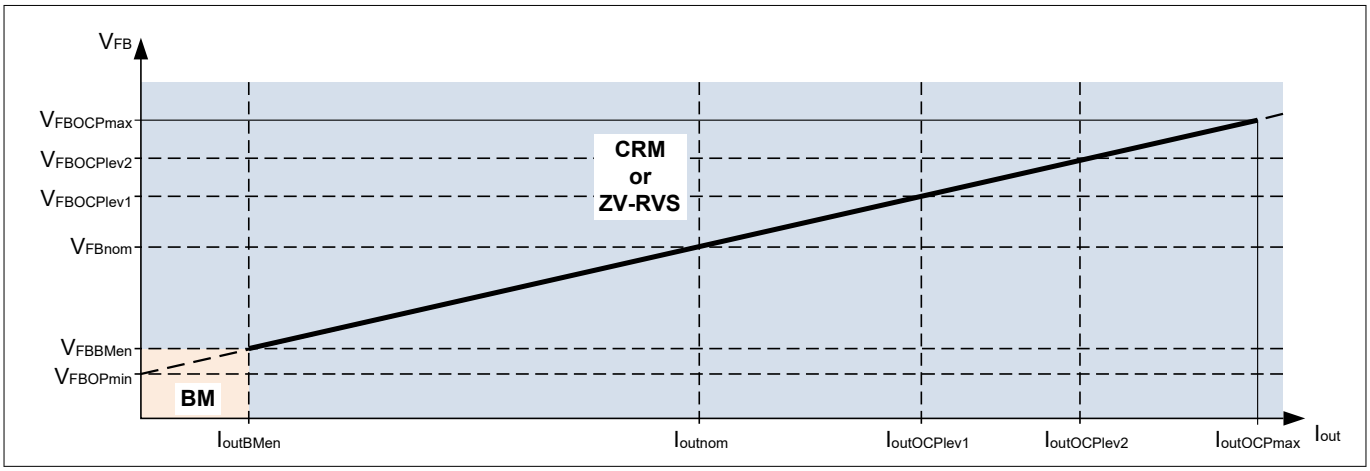

Figure 16 Control law for feedback voltage at FB pin

In the IC output current I_{out} is represented by the equivalent internal current set-point I_{SET}, which is then mapped to the positive magnetization level I_{MAGpos}. The peak current I_{MAGpos} is controlled by a comparator with variable threshold at pin CS. The relation between I_{SET} and I_{MAGpos} is different for CRM and ZV-RVS mode.

4.3.2.2 Keeping ZVS operation for wide Vbus voltage range

The ZVS operation in CRM is explained in Chapter 4.3.1.1. In ZV-RVS, the ZVS pulse length is set targeting a negative current I_{MAGneg} as described in Chapter 4.3.1.2. Here, $I_{MAGnegnom}$ is the target negative current at V_{bus} = V_{Cr}. For higher bus voltages the absolute value of the target negative current is increased considering the configurable value of an equivalent capacitance C_{Oeq}.

4.3.2.3 Keeping ZVS operation for wide output voltage range

When output voltage Vout is decreasing the demagnetization takes longer. In CRM, ZVS operation is ensured by adjusting the on time of the LS switch t_{LSon} to match with the changed Vout. In ZV-RVS, the ZVS pulse on-time t_{ZVS} is calculated from I_{MAGneg} and Vout and the first LS on-time t_{TRANS} decreases with increasing Vout (see Figure 17).

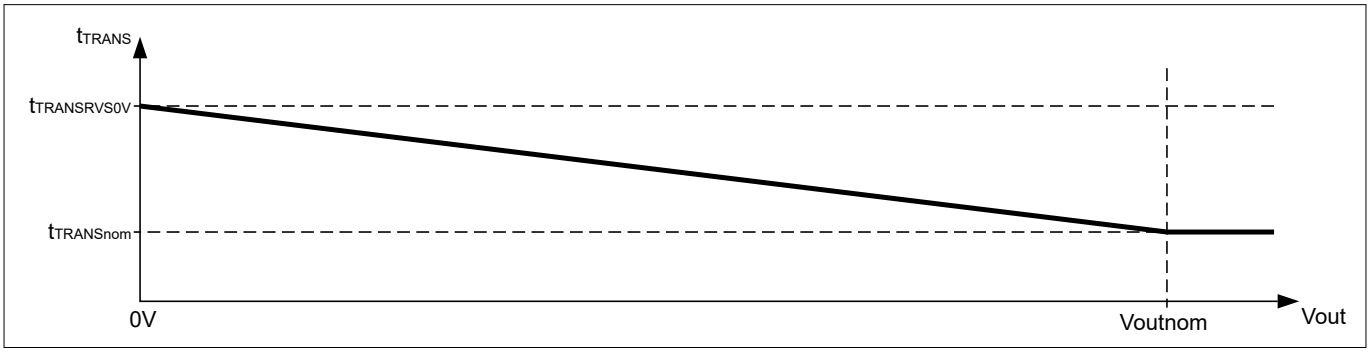

Figure 17 Vout compensation for t_{TRANS} in ZV-RVS mode

4.3.2.4 ZVS operation and body-diode cross-conduction prevention during CRM operation

A too short LS on-time can cause hard switching or even body diode cross conduction if the magnetizing current is still positive when LS is turned off. A too long on-time increases the reactive current and conduction losses and can even saturate the transformer. In order to exclude hard switching and body diode cross conduction, the controller activates the HS switch only after the voltage at pin ZCD indicates a changing half-bridge voltage V_{HB} (ZCD event). The controller adjusts the LS on-time to always ensure ZVS condition.

4.3.2.5 Propagation delay compensation (PDC)

During peak current control a propagation delay is impacting the peak current resulting in higher values. The overshoot depends on the voltage at the input voltage V_{bus} and reflected output voltage at resonant capacitor V_{Cr}. This dependency on V_{bus} and V_{Cr} impacts the current set-point threshold accuracy seen in the application and is therefore compensated to avoid errors on the feedback signal V_{FB} and the internal current set point I_{SET}.

4.3.3 Vout start-up control

A hybrid-flyback start-up takes place after the start-up conditions are met, see Chapter 4.1.1. At first several LS pulses are applied to precharge the bootstrap capacitor at HSVCC pin. After that ZV-RVS switching cycles smoothly ramp up the output voltage. Here, the first switching cycles run with a low fixed frequency until the voltage at pin ZCD is high enough for valley switching. The startup-phase is finished once the feedback loop takes over the peak current control.

During the first HS pulse the CS pin is checked for short circuit. For the ZVS pulse duration a maximum applies to prevent too long ZVS pulse due to very low ZCD voltage measurement. A transition from ZV-RVS to CRM may take place during the startup-phase if the voltage sampled at pin ZCD exceeds the related thresholds.

4.3.4 Frequency jitter

In order to reduce the EMI noise spectrum a switching frequency jitter is available. The jitter function is working in CRM and in ZV-RVS operation. In CRM-operation the jitter function is only active in case the bus voltage

exceeds the configurable bus voltage threshold $V_{busJitteren}$, while in ZV-RVS mode the jitter is enabled once the configurable parameter $I_{MAGnegjitter}$ has a non-zero value.

The switching frequency jitter is done by modulating the magnetizing current. In CRM, the modulation of the magnetizing current is done by changing the LS on-time t_{LSon}, while in ZV-RVS the ZVS pulse length t_{ZVS} is changed.

4.3.5 Half-bridge gate driver

The half-bridge gate driver consists of a low-side gate driver for LS switch, which is supplied by VCC and GND pin. The HS switch is driven by a floating high-side gate driver supplied by HSVCC and HSGND. The floating HS domain is galvanically isolated and steered via a coreless pulse transformer. The LS and HS gate drivers are enabled/disabled based on the corresponding undervoltage lockout thresholds (V_{VCCon}, V_{VCCoff}) and ($V_{HSVCCon}$, $V_{HSVCCoff}$) (see Chapter 4.5.2.1 and Chapter 4.5.2.2). Both drivers are clamping the maximum gate driver output voltage to $V_{LSGDhigh}$. If disabled the gate driver outputs are actively kept pulled down. When HSVCC exceeds the threshold $V_{HSVCCon}$ the high-side gate driver is enabled after a time period of $t_{HSGDendel}$.

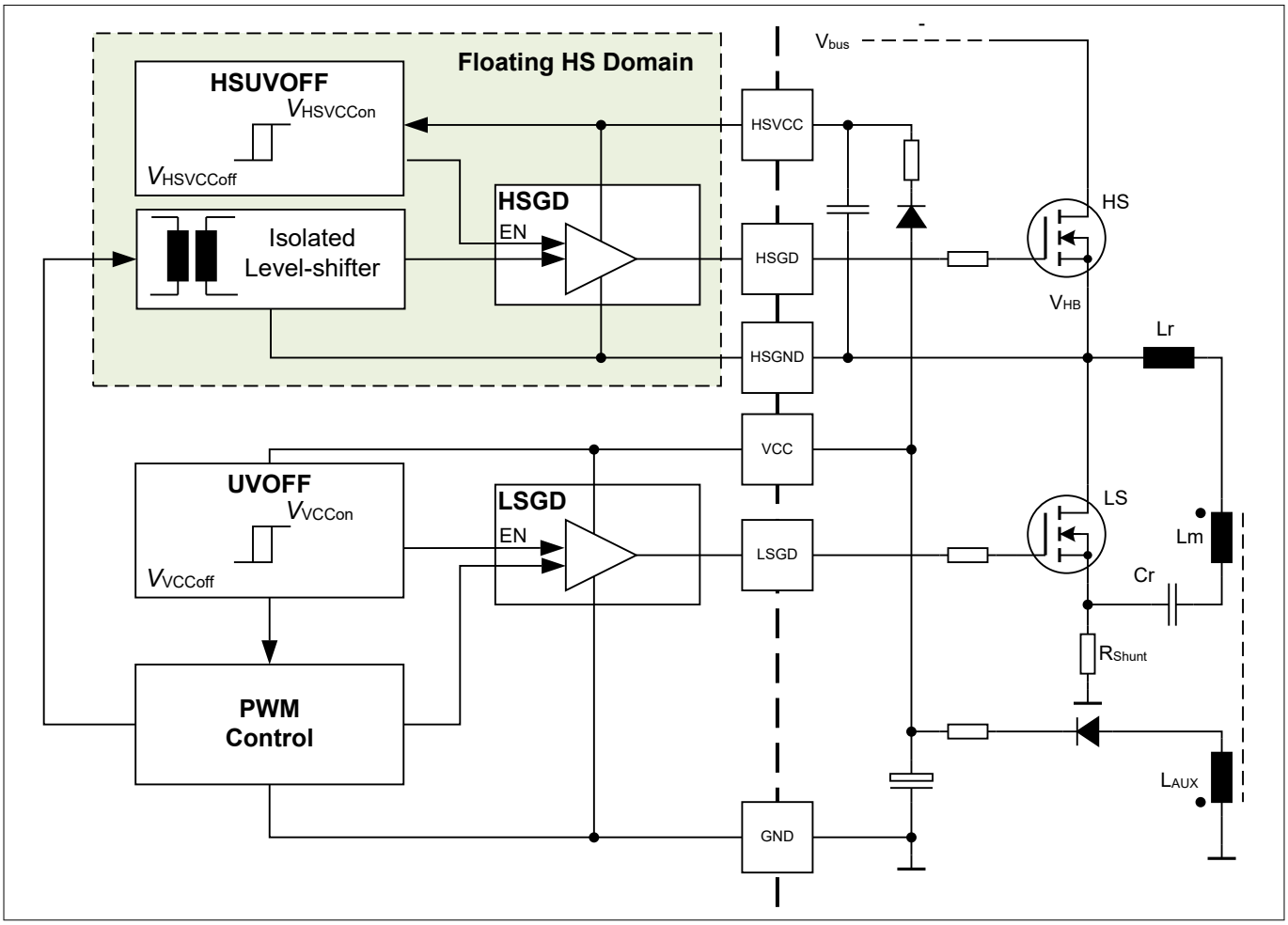

Figure 18 Half-bridge gate driver

In order to drive discrete GaN-HEMT devices in the half-bridge, a dedicated external RC-network is recommended, see Figure 3.

For the high voltage level $V_{LSGDhigh}$ of the LS gate driver two different values can be set by configuration.

4.4 Combo-control functions

In the following section the combo-controller functions with PFC and Hybrid-flyback controller interaction for an optimum system control are described.

4.4.1 Burst mode control

The IC contains a burst mode control block to enter a highly efficient operation mode at light-load. By introducing longer non-switching phases with IC entering a sleep mode the average switching and bias losses are reduced during burst mode operation. Both, the PFC stage and the hybrid-flyback, go into burst mode at low load. The burst mode operation is controlled by the hybrid-flyback controller in relation to the output current reflected by the feedback voltage V_{FB}. In general, the burst-mode operation of PFC and hybrid-flyback is synchronized. Figure 19 shows the main functions for the burst mode control.

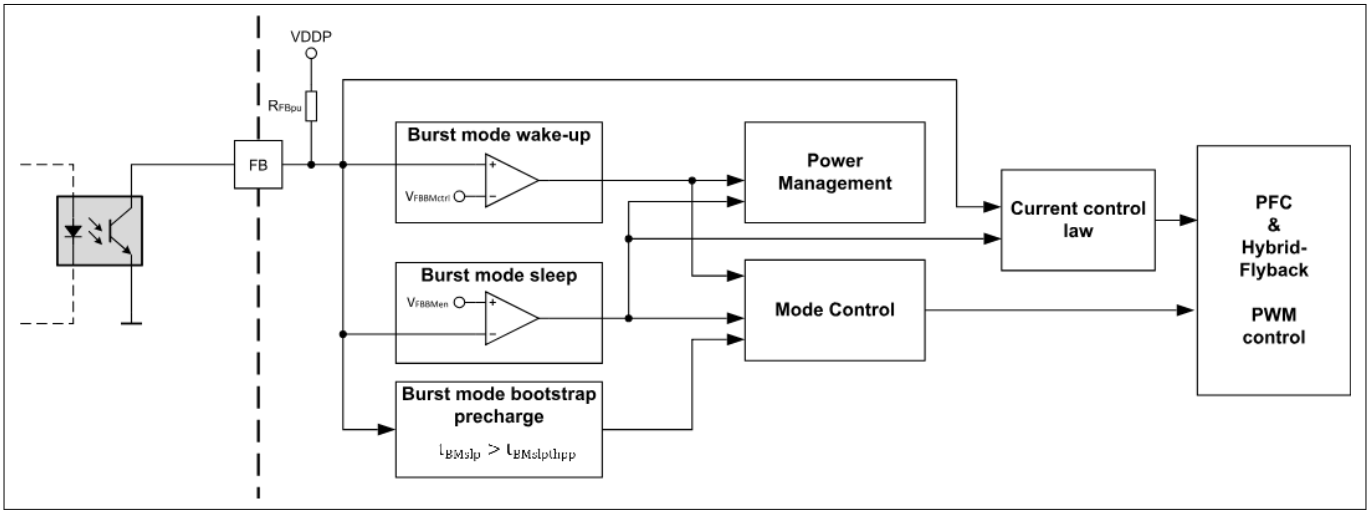

Figure 19 Burst mode control block

4.4.1.1 Burst mode entry

Once V_{FB} is dropping below V_{FBBMen} the generation of next switching pulse is stopped and burst mode is enabled by entering sleep mode with the reduced current consumption $I_{VCCBMpsm}$. At burst mode entry the HV start-up cell is turned on to charge up VCC until V_{VCCon} is reached.

4.4.1.2 Burst mode operation

The steady state burst mode operation is based on a burst frame on/off control by means of comparing the voltage at FB pin with the feedback thresholds V_{FBBMen} and $V_{FBBMctrl}$. The threshold V_{FBBMen} determines when the IC enters the sleep phase. During the sleep phase the threshold $V_{FBBMctrl}$ is used for for waking up. The burst frame duty cycle and burst frame frequency is fully controlled by means of $V_{FB.}$ VCC current consumption is reduced during the sleep phases.

The PFC is enabled and disabled synchronously with the hybrid-flyback. However, depending on the operation conditions, PFC might also be disabled (see Chapter 4.4.2), while the hybrid-flyback is switching.

4.4.1.3 Burst mode bootstrap precharge

Operation in burst mode at very light-load leads to long sleep phases without switching activities. During this sleep time period the HSVCC voltage may drop below the off-threshold $V_{HSVCCoff}$ and deactivate the floating HS gate driver. To ensure that a proper HSVCC supply is in place for turning on the HS switch after a long IC sleep phase, a train of $N_{BMprepulse}$ precharge pulses is introduced before the first ZV-RVS switching cycle. The precharge pulse train is only introduced when the captured burst mode sleep time has exceeded the threshold $t_{BMslpthrpp}$. Figure 20 shows a precharge pulse train pattern for the case $N_{BMprepulse}$=3.

Note: If a HS pulse is missing due to improper HSVCC supply, the subsequent LS pulse may lead to hard switching. Therefore, the controller tries to detect this case and may stop the switching operation.

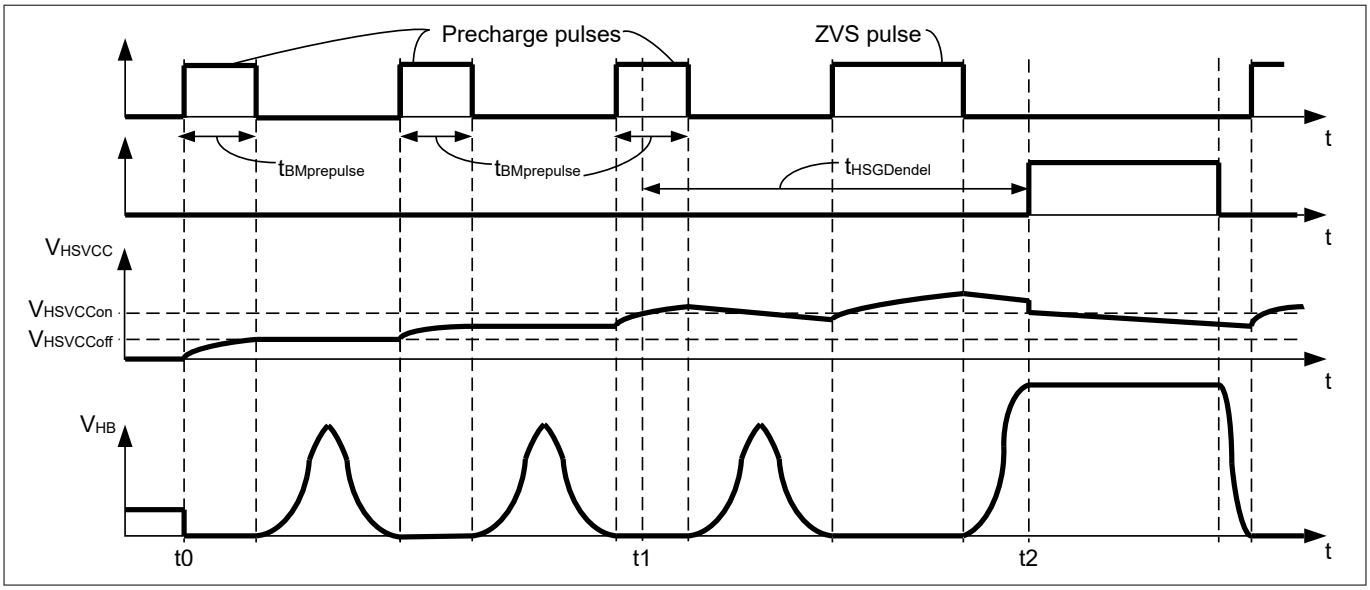

Figure 20 Precharge pulse train pattern

4.4.1.4 Burst mode exit

Burst mode exit is a smooth transition from on/off control back to the closed feedback control loop at load increase, no matter if the load jumps or increases slowly. In these cases the controller it will wake-up (in case it was not active yet) and starts switching. Since the load and the voltage at pin FB are high, the controller is not going to sleep anymore but changes to normal operation. This smooth transition is possible as in regular burst mode active phase regular peak current control based on the feedback control applies.

4.4.2 PFC enable/disable control

The PFC stage is enabled and active, when the load is above a certain level where power factor correction could be mandatory or the hybrid-flyback stage requires a minimum input voltage level for proper operation.

Whether the load requires PFC operation is decided by a hysteretic comparator with two thresholds $P_{PFCenable}$ and $P_{PFCdisable}$. However, the PFC may be enabled although the estimated power is below $P_{PFCdisable}$ to ensure proper hybrid-flyback operation. Whether the hybrid-flyback stage requires PFC operation is decided by a hysteretic comparator evaluating the AC line peak voltage with two thresholds derived from the sensed output voltage.

For the power-based disabling of the PFC with the estimated power going below $P_{PFCdisable}$ a configurable blanking time $t_{PFCblkdisable}$ applies.

4.4.3 Variable bus voltage target level

Compared to conventional PFC boost operation, the PFC bus voltage is not regulated to a fixed target value but the target voltage depends on the operation conditions and is set either by the hybrid-flyback stage or by the PFC itself. This functionality is closely related to the PFC enable/disable control (see Chapter 4.4.2).

For optimum operation of the hybrid-flyback stage over a wide output voltage range, the PFC bus voltage target level $V_{bustarget,HFB}$ requested by the hybrid-flyback stage is determined by the controller depending on the reflected output voltage $N \cdot V_{out}$, which is determined from the voltage at pin ZCD.

A proper PFC operation is only possible in case the target bus voltage target level is somewhat above the given AC line peak voltage $|V_{ACpk}|$. For that reason the PFC controller also determines a bus voltage target level $V_{bustarget,PFC}$ which is the detected rectified AC peak voltage plus an offset $V_{bustargetVacpkoffset}$.

Whenever PFC is enabled and switching the higher value of $V_{bustarget,HFB}$ and $V_{bustarget,PFC}$ is used as target value for the PFC regulation.

Furthermore, the bus voltage target value is limited to a minimum value $V_{bustargetmin}$ as well as to a maximum value $V_{bustargetmax}$.

4.5 Protections

The IC supports several protection functions resulting in different protection reactions.

For most protection events the IC enters a protection mode (see Chapter 4.5.1). In many cases the protection mode is configurable.

Table 2 Protection Features and Reaction

Protection Feature	Symbol	Protection Reaction
VCC undervoltage lockout	UVOFF	HW reset and restart
HSVCC undervoltage lockout	HSUVOFF	Disable HS gate driver
VCC overvoltage protection	VCCOVP	Configurable: Auto-restart or latch
Brown-in protection	BIP	Bang-bang mode, waiting for brown-in in start-up check phase
Brown-out protection	BOP	Stop operation and enter fast restart mode
PFC Start-up timeout protection	PFCSTTOP	Configurable: Auto-restart or latch
Output start-up timeout protection	VoutSTTOP	Configurable: Auto-restart or latch
AC overvoltage protection	ACOVP	Configurable: Auto-restart or latch
PFC bus overvoltage protection level 1	PFCOVP1	Stop PFC switching
PFC bus overvoltage protection level 2	PFCOVP2	Stop PFC switching (cycle-by-cycle)
PFC bus undervoltage protection	PFCUVP	Configurable: Auto-restart, latch or stop operation and enter fast restart mode
PFC overcurrent protection	PFCOCP	Stop PFC switching (cycle-by-cycle)
PFC CCM protection	PFCCCM	Configurable: Auto-restart or latch
Output overcurrent protection level 1	OCPlev1	Configurable: Auto-restart or latch
Output overcurrent protection level 2	OCPlev2	Configurable: Auto-restart or latch
Output maximum current protection	OCPmax	Configurable: Auto-restart or latch
HFB primary side overcurrent protection	CSPROT	Configurable: Auto-restart or latch
Vout overvoltage protection	VoutOVP	Configurable: Auto-restart or latch
Vout undervoltage protection	VoutUVP	Configurable: Auto-restart or latch
Vout short circuit protection	VoutSCP	Configurable: Auto-restart or latch
CS pin short protection	CSSCP	Configurable: Auto-restart or latch
FB pin start-up protection	FBSTUP	Stop operation and enter bang-bang mode for start-up check phase
HFB open loop protection	HFBOLP	Configurable: Auto-restart or latch
External overtemperature protection	extOTP	Configurable: Auto-restart or latch
Watchdog timer	WDOG	Configurable: Auto-restart or latch
Memory parity check	MEMPAR	Configurable: Auto-restart or latch

4.5.1 Protection modes

Once the protection mode is entered, the IC stops the gate driver switching at the PFCGD, LSGD and HSGD pins and enters stand-by mode. During stand-by mode, the HV start-up cell is operating in the bang-bang mode (see

Chapter 4.1.3) to keep the VCC voltage at a high level to have enough energy stored in the VCC capacitor for the system start-up. Three protections modes are supported as described in the sequel.

4.5.1.1 Deactivate IC after undervoltage lockout

In case VCC drops below V_{VCCoff} the undervoltage lockout protection is triggered, the IC is completely deactivated and is only restarted with the regular start-up mechanism, see Chapter 4.1.1.

4.5.1.2 Auto-restart mode

When auto-restart mode is activated, the controller stops switching at the gate driver pins. After a configurable auto restart time t_{ARM}, the control IC resumes its operation. During the auto restart time t_{ARM} the controller wakes up very $t_{ARMbase}$ in order to re-charge VCC to V_{VCCon} (see Chapter 4.1.3).

4.5.1.3 Latch mode

In latched operation the system stays in stand-by mode without any restart attempt. The latched operation can only be reset by VCC dropping below the UVOFF HW reset threshold V_{VCCoff}. In latch mode operation, the HV start-up cell is turned on at VCC pin voltage threshold $V_{VCCslpHVon}$ and turned off when reaching VCC pin voltage threshold V_{VCCon} (see Chapter 4.1.3).

4.5.1.4 Fast restart mode

In fast restart mode operation the IC enters bang-bang during brown-in phase (see Chapter 4.1.2). After entering the sleep mode the HV start-up cell turns on and charges up the VCC voltage until the threshold V_{VCCon}. Then the IC is activated again for restart.

4.5.2 Protection features

4.5.2.1 VCC undervoltage lockout

The implemented VCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the IC operation depending on the supply voltage at pin VCC. The UVOFF contains a hysteresis with the upper voltage threshold V_{VCCon} for activating the IC. A VCC voltage level dropping below the bottom threshold V_{VCCoff} resets and deactivates the IC during normal operation. In reset state the HV start-up cell is turned on, starting the next VCC charge cycle until VCC voltage exceeds V_{VCCon} (see Chapter 4.1.1).

4.5.2.2 HSVCC undervoltage lockout

The implemented HSVCC undervoltage lockout (UVOFF) ensures a defined activation and deactivation of the floating high-side driver. The HSUVOFF contains a hysteresis with the upper voltage threshold $V_{HSVCCon}$ for activating the high-side gate driver. A HSVCC voltage level dropping below the bottom threshold $V_{HSVCCoff}$ turns off and deactivates immediately the high-side driver. During deactivation phase the high-side driver current consumption is reduced.

4.5.2.3 VCC overvoltage protection

There is an over voltage detection at pin VCC. The detection function consists of a threshold V_{VCCOVP} and a blanking time of t_{VCCOVP}. The protection reaction once the overvoltage protection is triggered can be configured.

4.5.2.4 Brown-in protection

For successful brown-in two conditions must be fulfilled:

1. Input voltage above threshold with $V_{in} > V_{inbi}$ sensed via pin HV
2. PFC bus voltage above threshold with $V_{bus} > V_{busbi}$ sensed via pin PFCVS

When AC brown-in condition is not met before the timeout duration t_{HVbito} is expired, the AC brown-in time out protection reaction is triggered.

Since the brown-in is also based on the sensed bus voltage, this protection also acts as PFC open-loop protection during start-up.

4.5.2.5 Brown-out protection

Brown-out detection is based on AC peak voltage estimation: In case the PFC is disabled, the AC peak voltage is determined from the bus voltage V_{bus} sensed at pin PFCVS. In case the PFC is enabled the AC peak voltage is determined using the captured PFC switching cycle timings. If the estimated AC peak voltage is below the configurable threshold V_{inbo} for longer than the blanking time t_{bo}, the protection mode will be triggered and the IC enters brown-in detection phase. Please be aware, that the blanking time is only counted during active time, so that during burst-mode with sleep phases the duration to detect a brown-out is increased.

Afterwards, as described in Chapter 4.1.2, bang-bang mode is entered for an fast re-start in case AC input voltage comes back.

4.5.2.6 Start-up timeout protections

After the PFC is activated, the PFC performs a soft-start. In case the softstart cannot be completed within $t_{startPFC}$, the configured protection mode (auto-restart or latch) is entered.

A second start-up timeout function is implemented for the hybrid-flyback output. In case of overload during start-up the output voltage V_{out} may not reach the regulation target voltage, preventing the system from entering regulation. A timeout is detected if the current set-point determined by V_{FB} is not dropping below the current set-point determined by V_{out} start-up control within the maximum time period $t_{startto}$.

4.5.2.7 PFC bus overvoltage protection

The first overvoltage protection (PFCOVP1) threshold is given by the configurable parameter $V_{PFCVSovp1}$. Latest within $t_{SLWTASK}$ after this threshold is exceeded, the PFC stops switching. The hybrid-flyback stage continues switching. The PFC resumes operation when the measured voltage falls below the threshold $V_{PFCVSovp1res}$.

A second overvoltage protection mechanism (PFCOVP2) is implemented using an hardware comparator. It protects the system in case the bus voltage increases above the first OVP threshold in very short time without triggering PFCOVP1. The corresponding threshold $V_{PFCVSovp2}$ is a fixed voltage. In case the voltage sensed at PFCVS exceeds the threshold, no new PFC gate driver pulse is generated. As soon as the voltage at PFCVS is below the threshold $V_{PFCVSovp2}$ again, PFC pulses are generated again.

Neither in case of OVP1 nor in case of OVP2 a protection mode is entered. Hybrid-flyback switching remains unaffected.

4.5.2.8 AC overvoltage protection

The AC overvoltage protection (ACOVP) is also based on the bus voltage measured at PFCVS via external voltage divider. Compared to the bus overvoltage protections OVP1 and OVP2, which only stop PFC from switching (see Chapter 4.5.2.7), the ACOVP stops PFC and hybrid-flyback operation and enters protection mode. In case of AC overvoltage, the PFC stops switching due to OVP2, the bus voltage and thus the voltage at pin PFCVS represent the AC peak. In case the voltage measured at PFCVS is greater than the threshold $V_{PFCVSacovp}$ for longer than the configurable blanking time t_{ACovp} the configured protection mode (auto-restart or latch) is entered.

ACOVP can be enabled or disabled by configuration using parameter EN_{ACovp}.

4.5.2.9 PFC bus undervoltage protection

Undervoltage detection of the PFC bus voltage is sensed at the PFCVS pin and acts as protection mechanism for the hybrid-flyback stage.

The bus voltage undervoltage protection compares the bus voltage with the voltage V_{busUVP} every t_{sample} whereas the value of V_{busUVP} is set to the minimum of $V_{CrUVPoffset} + V_{Cr,avg}$ and $1.5 \cdot V_{Cr,avg}$. The undervoltage protection is blanked with the configurable blanking time t_{busUVP} and is sampled with a time period t_{sample}.

Once the protection is triggered, the configured protection mode (latch, auto-restart or fast restart mode) is entered. It is possible to choose different reactions for the protection being triggered during start-up and normal operation.

4.5.2.10 PFC overcurrent protection

Once the voltage at pin PFCCS exceeds the overcurrent threshold $V_{PFCCSocp}$ for longer than the blanking time $t_{PFCCSocp}$ the PFC gate PFCGD is turned off. Afterwards, the ZCD signal or the PFC maximum period timeout signal initializes the next switching cycle. This protection mechanism is active in every switching cycle.

4.5.2.11 PFC CCM cycle protection

During CCM operation, the magnetizing current in the PFC choke does not decay to zero prior to switch turn on. Quasi-resonant oscillation is missing in the V_{PFCCS} signal before the maximum switching period timeout is reached that turns the transistor on. This turn-on event without ZCD oscillation is monitored to protect the PFC converter from continuous CCM operation. If the ZCD signal is missing for longer than the blanking time $t_{PFCCSccm}$ the protection is triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.12 Hybrid-flyback overcurrent protection

The hybrid-flyback overcurrent protection contains several detection functions, which protect the application when operating under output overcurrent conditions or when exceeding a primary side peak current (see Figure 21).

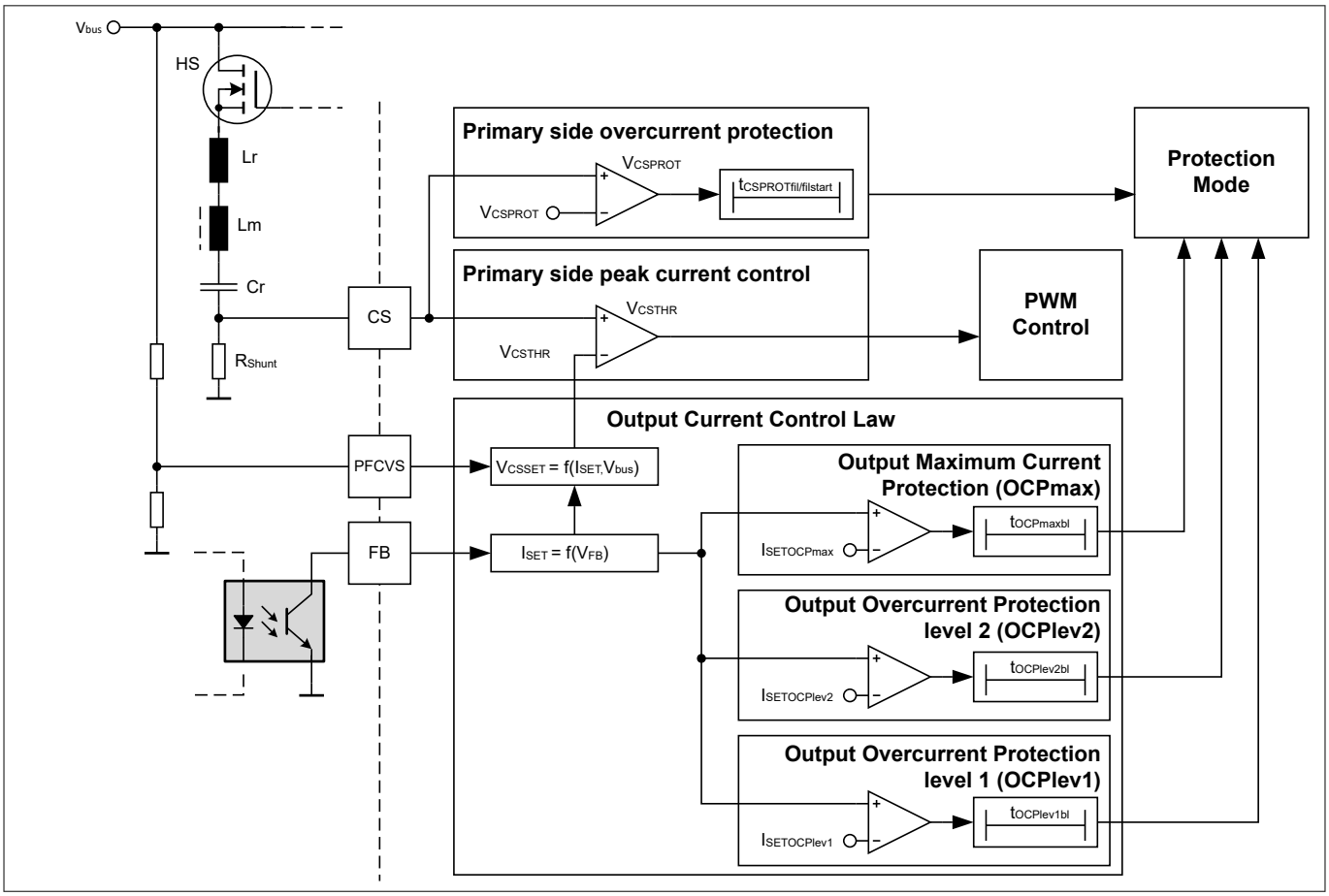

Figure 21 Overcurrent protection overview

4.5.2.12.1 Output overcurrent protection

The output overcurrent protection is implemented as a three level protection:

- Output overcurrent protection level 1
- Output overcurrent protection level 2
- Output maximum current protection

using different overcurrent level thresholds $I_{SETOCPlev1/lev2/max}$ and blanking times $t_{OCPlev1bl/lev2bl/maxbl}$.

The output overcurrent protection levels $I_{SETOCPlev1/lev2/max}$ are defined by the output current control law, whereas $I_{SETOCPmax}$ corresponds to the maximum output current level. Once the current set-point I_{SET} crosses the threshold levels a timer is started. The configured protection mode (auto-restart or latch) is entered when the timer reaches the thresholds $t_{OCPlev1bl/lev2bl/maxbl}$. The timer is reset when I_{SET} is dropping back below the thresholds.

Be aware, that once a higher output current corresponding to a current set point $I_{SET} > I_{SETOCPmax}$ is requested via V_{FB} control, the output current is kept limited. During this phase the output voltage is dropping because output current is higher than what is provided by the converter.

4.5.2.12.2 Primary side overcurrent protection CSPROT

V_{CSPROT} is a fixed threshold at CS pin and beyond the maximum operating range $V_{CSTHRmax}$. The CSPROT function is not blanked during the leading edge blanking time t_{HSleb}. Once exceeded the configured protection mode (auto-restart or latch) is entered.

In order to avoid false CSPROT events configurable blanking times $t_{CSPROTfilstart}$ and $t_{CSPROTfil}$ apply.

4.5.2.13 Output voltage protection

The IC provides two output voltage Vout protection mechanisms for output undervoltage and output overvoltage to ensure a reliable operation within a defined Vout operating range. The measurement is done at pin ZCD via the reflected voltage at the auxiliary winding of the transformer during the demagnetization phase when the LS switch is turned on (see Figure 22). Furthermore the zero-crossing detection during start-up phase is observed to detect short circuit conditions at the output.

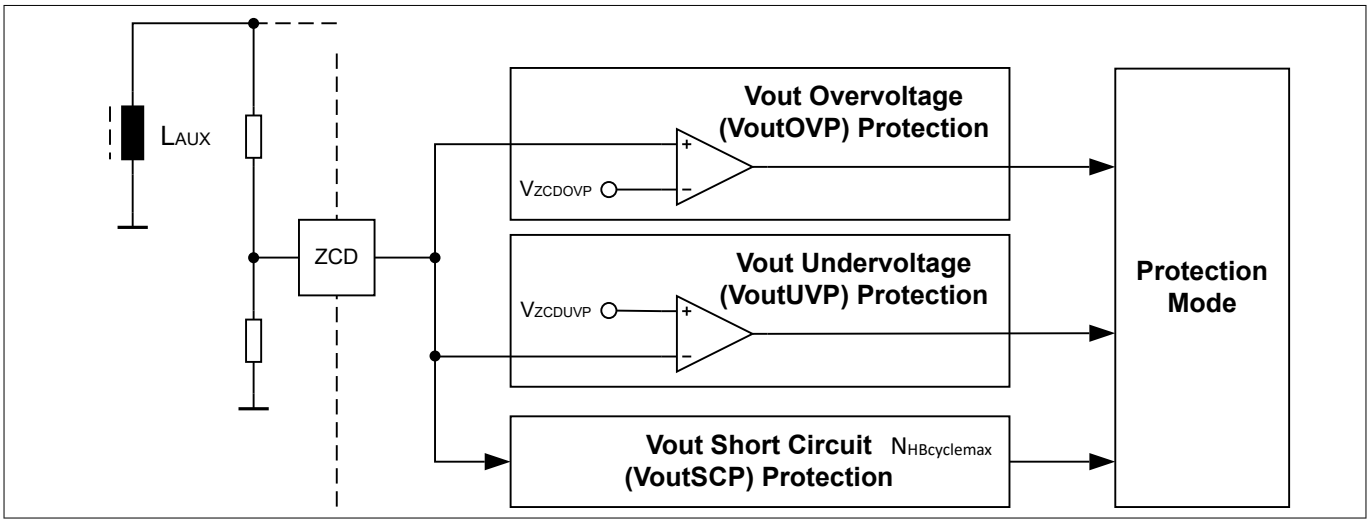

Figure 22 Output voltage protections

4.5.2.13.1 Vout overvoltage protection

The IC provides primary side output overvoltage detection via the voltage measured every switching cycle during the LS on-time at the ZCD-pin from the auxiliary transformer winding. Output overvoltage is detected when the reflected output voltage is exceeding the threshold V_{ZCDOVP} (corresponding to the configurable threshold V_{outOVP}) longer than the configurable blanking time $t_{outOVPbl}$. Once detected a protection mode is immediately triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.13.2 Vout undervoltage protection

Output undervoltage detection is detected via the voltage measured at the ZCD-pin. After the start-up is finished Vout undervoltage can triggered when the voltage measured at pin ZCD is dropping below the threshold V_{ZCDUVP}, which corresponds to the configurable threshold V_{outUVP}. Once detected the configured protection mode (auto-restart or latch) is entered.

In burst-mode operation, after wake-up from sleep, the voltage measured at pin ZCD might be distorted due to various reasons. In order to avoid mis-triggering the output undervoltage protection the detection can be blanked. The blanking time can be configured using the parameter $Config_{VoutUVPBM}$.

4.5.2.13.3 Vout short circuit protection

For a short circuit protection at the output, two different mechanisms are implemented. One is only active during start-up, the other one is meant for protection during active operation.

During start-up, the Vout short circuit protection limits the number of half-bridge switching cycles. After a start-up request only a maximum of $N_{HBcyclemax}$ consecutive half-bridge switching cycles without zero-crossing detection are allowed. If $N_{HBcyclemax}$ is exceeded, the (re-)start phase is stopped and the configured protection mode (prematurely auto-restart mode sleeping phase or latch) is entered.

During operation another Vout short circuit protection mechanism is active using two criteria. If the difference between the actual voltage V_{ZCD} and its internally averaged value V_{ZCDavg} is bigger than the internal threshold $\Delta V_{ZCDshort}$, an output short circuit protection is triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.14 CS pin short circuit protection

During Vout start-up a short circuit detection at CS pin is activated for the very first HS switch pulse to protect the application operating with a shortened R_{Shunt}.

4.5.2.15 FB pin start-up protection

During the start-up check phase, the voltage at pin FB is evaluated for error. The system will only start up in case $V_{FB} > V_{FBBMctrl}$. In case the system cannot be started due to too low voltage at pin FB the configured protection event with parameter $EV_{StartFBlow}$ will be triggered.

4.5.2.16 Hybrid-flyback open loop protection

The open control loop protection is using a similar method as the output short protection (see Chapter 4.5.2.13.3). Only in case of a saturated feedback voltage at FB, the reflected output voltage measured via ZCD pin is evaluated: If the difference between the actual voltage V_{ZCD} and its internally averaged value V_{ZCDavg} is bigger than the internal threshold ΔV_{ZCDolp}, which is related to the configurable output voltage threshold ΔV_{outolp}, an open loop protection is triggered and the configured protection mode (auto-restart or latch) is entered.

4.5.2.17 External overtemperature protection

The external overtemperature protection (ExtOTP) is based on measuring an external NTC thermistor at pin MFIO, see Figure 23. Once the external resistance is falling below the threshold $R_{MFIOOTPtrig}$ a protection mode is entered. The protection reaction can be configured. In case of auto-restart, a restart cycle can only take place in case the value of the the external resistance exceeding the threshold $R_{MFIOOTPrel}$. The auto-restart cycles after ExtOTP was triggered are counted. When the number of auto-restarts after external OTP events exceeds the threshold $N_{OTPevmax}$ latch mode is entered, too.

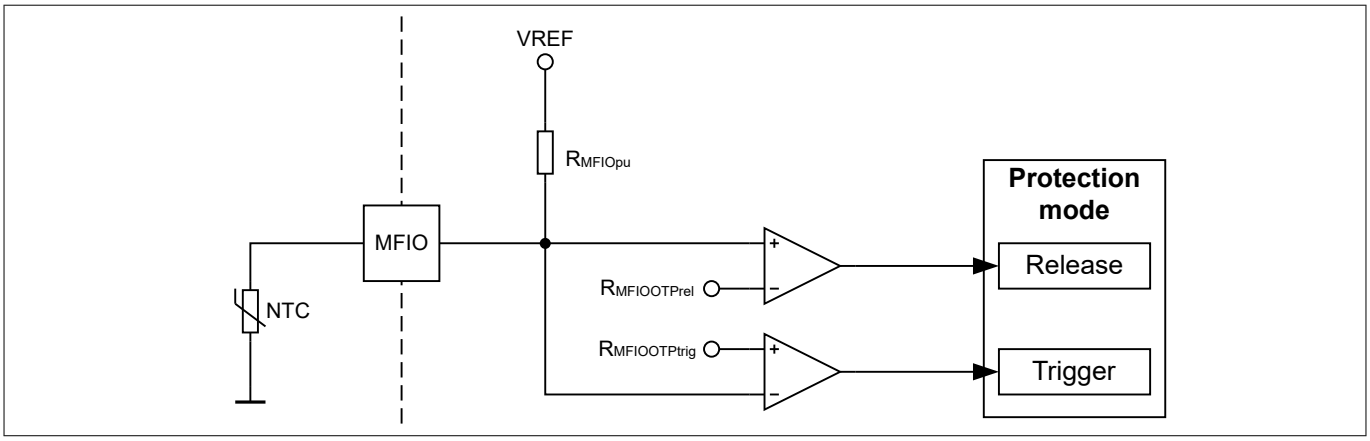

Figure 23 External overtemperature protection using NTC-thermistor at MFIO pin

4.5.2.18 Memory parity check

For memory integrity a parity check is continuously provided during operation. Once a parity error is detected the controller is reset and the configured protection mode (auto-restart mode or latch) is entered.

4.5.3 Error read-out at MFIO-pin

After a latch or auto-restart mode has been entered an error code showing which protection has been triggered, can be read out at pin MFIO.

5 Configuration

The configuration of the controller is supported by the GUI tool .dpVision provided by Infineon. This chapter gives an overview about the configurable parameters, which are programmable via the UART interface at MFIO pin. Chapter 5.1 shows the functional description and the parameter names used in .dpVision GUI tool. Furthermore the associated tolerance classes are assigned to the configurable typical parameters, which can be found in Chapter 5.2.

5.1 Configurable parameters and functions

The following tables show the IC configurable parameters and the default value which is programmed to the IC based on CSV-file version "CSV1005".

Notes:

1. *Every combination of parameter sets / configurations needs to be fully evaluated by a technical expert. Make sure that the used combination of parameters matches your application needs. It is the customers responsibility to make sure that the chosen parameters meet all requirements, including safety-related requirements.*
2. *Before using a parameter set, make sure that the system - including any programming / OTP burning hardware- is fully tested and working as expected.*
3. *Every parameter set is only valid for the dedicated evaluated hardware configuration, including PCB, Layout, used topology and all used electronic components (e.g. MOSFET, Transformer, ...)*

5.1.1 System settings

Table 3 System setting

Symbol	Description	Default value	Unit	Tolerance class
k_{PFCVS}	Ratio of resistor divider connected at PFCVS pin and bulk voltage	161.0		
I_{outnom}	Maximum nominal output current without overcurrent condition	5.0	A	
N	Transformer turns ratio of primary winding Np and secondary winding Ns, defined by Np/Ns	7.0		
V_{outnom}	Maximum nominal regulated output voltage	28.0	V	
L_p	Primary side magnetizing inductance (optional; if set to zero, value is calculated internally)	0	µH	

5.1.2 Supply management

Table 4 Supply management

Symbol	Description	Default value	Unit	Tolerance class
R_{HV}	External resistor connected to HV pin	51.0	kΩ	
$EN_{VCCcharge}$	Enable of HV cell charging during burst-mode	Enabled		

5.1.3 Start-up

Table 5 Start-up

Symbol	Description.	Default value	Unit	Tolerance class
V_{inbi}	Input peak voltage for brown-in	124.0	V	TC_I1 for I_{HVBI}
V_{busbi}	Bus voltage threshold for brown-in	120.0	V	TC_V1b
$V_{busACovp}$	Bus voltage threshold for AC overvoltage protection	435.0	V	TC_V1b
$N_{HBcyclemax}$	Maximum number of allowed half-bridge switching cycles without subsequent zero-crossing detection (ZCD) during ZCD search phase at Vout start-up	500		
$t_{startzcdto}$	Timeout for zero-crossing detection for generating next pulse only during ZCD search phase	50.0	µs	TC_T1
$t_{CSPROTfilstart}$	Blanking time of primary overcurrent protection CSPROT at start-up and 1st pulse in burst-mode	200.0	ns	TC_T1
$t_{CSPROTfil}$	Blanking time of primary overcurrent protection CSPROT	32.0	ns	TC_T1
$I_{MAGpos1st\%}$	Peak current of first HFB switching cycle during start-up phase	65.0	%	
$I_{SETstmax\%}$	Maximum target current set-point during start-up phase in percentage	100.0	%	

5.1.4 Hybrid-flyback operation

Table 6 Hybrid-flyback operation

Symbol	Description	Default value	Unit	Tolerance class
$t_{TRANSnom}$	LS switch on-time at the nominal output voltage and current	2.4	µs	
$t_{TRANSlimit}$	Enable limitation of LS switch on-time during energy transfer	Yes		
t_{deadLS}	Dead-time between HS pulse falling edge and LS pulse rising edge	150.0	ns	TC_T1
$t_{deadHSRVS}$	Dead-time between ZVS pulse falling edge and HS pulse rising edge in ZV-RVS mode during start-u	400.0	ns	TC_T1
t_{HSleb}	HS switch leading edge blanking (LEB) determining minimum on-time (blanking time of CSTHR)	300.0	ns	TC_T1
$t_{ZCDfilRVS}$	Filtering time between ZCD rising edge event and ZVS pulse rising edge in ZV-RVS mode operation	290.0	ns	TC_T1
V_{ZCDnom}	ZCD pin nominal voltage during LS pulse at V_{outnom}	2.559	V	

(table continues...)

Table 6 (continued) Hybrid-flyback operation

$t_{CSTHRfil}$	Blanking time of CSTHR events	0	ns	TC_T1
t_{CSPDC}	Propagation delay compensation time	200.0	ns	
$f_{swDCMmin}$	Minimum switching frequency limit during DCM operation	20.0	kHz	TC_T1
$V_{LSGDhigh}$	LS gate driver output voltage at high state	10.0	V	
$T_{CVzcdavg}$	Filter time constant on ZCD pin voltage measurement	7		
$t_{LS2ZCDmax}$	Target delay time delay from LSGD falling edge to ZCD falling edge for the corner $V_{bus} = V_{Cr}$	300.0	ns	
$t_{LS2ZCDmin}$	Target delay time delay from LSGD falling edge to ZCD falling edge for the corner $V_{bus} = V_{busACovp}$ and $V_{Cr} = N^*_{VoutCRM2RVS}$	65.0	ns	
t_{ZCD2HS}	Delay from falling edge ZCD and HS pulse rising edge	180.0	ns	TC_T1
$I_{MAGnegnom\%}$	Target negative magnetizing current level in percent required to achieve ZVS	15.0	%	
C_{Oeq}	Equivalent capacitance of total capacitance associated to half-bridge node	500.0	pF	
t_{ZVSmin}	Minimum ZVS pulse width during ZV-RVS mode operation	600.0	ns	TC_T1
$t_{TRANSRVS0V\%}$	LS switch on-time in ZV-RVS mode for V_{out} = 0V in percentage of $t_{TRANSnom}$ for t_{TRANS} modulation depending on output voltage	220.0	%	
$V_{FBOPmin}$	Minimum FB feedback voltage	0.4	V	TC_V4a
R_{FBpu}	Pull-up resistor configuration at pin FB	9		Tolerance ±20%
$I_{MAGposRVSmax\%}$	Minimum peak current in ZV-RVS mode for V_{ZCDnom} in percentage	80.0	%	
$I_{MAGposRVS0V\%}$	Minimum peak current in ZV-RVS mode for V_ZCD = 0V in percentage	30.0	%	
$I_{MAGposRVSabsmin\%}$	Absolute minimum peak current after hitting minimum DCM switching frequency in percentage	30.0	%	
$I_{MAGposhysteresisCRM2RVS\%}$	Offset of peak current used for change from CRM to ZV-RVS mode in percentage of peak current	10.0	%	
$V_{outRVS2CRM}$	Output voltage threshold for switching over from ZV-RVS mode to CRM	10.5	V	
$V_{outCRM2RVS}$	Output voltage threshold for switching over from CRM to ZV-RVS mode	11.0	V	
V_{FBBMen}	Burst mode entry FB feedback voltage threshold	0.47	V	TC_V4a
$N_{BMprepulse}$	Number of precharge pulses	5		
$t_{BMprepulse}$	Pulse width to precharge the bootstrap capacitor after a period longer than $t_{BMslpthrpp}$	0.66	µs	TC_T1

(table continues...)

Table 6 (continued) Hybrid-flyback operation

$t_{BMppswmax}$	Maximum precharge pulse period	3.0	µs	TC_T1
$t_{BMslpthrpp}$	Burst sleep time threshold for enabling precharge pulse	1.0	ms	
$N_{BMWakeupvalley}$	Target valley number at burst mode wakeup until loop control takes over	3		
$V_{busJitteren}$	Bus voltage jitter enable threshold	437.0	V	TC_V1b
$d_{Jitterspread\%}$	Frequency jitter spread on a percentage base of switching frequency	6.3	%	
$t_{Jitterstpdel}$	Time delay for next frequency jitter step	1.0	ms	TC_T3
$I_{MAGnegJitter\%}$	Jitter spread of negative magnetizing current	0.0	%	
$T_{JitterstpdelRVS}$	Time delay for next frequency jitter step based on time period in ZV-RVS mode	1.3	ms	TC_T3

5.1.5 PFC operation

Table 7 PFC operation

Symbol	Description	Default value	Unit	Tolerance class
$EN_{PFCoperation}$	Enable PFC operation (if disabled, PFC is completely and permanently disabled)	Yes		
$t_{PFCCSleb}$	Leading edge blanking time of PFCCS	260.0	ns	TC_T1
$t_{PFCCSzcd}$	PFC ZCD filter and delay time for comparator low threshold	190.0	ns	
$t_{PFCCSzcdreset}$	PFC ZCD filter and delay time for comparator high threshold	175.0	ns	
$t_{PFCCSzcdblk}$	PFC ZCD blanking time after PFCGD off	500.0	ns	
$t_{PFConmin}$	Minimum PFC on-time	0.26	µs	TC_T1
$t_{PFConmax}$	Maximum PFC on-time	12.0	µs	TC_T1
$f_{swPFCmin}$	Minimum PFC switching frequency	35.0	kHz	
$f_{swPFCmax}$	Maximum PFC switching frequency	250.0	kHz	
$f_{swQRmax}$	Lower PFC switching frequency threshold leading to valley transition	75.0	kHz	
$f_{swQRmax}$	Lower PFC switching frequency threshold leading to valley transition	155.0	kHz	
$N_{PFCvalleymax}$	Maximum valley number during PFC QRM	8		
$t_{QRblkinc}$	Blanking time before incrementing the valley number	2.2	ms	TC_T3
$t_{QRblkdec}$	Blanking time before decreasing the valley number	2.2	ms	TC_T3

(table continues...)

Table 7 (continued) PFC operation

$CFG_{PFContime}$	Configuration for initial soft-start on-time and on-time threshold for pulse skipping	Enhanced		
$CFG_{PFCvalley1BMwu}$	Configuration of PFC valley number after burst-mode wake-up	No		
PFC_{CoefA}	PFC regulator PI-filter coefficient A	256.0		
PFC_{CoefB}	PFC regulator PI-filter coefficient B	822.0		
PFC_{CoefT1}	PFC regulator T1-filter coefficient	5.0		

5.1.6 PFC bus voltage target settings

Table 8 PFC bus voltage target settings

Symbol	Description	Default value	Unit	Tolerance class
$P_{PFCenable}$	Output power level at which the PFC is enabled	60	W	
$P_{PFCdisable}$	Output power level at which the PFC is disabled	50	W	
$t_{PFCblkdisable}$	Blanking time for PFC disable	0.0	ms	TC_T3
$V_{bustarget2Vcroffset}$	Offset of V_{bus} target voltage setting over 2 x V_{Cr}	50.0	V	
$V_{busPFCenable2Vcroffset}$	Offset on V_{bus} for PFC enable condition	0.0	V	
$V_{bustargetmax}$	Maximum PFC bus target voltage	400.0	V	TC_V1b
$V_{bustargetmin}$	Maximum PFC bus target voltage	130.0	V	TC_V1b
$V_{bustargetVacpkoffset}$	Offset of V_{bus} target voltage setting over V_{acpk}	80.0	V	
$V_{ACpkPFCdisablehysteresis}$	Hysteresis on AC peak voltage to disable PFC	110.0	V	

5.1.7 Protections

Table 9 Protections

Symbol	Description	Default value	Unit	Tolerance class
t_{ARM}	Auto-restart time	3.0	s	TC_T2
EV_{VCCOVP}	Disable and reaction event to VCC overvoltage protection	Auto-restart		
V_{inbo}	Input peak voltage threshold for brown-out protection	106.0	V	
EN_{ACovp}	Enable AC overvoltage protection	Enabled		
EV_{ACovp}	Reaction event on AC overvoltage protection	Auto-restart		
t_{ACovp}	AC overvoltage protection blanking time	400.0	µs	TC_T3

(table continues...)

Table 9 (continued) Protections

$EV_{startFBlow}$	Reaction event to low FB-voltage at start-up	Auto-restart		
$EV_{VoutSTTOP}$	Reaction event to Vout start-up timeout protection	Auto-restart		
$t_{startto}$	Maximum allowed start-up time until start drop of feedback voltage	50.0	ms	TC_T3
$EV_{PFCSTTOP}$	Reaction event to PFC soft-start timeout	Auto-restart		
V_{busovp}	PFC bus voltage first level overvoltage protection (OVP1) threshold	424.7	V	TC_V1b
$V_{busovp1res}$	PFC bus voltage threshold to resume switching after OVP1	400.0	V	TC_V1b
EV_{busUVP}	Reaction to Vbus undervoltage protection	Auto-restart		
$EV_{busUVPst}$	Reaction to Vbus undervoltage protection during start-up	Auto-restart		
$V_{CrUVPoffset}$	Offset of dynamic PFC bus undervoltage protection	100.0	V	
t_{busUVP}	Blanking time of bus undervoltage protection (PFCUVP)	0.4	ms	TC_T3
$V_{busPFCtonmaxUVPoffset}$	Difference of Vbus voltage level to bus undervoltage protection level for enabling max. PFC on-time	20.0	V	
EV_{PFCCCM}	Reaction event for CCM protection	Auto-restart		
$t_{PFCCSCCM}$	CCM protection blanking time	2.0	ms	TC_T3
$EV_{OCPlev1}$	Reaction to output overcurrent protection level 1	Auto-restart		
$I_{SETOCPlev1\%}$	Current set-point threshold in percentage of nominal set-point for output overcurrent protection level 1	125.0	%	
$t_{OCPlev1bl}$	Output overcurrent protection level 1 blanking time	12.0	s	TC_T4
$EV_{OCPlev2}$	Reaction to output overcurrent protection level 2	Auto-restart		
$I_{SETOCPlev2\%}$	Current set-point threshold in percentage of nominal set-point for output overcurrent protection level 2	140.0	%	
$t_{OCPlev2bl}$	Output overcurrent protection level 2 blanking time	1000.0	ms	TC_T3
EV_{OCPmax}	Reaction event for output maximum overcurrent protection	Auto-restart		
$I_{SETOCPlevmax\%}$	Current set-point in percentage of nominal set-point for output maximum current limitation	150	%	
$t_{OCPlevmaxbl}$	Maximum overcurrent limitation blanking time	6.0	ms	TC_T3

(table continues...)

Table 9 (continued) Protections

EV_{CSPROT}	Reaction event primary side overcurrent protection CSPROT	Latch		
EV_{OLP}	Reaction event to open-loop protection	Latch		
ΔV_{outolp}	Threshold for difference in output voltage for open loop protection	28.0	V	TC_V3b for the voltage sampled at pin ZCD
EV_{CSSCP}	Reaction event to CS pin short protection	Auto-restart		
$EV_{VoutOVP}$	Reaction event for Vout overvoltage protection	Latch		
V_{outOVP}	Threshold for Vout overvoltage protection	30.0	V	
$t_{outOVPbl}$	Vout overvoltage protection blanking time	1.0	ms	TC_T3
$EV_{VoutUVP}$	Reaction event for Vout undervoltage protection	Latch		
V_{outUVP}	Threshold for Vout undervoltage protection	2.5	V	TC_V3b
$CFG_{VoutUVPBM}$	Configuration of blanking for output undervoltage protection after burst-mode wake-up	Opt. C		
$EV_{VoutSCP}$	Reaction event to Vout short-circuit protection	Latch		
$EV_{STnoZCD}$	Reaction event to start-up no-ZCD protection	Auto-restart		
$\Delta V_{outshort}$	Threshold for difference in output voltage for output short detection	28.0	V	
EV_{OTP}	Reaction on external overtemperature protection	Auto-restart		
$R_{MFIOOTPtrig}$	Overtemperature protection trigger threshold	7.7	kΩ	TC_R1
$R_{MFIOOTPrel}$	Overtemperature protection release threshold	51.4	kΩ	TC_R2
$N_{OTPevmax}$	External overtemperature protection number of allowed triggered events before entering latch mode	2		
EV_{WDOG}	Reaction event to watchdog timer protection	Latch		
EV_{MEMPAR}	Reaction event to memory parity check	Auto-restart		

5.2 Tolerance classes for configurable parameters

The are several configurable parameters available, having different tolerance classes. Parameters defining events, configuration registers, digital numbers or constants are not assigned to tolerance ranges. The available tolerance classes are named with TC_xxx and listed in the following Table 28. Described is how minimum and maximum tolerance values can be derived for the typical value X_{typ} of the configurable parameters. The timing related parameters refer to digital events and pulses inside the IC.

Table 10 Tolerance classes

Tol.-Class	Description	Min. value	Max. value
TC_T1	Timing parameter below 1215ns (based on main clock t_{MCLK} = 15.8 ns(typ.))	t_{typ} x 0.95 - 15.8ns	t_{typ} x 1.05 + 15.8ns
	Timing parameter above 1215ns (based on main clock t_{MCLK} = 15.8 ns(typ.))	t_{typ} x 0.937	t_{typ} x 1.063
	Frequency parameter below 500kHz (based on main clock t_{MCLK} = 15.8 ns(typ.))	F_{typ} x 0.937	F_{typ} x 1.063
TC_T2	Timing parameter based on stand-by clock (t_{STBCLK} = 10 µs(typ.))	t_{typ} x 0.90	t_{typ} x 1.12
TC_T3	Timing parameter (integer multiple of 0.1ms) based on slow task period (t_{STBCLK} = 0.12 ms(typ.)), does not apply in case of burst mode operation.	t_{typ} x 0.937 - 0.13ms	t_{typ} x 1.063 + 0.13ms
TC_T4	Timing parameter (integer multiple of 5ms) based on very slow task period (t_{STBCLK} = 5 ms(typ.)), does not apply in case of burst mode operation.	t_{typ} x 0.937 - 5.5ms	t_{typ} x 1.063 + 5.5ms
TC_V1a	Voltage threshold at pin PFCVS	(V_{VStyp} x 0.994) - 0.099V	(V_{VStyp} x 1.006) + 0.099V
TC_V1b	Voltage threshold at pin PFCVS	(V_{VStyp} x 0.994) - 0.040V	(V_{VStyp} x 1.006) + 0.040V
TC_V2	Voltage threshold for CSTHR comparator at pin CS	$V_{CSTHRtyp}$ - 0.034V	$V_{CSTHRtyp}$ + 0.034V
TC_V3a	Voltage threshold at pin ZCD	(V_{ZCDtyp} x 0.995) - 0.091V	(V_{ZCDtyp} x 1.005) + 0.091V
TC_V3b	Voltage threshold at pin ZCD	(V_{ZCDtyp} x 0.995) - 0.024V	(V_{ZCDtyp} x 1.005) + 0.024V
TC_V3c	Voltage change threshold at pin ZCD	V_{ZCDtyp} - 0.077V	V_{ZCDtyp} + 0.077V
TC_V4	Voltage threshold at pin FB	(V_{FBtyp} x 0.984) - 0.084V	(V_{FBtyp} x 1.016) + 0.084V

(table continues...)

Table 10 (continued) Tolerance classes

Tol.-Class	Description	Min. value	Max. value
TC_V4a	Voltage threshold at pin FB	(V_{FBtyp} x 0.984) - 0.026V	(V_{FBtyp} x 1.016) + 0.026V
TC_I1	Current threshold at pin HV	(I_{HVtyp} x 0.98) - 0.004mA	(I_{HVtyp} x 1.02) + 0.004mA

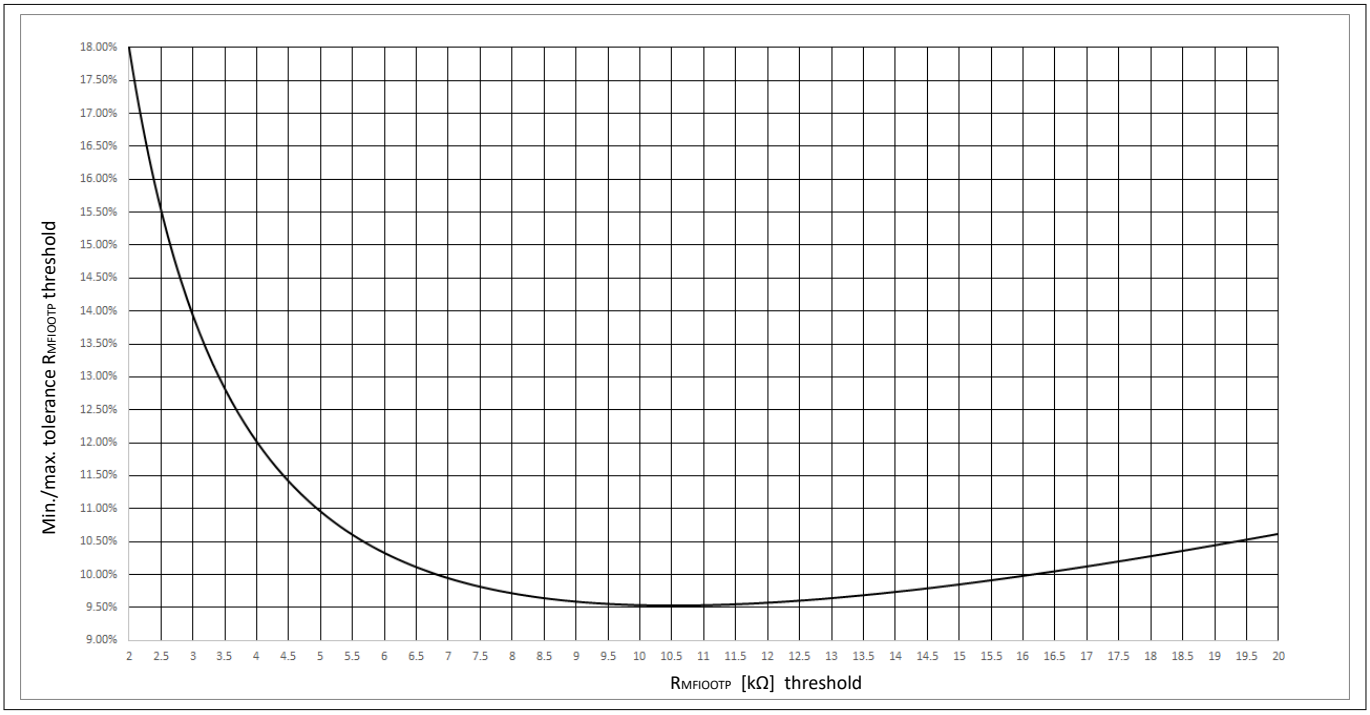

Figure 24 Tolerance class TC_R1 for resistor threshold at pin MFIO

5 Configuration

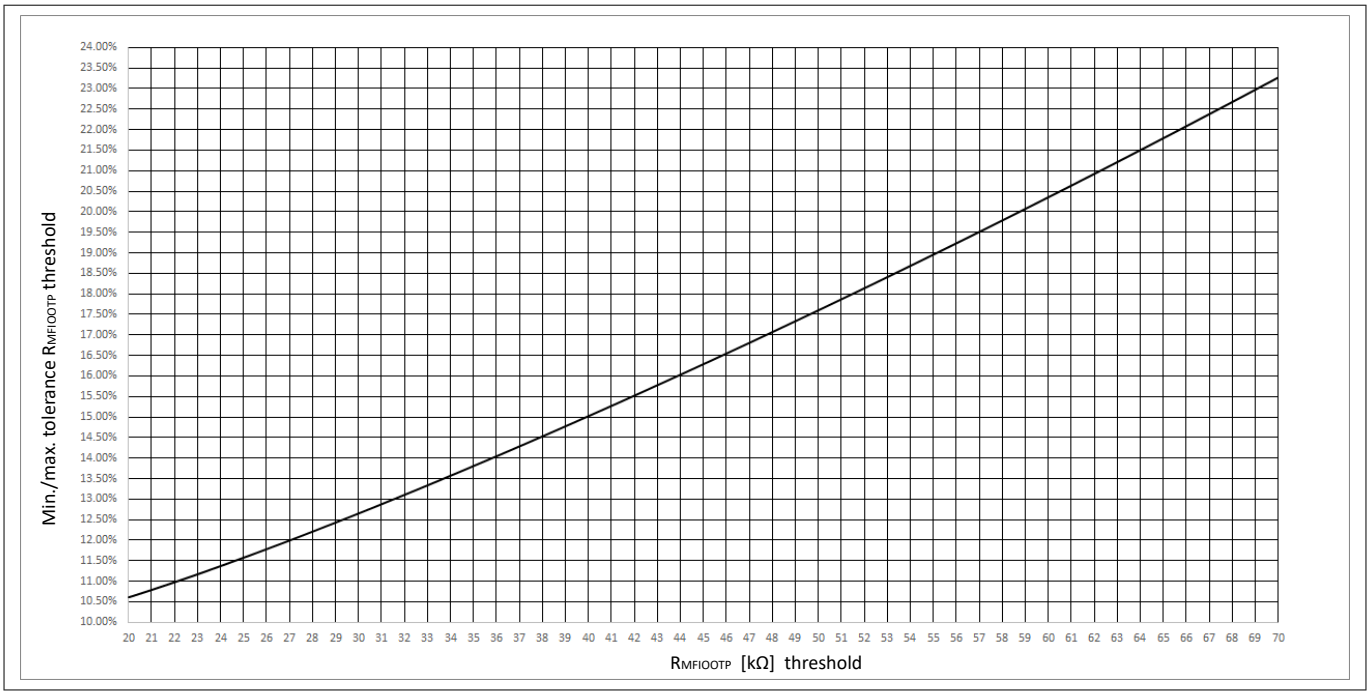

Figure 25 Tolerance class TC_R2 for resistor threshold at pin MFIO

Timing parameters relating to external switch events have an offset from system delays that is not included in TC_T1

6 Electrical characteristics

All signals are measured with respect to ground GND pin. The voltage levels are valid if other ratings are not violated.

Figure 26 illustrates the definition for the voltage and current parameters used in this data sheet.

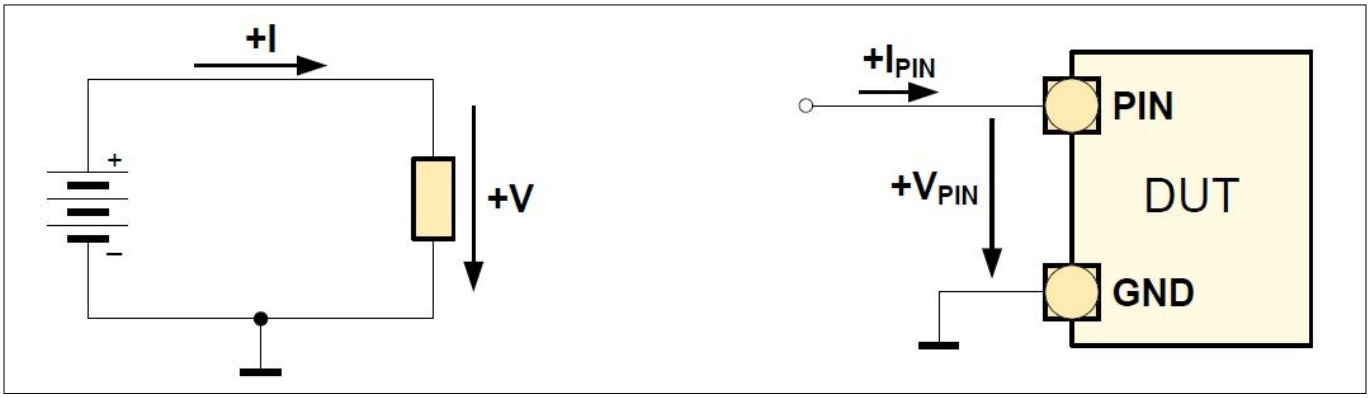

Figure 26 Voltage and current definitions

6.1 Absolute maximum ratings

Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for given periods may affect device reliability. Maximum ratings are absolute ratings; exceeding anyone of these values may cause irreversible damage to the device.

Table 11 Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at pin HV	V_{HV}	–0.3		600	V	1)
Maximum current into pin HV	I_{HV}	-		10	mA	1)
Voltage at pin VCC	V_{VCC}	–0.5		26	V	1)
Voltage at pin MFIO	V_{MFIO}	–0.5		3.6	V	1)
Voltage at pin PFCVS	V_{PFCVS}	–0.5		3.6	V	1)
Voltage at pin FB	V_{FB}	–0.5		3.6	V	1)
Voltage at pin ZCD	V_{ZCD}	–0.5		3.6	V	1)
Maximum negative transient voltage at pin ZCD	$-V_{ZCDN\_TR}$	-		1.5	V	pulse < 500ns
Maximum permanent negative clamping current for pin ZCD	$-I_{ZCDCLN\_DC}$	-		2.5	mA	RMS
Maximum transient negative clamping current for pin ZCD	$-I_{ZCDCLN\_TR}$	-		10	mA	pulse < 500ns
Voltage at pin CS	V_{CS}	–0.5		3.6	V	1)

(table continues...)

1 Permanently applied as DC value.

Table 11 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum negative transient voltage at pin CS	$-V_{CSN\_TR}$	-		3	V	pulse < 500ns
Maximum permanent negative clamping current for pin CS	$-I_{CSCLN\_DC}$	-		2.5	mA	RMS
Maximum transient negative clamping current for pin CS	$-I_{CSCLN\_TR}$	-		10	mA	pulse < 500ns
Maximum permanent positive clamping current for pin CS	I_{CSCLP_DC}	-		2.5	mA	RMS
Maximum transient positive clamping current for pin CS	I_{CSCLP_TR}	-		10	mA	pulse < 500ns
Voltage at pin PFCCS	V_{PFCS}	–0.5		3.6	V	[1]
Maximum negative transient voltage at pin PFCCS	$-V_{PFCCSN\_TR}$	-		3	V	pulse < 500ns
Maximum permanent negative clamping current for pin PFCCS	$-I_{PFCCSCLN\_DC}$	-		2.5	mA	RMS
Maximum transient negative clamping current for pin PFCCS	$-I_{PFCCSCLN\_TR}$	-		10	mA	pulse < 500ns
Maximum permanent positive clamping current for pin PFCCS	$I_{PFCCSCLP\_DC}$	-		2.5	mA	RMS
Maximum transient positive clamping current for pin PFCCS	I_{CSCLP_TR}	-		10	mA	pulse < 500ns
Voltage at pin LSGD	V_{LSGD}	–0.5		V_{VCC}+ 0.3	V	Limited by internal clamping
Voltage at pin PFCGD	V_{PFCGD}	- 0.5		V_{VCC}+ 0.3	V	
Voltage at pin HSGND	V_{HSGND}	-650		650	V	referred to GND
Voltage at pin HSVCC	V_{HSVCC}	–0.5		26	V	referred to HSGND
Voltage at pin HSGD	V_{HSGD}	–0.5		V_{HSVCC} +0.3	V	referred to HSGND
Slew-rate for floating high-side domain	dV_{HS}/dt	–50		50	V/ns	
Junction operation temperature	T_J	–40		125	°C	
Storage temperature	T_S	–55		150	°C	
Maximum power dissipation	P_{TOT}	-		0.63	W	T_A = 50 °C, T_J = 125 °C
Soldering temperature	T_{Sold}	-		260	°C	[2] Wave soldering

(table continues...)

1 Permanently applied as DC value.
2 According to JESD22-A111

Table 11 (continued) Absolute maximum rating

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD HBM capability	V_{HBM}	-		2000	V	[3] Human body model
ESD CDM capability	V_{CDM}	-		500	V	[4] Charged device model
Latch-up capability	I_{LU}	-		150	mA	[5] Pin voltages acc. to abs. max. rating

6.2 Package Characteristics

Table 12 Package characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance from junction to ambient	R_{thJA}	-		119	K/W	JEDEC 1s0p
Creepage distance between HV and HSxxx to GND-related pins	D_{crp}	2.1		-	mm	

6.3 Operating conditions

The table below shows the operating range, in which the electrical characteristics shown in the next chapter are valid.

Table 13 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction operation temperature	T_J	-25		125	°C	
Voltage at pin HV	V_{HV}	–0.3		600	V	
External voltage at pin VCC	V_{VCC}	11		24	V	Max. value needs to consider internal power losses
Voltage at pin MFIO	V_{MFIO}	–0.3		3.3	V	
Voltage at pin FB	V_{FB}	–0.3		3.3	V	
Voltage at pin ZCD	V_{ZCD}	–0.3		3.3	V	
Voltage at pin CS	V_{CS}	–0.3		3.3	V	

(table continues...)

3 According to ANSI/ESDA/JEDEC JS-001
4 According to JESD22-C101
5 According to JESD78, 85 °C (Class II) temperature

Table 13 (continued) Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Total maximum current out of pins FB and MFIO	$-I_{FB}$-I_{MFIO}	-		0.63	mA	During sleep phase in burst mode
Voltage at pin LSGD	V_{LSGD}	–0.3		V_{VCC} + 0.3	V	Internally clamped at $V_{LSGDhigh}$
Maximum low state output reverse current at pin LSGD	$-I_{LSGDLREV}$	-		100	mA	[6] Applies if V_{LSGD} < 0 V and driver at low state
Voltage at pin HSGD	V_{HSGD}	–0.3		V_{HSVCC} + 0.3	V	Internally clamped at $V_{HSGDhigh}$
Maximum low state output reverse current at pin HSGD	$-I_{HSGDLREV}$	-		100	mA	Applies if V_{HSGD} < 0 V and driver at low state
Voltage at pin HSVCC	V_{HSVCC}	10		24	V	Referred to HSGND
Voltage at pin HSGND	V_{HSGND}	–0.3		600	V	
UART Baudrate at pin MFIO	t_{BD}	10k		115k	Bd	
Voltage at pin PFCVS	V_{PFCVS}	–0.3		3.3	V	
Voltage at pin PFCCS	V_{PFCCS}	–0.3		3.3	V	
Voltage at pin PFCGD	V_{PFCGD}	–0.3		V_{VCC} + 0.3	V	Internally clamped at $V_{PFCGDhigh}$

6.4 Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature. Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is VCC = 14.0 V if not otherwise specified.

6.4.1 High voltage (HV pin)

Table 14 Electrical characteristics of HV-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HV VCC charge current capability	$I_{HVchargeVCC}$	2.4	5.0	7.5	mA	[7] V_{VCC} = 1 V, V_{HV} = 30 V; Peak current limited in application by external resistor

(table continues...)

6 Assured by design.
7 Max. peak charge current will be limited in the application by an external resistor connected to HV pin.

Table 14 (continued) Electrical characteristics of HV-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum leakage current at HV pin	I_{HVLK}	-	-	10	µA	V_{HV} = 600 V, HV start-up cell disabled
Brown-in timeout	t_{HVbito}	-	20	-	ms	I_{HVbi} > 0 mA
Brown-in timeout	t_{HVbito}	-	2	-	ms	I_{HVbi} = 0 mA

6.4.2 Power supply (VCC pin)

Table 15 Electrical characteristics of power supply (VCC pin)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Turn-on threshold	V_{VCCon}	19.0	-	22.0	V	Rising slope
Turn-off threshold	V_{VCCoff}	7.98	-	8.82	V	Falling slope, IC not in auto-restart or latch mode
Turn-off threshold	V_{VCCoff}	2.90	-	5.70	V	Falling slope, IC in auto-restart or latch mode
Threshold to activate HV cell for VCC-supply during burst mode	$V_{VCCslpHVon}$	9.97	10.5	11.03	V	Falling slope
UVOFF current	$I_{VCCUVOFF}$	-	20	40	µA	V_{VCC} < $V_{VCCoff(min)}$ − 0.3 V
Supply current	$I_{VCCopnm}$	-	11	14.5	mA	Without gate driver gate charge losses and during brown-in phase
Quiescent current during burst mode power saving-phase	$I_{VCCBMpsm0}$	-	0.7	3.4	mA	Burst mode entered; pin MFIO and FB open
Quiescent current during bang-bang mode	I_{VCCBB}	-	0.32	0.58	mA	Protection mode entered; pin MFIO and FB open
Overvoltage protection threshold	V_{VCCOVP}	22.0	23.0	24.0	V	
Overvoltage protection blanking time	t_{VCCOVP}	-	1.0	-	ms	

6.4.3 Floating HS domain (HSGND, HSVCC and HSGD pin)

Table 16 Electrical characteristics of HS domain pins

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HSVCC turn-on threshold	$V_{HSVCCon}$	8.7	9.2	9.7	V	Rising slope
HSVCC turn-off threshold	$V_{HSVCCoff}$	6.2	6.7	7.2	V	Falling slope
HSVCC idle current	$I_{HSVCCidle}$	-	0.3	0.8	mA	Without gate driver gate charge losses, VHSVCC = 14 V
HSGD enabling delay time after HSVCC voltage is exceeding turn-on threshold	$t_{HSGDendel}$	-	2.3	4.1	µs	V_{HSVCC} = 11 V
HSGD voltage at high state	$V_{HSGDhigh}$	10	11	12	V	I_{HSGD} = –20 mA
HSGD voltage at active shutdown	$V_{HSGDaSD}$	-	25	200	mV	I_{HSGD} = 20 mA, V_{HSVCC} = 5 V
HSGD peak source current	$-I_{HSGDpksrc}$	130	-	-	mA	
HSGD peak sink current	$I_{HSGDpksnk}$	450	-	-	mA	
HSGD driver output low impedance	R_{HSGDLS}	-	-	5	Ω	I_{HSGD} = 100 mA

6.4.4 Bus voltage sensing (PFCVS pin)

Table 17 Electrical characteristics of PFCVS-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	$I_{PFCVSlk}$	–0.2	-	0.2	µA	0 V < V_{PFCVS} < 2.9 V
Dynamic voltage range	V_{PFCVS}	0.13	-	2.75	V	
Second level overvoltage protection (OVP2) threshold	$V_{PFCVSovp2}$	2.7	2.8	2.9	V	
PFC soft-start timeout	$t_{startPFC}$	-	500	-	ms	

6.4.5 PFC current sense and zero crossing detection (PFCCS pin)

Table 18 Electrical characteristics of PFCCS pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent protection (OCP) threshold	$V_{PFCCSocp}$	605	638	671	mV	
Overcurrent protection (OCP) blanking time	$t_{PFCCSocp}$	37.5	47.4	58.1	ns	
ZCD comparator logic "0" threshold	$V_{PFCCSzcd}$	0.42	0.54	0.66		
ZCD comparator logic "1" threshold	$V_{PFCCSzcdreset}$	1.41	1.53	1.65	V	

6.4.6 Hybrid-flyback zero crossing detection (ZCD pin)

Table 19 Electrical characteristics of ZCD pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{ZCDlk}	–10	-	10	µA	V_{ZCD} = 0 V / 3.0 V
Maximum pin voltage threshold for Vout overvoltage protection	$V_{ZCDOVPmax}$	-	2.75	-	V	
Zero-crossing detection threshold	V_{ZCDTHR}	15	40	70	mV	Falling slope
Input voltage negative clamping	$-V_{ZCDCLN}$	140	180	220	mV	

6.4.7 Multifunctional input and output (MFIO pin)

Table 20 Electrical characteristics of MFIO-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull-up resistor	R_{MFIOpu}	8.8	11	13.2	kΩ	8)
Open circuit output voltage	V_{MFIOoc}		V_{REF}		V	8)
Input high current with active weak pull-down	$-I_{MFIOhpd}$	90	-	300	uA	Measured at min. V_{MFIOIH}
Leakage current	I_{MFIOlk}	-5	-	1	uA	V_{MFIO} = 0 V / 3.0 V
Input capacitance	C_{MFIOIN}	-	-	10	pF	
Input threshold for logic “0”	V_{MFIOIL}	-	-	1	V	8)
Input threshold for logic “1”	V_{MFIOIH}	2	-	-	V	8)
Output voltage for logic “0”	V_{MFIOOL}	-	-	0.8	V	8) I_{MFIOOL} = 2 mA
Output voltage for logic “1”	V_{MFIOOH}	2.2	-	-	V	8) I_{MFIOOH} = –2 mA
Maximum output sink current	I_{MFIOOL}	-	-	2	mA	8)
Maximum output source current	$-I_{MFIOOH}$	-	-	2	mA	8)
Output rise time (0 → 1)	$t_{MFIOrise}$	-	-	25	ns	20 pF load
Output fall time (1 → 0)	$t_{MFIOfall}$	-	-	25	ns	20 pF load

6.4.8 Hybrid-flyback current sensing (CS pin)

Table 21 Electrical characteristics of CS-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Leakage current	I_{CSlk}	–10	-	10	µA	0 V < VCS < 2.8 V

(table continues...)

8 During active phase

Table 21 (continued) Electrical characteristics of CS-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum operating current range	$V_{CSTHRmax}$	394	426	458	mV	
CSTHR propagation delay	$t_{CSTHRpd}$	121	213	305	ns	input signal slope, dVCS/dt = 150 mV/µs
CSPROT threshold	V_{CSPROT}	550	600	650	mV	

6.4.9 Hybrid-flyback output feedback (FB pin)

Table 22 Electrical characteristics of FB-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Open circuit output voltage	V_{FBoc}	3.04	3.2	3.36	V	
Threshold maximum usable range	$V_{FBOPmax}$	-	-	2.428	V	
Burst mode wake-up threshold	$V_{FBBMctrl}$	510	580	610	mV	During sleep phase in burst mode

6.4.10 Low-side gate driver (LSGD pin)

Table 23 Electrical characteristics of LSGD-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltage at active shutdown	$V_{LSGDaSD}$	-	-	1.6	V	I_{LSGD} = 5 mA, V_{VCC} = 5 V
Peak sink current	$I_{LSGDpksnk}$	500	-	-	mA	V_{LSGD} = 4.0 V
Peak source current	$-I_{LSGDpksrc}$	-	120	-	mA	
Driver output low impedance	R_{LSGDLS}	-	-	7.0	Ω	I_{LSGD} = 100 mA

6.4.11 PFC gate driver (PFCGD pin)

Table 24 Electrical characteristics of PFCGD-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal output high voltage	$V_{PFCGDhigh}$	9.9	10.5	11.1	V	I_{PFCGD} = –20 mA
Voltage at active shutdown	$V_{PFCGDaSD}$	-	-	1.6	V	I_{PFCGD} = 5 mA, V_{VCC} = 5 V
Peak sink current	$I_{PFCGDpksnk}$	800	-	-	mA	V_{PFCGD} = 4.0 V

(table continues...)

Table 24 (continued) Electrical characteristics of PFCGD-pin

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak source current	$-I_{PFCGDpksrc}$	-	360	-	mA	
Driver output low impedance	$R_{PFCGDLS}$	-	-	4.4	Ω	I_{PFCGD} = 100 mA

6.4.12 Central control functions

Table 25 Electrical characteristics of central control functions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDP power supply	V_{VDDP}	3.04	3.2	3.36	V	
VREF reference voltage	V_{VREF}	2.391	2.428	2.465	V	
Main clock oscillation period time base	t_{MCLK}	15	15.8	16.6	ns	
Stand-by clock oscillation period time base	t_{STBCLK}	9	10	11.2	µs	
Slow task period time base	$t_{SLWTASK}$	111	120	129	µs	
Very slow task period time base	$t_{VSLWTASK}$	4.68	5	5.32	ms	
Sampling time period	t_{sample}		$t_{SLWTASK}$		µs	
Restart step time base for auto-restart mode	$t_{ARMbase}$	270	300	336	ms	Base for configurable auto-restart time t_{ARMslp} when auto-restart mode entered
Limited maximum change in on-time control for HS switch during CRM operation	$\Delta t_{HSonmaxCRM}$	75	80	85	ns	CRM operation, t_{HSon} not limited by V_{CSSET}, only applies for small V_{bus}
Blanking time for brown-out protection	t_{bo}	-	70	-	ms	

7 Package dimensions

You can find all of our packages, sorts of packing and others in our Infineon internet page “Products: http://www.infineon.com/products”.

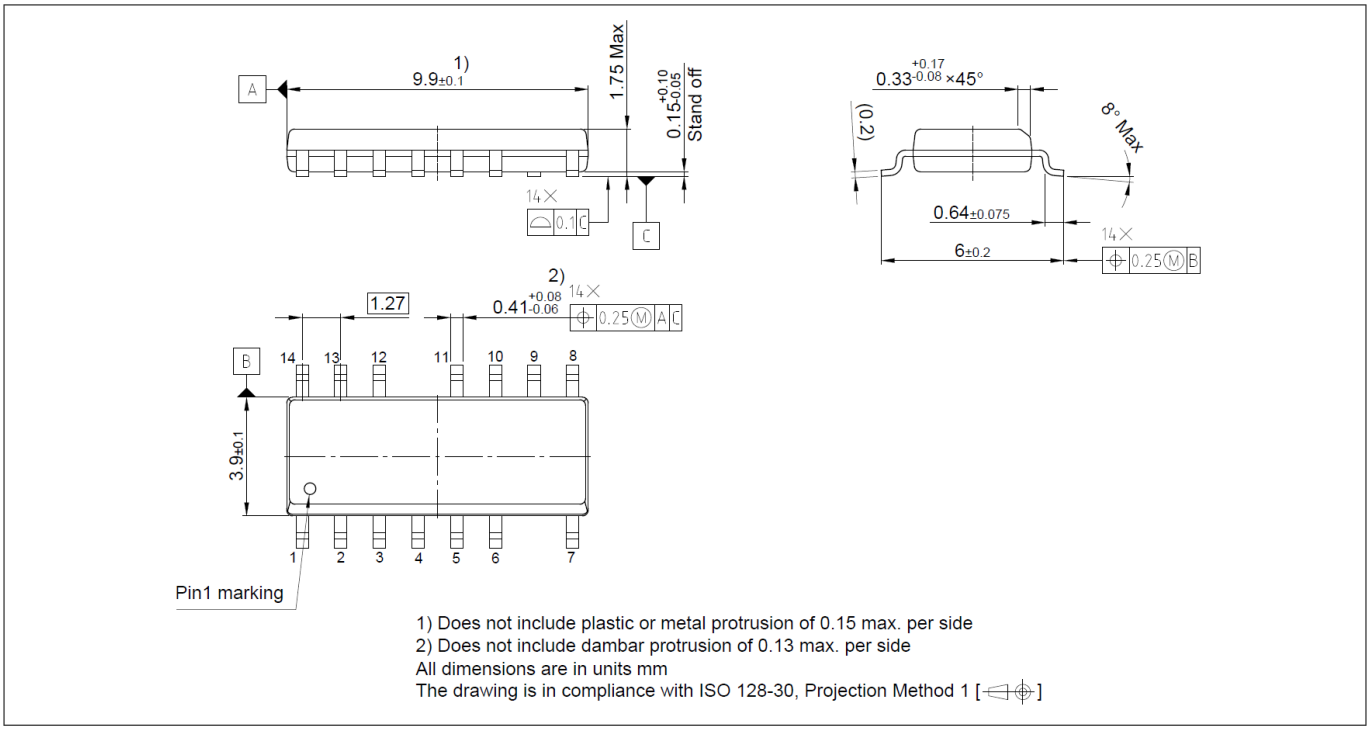

Figure 27 PG-DSO-14 outline

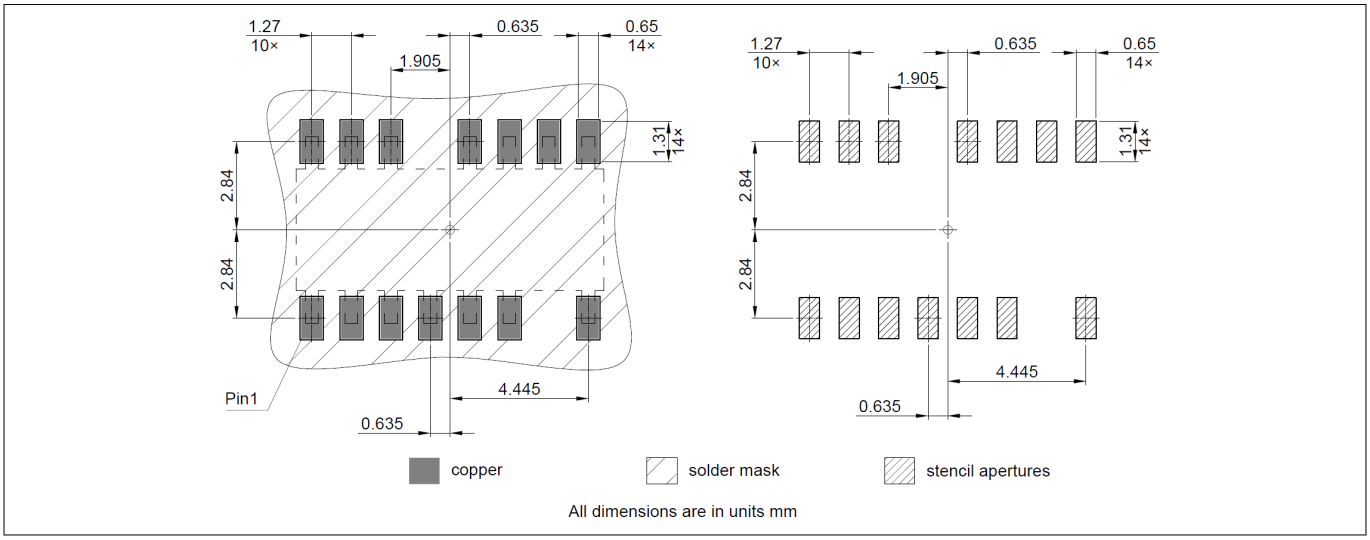

Figure 28 PG-DSO-14 footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pbfree finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

8 Revision history

Document version	Date of release	Description of changes
Rev. 1.0	2022-10-13	Initial release
Rev. 1.1	2022-11-09	• Added firmware version to "Ordering Information" • Refined X-capacitor discharge description • Corrections in chapter 4.3 • Corrections in configurable parameter tables • Corrections in electrical characteristics
Rev. 1.2	2023-10-23	• Firmware version update • AC Brown-in/out functionality: Thresholds are referred to input voltage • Removed X-capacitor discharge functionality • Corrections in VCC supply during protection modes (chapter 4.1.3 and 4.5.1) • Added information about timeout in CRM operation • Updates and corrections in ZVS functionality (chapters 4.3.1 and 4.3.2.2) • Added description on output voltage measurement and related filter time constant • Updates in Jitter functionality (chapter 4.3.4) • Added blanking time of power based PFC disable (chapter 4.4.2) • Added description of "Fast restart mode" (chapter 4.5.1.4) • New functionality: Memory parity check (chapter 4.5.2.18) • Updates and corrections in configurable parameter tables • Corrections in electrical characteristics - Removed typ.-values for V_VCCon and V_VCCoff - Added different values for V_VCCoff durning during protection mode - Corrected min./typ./max.-values of V_PFCCSocp - Corrected typ./max.-value of V_FBBMctrl - Added min./max.-value of R_MFIOpu • Updated figure of IC footprint • Minor corrections in text descriptions

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