IOR HiRel
An Infineon Technologies Company

Minimize PCB thermal stresses and ESD events with the rad hard SMD-0.2e

About this document

Scope and purpose

This application note presents International Rectifier HiRel (IR HiRel)'s SMD-0.2e discrete package and its inherent ability to mitigate issues from thermal mismatches between different materials and electrostatic discharge (ESD) hazards. This document highlights the improvements implemented within the new SMD-0.2e package (the “e” designates the enhanced version of the legacy SMD-0.2 package).

Intended audience

This document is intended for application engineers and designers looking for radiation-hardened (rad hard) power discrete solutions for space and other harsh environment applications where strenuous temperature cycles and radiation could be a concern. The goal of this application note is to guide the designer in selecting the right package to suit the needs and constraints of the application.

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1 Introduction

With a footprint of 8.2 x 5.8 mm^2, SMD-0.2 package styles are best suited for smaller-sized dies where board space comes at a premium cost and high power densities is desired. Several applications supported by MOSFETs housed within SMD-0.2 variants include DC-DC converters, motor drives, electric propulsion, thermal management, and point-of-load (PoL) converters for FPGA, ASIC, and DSP core rails.

Material differences between PCB boards and legacy SMD-0.2 power devices directly mounted onto those boards may result in solder joint damage and potentially jeopardize the structural integrity of the highly reliable, hermetically sealed packaged device. New advancements in SMD package technology developed by IR HiRel effectively confronts both concerns (solder joint fatigue and hermetic package integrity).

An additional concern for traditional SMD packages is the total ionizing dosage (TID) these packages may receive when they are expected to perform in irradiated environments. Constant high-energy irradiation may result in an arc discharge from the floating metals on legacy packages to nearby charge sinks. Isolated metal lids such as the SMD-0.2 and SMD-0.5 are prone to ESD events. To limit the possibility of severe charge buildup, more ceramic materials are incorporated into packages when practical.

The new SMD-0.2e package design implements several features for IR HiRel's radiation-hardened (rad hard) power MOSFETs to mitigate thermal stresses and ESD events.

This application note has the following general outline:

- Describe the issues pertaining to thermal mismatch and TID-induced ESD events for RH discretes
- Review some of the prior art that allowed for a solution to each problem
- Show the new package and describe the mechanical features of interest
- Describe the environmental qualifications of the new SMD-0.2e package as mounted on a printed circuit board (PCB)
- Summarize the benefits of the new package for rad hard devices and present a solder pad layout reference that was used during Infineon's own PCB-level package qualification testing

2 Design challenges

2.1 Interfacing materials with different thermal properties

Temperature cycling is a well-established design concern for high reliability power systems. Space grade discretes developed by IR HiRel are designed to perform reliability within the standard military temperature range of –55°C to +150°C. PCBs and components assembled onto them should be considered as a heterogenous mixture of different materials that behave differently to various changes in temperature. A key aspect to consider is how these materials may interact with each other according to their material properties.

One major property is a material's propensity to expand and contract with temperature changes, known as the "coefficient of thermal expansion" (CTE) [1]. Different materials have different CTEs. A wide temperature range can potentially give rise to excessive stress and strain between mated materials with dissimilar CTEs. PCBs commonly contain materials such as FR-4 or polyimide while IR HiRel hermetic packages are constructed with metals, ceramics, and glass. The ceramic components of the discrete packages are intrinsically brittle and will crack under significant stress [2]. Metals are ductile and will conform more easily to interfaced materials changing their form. Table 1 summarizes the CTE for some common PCB and discrete package materials.

Table 1 CTE of different materials in hermetic package and PCBs

Material	CTE α (10^{-6}/K)
FR-4 circuit board [3]	11–15
Polyimide circuit board [4]	~15 (in plane)
Copper [5]	17–18
Ceramic/glass	6

In one dimension, the change in length of a material due to a variation in temperature is described by the following equation:

$$\Delta l = \alpha * l_0 * \Delta T$$

Equation 1 Linear thermal expansion

- l is material length
- α is the coefficient of material expansion (commonly referenced with 10^{-6}/K or ppm/K)
- T is temperature referenced in Kelvin

Materials in real-world applications volumetrically expand and contract in three dimensions. Therefore, the stress that interfaced materials with significantly different CTEs experience over a wide temperature range is a more complicated exercise to understand than what is described within Equation 1. In addition, smaller packages such as the SMD-0.2 or SMD-0.1 also offer a higher power density, potentially dissipating more heat per unit of area.

High power densities could create hot spots on a PCB, resulting in a non-uniform temperature distribution throughout a PCB. Therefore, the measured data of a package's mechanical performance when mounted on a PCB over different temperature cycles will give a designer the greatest confidence in the part's survivability. IR HiRel conducts PCB-level package qualification test campaigns to ensure that parts are effective in realistic applications.

Power devices directly mounted onto PCBs that are expected to experience large temperature variations and power dissipations are vulnerable to stress fractures in their ceramic base (see the SMD-0.5 variant within SMD-0.5e application note for several examples). SMD package variants that utilize metal lids such as the SMD-0.2 and SMD-0.5 also require seam sealing to incorporate the metal lid; the significant CTE mismatch between the metal lid and ceramic sidewalls results in high package stress (see Figure 1).

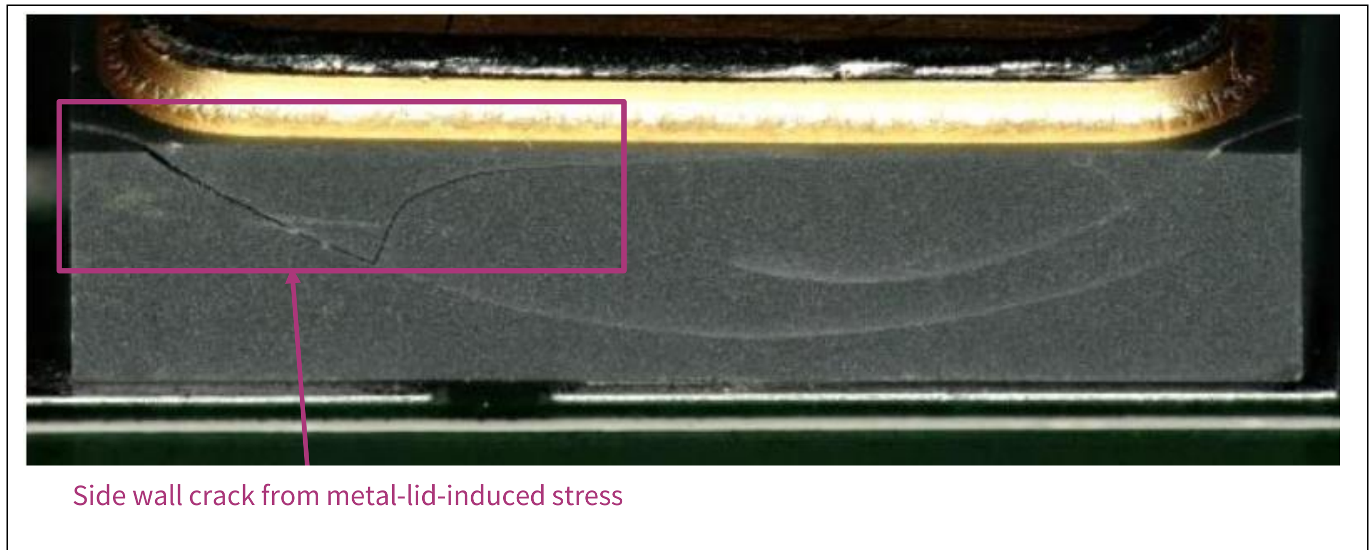


Figure 1 SMD-0.2 sidewall crack after PCB mounting

Improvements in package technology must keep pace with thermal requirements and the introduction of the SMD-0.2e is one result of this effort.

2.2 Challenges pertaining to TID-induced ESD events

Electrical systems operating within space must contend with several different space plasmas (solar flares, Van Allen Belts, galactic cosmic rays, etc.) that may deliver a significant amount of total ionizing dosage (TID) over the system's operating lifetime. Floating conductors will cumulatively amass charge when subjected to radiation. If these floating pieces of metal are located near grounded charge sinks, the relationship between both pieces can be modeled as a capacitor. Sufficient charge buildup within a capacitor-like system results in a potential difference between both electrodes (in this case, between the floating and grounded pieces of metal). Excessive voltage could induce an electrostatic discharge event where an arc is formed and a potentially dangerous amount of current flows. Nearby electronics or the die within the package could be damaged by the significant charge flow or experience a spurious signal which may disrupt the operation (see Figure 2 for several examples).

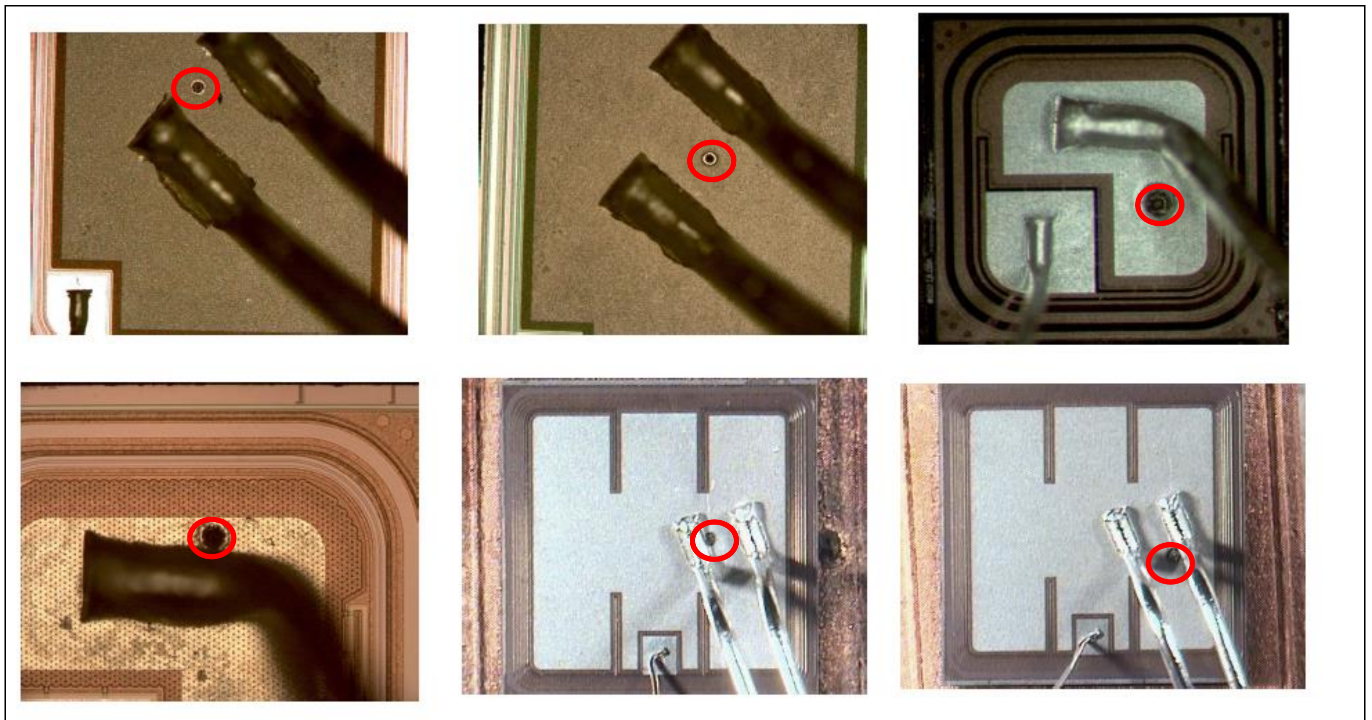


Figure 2 Possible TID-induced electrical burns of IGBT dies from high current passing into them for an extremely short period of time

Historically, space-grade circuit board designs could follow this general rule: any conductive elements on a circuit board larger than 0.3 cm^2 or longer than 25 cm in length must be ground-referenced [6]. Evidently, more nuance was needed because the recently released *Mitigating In-space Charging Effects* guideline (NASA-HDBK-4002B) advised system designers to appraise the electrostatic sensitivity of any electronics located near a floating conductor that could be a victim of an ESD event, regardless of whether the floating metal was below 0.3 cm^2 [7]. Bodeau M., et al concluded that floating metals should be tested in-flight relevant conditions to prove that the system is safe [8].

IR HiRel offers a wide variety of packages that follow this design rule: through-hole and SMD-style cases (except for leads and pads respectively) must be electrically isolated from the die within. This rule helps prevent any attached heatsinks from being energized by the die itself and reduce the drain capacitance the die may experience. The tradeoff is that these packages may have floating segments of metal (like the isolated lids of SMD-0.5 and SMD-0.2 variants) that must be grounded to avoid ESD events. Advanced package designs like SMD-0.2e also address ESD issues.

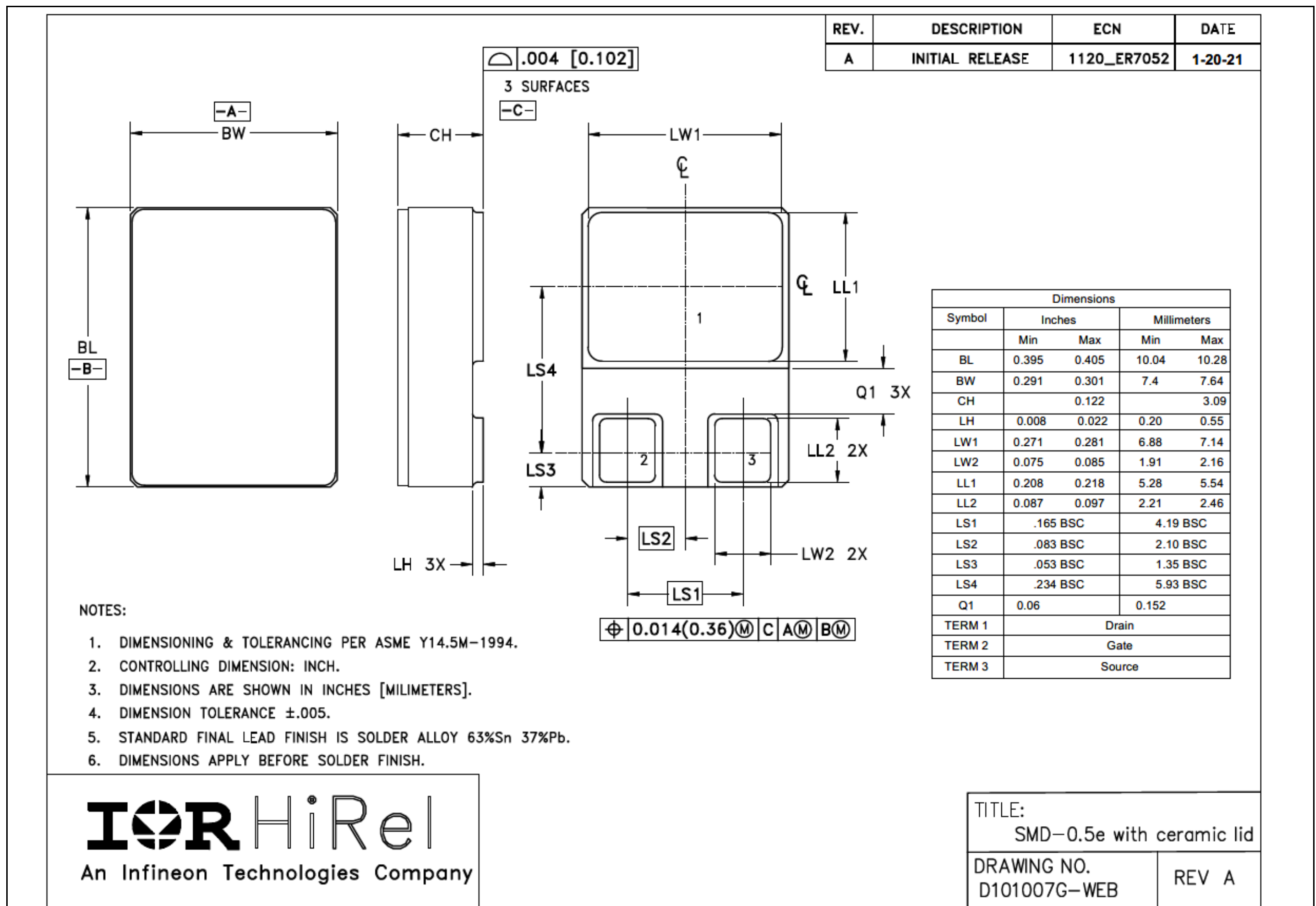
3 Existing solutions for SMD-0.2 thermal and ESD issues

3.1 Directly mounting SMD-0.2 packages

The SMD-0.2 package family offered by IR HiRel supports the following die sizes: 2.54 x 2.01 mm^2 (die size “1”) and 3.07 x 2.21 mm^2 (die size “1.7”). Presently, this package is the only SMD-style variant that houses die size 1.7. SMD-0.1 does not contain sufficient volume; larger SMD packages like the SMD-0.5e would take up excessive board space. Therefore, designers who wish to employ a relatively small die size like 1.7 may need to work with SMD-0.2; the general solution is to directly mount the part onto the PCB.

If thermal stresses could potentially exceed the capability of SMD-0.2, the next alternative package is SMD-0.5e, which takes up more board space, thereby limiting the power density (see Figure 3 and Figure 4 for a size comparison between SMD-0.5e and SMD-0.2 respectively).

As mentioned in the previous section, SMD-0.2 employs a metal lid that is seam-sealed to ceramic (AlN) sidewalls. A coefficient of thermal expansion (CTE) mismatch present on the package itself in addition to the mismatch between the SMD-0.2 pads and the PCB adds a high stress to the package. One incremental improvement was the development of SMD-0.2c where this package has an alumina (Al_2O_3) lid instead of metal, removing the need for seam sealing (see Figure 5). However, the fracture toughness of SMD-0.2 and SMD-0.2c was deemed inadequate for both packages because the sidewalls of each package employed the brittle ceramic AlN (typical measured value of 2.5 to 3.2 $\mathrm{MPa} * \mathrm{m}^{\frac{1}{2}}$) [9]. Therefore, a stronger ceramic was needed to make the package construction more robust.



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
BL	0.395	0.405	10.04	10.28
BW	0.291	0.301	7.4	7.64
CH		0.122		3.09
LH	0.008	0.022	0.20	0.55
LW1	0.271	0.281	6.88	7.14
LW2	0.075	0.085	1.91	2.16
LL1	0.208	0.218	5.28	5.54
LL2	0.087	0.097	2.21	2.46
LS1	.165 BSC		4.19 BSC	
LS2	.083 BSC		2.10 BSC	
LS3	.053 BSC		1.35 BSC	
LS4	.234 BSC		5.93 BSC	
Q1	0.06		0.152	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

Figure 3 SMD-0.5e package drawing (see website for updated specifications)

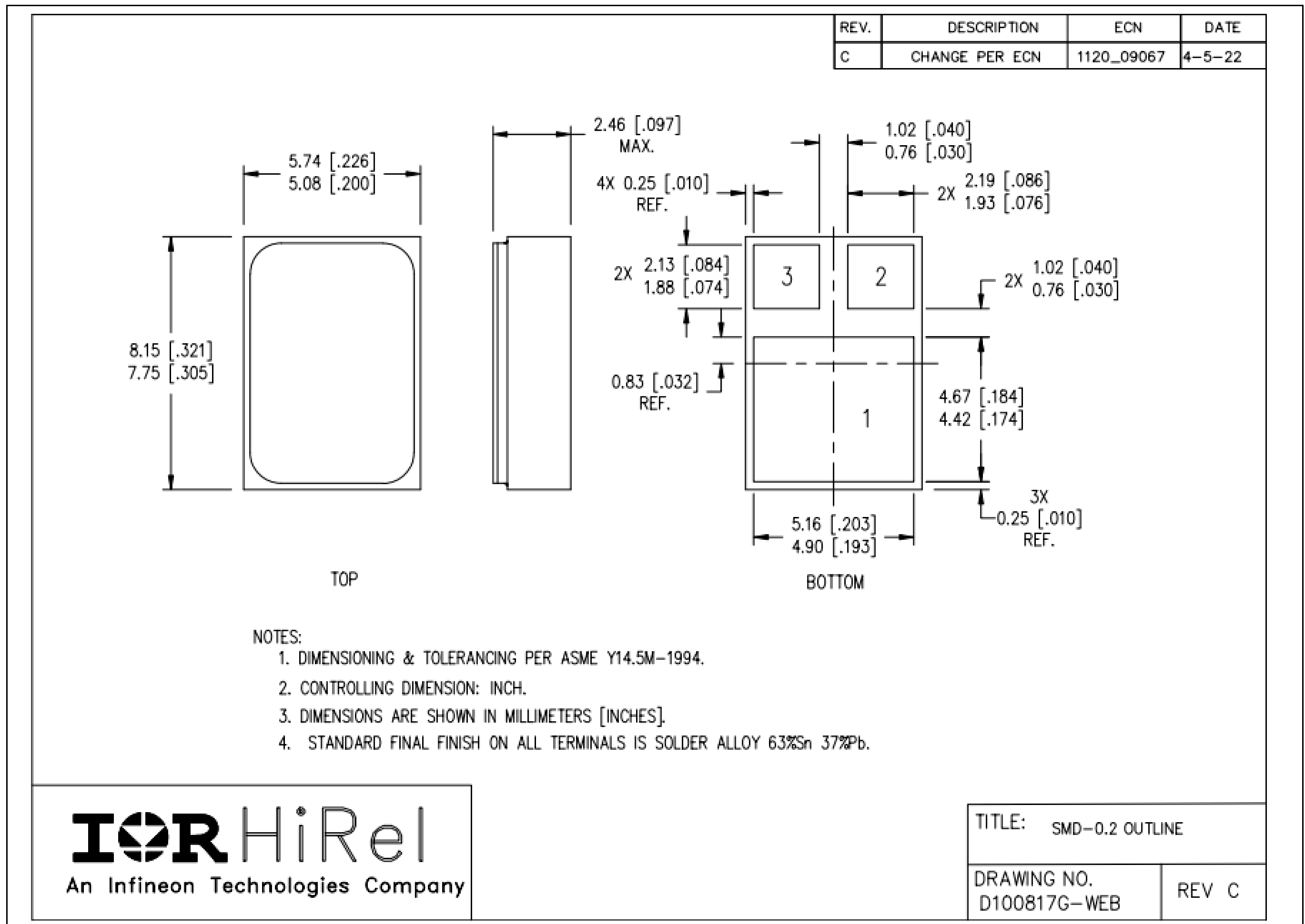


Figure 4 SMD-0.2 package drawing (see website for updated specifications)

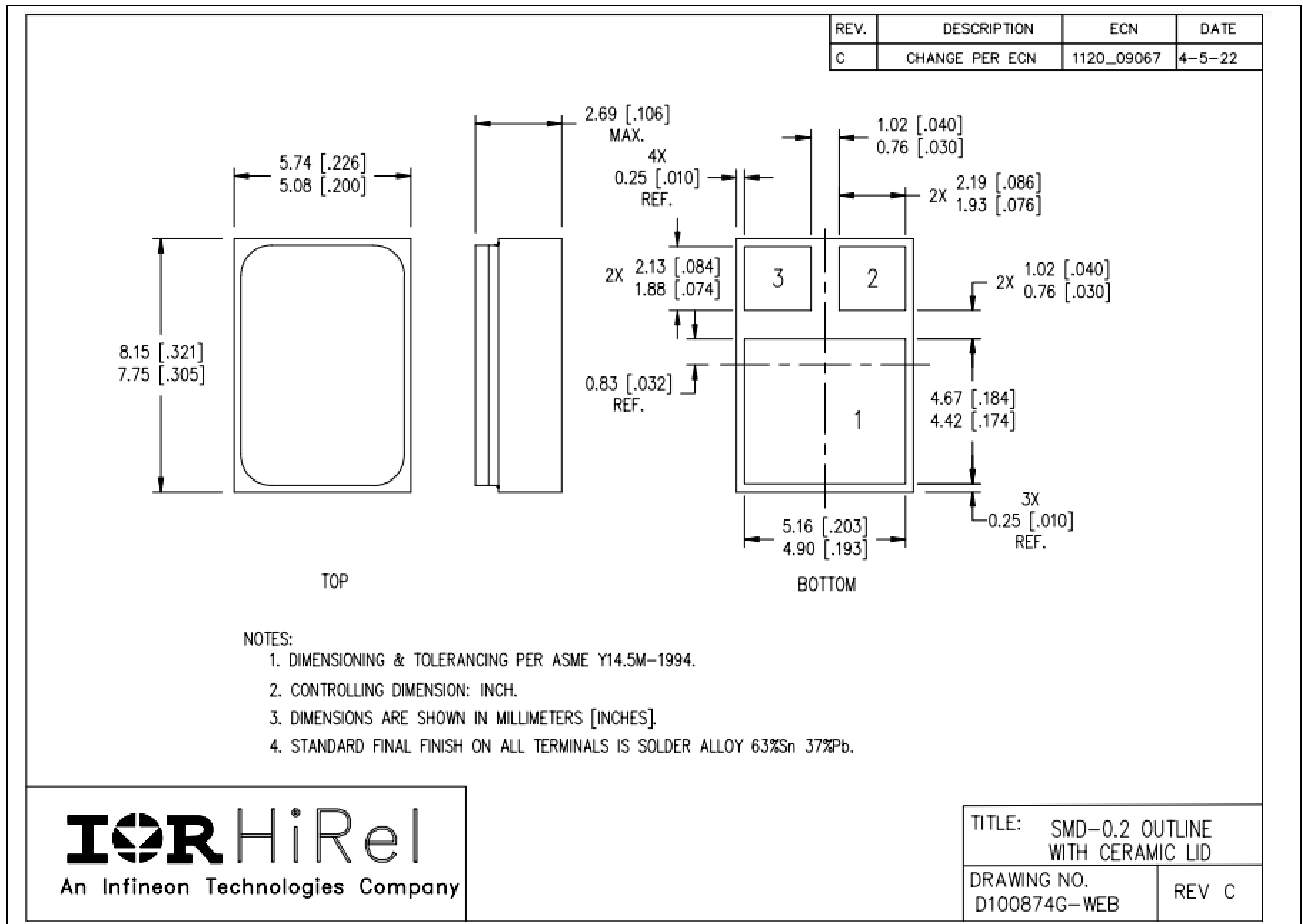


Figure 5 SMD-0.2c package drawing (see website for updated specifications)

3.2 Implementation of charge bleeding pathways

Floating metals on a circuit board must be identified and provided a conductive pathway to a ground node to dissipate any accumulated charge. It is best practice to connect conducting elements to a common electrical ground reference. For example, the RIC7S113A4 rad hard high- and low-side gate driver has a floating metal lid; enough wire connecting the lid to a charge sink will provide sufficient protection from ESD events (see Figure 6).

Some discrete packages supported by IR HiRel like the UB 4-pad offers a bleed pathway along the package corner to remove any need for external wiring (see Figure 7 and Figure 8). The UB 4-pad is designed for small-signal FETs; therefore, they cannot support the power dissipation metrics that several dies housed in SMD-0.2 or SMD-0.2c require.

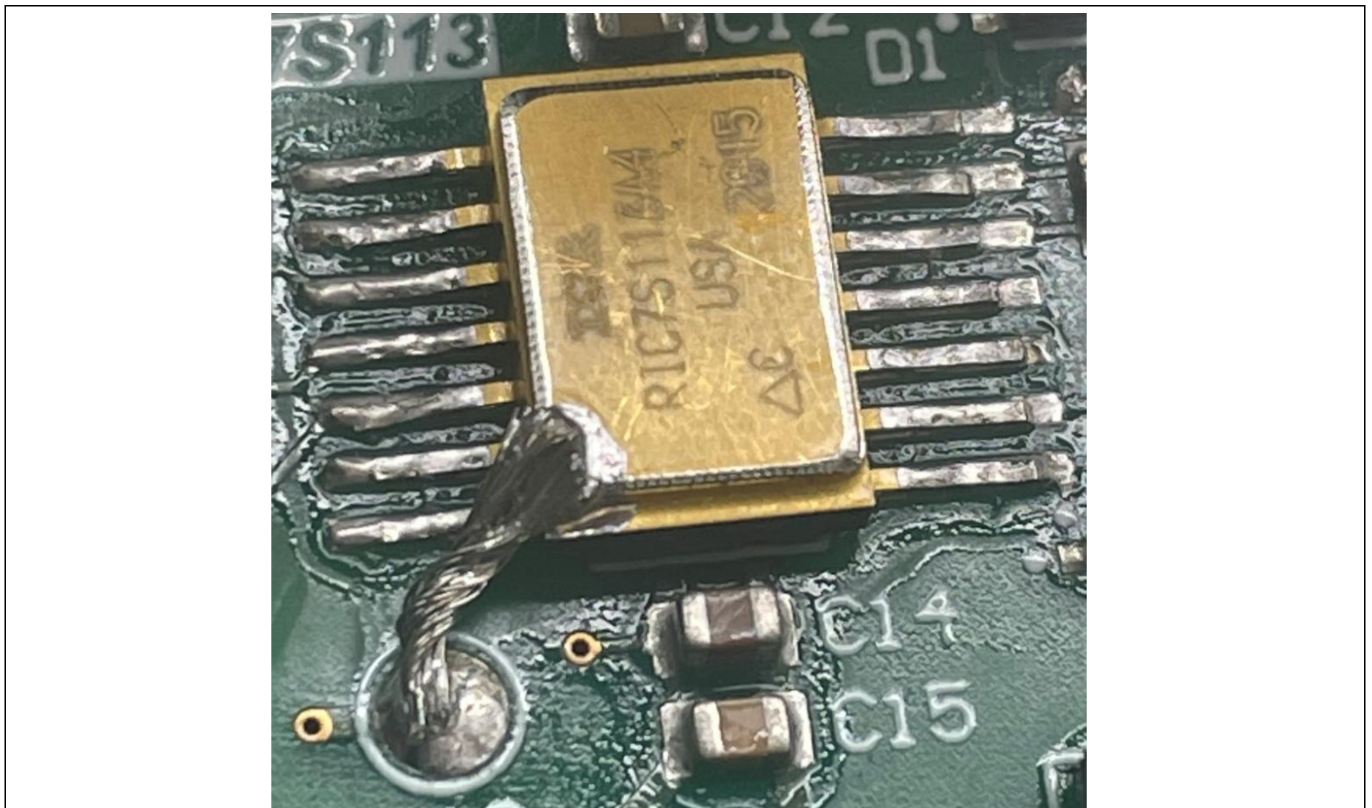


Figure 6 **Bonded wire to bleed charge from floating metal lid of RIC7S113A4 14 lead flatpack**

REV.	DESCRIPTION	ECN	DATE
B	CHANGE PER ECN	1120_08548	4–20–21

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HATCHED AREAS ON PACKAGE DENOTE METALIZATION AREAS.
5. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.
6. PAD 4 IS ELECTRICALLY CONNECTED TO THE SEAL RING.

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TITLE: UB PACKAGE OUTLINE 4 PAD WITH METAL LID
DRAWING NO. D100914G–WEB
REV B

Figure 7 UB 4-pad package with metal lid grounded by corner metallization

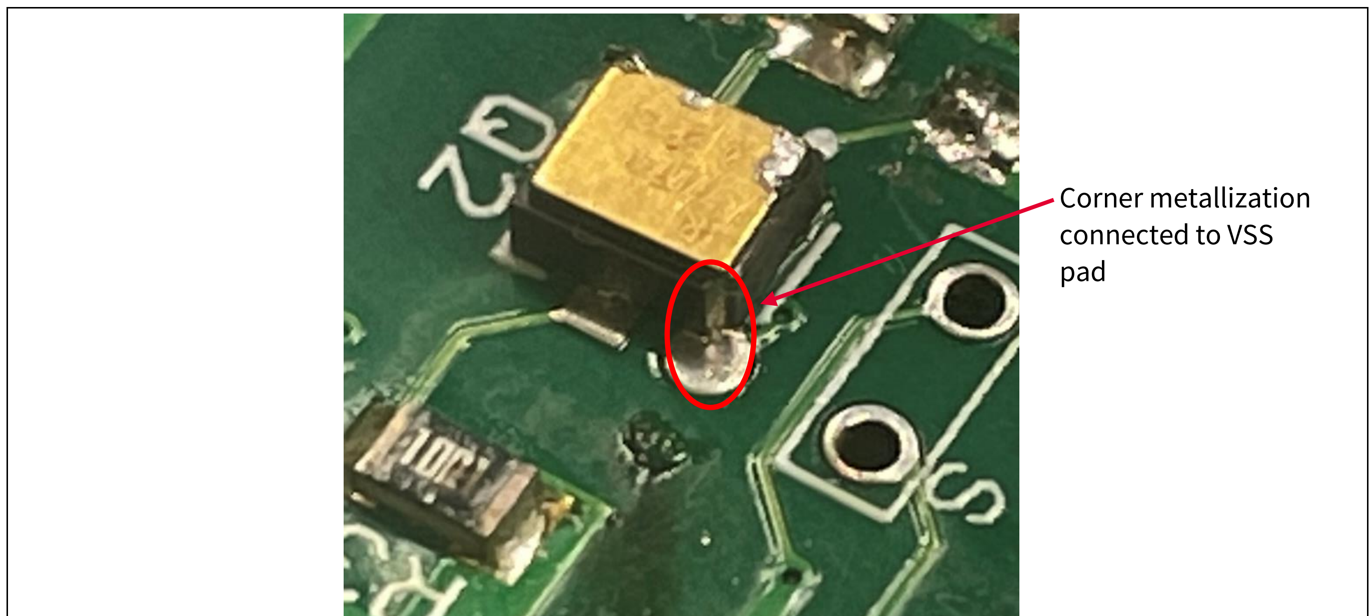


Figure 8 Example of UB 4 pad with metal lid grounded to copper pour

If there are concerns of an overheating the die inside when soldering a wire to the lid, a conductive epoxy solution can be used instead.

4 SMD-0.2e: A better solution

4.1 Minimizing the CTE mismatch between package and PCB

Already implemented in the SMD-0.5e variant, the SMD-0.2e package employs a novel material mixture at the base pads of the package to gradually shift the coefficient of thermal expansion (CTE) from ceramic-based to PCB-based materials to minimize large CTE mismatches (see US patent 9,887,143 filed by Infineon Technologies) [10]. Figure 9 shows how the die is directly mounted to the drain pad and wirebonded to the source and gate pads. This gradual shift ultimately reduces the mechanical stress that the hermetically sealed package will experience over large temperature cycles and prolong the lifetime.

A more robust ceramic material, alumina (Al_2O_3), was used to construct the base and sidewalls of SMD-0.2e to improve the package's strength. Alumina used for electronic SMD packages generally has a fracture toughness of 4.1 $\mathrm{MPa} * \mathrm{m}^{\frac{1}{2}}$, outclassing the previously mentioned fracture toughness of AlN (2.5 to 3.2 $\mathrm{MPa} * \mathrm{m}^{\frac{1}{2}}$). The SMD-0.2e package fits in the same PCB footprint as SMD-0.2 to provide drop-in compatibility (see Figure 10 and Figure 11 for package images).

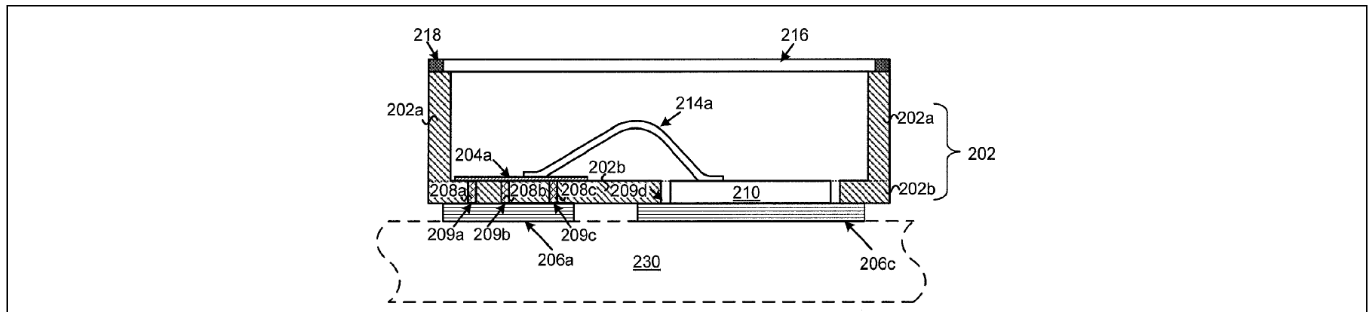
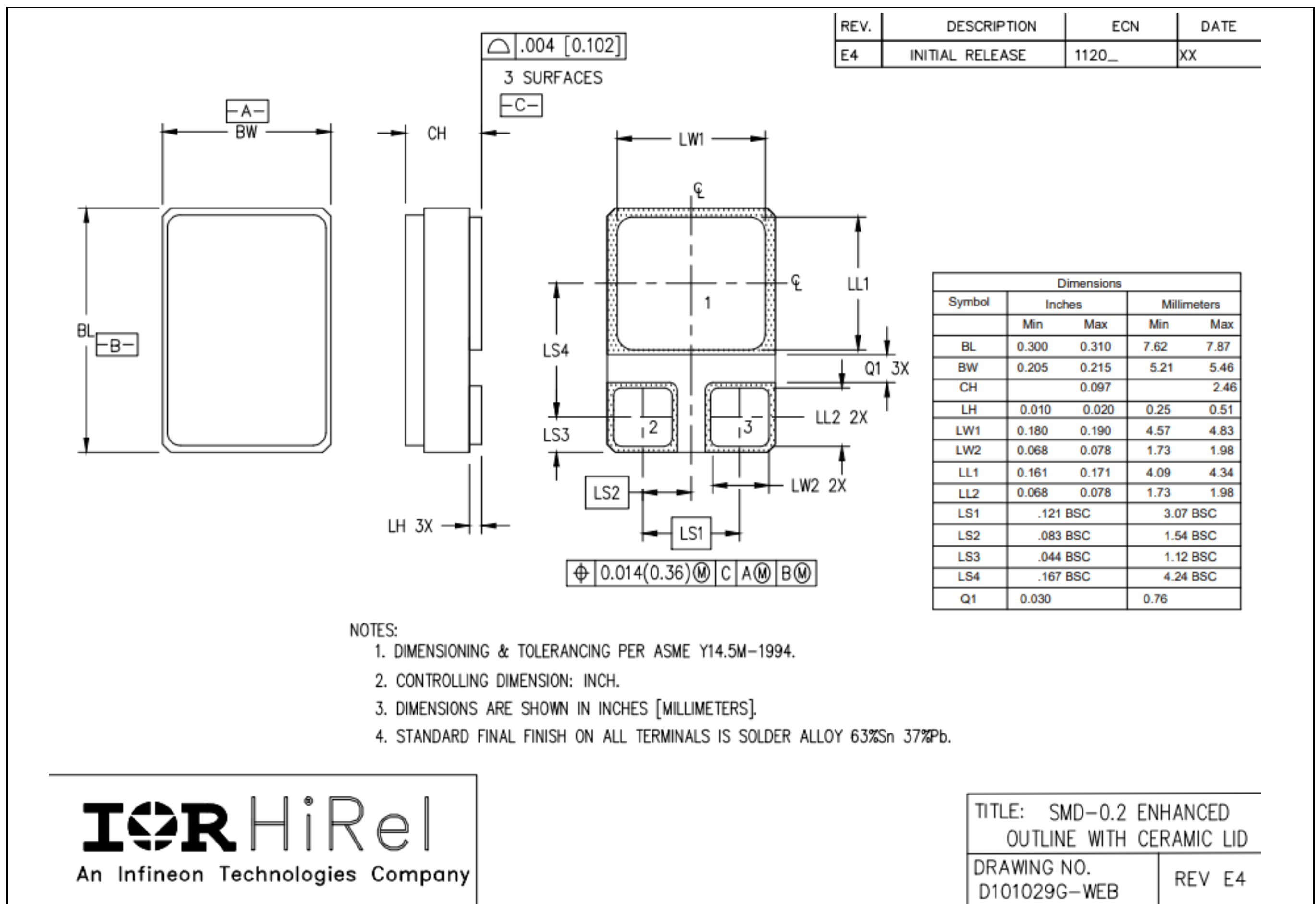


Figure 9 SMD-0.2e, a new design concept (cutaway view showing the chip and wirebond inside)

Figure 10 SMD-0.2e package image



Symbol	Dimensions Inches Min	Inches Max	Millimeters Min	Millimeters Max
BL	0.300	0.310	7.62	7.87
BW	0.205	0.215	5.21	5.46
CH		0.097		2.46
LH	0.010	0.020	0.25	0.51
LW1	0.180	0.190	4.57	4.83
LW2	0.068	0.078	1.73	1.98
LL1	0.161	0.171	4.09	4.34
LL2	0.068	0.078	1.73	1.98
LS1	.121 BSC		3.07 BSC	
LS2	.083 BSC		1.54 BSC	
LS3	.044 BSC		1.12 BSC	
LS4	.167 BSC		4.24 BSC	
Q1	0.030		0.76	

Figure 11 SMD-0.2e package drawing (see website for all package drawings)

The internal attachment layout of the die within the SMD-0.2e package has also been improved to enhance the heat transfer and electrical performance of SMD-0.2e discretes. To address the relatively weak thermal conductivity of alumina (12 $\frac{\mathrm{W}}{\mathrm{m*K}}$), the drain section of the die encased within SMD-0.2e is directly mounted to a large CuW pad to minimize the junction-to-case thermal impedance (Zth_{jc}). A greater density of vias to connect each package pad to the die has resulted in a lower die-free package resistance (DPFR) despite SMD-0.2e having thicker and smaller pads in general (in comparison to SMD-0.2 and SMD-0.2c; see Figure 12 and Figure 13). Table 2 provides some details on the SMD-0.2e package's thermal and electrical impedance characteristics.

Table 2 Heat transfer and electrical impedance between SMD-0.2 package variants

Package variant	Zthjc (K/W)	DPFR (mΩ)
Current SMD-0.2 styles	0.878	2.12
SMD-0.2e	0.656	2.07

Enhanced SMD 0.2

C350049 (SMD-0.2)

Figure 12 (Bottom view) SMD-0.2e (left) has smaller soldering areas for all three pads but will effectively mate with SMD-0.2 (right) PCB footprints

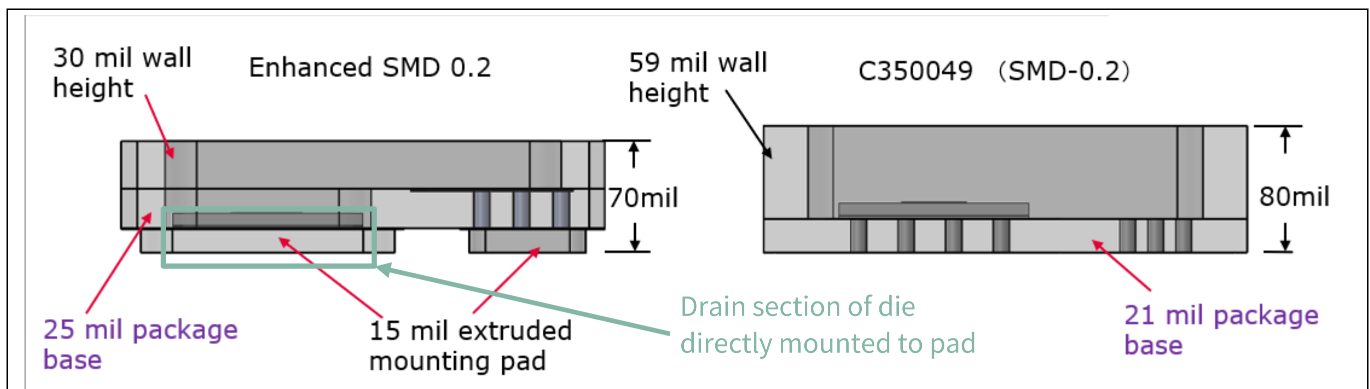


Figure 13 (Side view) SMD-0.2e (left) has a lower profile (10 mils shorter) than SMD-0.2 (right); die is directly mounted to the drain pad

Finite Element Analysis (FEA) was employed to evaluate the SMD-0.2e package in various environmental conditions. Ceramic stress is the main indicator for package survivability when subjected to the worst case (WC) conditions (WC situations involve colder temperatures and when mounted onto a PCB as depicted in Figure 14, Figure 15, and Figure 16). The following images show the maximum stress each SMD-0.2 style package experienced when mounted onto a PCB and temperature cycled down to –55°C (see Table 3 for a numerical comparison).

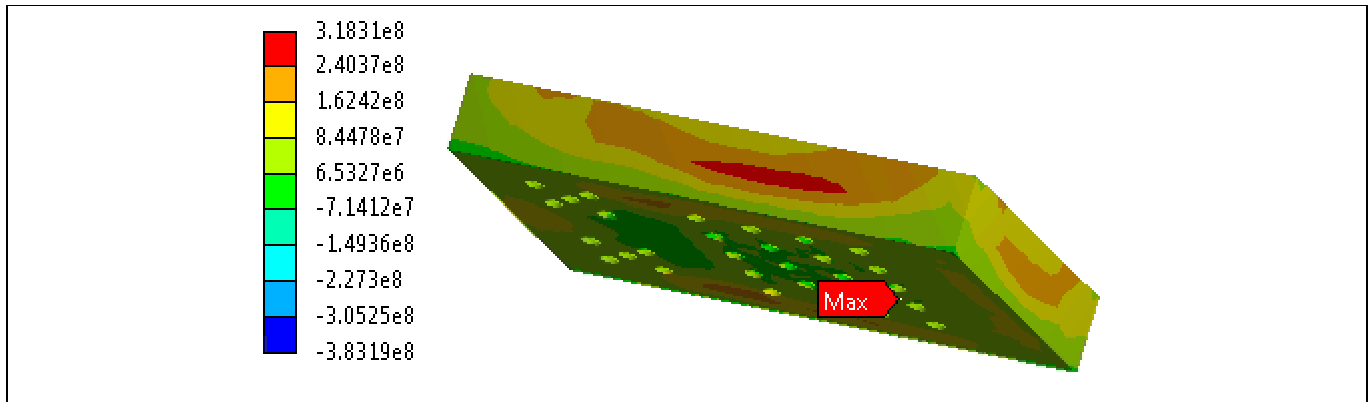


Figure 14 SMD-0.2 package worst-case stress found at the sidewall (agrees with physical depiction shown in Figure 1)

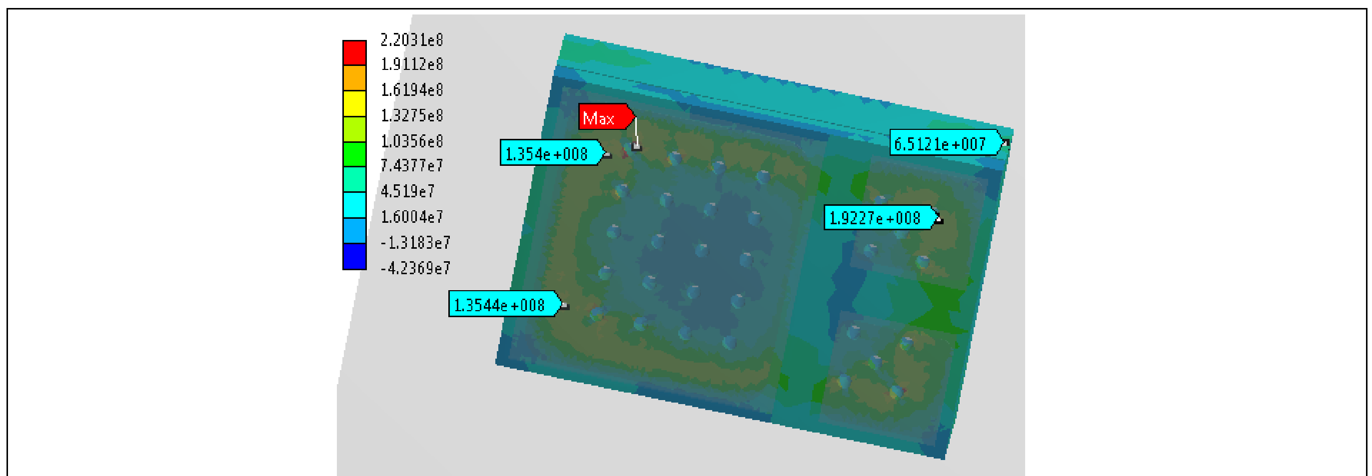


Figure 15 SMD-0.2c package worst-case stress found at the interface between package pad and PCB

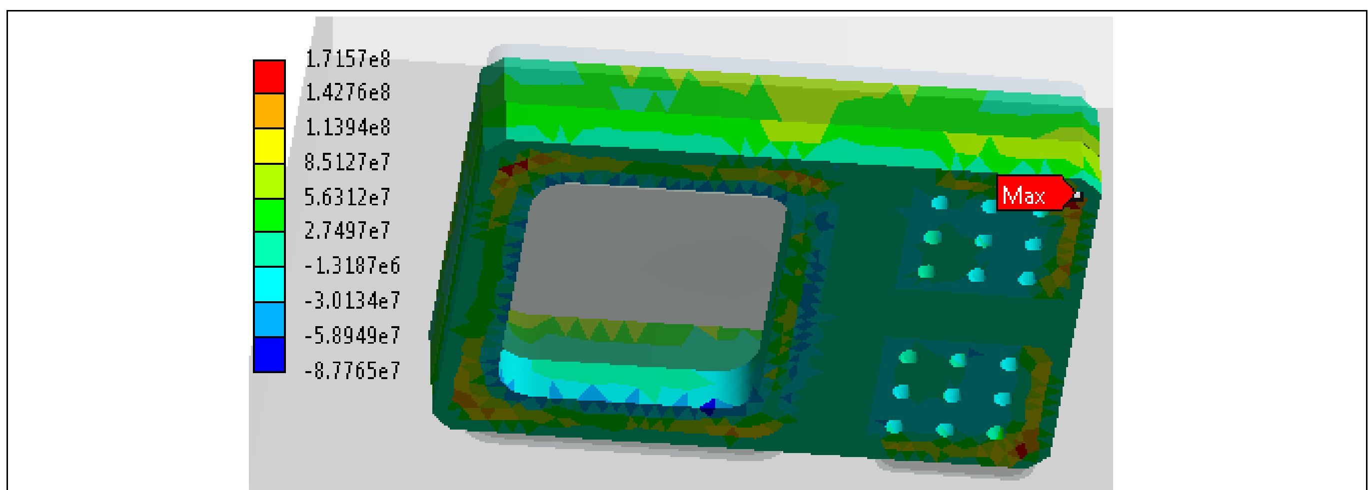


Figure 16 SMD-0.2e package worst-case stress found at the interface between package pad and PCB

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Table 3 Maximum simulated package stress comparisons (PCB mounted and temperature cycled)

Package variant	Ceramic stress (MPa)	Safety factor
SMD-0.2	318	0.94
SMD-0.2c	220	1.36
SMD-0.2e	171	1.6

Note: SMD-0.2 and SMD-0.2c packages employ AlN at their base and sidewalls while SMD-0.2e utilizes alumina.

The SMD-0.2 package is especially at risk of hermeticity loss because the metal lid adds more strain to the ceramic sidewalls. It is risky to utilize a part that is below a safety factor of 1 when testing at worst-case conditions. SMD-0.2e enjoys the greatest margin of safety with its modified padding structure and more robust material selection (alumina instead of AlN).

4.2 Material changes to address ESD concerns

Alumina is employed to form the lid, frame, and base of the SMD-0.2e package, resulting in a minimal amount of conductive material used within the SMD-0.2e package. In addition to lower mechanical stress as detailed in the previous section, SMD-0.2e is significantly less prone to potential ESD events. Table 4 summarizes the material composition of all three SMD-0.2 package variants.

Table 4 Material composition of SMD-0.2 package family

<table>
<tr><th rowspan="2">Package Variant</th><th colspan="2">Lid</th><th>Frame</th><th>Base</th></tr>
<tr><th>Material</th><th>Finish</th><th>Material</th><th>Material</th></tr>
<tr><td>SMD-0.2</td><td>Kovar</td><td rowspan="3">NiAu</td><td rowspan="2">AlN</td><td rowspan="2">AlN</td></tr>
<tr><td>SMD-0.2c</td><td rowspan="2">Alumina</td></tr>
<tr><td>SMD-0.2e</td><td>Alumina</td><td>Alumina</td></tr>
</table>

5 PCB-level qualifications

5.1 Qualification testing

PCB-level qualifications are necessary to validate the accuracy of FEA simulations and confirm package survivability. A series of tests were performed (satisfying the qualification criteria outlined by MIL-PRF-19500) to stress the SMD-0.2e package in conditions that are conducive to application-relevant scenarios [11]. A set of SMD-0.2e test packages were mounted onto a PCB (see Table 5 for test board specifications and Figure 17 for PCB depiction) and subjected to random vibration, mechanical shock, and temperature cycling tests (in that order). Figure 18 shows the test setup; approximately 12 DUTs were tested. Similar to other IR HiRel parts, discretes within this package go through Group A, B, C, D, and E of the Quality Conformance Inspection list, (QCI; see the website for detailed information on test requirements).

Table 5 Dimensions of SMD-0.2e PCB test board

Dimensional element	Measurement (mm)
Length	152
Width	102
Height[1]	1.78

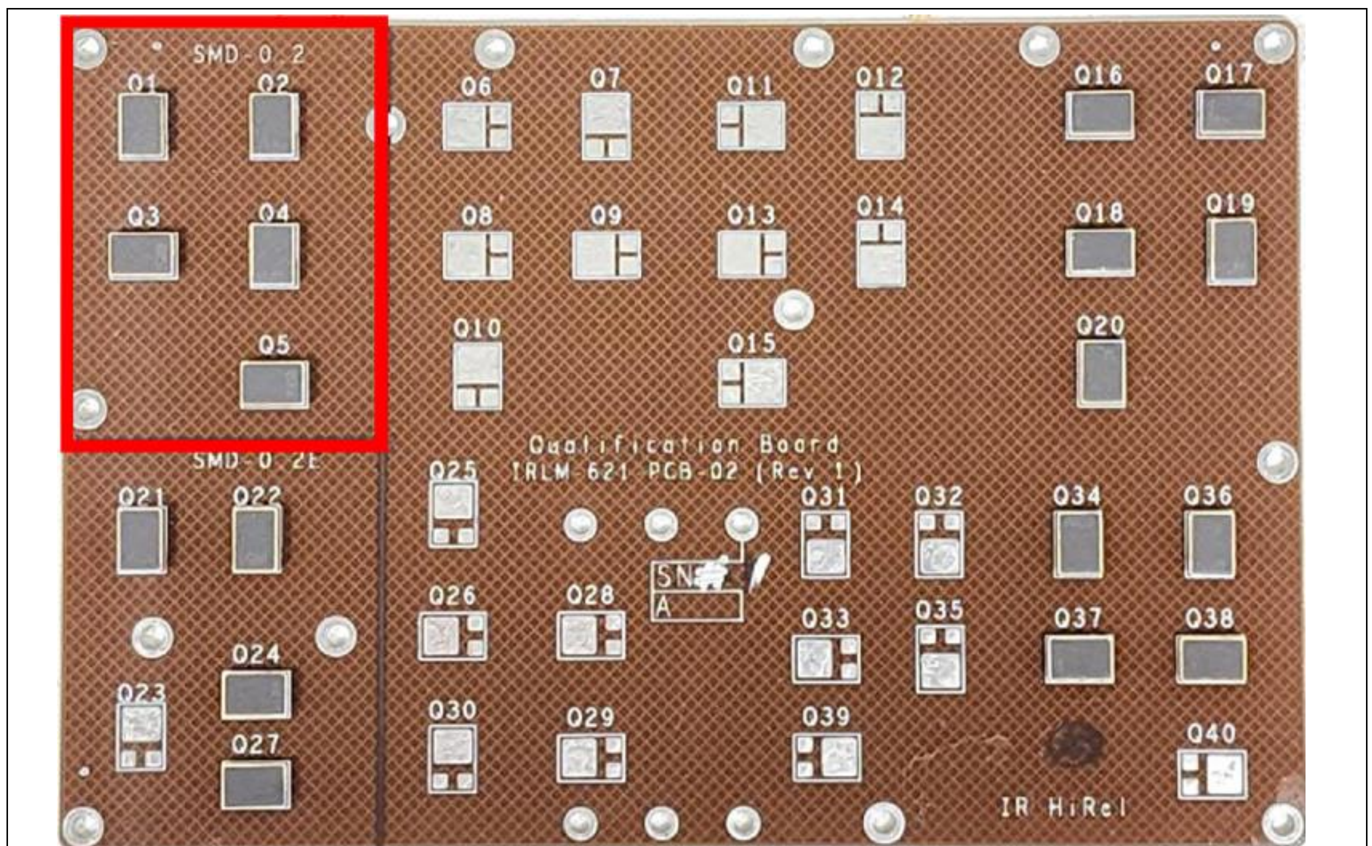

Figure 17 PCB-qualification test board (Q1 through Q5 in red box were subjected to temperature cycle tests – see Section 5.1.3)

[1] PCB was composed of 8 layers (2 oz. pour on all copper layers) with polyimide as dielectric.

5.1.1 Random vibration testing

Random vibration testing was executed and completed as required by ECSS-Q-ST-70-61C except that Grms was increased from 30 Grms to approximately 40 Grms [12]. A summary of the test conditions is provided in Table 6 and Table 7.

Table 6 Sinusoidal vibration levels

Range (Hz)	Level (peak-to-peak)	Sweep rate (octave/min)
25-30	13 G	1
30-100	20 G	
100-200	15 G	
Duration: 1 cycle up from 25 Hz to 200 Hz		

Table 7 Random vibration testing criteria

Axis	Frequency range (Hz)	Level	Grms	Duration (s)
x,y,z	20-100	+6 dB/oct	39.9	300
	100-1000	$1\ g^2/\mathrm{Hz}$		
	1000-1500	−3 dB/oct		
	1500-2000	−6 dB/oct		

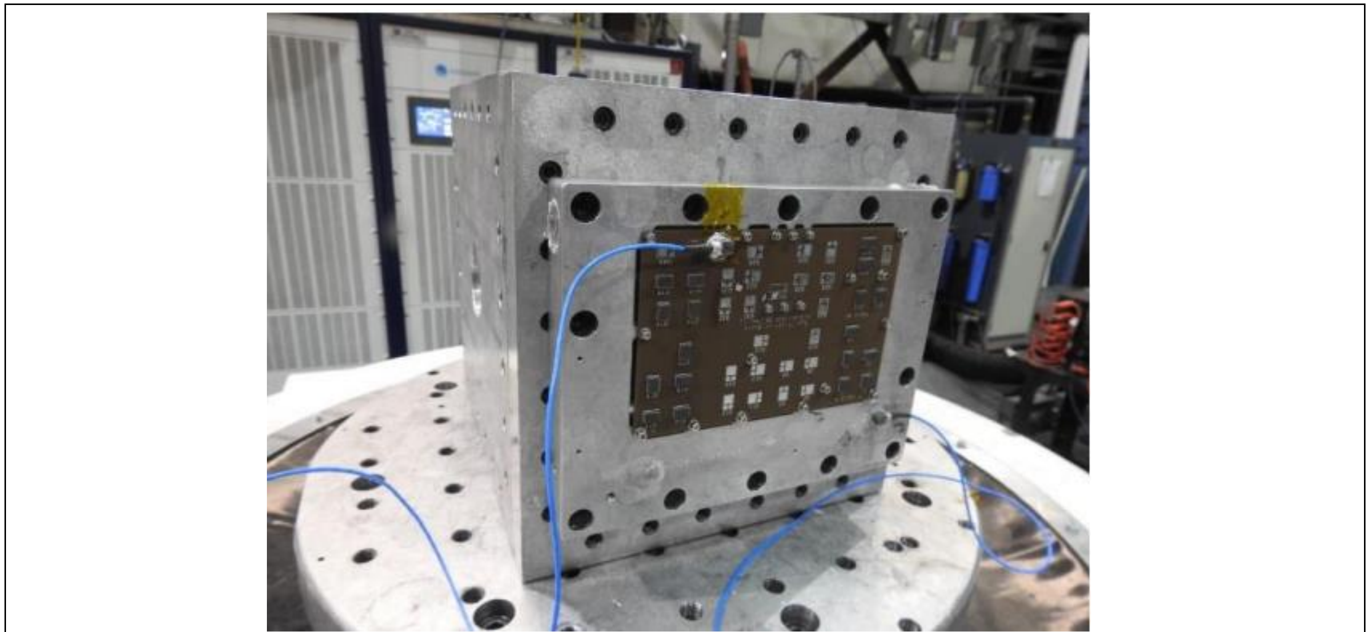

Figure 18 Random vibration test setup

5.1.2 Mechanical shock testing

Mechanical shock testing was performed in accordance with MIL-STD-883J Test Method 2002.5 Condition B [13]. The test conditions utilized involved 10 separate 0.5 ms shocks (5 moving in the negative direction and 5 moving in the positive direction) of 1500 G per cartesian axis (x, y, and z directions) resulting 30 total shocks per part.

5.1.3 Thermal cycling tests

All temperature cycling tests adhered to MIL-STD-750F, Test Method 1051 [14]. Package qualification requires 500 temperature cycles between a range of –55°C to +100°C with a 10°C/min ramp and a 15 min dwell time. Package inspections were performed after every 100 cycle intervals to confirm package survivability before it was subjected to additional test stages. Figure 19, Figure 20, and Figure 21 show the scanning electron microscope (SEM) cross-section images of SMD-0.2e pads on a PCB.

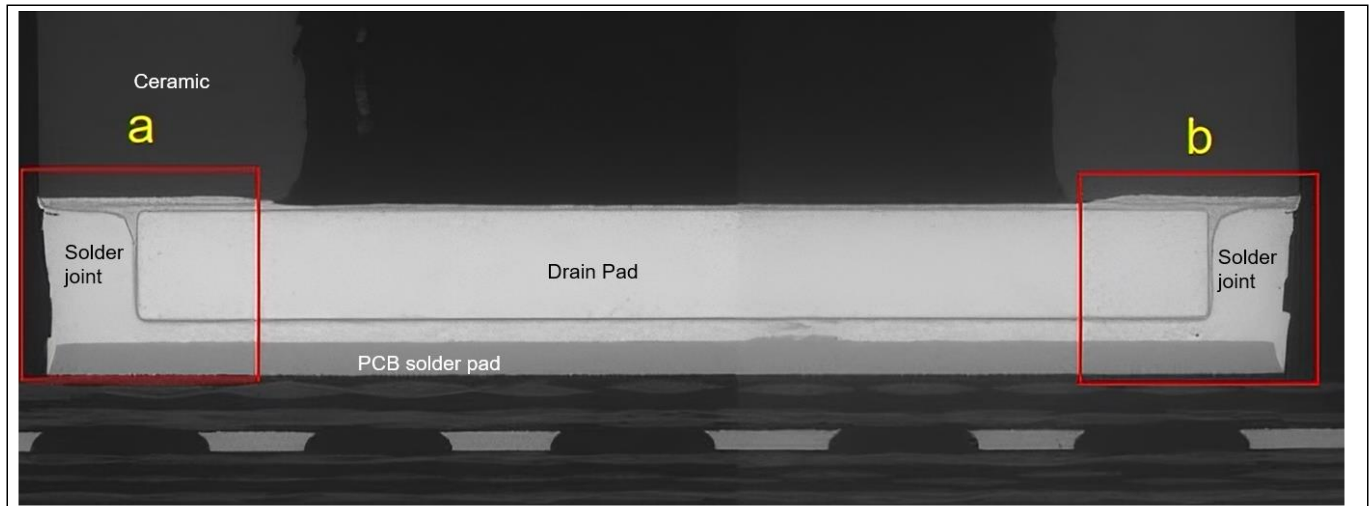

Figure 19 SEM cross section of SMD-0.2e drain pad bonded to PCB after 500 temp cycles. Bondline under pad and ceramic appear to be crack-free

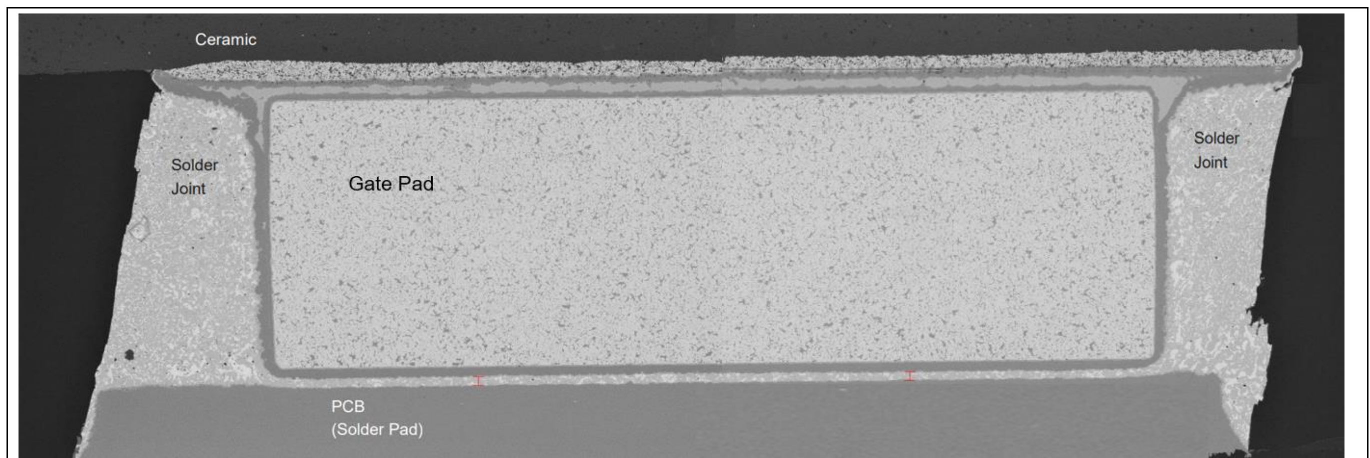

Figure 20 SEM cross section of SMD-0.2e gate pad bonded to PCB after 500 temp cycles. Bondline under pad appears to be crack-free

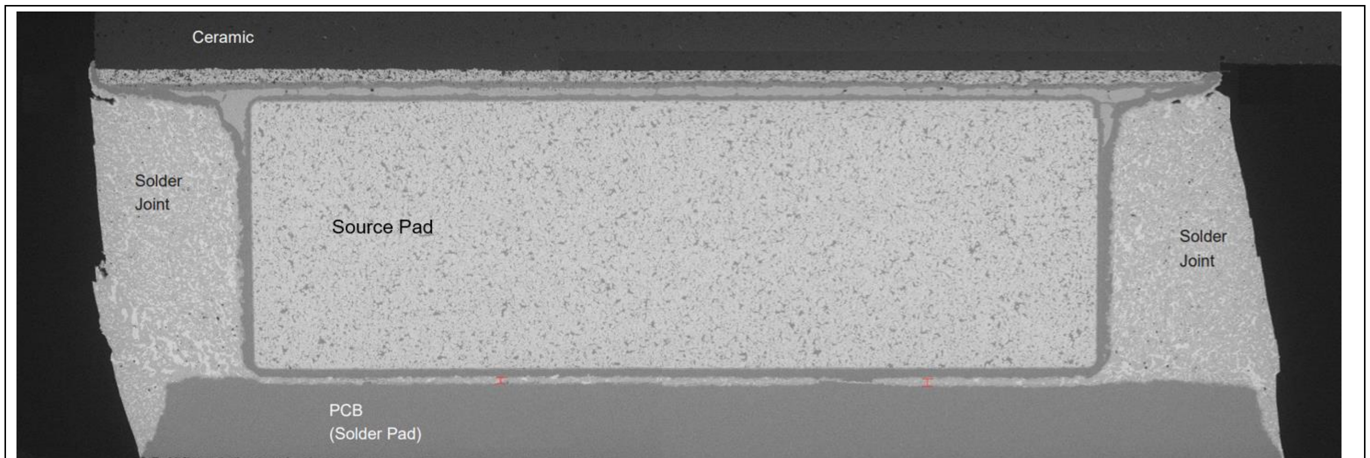

Figure 21 SEM cross section of SMD-0.2e source pad bonded to PCB after 500 temp cycles. Bondline under pad appears to be crack-free

5.2 Qualification results

After these three test groups (random vibration, mechanical shock, and temperature cycling) were completed, several SMD-0.2e test samples were selected for visual examinations (per MIL-STD-750 TM 2069) and then subjected to fine and gross leakage tests (per ECSS-Q-ST-70-61C). No leaks were detected.

6 Application

Directly mounting the SMD-0.2e package onto a PCB is highly recommended to maximize the transfer of heat away from the die and to maintain a small device form factor. This package works well with common PCB materials like FR-4 and polyimide. Lead-tin eutectic solder (Sn63Pb37) is recommended.

Figure 22 shows the pad layout used during internal PCB-level qualification tests mentioned throughout Section 5. Any pad layouts that were previously designed for SMD-0.2 or SMD-0.2c will also be appropriate for SMD-0.2e because this new package is a drop-in replacement.

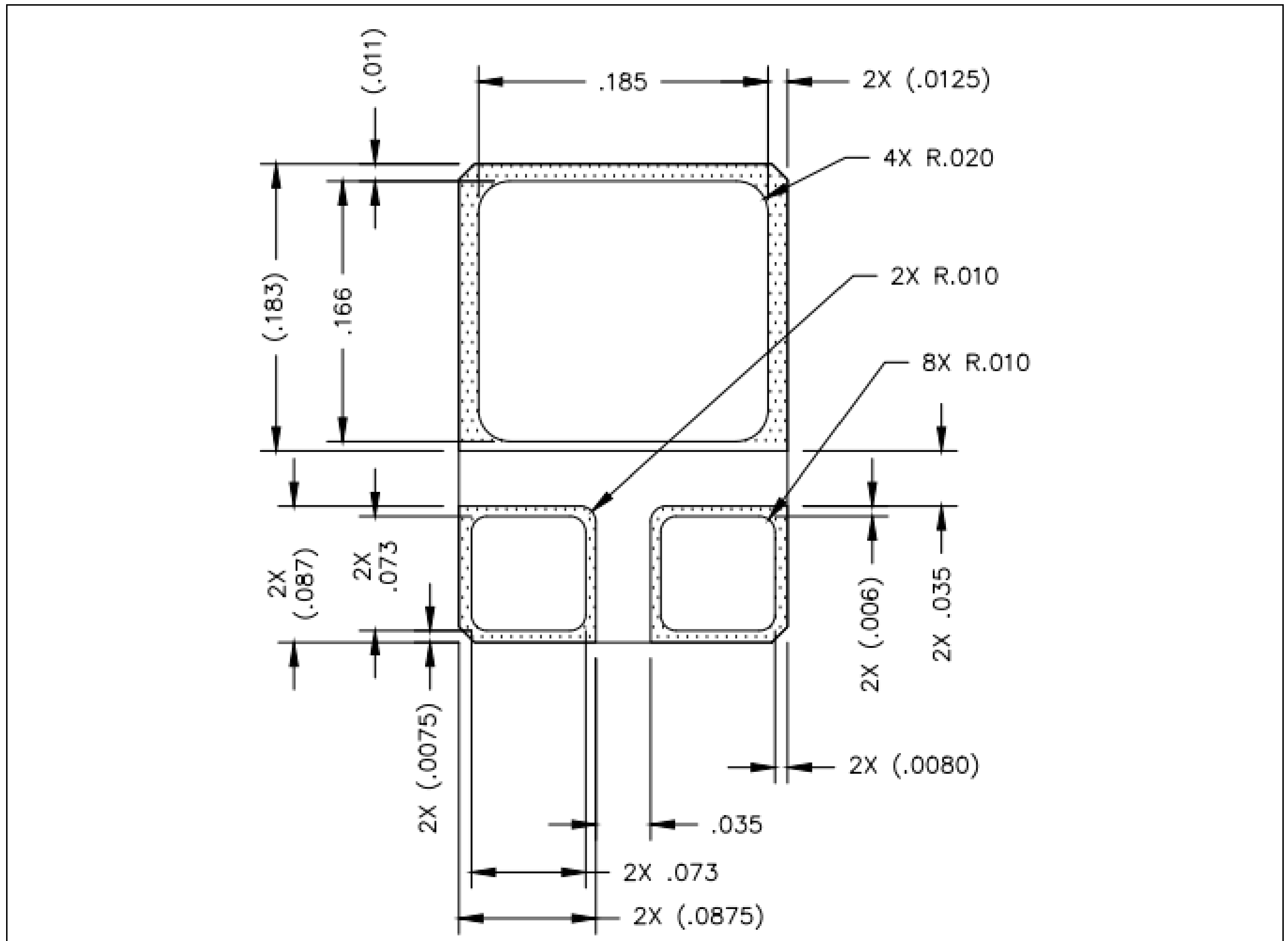

Figure 22 Case outline with dimensions that were used to generate PCB solder pads for SMD-0.2e mounting during PCB-qualification tests, dimensions are in inches

The product nomenclature for SMD-0.2e power discrete devices includes the term “NME” (see the website for the complete listing of product nomenclatures). For QPL devices, the product nomenclature includes the “U8CE” suffix.

7 Conclusions

Validated through extensive design, simulation, and testing, SMD-0.2e is a robust package against thermal stresses and ESD hazards. Designers can employ the SMD-0.2e package with confidence that the package will maintain hermetic integrity and keep a strong solder joint. This package also enjoys internal die layout improvements to facilitate heat dissipation and improve the performance of any application that this package is implemented to support. Specific details on each released discrete that utilizes this package can be found in their corresponding datasheets on the website.

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Revision history

Document revision	Date	Description of changes
1.00	2024-09-25	Initial release

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Edition 2024-09-25

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

AN010144

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