PCB layout guidelines for MOSFET gate driver

Part I: 2EDN/1EDN family

About this document

Scope and purpose

The PCB layout is essential to the optimal function of the MOSFET gate driver. It is also essential for high-current, fast-switching devices to ensure reliable and robust operation of the system, especially for MOSFET gate drivers. As the 2EDN/1EDN EiceDRIVER™ family of gate drivers has powerful output stages that are capable of delivering large current peaks with fast rise and fall times at the gate of the power MOSFET to facilitate very fast voltage transitions, several guidelines must be followed when designing the PCB.

Intended audience

This document is intended for PCB board designers and users of MOSFET gate driver-related circuits.

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1 Introduction

The example application for the PCB layout guidelines is an 800 W Platinum® server power supply [1]. The MOSFET gate driver is applied to the Power Factor Correction (PFC), primary-side LLC resonant converter, Synchronous Rectifier (SR) and O-ring, as shown in Figure 1.

Non-isolated gate driver EiceDRIVER™ 2EDN7524F is applied to drive the PFC, the low-side of the primary-side LLC resonant converter, and the SR, while the EiceDRIVER™ galvanic isolated gate driver 1EDI20N12AF is applied to drive the high-side of the primary-side LLC resonant converter and Or-ing.

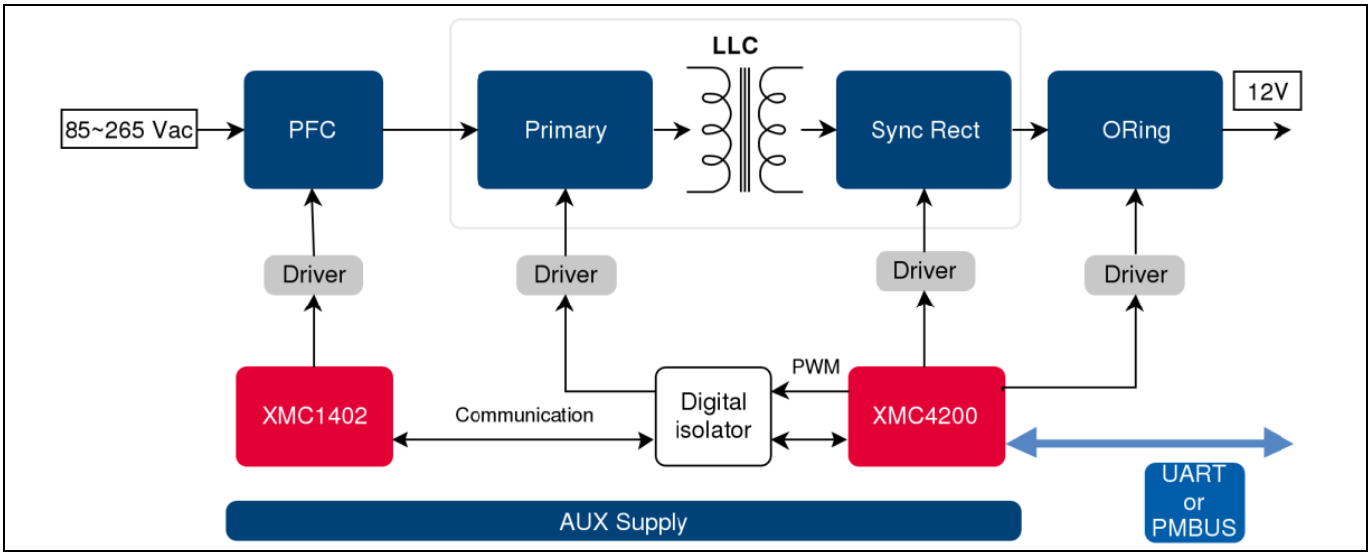

Figure 1 800 W server power supply block diagram

The bottom of the board shows all the places where the gate driver is used, the locations of the SR and Or-ing, and the location of the auxiliary power supply using the QR flyback controller, as shown in Figure 2.

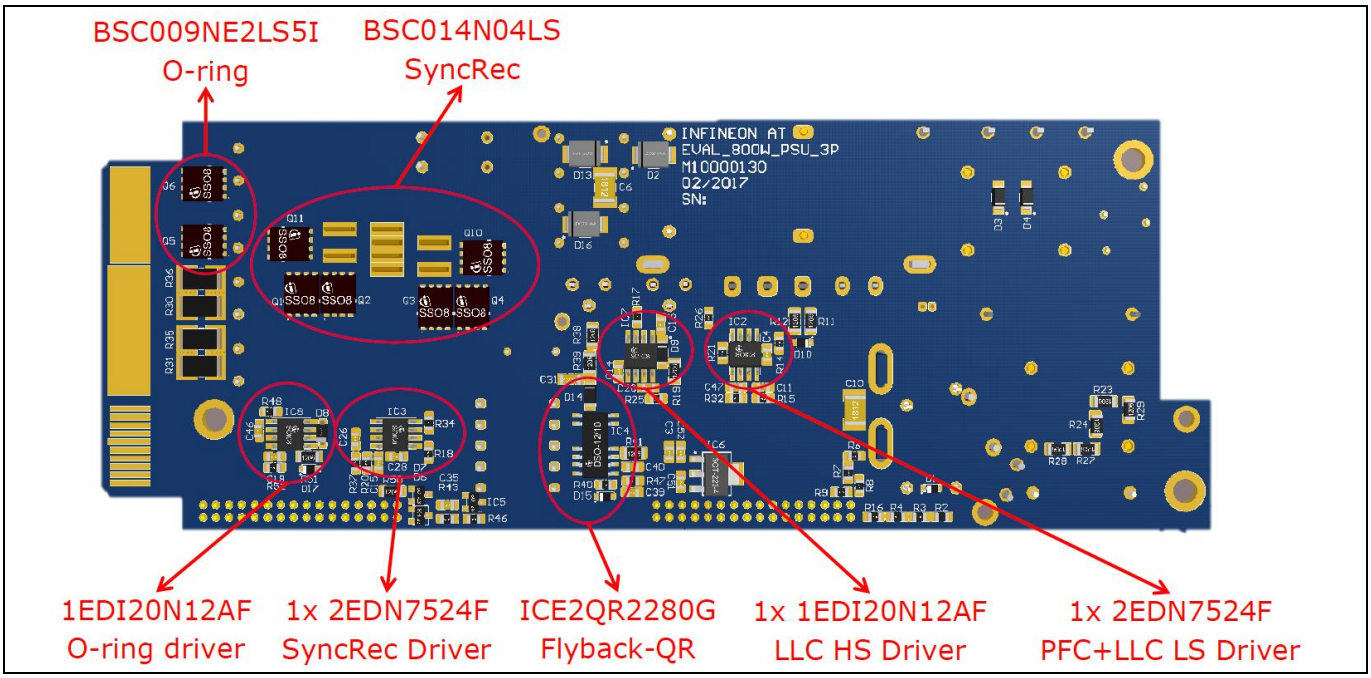

Figure 2 Bottom view of the 800 W server power supply main board

Figure 3 shows part of the schematic in the middle of the board, where EiceDRIVER™ 2EDN7524F (IC2) gate driver is used to drive low-side TO-220 600 V CoolMOS™ P7 SJ MOSFET (Q8) on the primary side of the LLC resonant converter and the TO-247 3-pin 600 V CoolMOS™ P7 SJ MOSFET (Q9) in the PFC boost converter.

The yellow line shows the isolation between the primary and secondary side of the LLC resonant converter.

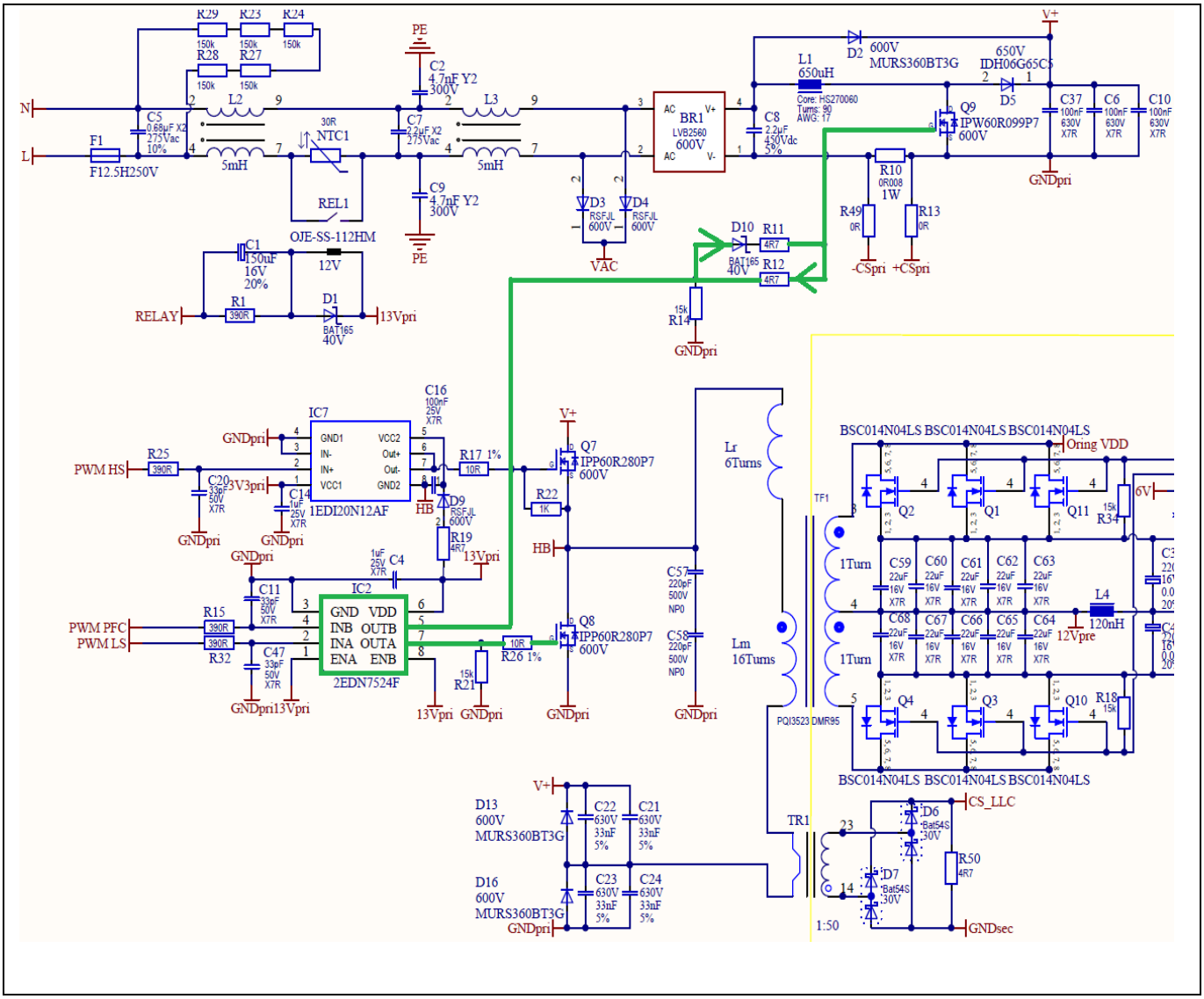

Figure 3 Schematic of 2EDN7524F driving MOSFET in the PFC and low-side MOSFET in the primary side of LLC

In Figure 4, the corresponding PCB circuit around EiceDRIVER™ 2EDN7524F (IC2) can be found with the low-side MOSFET (Q8) and the PFC MOSFET (Q9).

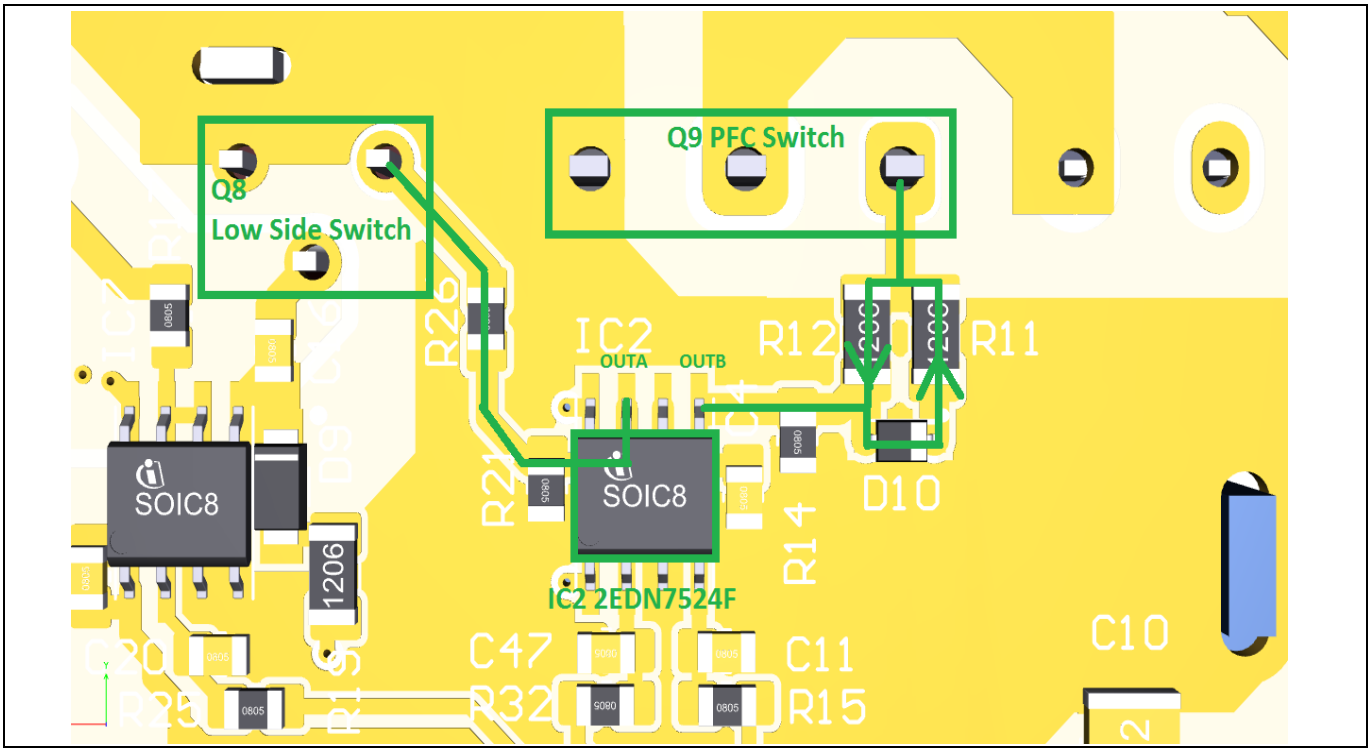

Figure 4 **PCB of 2EDN7524F driving MOSFET in the PFC and low-side MOSFET in the primary side of the LLC**

2 Create a ground plane

Grounding is always one of the important topics in PCB design, and a ground plane is used to provide noise shielding. If traces are used to route the ground signal, their resistance will create voltage drops that will make different “grounds” in the PCB. To avoid that, a ground plane needs to be created with a large area of copper or even a layer for the plane reserved. In addition to noise shielding, the ground plane can act as a heatsink and assist in power dissipation. The ground plane can be completely filled with copper, shown in brown in Figure 5.

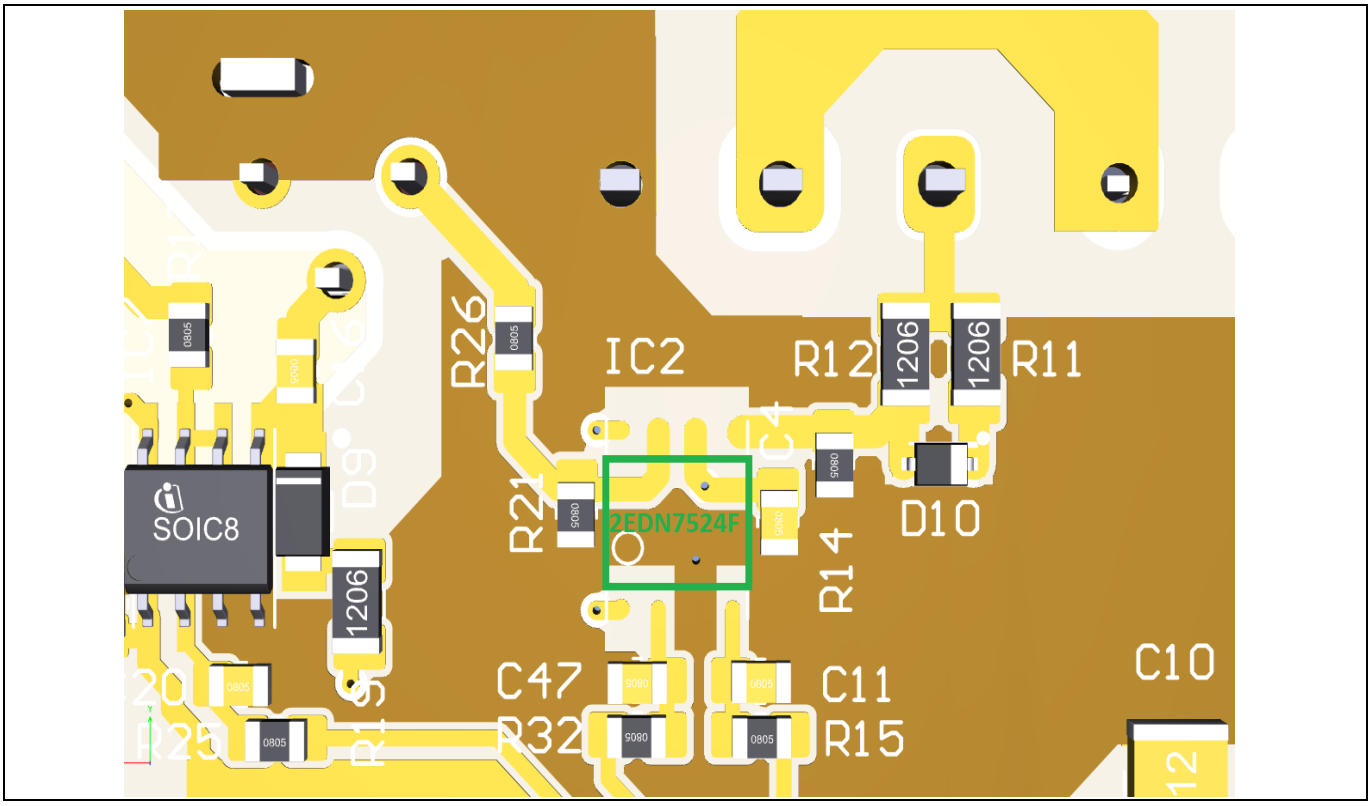

Figure 5 Ground plane for noise shielding in brown

3 Bypass capacitor for gate driver

Bypass capacitors are used to filter AC components from the constant power supply and conduct an alternating current around the gate driver. The V_{DD} bypass capacitor should be placed as close as possible to the gate driver to improve the AC noise filtering performance and reduce the lead inductance, as shown in yellow in Figure 6.

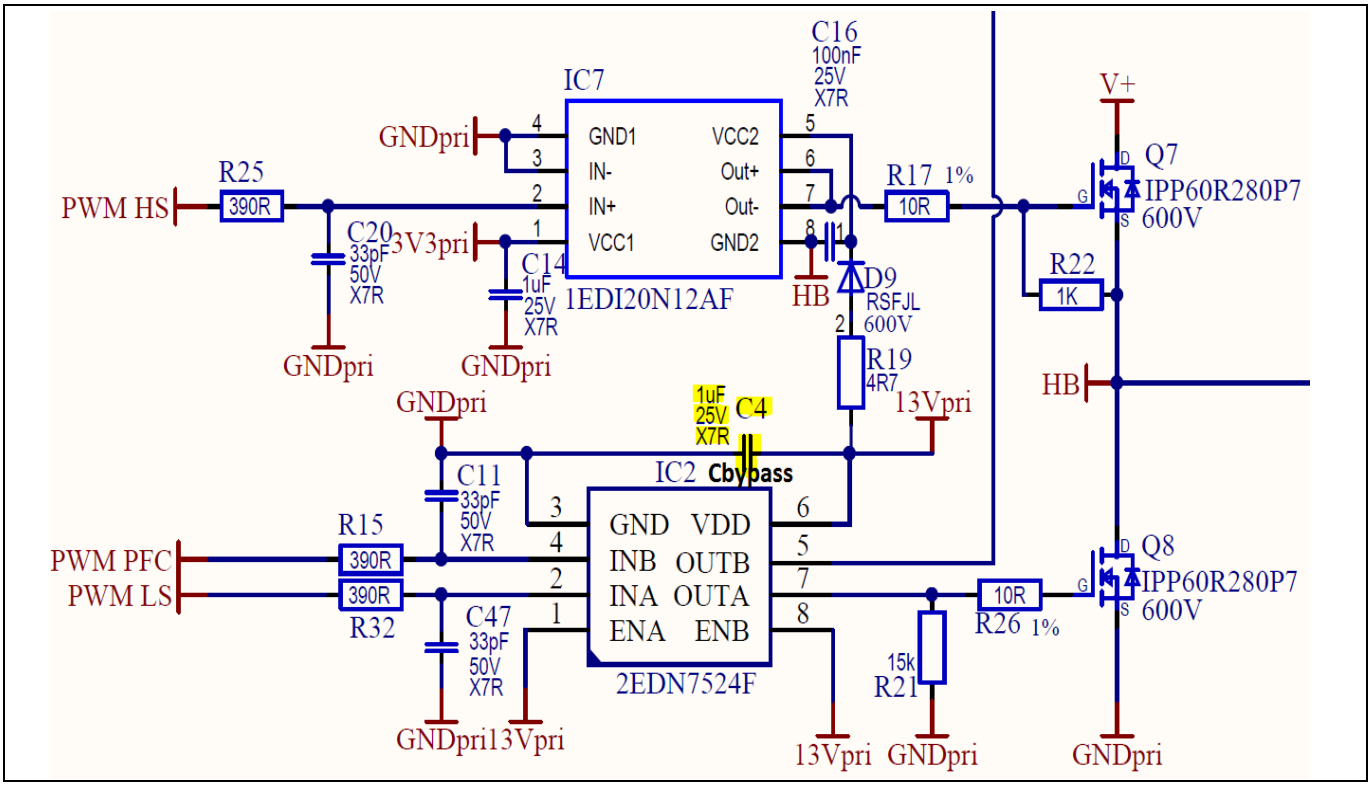

Figure 6 Bypass capacitor C_{bypass} in 2EDN7524F low-side driver

The bypass capacitor is put at the end of the gate driver package (and no further), as shown in Figure 7. The traces of V_{DD} in purple and ground in black should be run under the package and lie very close to one another. This close proximity will help cancel the magnetic fields between the two traces.

Attention: The V_{DD} bypass capacitor should be placed as close as possible to the gate driver!

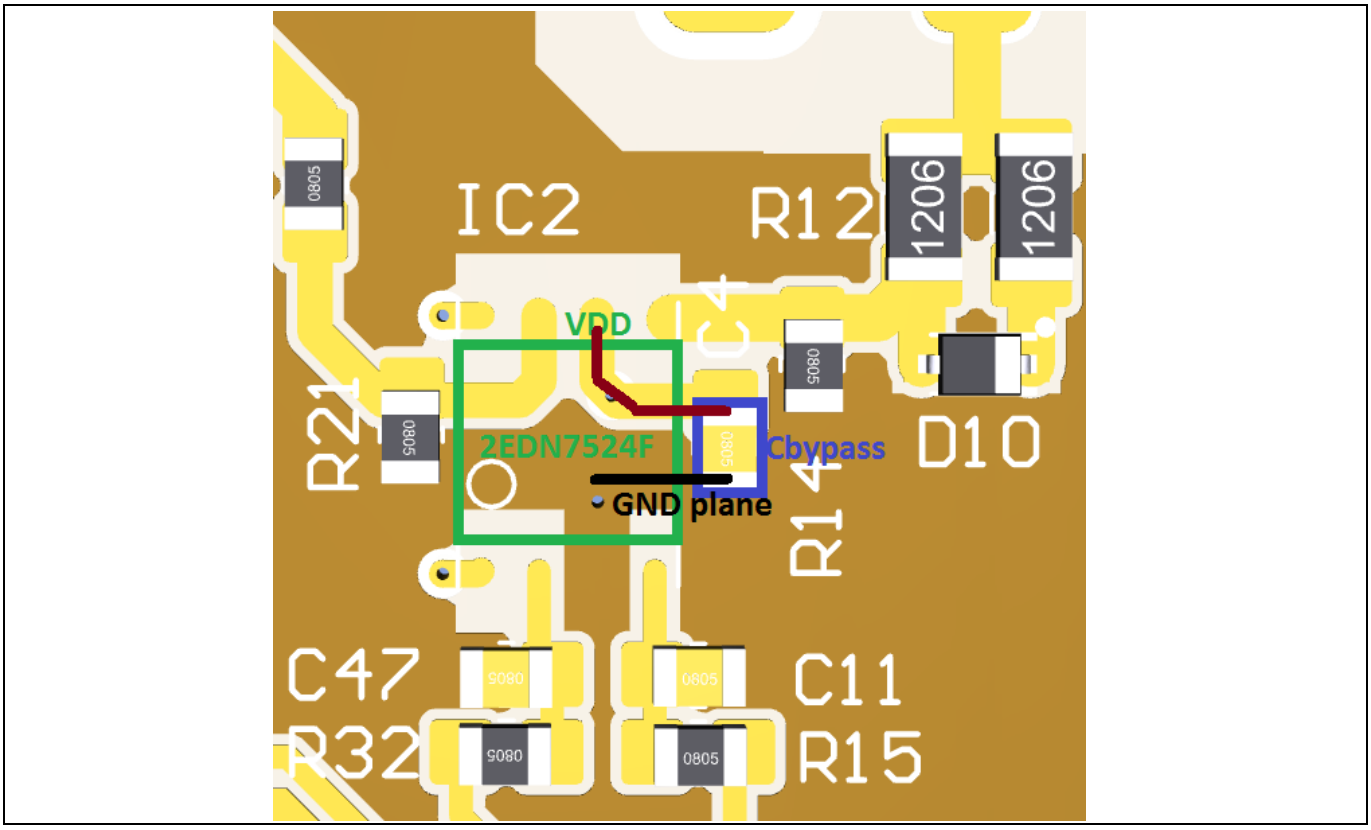

Figure 7 Layout for bypass capacitor of gate driver

The capacitor stores energy during the switching event. Switching high energy at a MOSFET gate through the driver often causes unwanted oscillation from parasitic inductance in the current path. Low capacitance value is not enough for spikes or ripples on the supply voltage. As a rule of thumb, if 5 percent ripple on V_{DD} is demanded, the value of a bypass capacitor has to be 20 times bigger than the value of the load capacitance on the channel that is normally regarded as input capacitance C_{iss} ($C_{iss} = C_{GS} + C_{GD}$ when C_{DS} shorted) of the MOSFET, as shown in Figure 8. If a bypass capacitor with 10 nF is used in case of the load capacitance being 10 nF, V_{DD} fluctuates from 6 V to 15.5 V.

In order to ensure the reliability of the circuit, for example with a 10 nF load, a block capacitor of at least 200 nF should be used. SMD components are highly recommended to maintain low inductances.

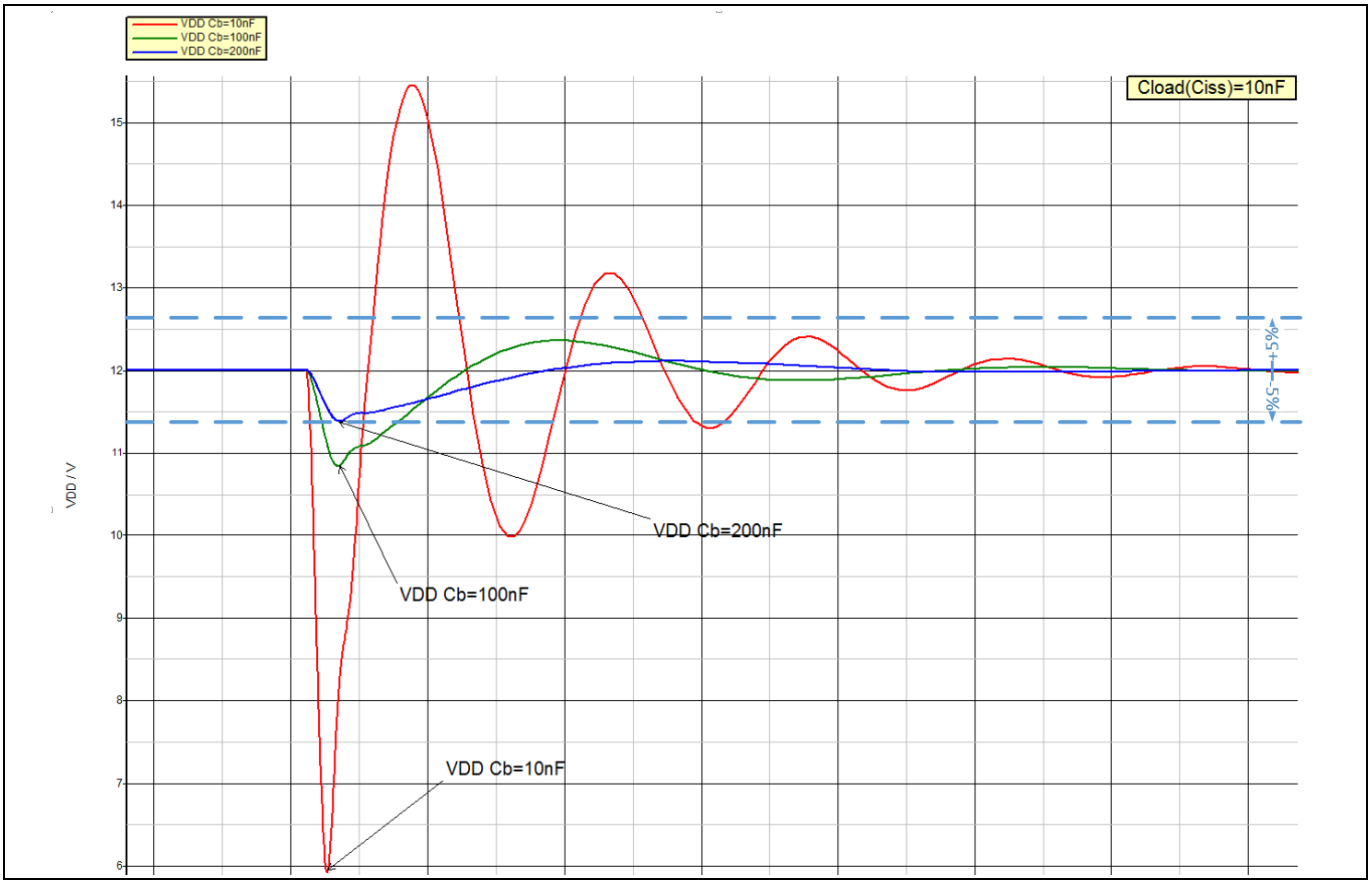

Figure 8 Driver supply voltage simulation depending on bypass capacitor

4 Further considerations

4.1 Shorten the trace between gate and driver output

As shown in Figure 9, the driver should be placed as close as possible to the MOSFET in order to minimize the length of any high-current traces between the driver output pins and the gate of the MOSFET (shown in green) and for traces of the gate of the low-side MOSFET and the gate of the PFC MOSFET. This decreases inductance and should be as wide as possible to reduce resistance.

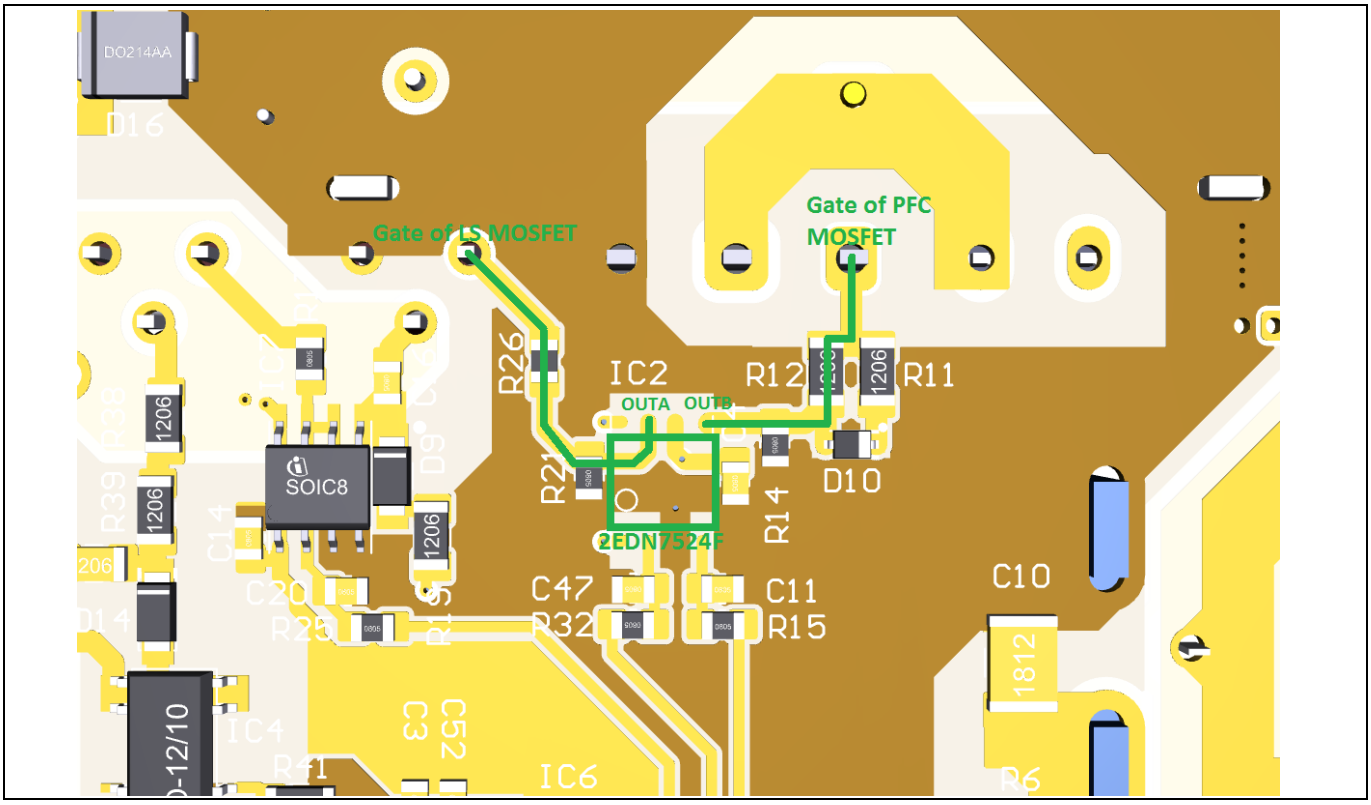

Figure 9 Shorten the trace between gate and driver output

4.2 Input RC filter

Normally the input RC network is not necessary for the EiceDRIVER™ 2EDN/1EDN.

Sometimes the PWM signal generated in a daughter board and the trace between the controller output and driver input are unavoidably long. If the signal line is not well ground-shielded, it is also recommended to add an input RC network, as shown in Figure 10, to improve the performance against noise with cut-off frequency, as below.

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 390\ \text{ohm x}\ 33\ \text{pF}} = 12.37\ MHz$$

If the RC network is designed, it should be placed as close as possible to the input pins of the gate driver, as the input circuitry is the noise sensitive part, as shown in Figure 11.

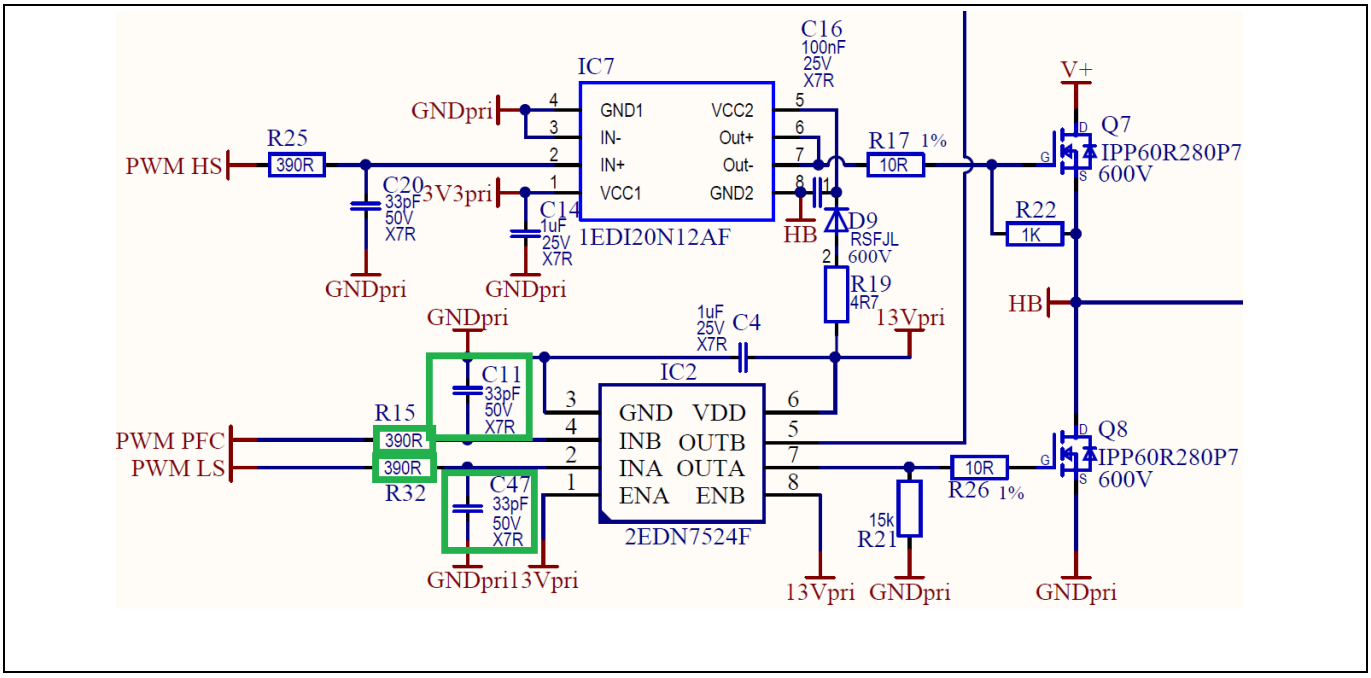

Figure 10 Input RC filter schematic – shown in green

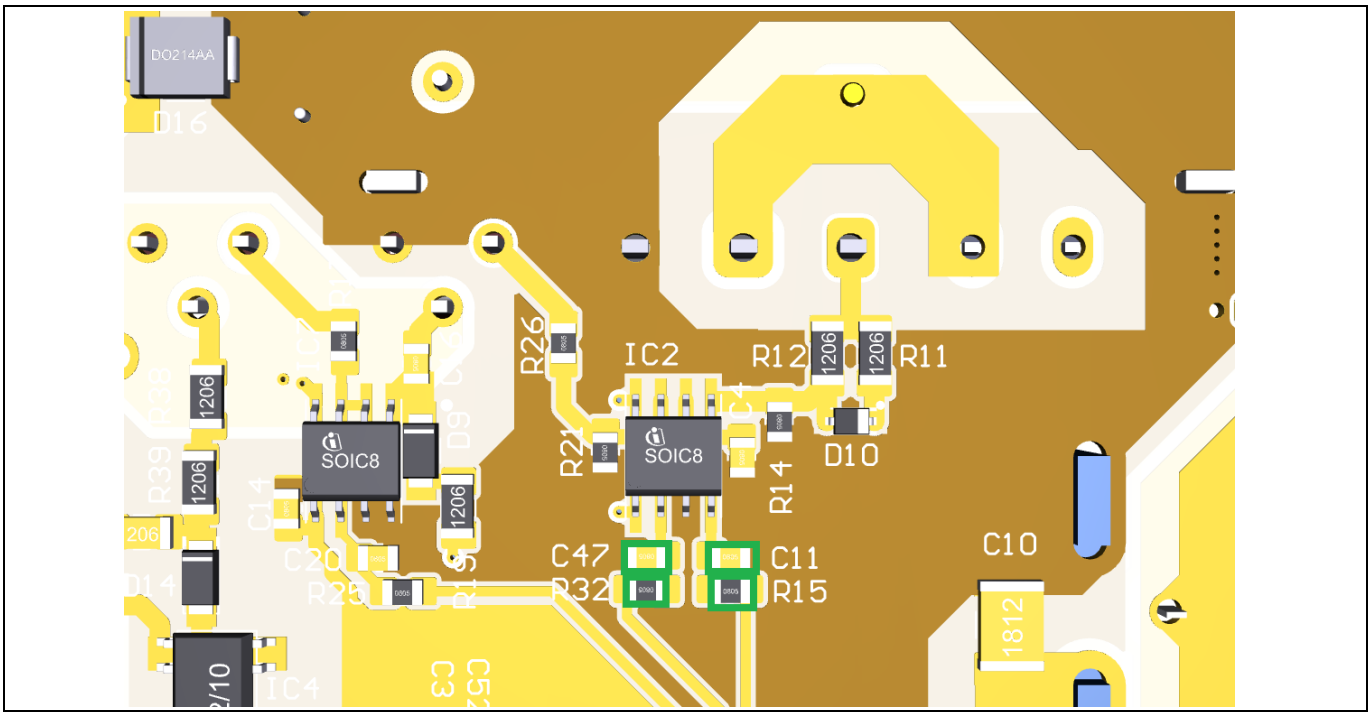

Figure 11 Input RC filter layout – shown in green

4.3 Resistor at V_{CC}

On the other side, the gate driver stage is a noise-generating part. In order to prevent noise or peak current from the V_{CC} pin to the V_{CC} supply pin, a resistor valued between 4 Ω and 10 Ω can be placed between the V_{CC} pin of the gate driver and the V_{CC} supply pin.

It is also recommended to place an SMD ferrite bead with a resistance around ~ 1k Ω at 100 MHz between the V_{CC} pin of the gate driver and the V_{CC} supply pin to damp the noise.

5 References

[1] AN_201710_PL52_002 800 W Platinum® server power supply – using 600 V CoolMOS™ P7 and digital control with XMC™

6 Revision history

Document version	Date of release	Description of changes

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Edition 2018-01-31

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_1801_PL52_1801_132230

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